TS4909

Dual mode low power 150mW stereo headphone amplifier with capacitor-less and single-ended outputs

Features

- No output coupling capacitors necessary
- Pop-and-click noise reduction circuitry
- Operating from V_{CC} = 2.2V to 5.5V
- Standby mode active low
- Output power:
  - 158mW @5V, into 16Ω with 1% THD+N max (1kHz)
  - 52mW @3.0V into 16Ω with 1% THD+N max (1kHz)
- Ultra low current consumption: 2.0mA typ.@3V
- Ultra low standby consumption: 10nA typ.
- High signal-to-noise ratio: 105 dB typ.@5V
- High crosstalk immunity: 110dB (F=1kHz) for single-ended outputs
- PSRR: 72dB (F=1kHz), inputs grounded, for phantom ground outputs
- Low t_{WU}: 50ms in PHG mode, 100ms in SE mode
- Available in lead-free DFN10 3x3mm

Applications

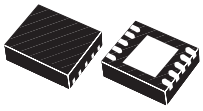
- Headphone amplifier
- Mobile phone
- PDA, portable audio player

Description

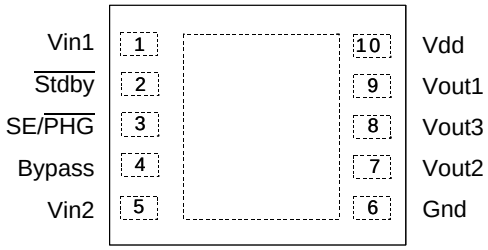
The TS4909 is a stereo audio amplifier designed to drive headphones in portable applications.

The integrated phantom ground is a circuit topology that eliminates the heavy output coupling capacitors. This is of primary importance in portable applications where space constraints are very high. A single-ended configuration is also available, offering even lower power consumption because the phantom ground can be switched off.

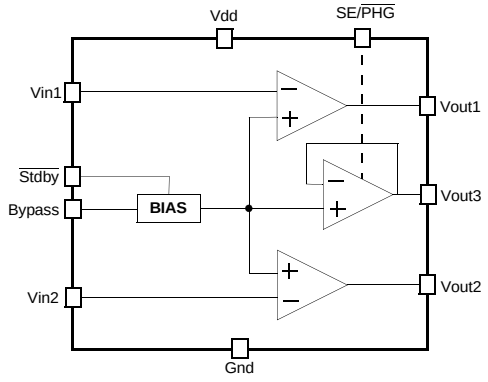
DFN10 (3x3)



Pin connections (top view)



Functional block diagram



Pop-and-click noise during switch-on and switch-off phases is eliminated by integrated circuitry.

Specially designed for applications requiring low power supplies, the TS4909 is capable of delivering 31mW of continuous average power into a 32Ω load with less than 1% THD+N from a 3V power supply.

Featuring an active low standby mode, the TS4909 reduces the supply current to only 10nA (typ.). The TS4909 is unity gain stable and can be configured by external gain-setting resistors.

Contents

1 Typical application schematics

Figure 1. Typical applications for the TS4909

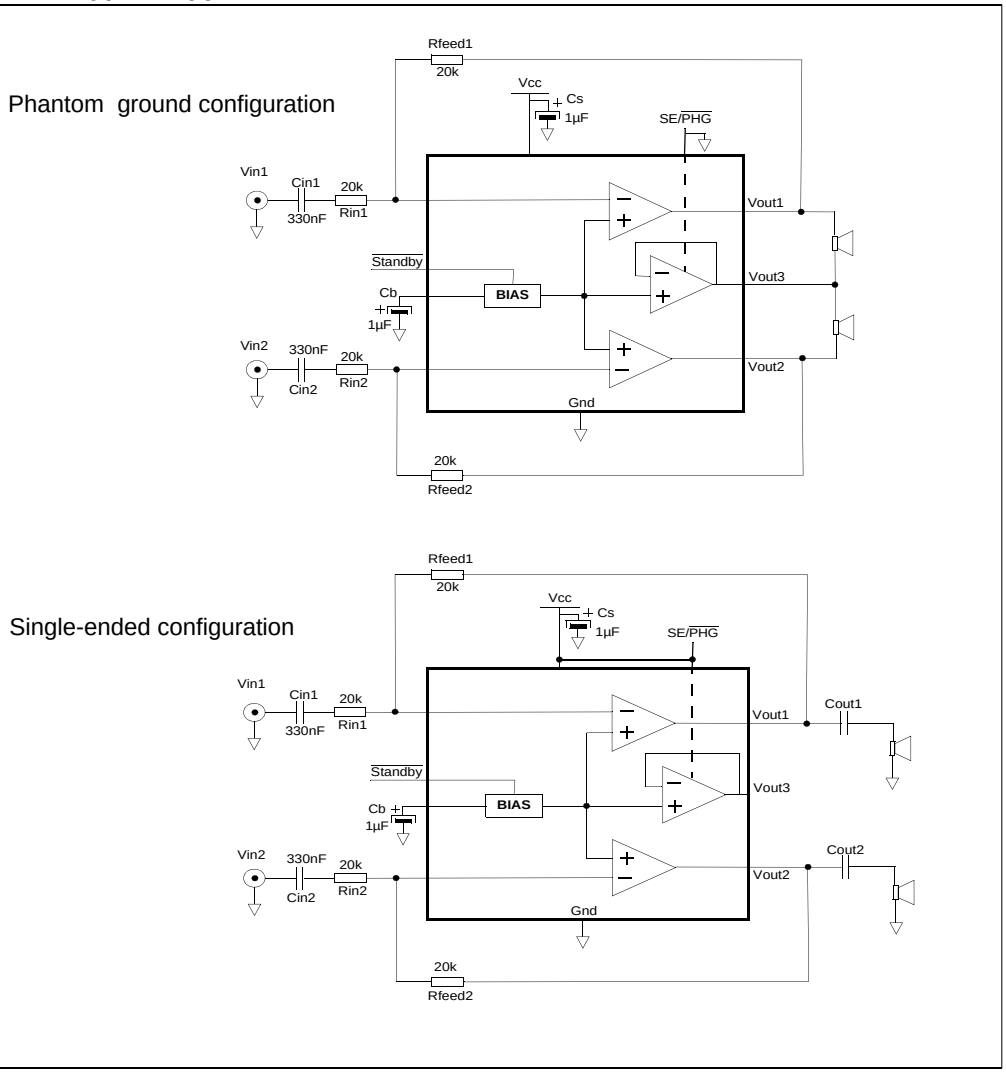


Table 1. Application component information

Component	Functional description
$R_{in1,2}$	Inverting input resistor that sets the closed loop gain in conjunction with R_{feed}. This resistor also forms a high pass filter with C_{in} (f_c = 1 / (2 x Pi x R_{in} x C_{in})).
$C_{in1,2}$	Input coupling capacitor that blocks the DC voltage at the amplifier's input terminal.
$R_{feed1,2}$	Feedback resistor that sets the closed loop gain in conjunction with R_{in}. A_V= closed loop gain = -R_{feed}/R_{in}.
C_b	Half supply bypass capacitor.
C_s	Supply bypass capacitor that provides power supply filtering.

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage	-0.3V to V_{CC} +0.3V	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient DFN10	120	°C/W
P_{diss}	Power dissipation (2) DFN10	1.79	W
ESD	Human body model (pin to pin)	2	kV
ESD	Machine model 220pF - 240pF (pin to pin)	200	V
Latch-up	Latch-up immunity (all pins)	200	mA
	Lead temperature (soldering, 10 sec)	260	°C
	Output current	170 (3)	mA

1. All voltage values are measured with respect to the ground pin.
2. P_d is calculated with T_{amb} = 25°C, $T_{junction}$ = 150°C.
3. Caution: this device is not protected in the event of abnormal operating conditions, such as for example, short-circuiting between any one output pin and ground, between any one output pin and V_{CC}, and between individual output pins.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.2 to 5.5	V
R_L	Load resistor	≥ 16	Ω
T_{oper}	Operating free air temperature range	-40 to + 85	°C
C_L	Load capacitor R_L = 16 to 100Ω R_L > 100Ω	 400 100	pF
V_{STBY}	Standby voltage input TS4909 in STANDBY TS4909 in active state	 GND ≤ V_{STBY} ≤ 0.4 (1) 1.35V ≤ V_{STBY} ≤ V_{CC}	V
$V_{SE/\overline{PHG}}$	Single-ended or phantom ground configuration voltage Input TS4909 outputs in single-ended configuration TS4909 outputs in phantom ground configuration	 $V_{SE/\overline{PHG}}$=V_{CC} $V_{SE/\overline{PHG}}$=0	V
R_{thja}	Thermal resistance junction to ambient DFN10(2)	41	°C/W

1. The minimum current consumption (I_{STBY}) is guaranteed at ground for the whole temperature range.
2. When mounted on a 4-layer PCB.

3 Electrical characteristics

Table 4. Electrical characteristics at V_{CC} = +5V with GND = 0V and T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load, single-ended No input signal, no load, phantom ground		2.1 3.1	3.2 4.8	mA
I_{STBY}	Standby current	No input signal, R_L=32Ω		10	1000	nA
P_{out}	Output power	THD+N = 1% max, F = 1kHz, R_L = 32Ω, single-ended THD+N = 1% max, F = 1kHz, R_L = 16Ω, single-ended THD+N = 1% max, F = 1kHz, R_L = 32Ω, phantom ground THD+N = 1% max, F = 1kHz, R_L = 16Ω, phantom ground	60 95 60 95	88 158 85 150		mW
THD+N	Total harmonic distortion + noise (A_v=-1)	R_L = 32Ω, P_{out} = 60mW, 20Hz ≤ F ≤ 20kHz, single-ended R_L = 16Ω, P_{out} = 90mW, 20Hz ≤ F ≤ 20kHz, single-ended R_L = 32Ω, P_{out} = 60mW, 20Hz ≤ F ≤ 20kHz, phantom ground R_L = 16Ω, P_{out} = 90mW, 20Hz ≤ F ≤ 20kHz, phantom ground		0.3 0.3 0.3 0.3		%
PSRR	Power supply rejection ratio	Inputs grounded(1), A_v = -1, R_L>=16Ω, C_b=1µF, F = 217Hz, V_{ripple} = 200mVpp Single-ended output referenced to phantom ground Single-ended output referenced to ground	 66 61	 72 67		dB
I_{out}	Max output current	THD +N ≤ 1%, R_L = 16Ω connected between out and V_{CC}/2		140		mA
V_O	Output swing	V_{OL}: R_L = 32Ω V_{OH}: R_L = 32Ω V_{OL}: R_L = 16Ω V_{OH}: R_L = 16Ω	 4.39 4.17	0.14 4.75 0.25 4.55	0.47 0.69	V
SNR	Signal-to-noise ratio	A-weighted, A_v=-1, R_L = 32Ω, THD +N < 0.4%, 20Hz ≤ F ≤20kHz Single-ended Phantom ground		 104 105		dB
Cross-talk	Channel separation	R_L = 32Ω, A_v=-1, phantom ground F = 1kHz F = 20Hz to 20kHz R_L = 32Ω, A_v=-1, single-ended F = 1kHz F = 20Hz to 20kHz		 -73 -68 -110 -90		dB
V_{OO}	Output offset voltage	Phantom ground configuration, floating inputs, R_{feed}=22KΩ		5	20	mV
t_{WU}	Wake-up time	Phantom ground configuration Single-ended configuration		50 100	80 160	ms

1. Guaranteed by design and evaluation.

Table 5. Electrical characteristics at V_{CC} = +3.0V with GND = 0V, T_{amb} = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load, single-ended No input signal, no load, phantom ground		2 2.8	2.8 4.2	mA
I_{STBY}	Standby current	No input signal, R_L=32Ω		10	1000	nA
P_{out}	Output power	THD+N = 1% max, F = 1kHz, R_L = 32Ω, single-ended THD+N = 1% max, F = 1kHz, R_L = 16Ω, single-ended THD+N = 1% max, F = 1kHz, R_L = 32Ω, phantom ground THD+N = 1% max, F = 1kHz, R_L = 16Ω, phantom ground	20 30 20 30	31 52 31 54		mW
THD+N	Total harmonic distortion + noise (A_V=-1)	R_L = 32Ω, P_{out} = 25mW, 20Hz ≤ F ≤ 20kHz, single-ended R_L = 16Ω, P_{out} = 40mW, 20Hz ≤ F ≤ 20kHz, single-ended R_L = 32Ω, P_{out} = 25mW, 20Hz ≤ F ≤ 20kHz, phantom ground R_L = 16Ω, P_{out} = 40mW, 20Hz ≤ F ≤ 20kHz, phantom ground		0.3 0.3 0.3 0.3		%
PSRR	Power supply rejection ratio	Inputs grounded (2), A_V=-1, RL>=16Ω, C_b=1µF, F = 217Hz, V_{ripple} = 200mVpp Single-ended output referenced to phantom ground Single-ended output referenced to ground	 64 59	 70 65		dB
I_{out}	Max output current	THD +N ≤ 1%, R_L = 16Ω connected between out and V_{CC}/2		82		mA
V_O	Output swing	V_{OL}: R_L = 32Ω V_{OH}: R_L = 32Ω V_{OL}: R_L = 16Ω V_{OH}: R_L = 16Ω	 2.6 2.45	0.12 2.83 0.19 2.70	0.34 0.49	V
SNR	Signal-to-noise ratio	A-weighted, A_V=-1, R_L = 32Ω, THD +N < 0.4%, 20Hz ≤F ≤ 20kHz Single-ended Phantom ground		 100 101		dB
Cross-talk	Channel separation	R_L = 32Ω, A_V=-1, phantom ground F = 1kHz F = 20Hz to 20kHz R_L = 32Ω, A_V=-1, single-ended F = 1kHz F = 20Hz to 20kHz		 -73 -68 -110 -90		dB
V_{OO}	Output offset voltage	Phantom ground configuration, floating inputs, R_{feed}=22KΩ		5	20	mV
t_{WU}	Wake-up time	Phantom ground configuration Single-ended configuration		50 100	80 160	ms

1. All electrical values are guaranteed with correlation measurements at 2.6V and 5V.
2. Guaranteed by design and evaluation.

Table 6. Electrical characteristics at V_{CC} = +2.6V with GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load, single-ended No input signal, no load, phantom ground		1.9 2.8	2.7 4	mA
I_{STBY}	Standby current	No input signal, R_L=32Ω		10	1000	nA
P_{out}	Output power	THD+N = 1% max, F = 1kHz, R_L = 32Ω, single-ended THD+N = 1% max, F = 1kHz, R_L = 16Ω, single-ended THD+N = 1% max, F = 1kHz, R_L = 32Ω, phantom ground THD+N = 1% max, F = 1kHz, R_L = 16Ω, phantom ground	15 22 15 22	23 38 23 39		mW
THD+N	Total harmonic distortion + noise (A_v=-1)	R_L = 32Ω, P_{out} = 20mW, 20Hz ≤ F ≤ 20kHz, single-ended R_L = 16Ω, P_{out} = 30mW, 20Hz ≤ F ≤ 20kHz, single-ended R_L = 32Ω, P_{out} = 20mW, 20Hz ≤ F ≤ 20kHz, phantom ground R_L = 16Ω, P_{out} = 30mW, 20Hz ≤ F ≤ 20kHz, phantom ground		0.3 0.3 0.3 0.3		%
PSRR	Power supply rejection ratio	Inputs grounded (1), A_v=-1, RL>=16Ω, C_b=1µF, F = 217Hz, V_{ripple} = 200mVpp Single-ended output referenced to phantom ground Single-ended output referenced to ground	 64 59	 70 65		dB
I_{out}	Max output current	THD +N ≤1%, R_L = 16Ω connected between out and V_{CC}/2		70		mA
V_O	Output swing	V_{OL}: R_L = 32Ω V_{OH}: R_L = 32Ω V_{OL}: R_L = 16Ω V_{OH}: R_L = 16Ω	 2.25 2.11	0.11 2.45 0.18 2.32	0.3 0.44	V
SNR	Signal-to-noise ratio	A weighted, A_v=-1, R_L = 32Ω, THD +N < 0.4%, 20Hz ≤ F ≤ 20kHz Single-ended Phantom ground		 99 100		dB
Cross-talk	Channel separation	R_L = 32Ω, A_v=-1, phantom ground F = 1kHz F = 20Hz to 20kHz R_L = 32Ω, A_v=-1, single-ended F = 1kHz F = 20Hz to 20kHz		 -73 -68 -110 -90		dB
V_{OO}	Output offset voltage	Phantom ground configuration, floating inputs, R_{feed}=22KΩ		5	20	mV
t_{WU}	Wake-up time	Phantom ground configuration Single-ended configuration		50 100	80 160	ms

1. Guaranteed by design and evaluation.

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Figure 2. Open-loop frequency response

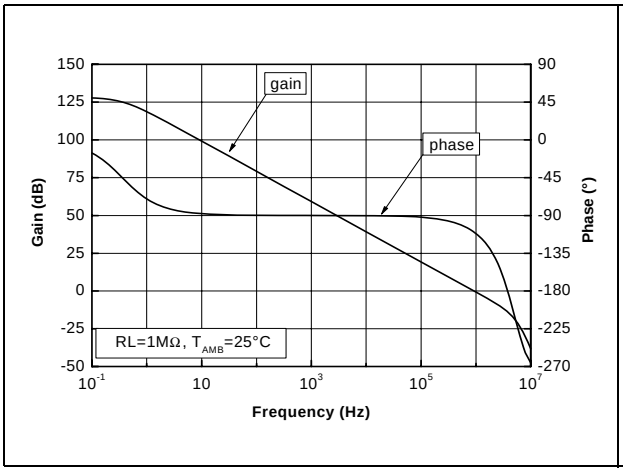


Figure 3. Open-loop frequency response

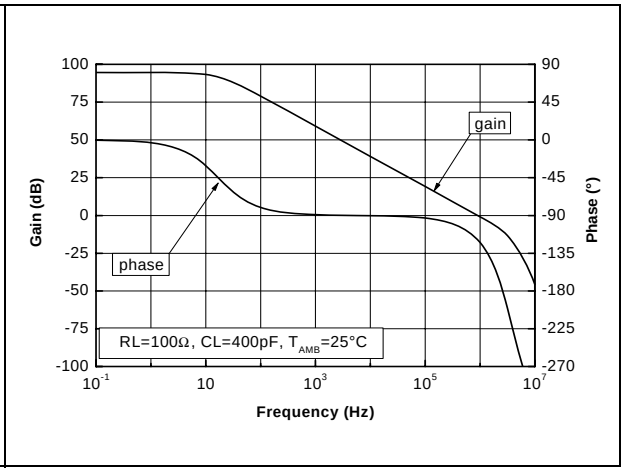


Figure 4. Open-loop frequency response

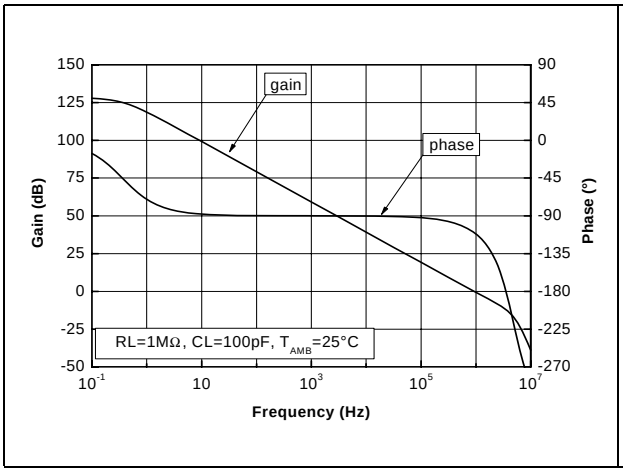


Figure 5. Open-loop frequency response

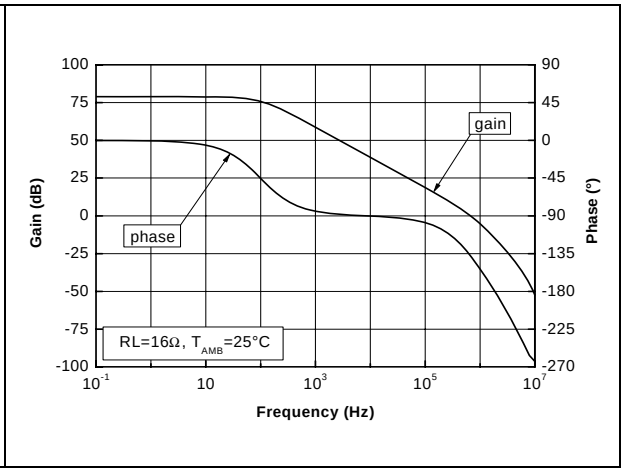


Figure 6. Open-loop frequency response

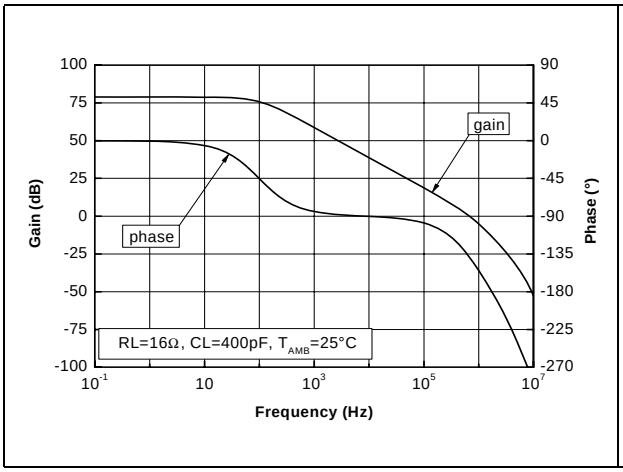


Figure 7. Output swing vs. power supply voltage

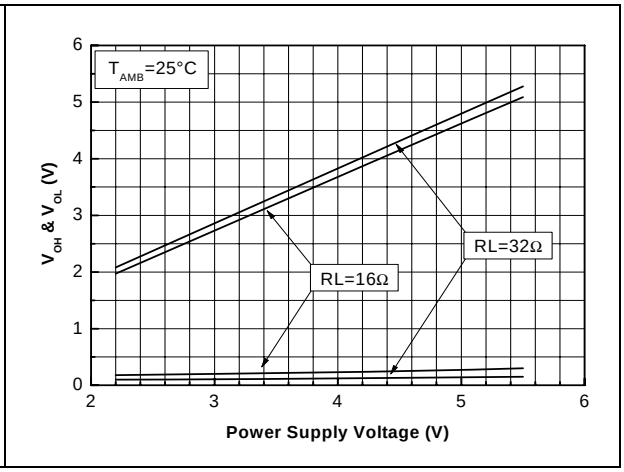


Figure 8. THD+N vs. output power

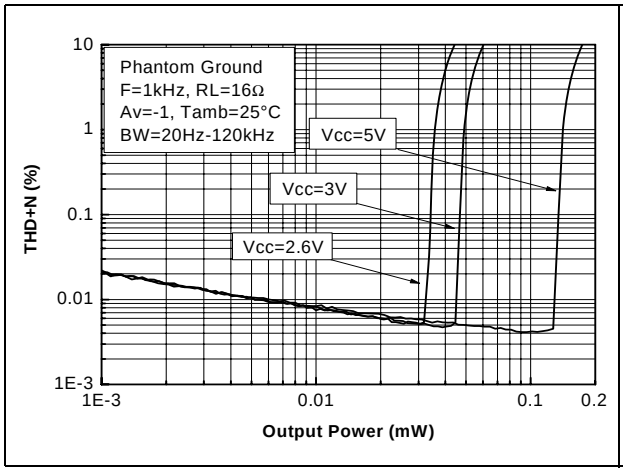


Figure 9. THD+N vs. output power

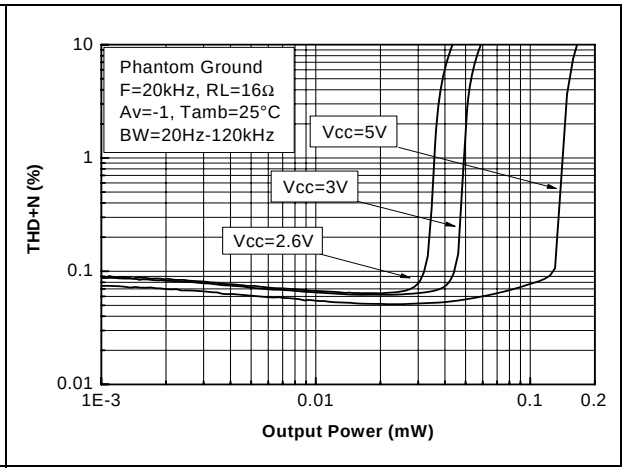


Figure 10. THD+N vs. output power

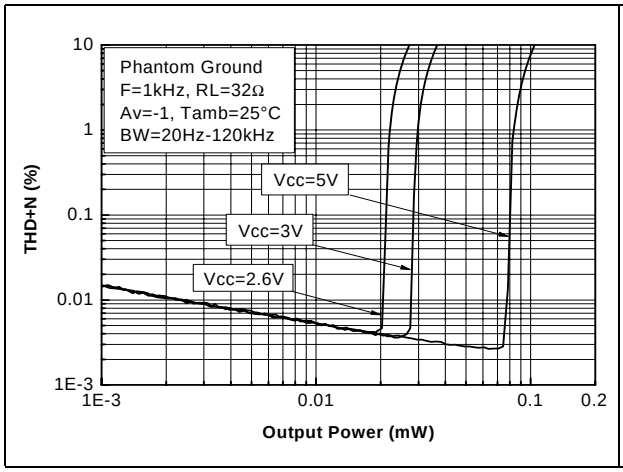


Figure 11. THD+N vs. output power

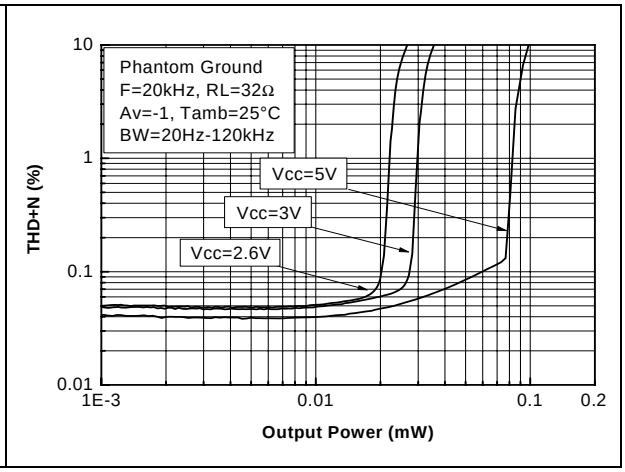


Figure 12. THD+N vs. output power

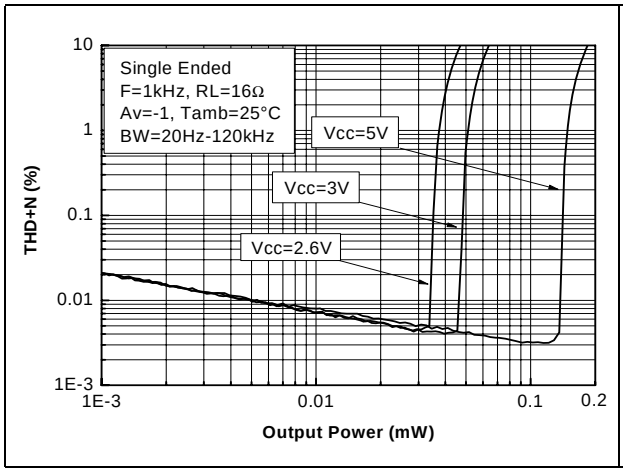


Figure 13. THD+N vs. output power

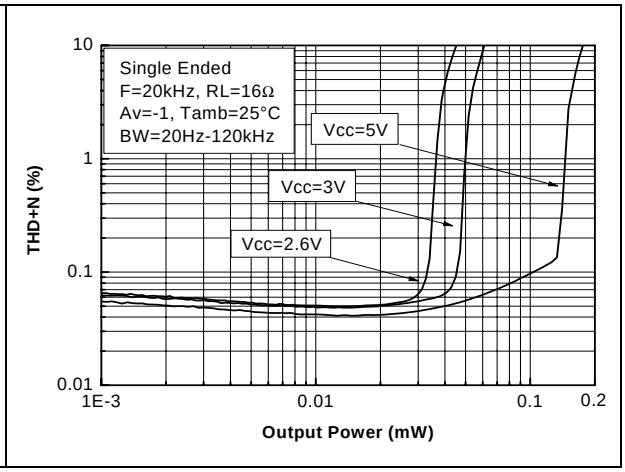


Figure 14. THD+N vs. output power

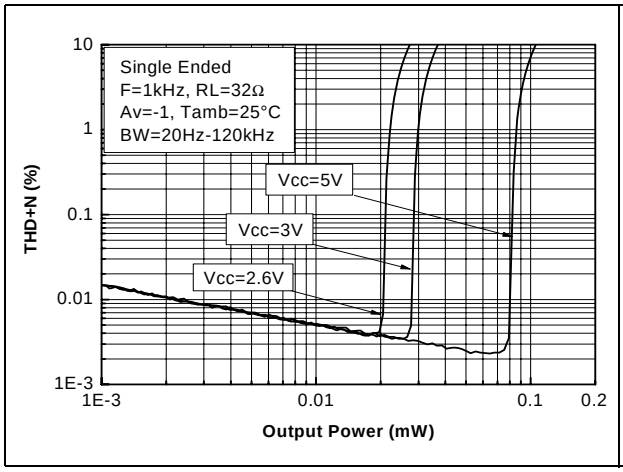


Figure 15. THD+N vs. output power

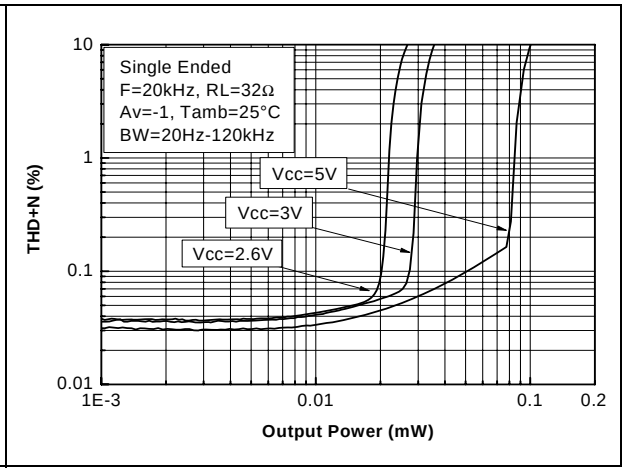


Figure 16. THD+N vs. output power

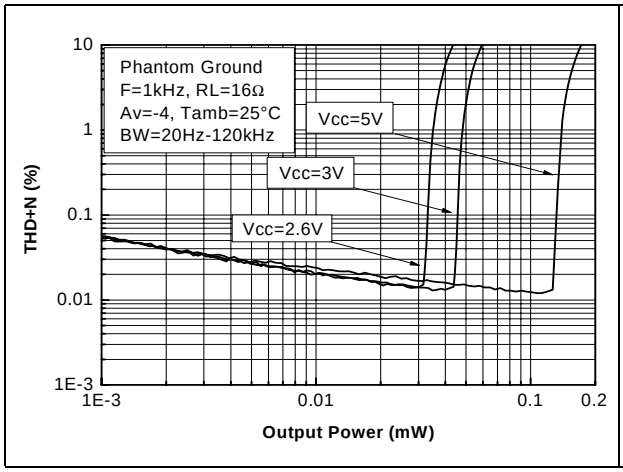


Figure 17. THD+N vs. output power

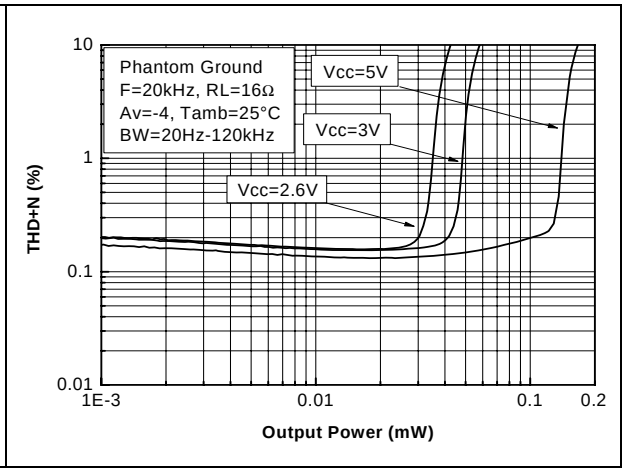


Figure 18. THD+N vs. output power

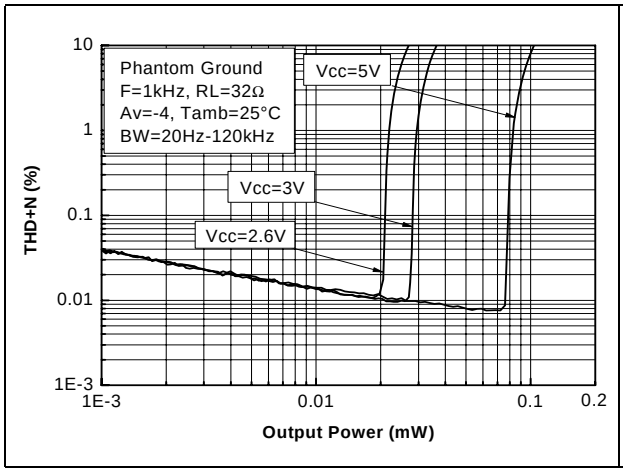


Figure 19. THD+N vs. output power

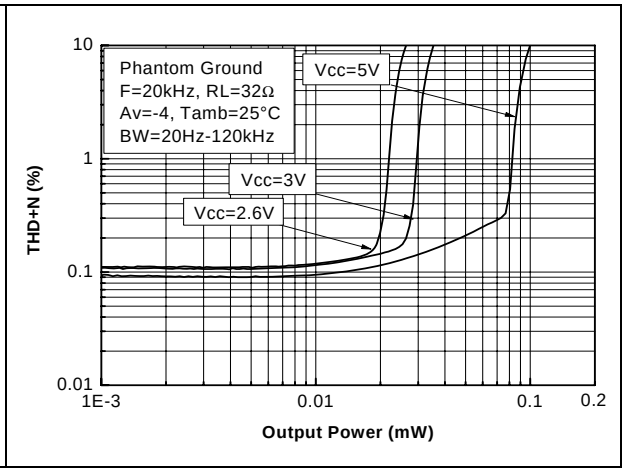


Figure 20. THD+N vs. output power

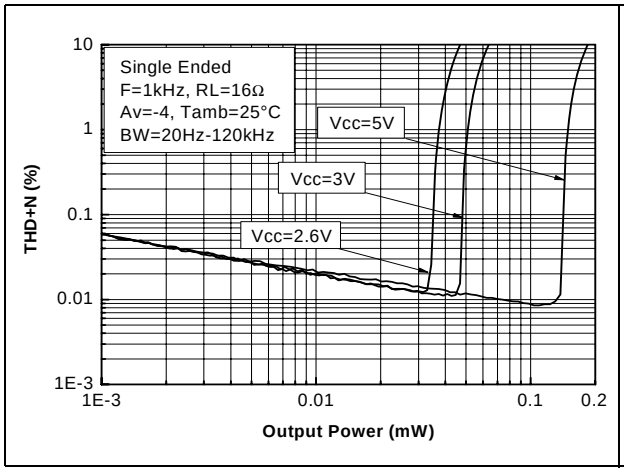


Figure 21. THD+N vs. output power

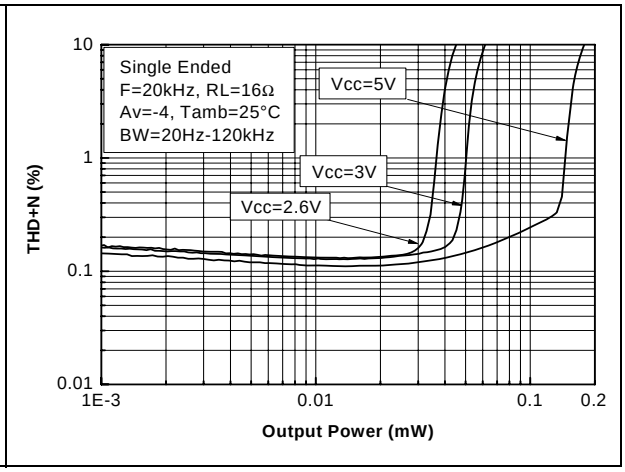


Figure 22. THD+N vs. output power

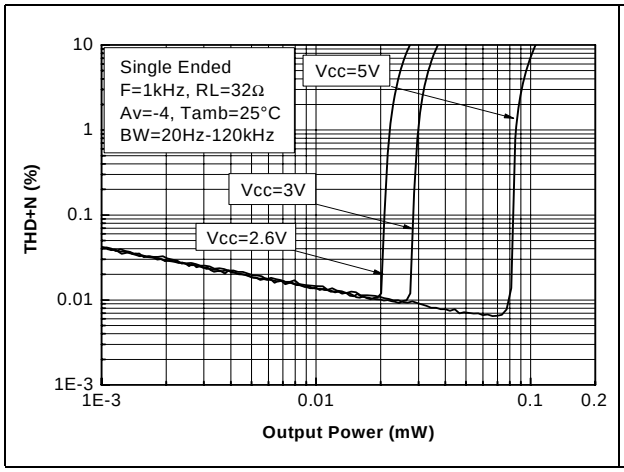


Figure 23. THD+N vs. output power

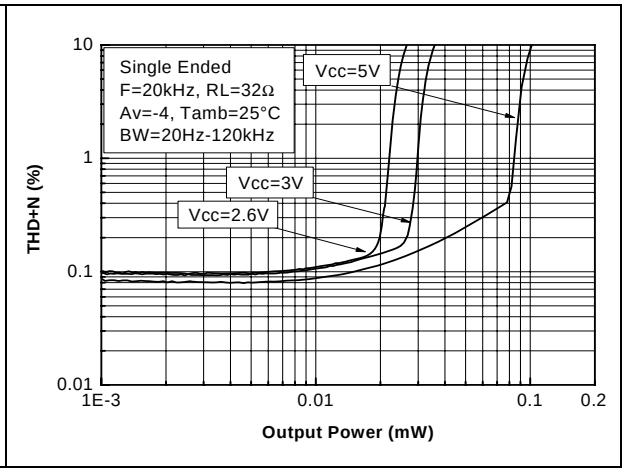


Figure 24. THD+N vs. frequency

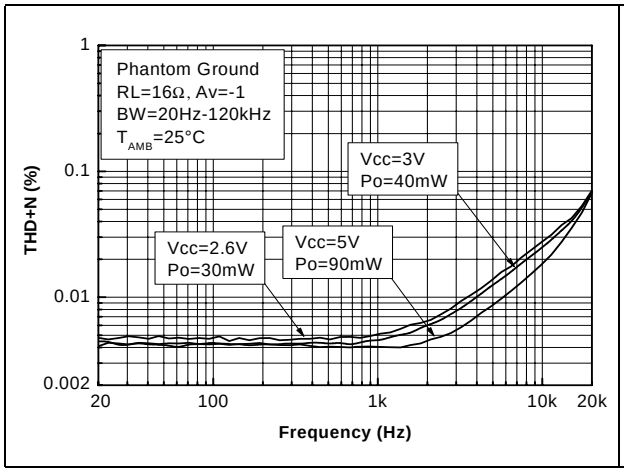


Figure 25. THD+N vs. frequency

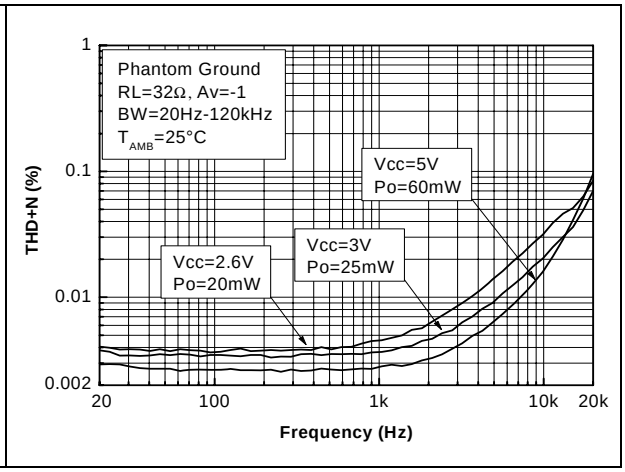


Figure 26. THD+N vs. frequency

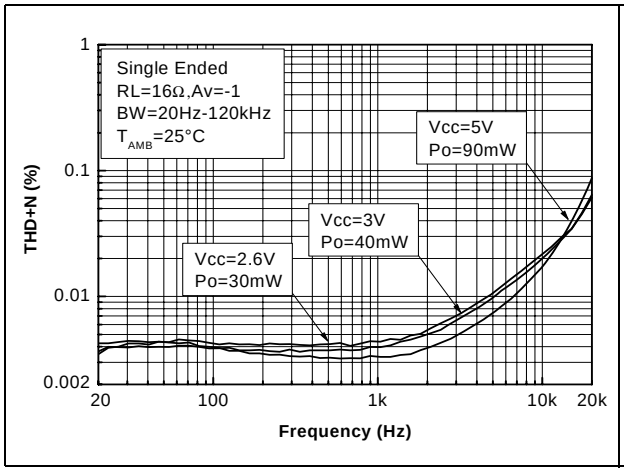


Figure 27. THD+N vs. frequency

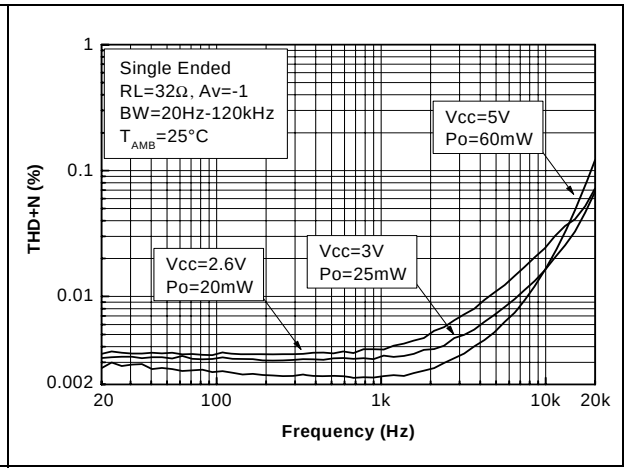


Figure 28. THD+N vs. frequency

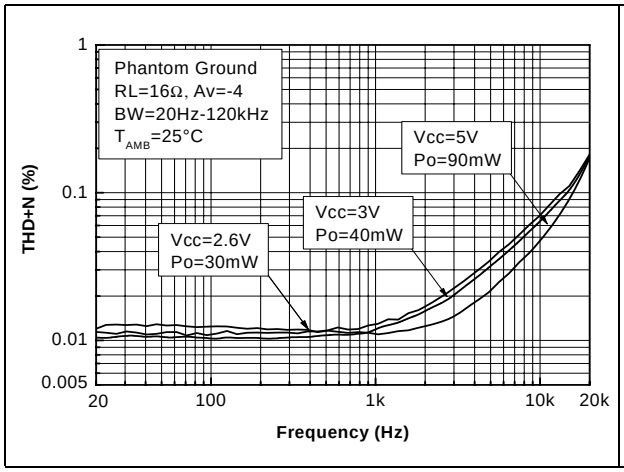


Figure 29. THD+N vs. frequency

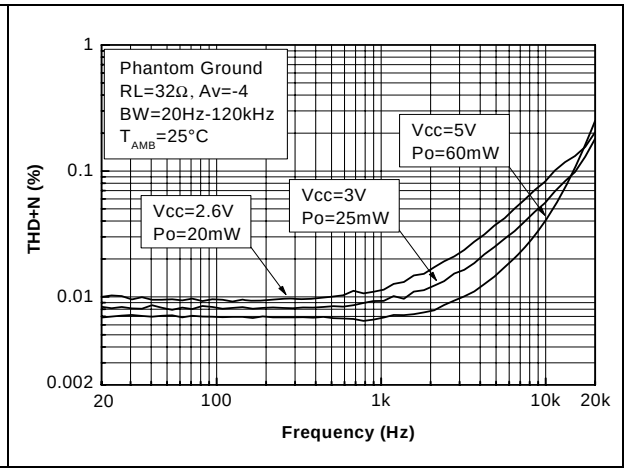


Figure 30. THD+N vs. frequency

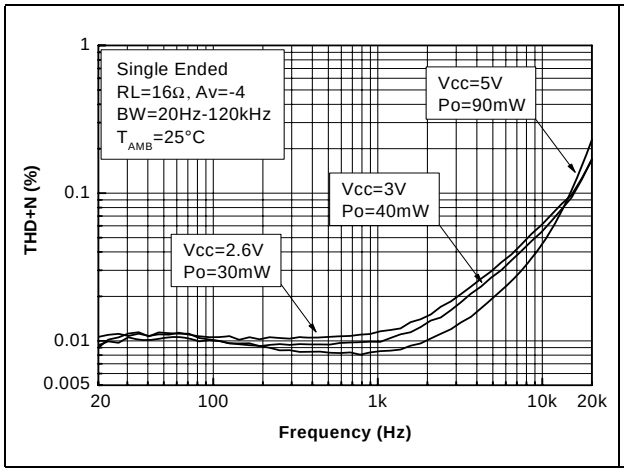


Figure 31. THD+N vs. frequency

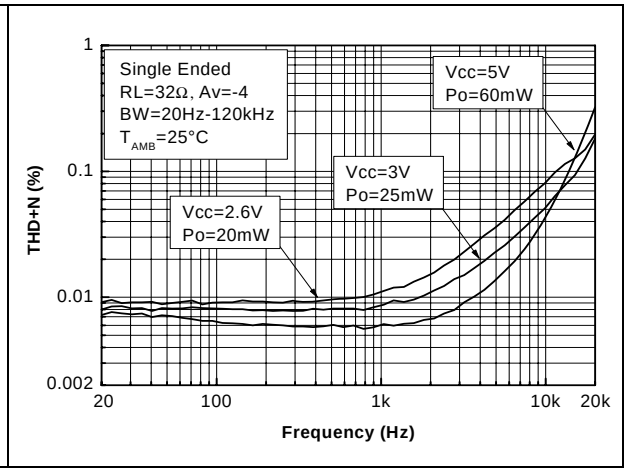


Figure 32. Output power vs. power supply voltage

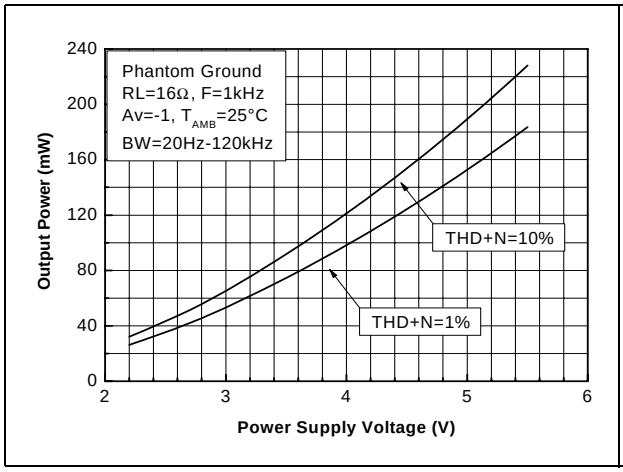


Figure 33. Output power vs. power supply voltage

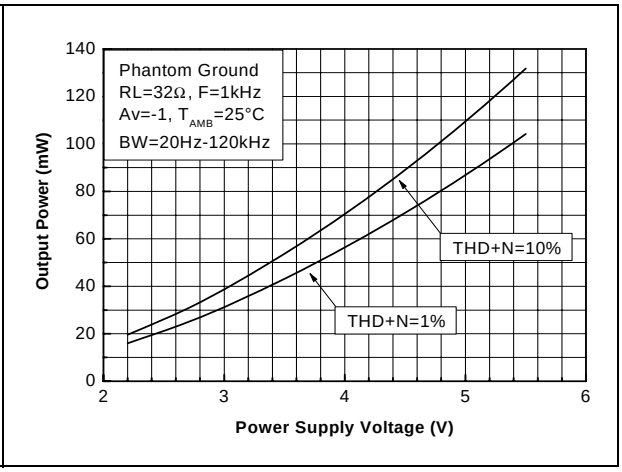


Figure 34. Output power vs. power supply voltage

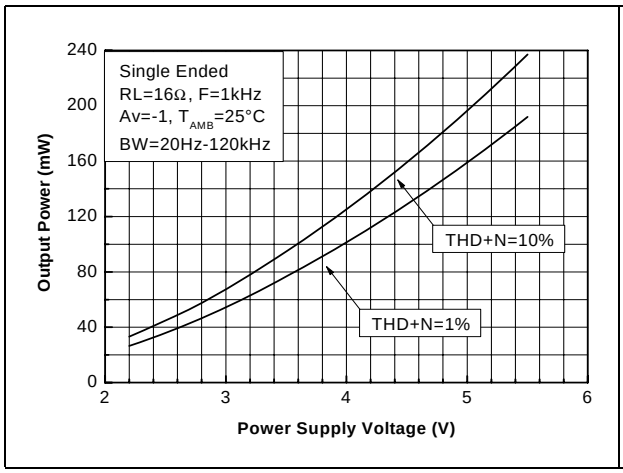


Figure 35. Output power vs. power supply voltage

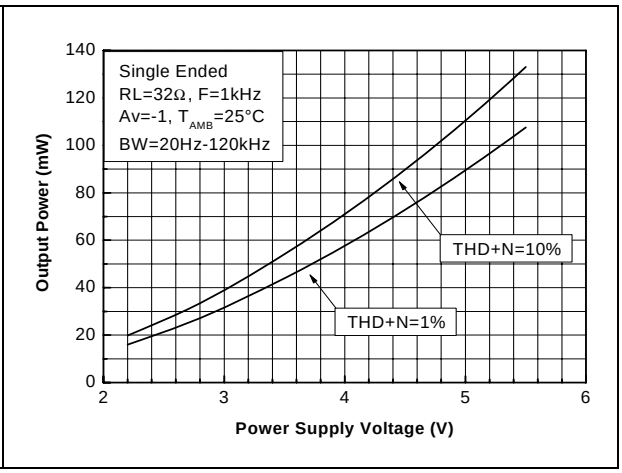


Figure 36. Output power vs. load resistance

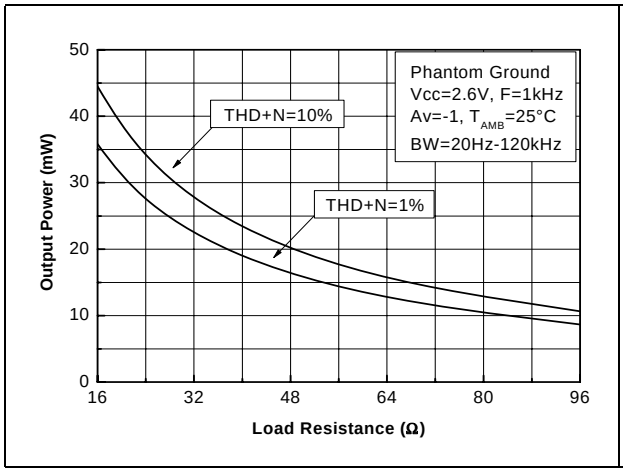


Figure 37. Output power vs. load resistance

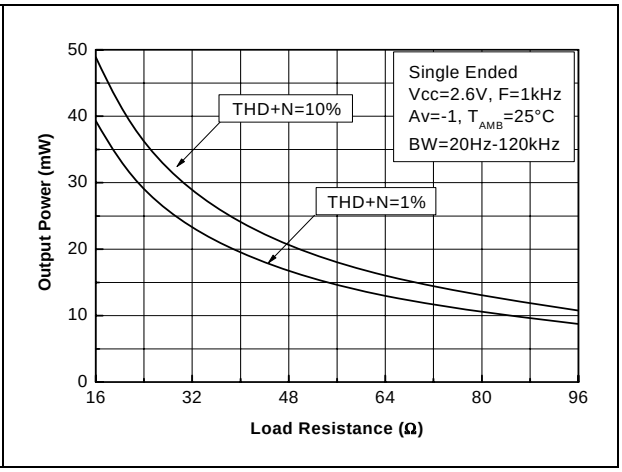


Figure 38. Output power vs. load resistance

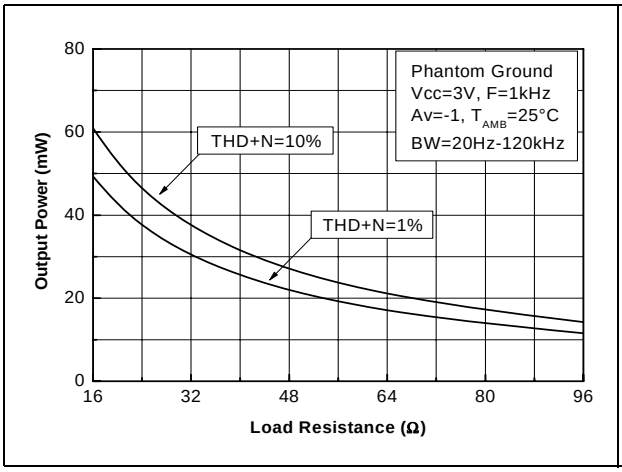


Figure 39. Output power vs. load resistance

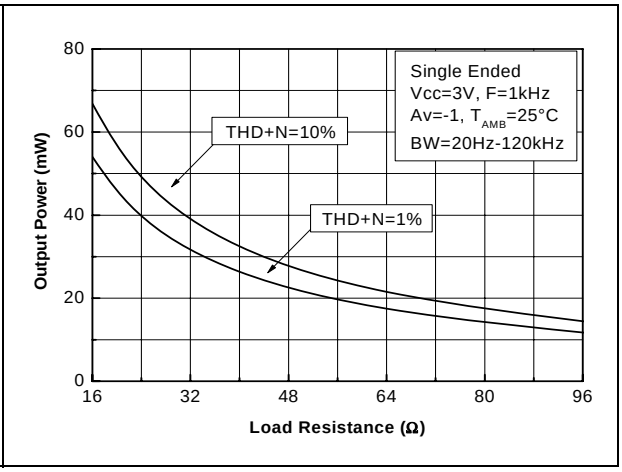


Figure 40. Output power vs. load resistance

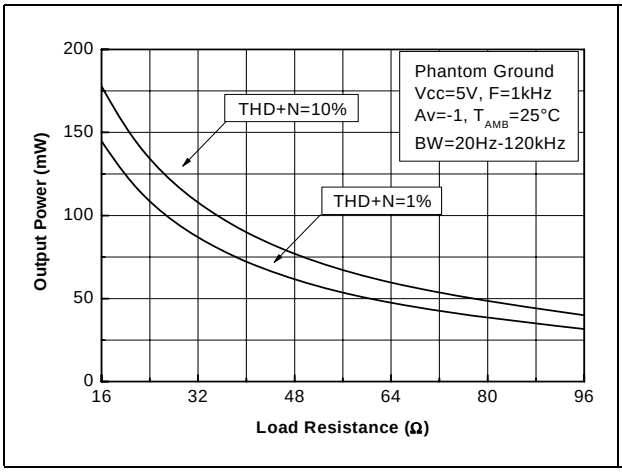


Figure 41. Output power vs. load resistance

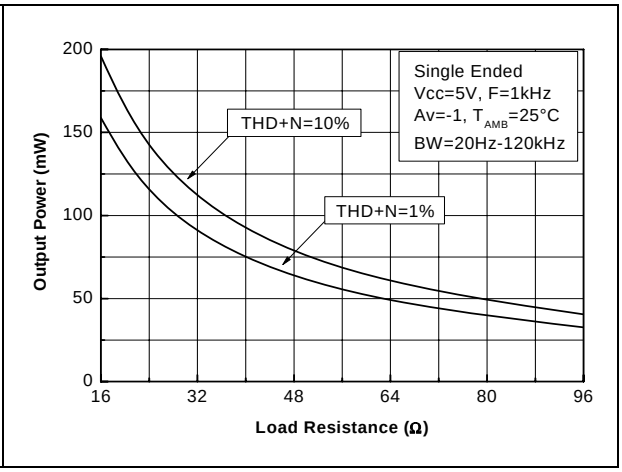


Figure 42. Power dissipation vs. output power

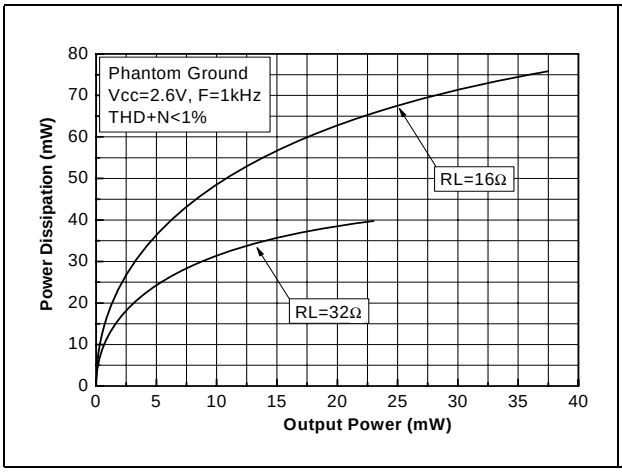


Figure 43. Power dissipation vs. output power

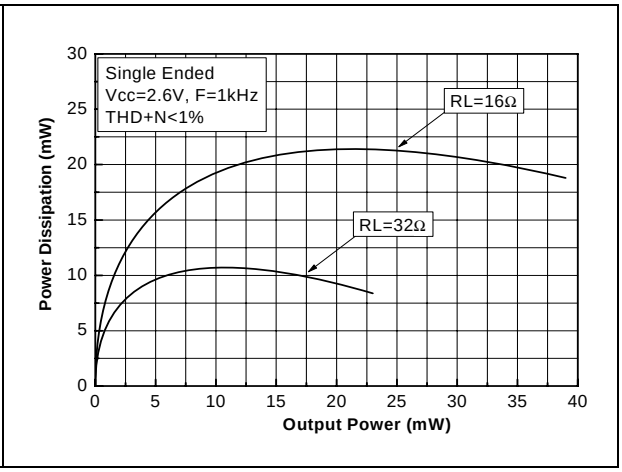


Figure 44. Power dissipation vs. output power

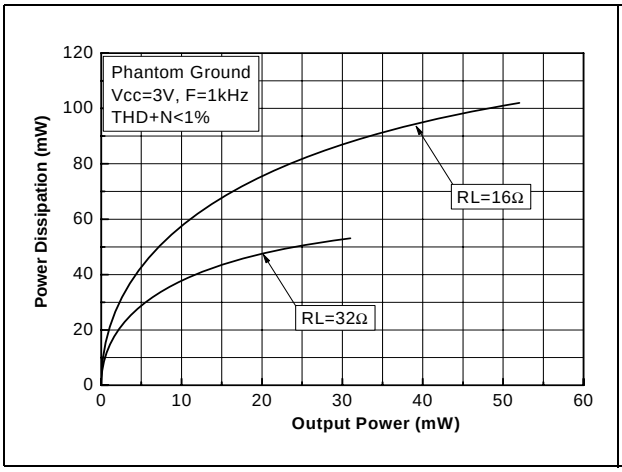


Figure 45. Power dissipation vs. output power

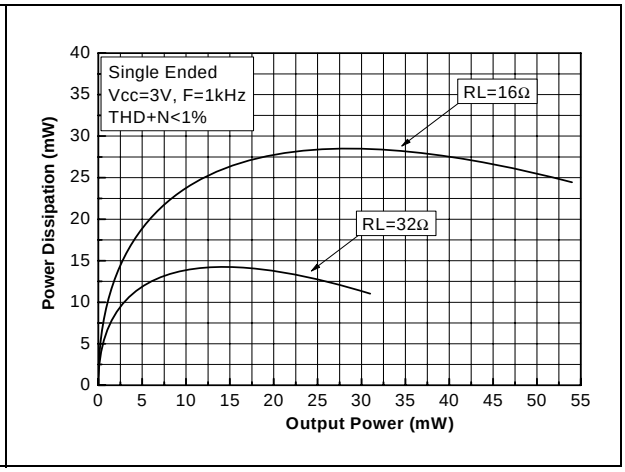


Figure 46. Power dissipation vs. output power

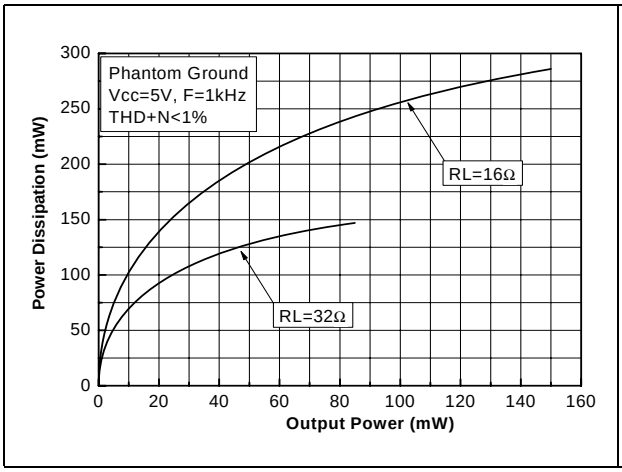


Figure 47. Power dissipation vs. output power

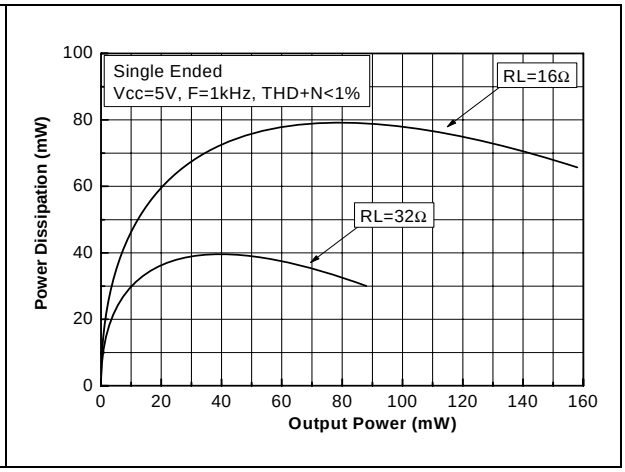


Figure 48. Crosstalk vs. frequency

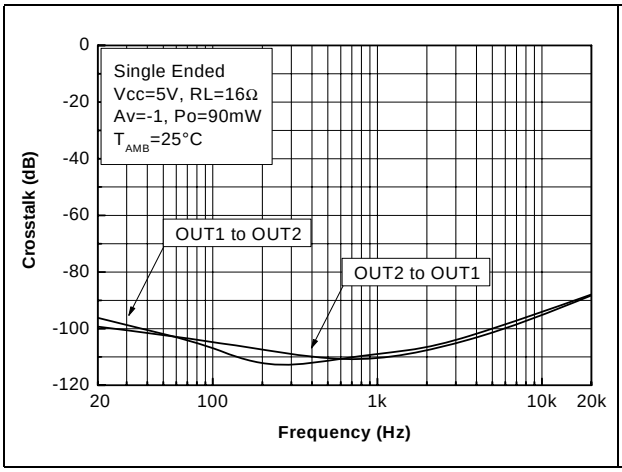


Figure 49. Crosstalk vs. frequency

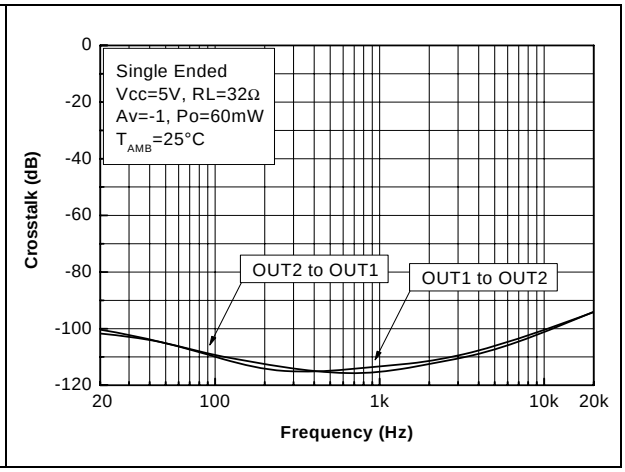


Figure 50. Crosstalk vs. frequency

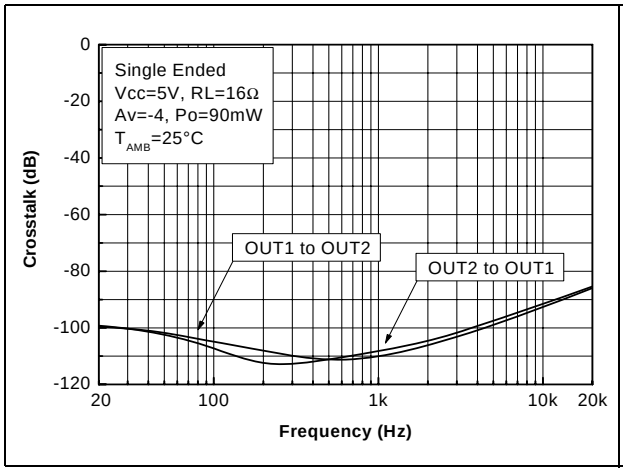


Figure 51. Crosstalk vs. frequency

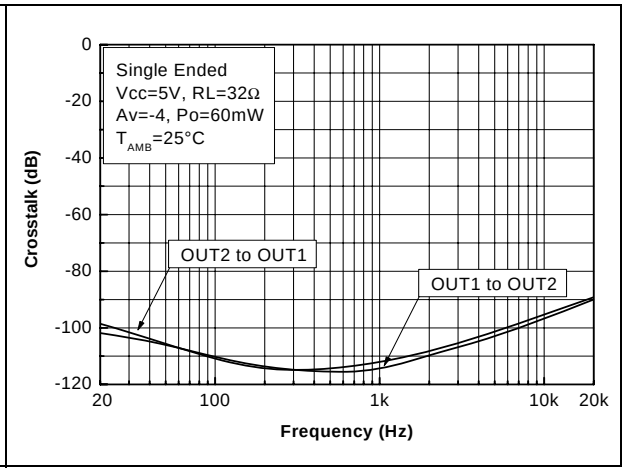


Figure 52. Crosstalk vs. frequency

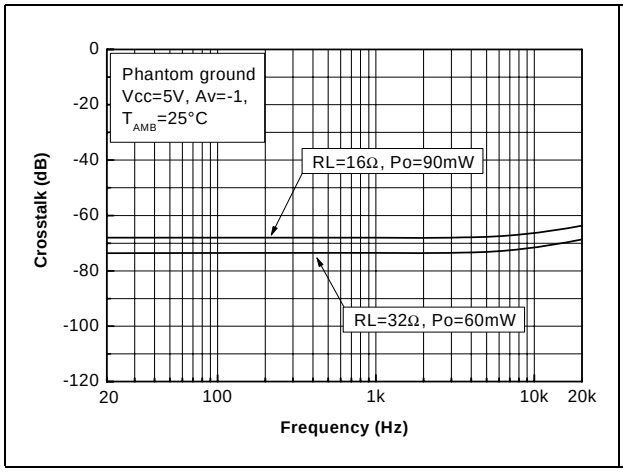


Figure 53. Crosstalk vs. frequency

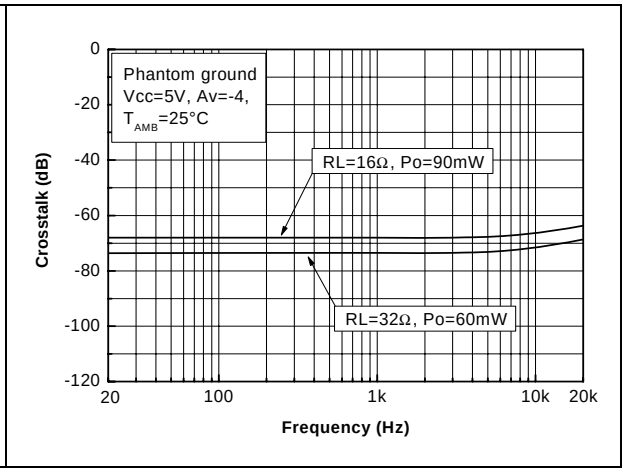


Figure 54. Signal to noise ratio vs. power supply voltage

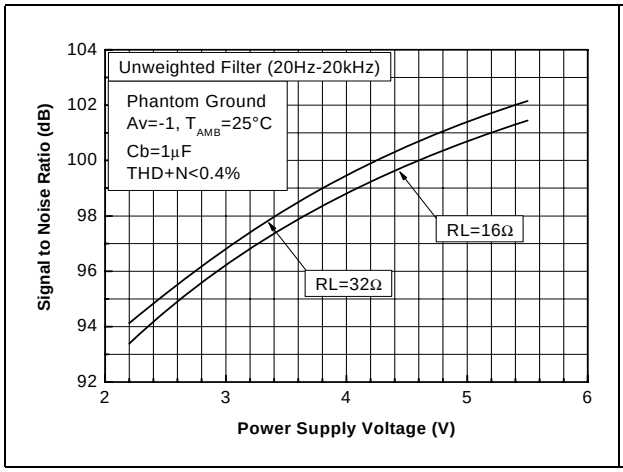


Figure 55. Signal to noise ratio vs. power supply voltage

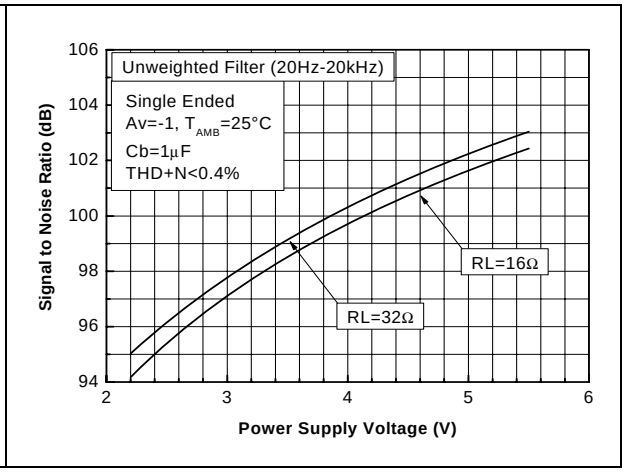


Figure 56. Signal to noise ratio vs. power supply voltage

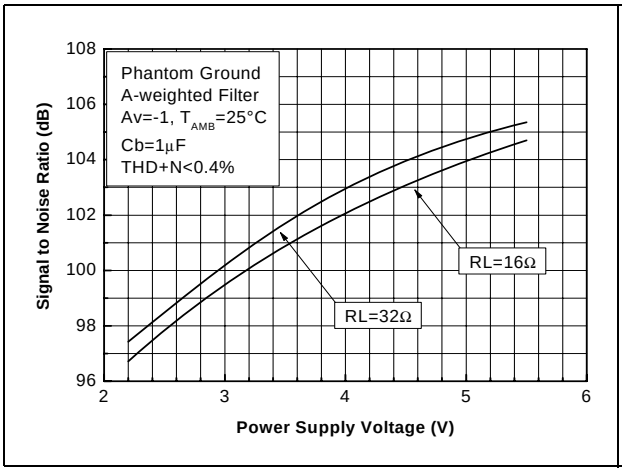


Figure 57. Signal to noise ratio vs. power supply voltage

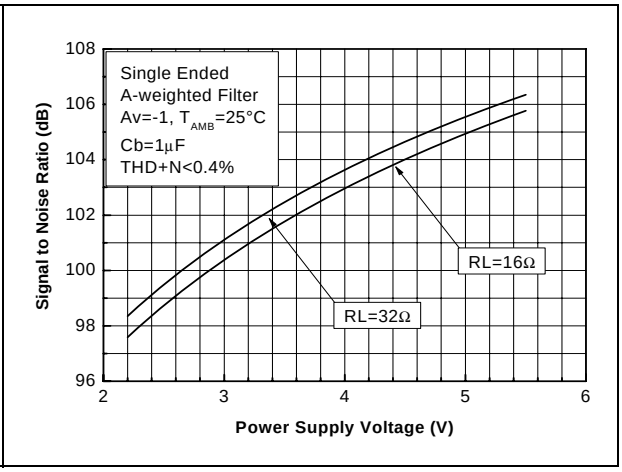


Figure 58. Signal to noise ratio vs. power supply voltage

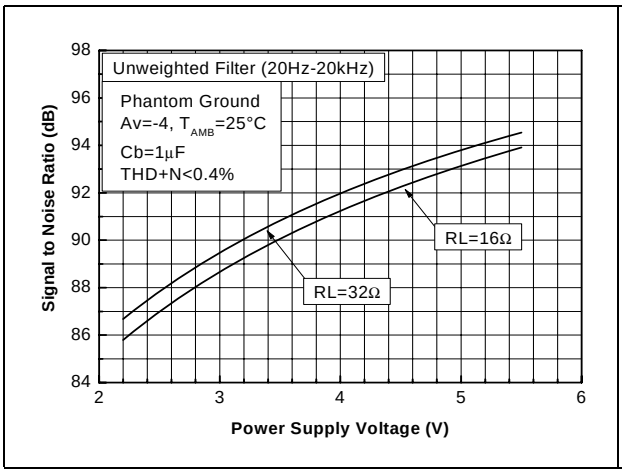


Figure 59. Signal to noise ratio vs. power supply voltage

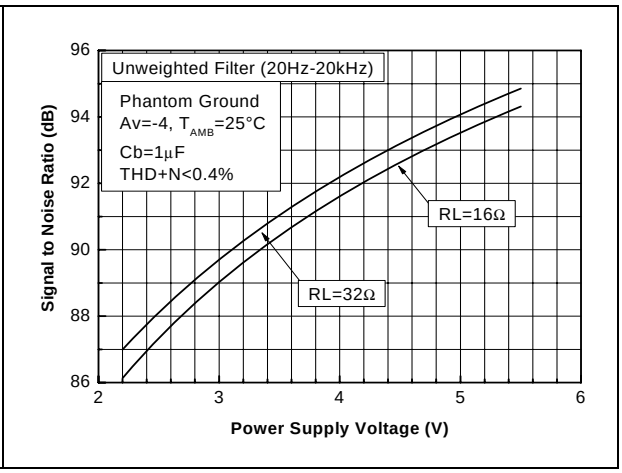


Figure 60. Signal to noise ratio vs. power supply voltage

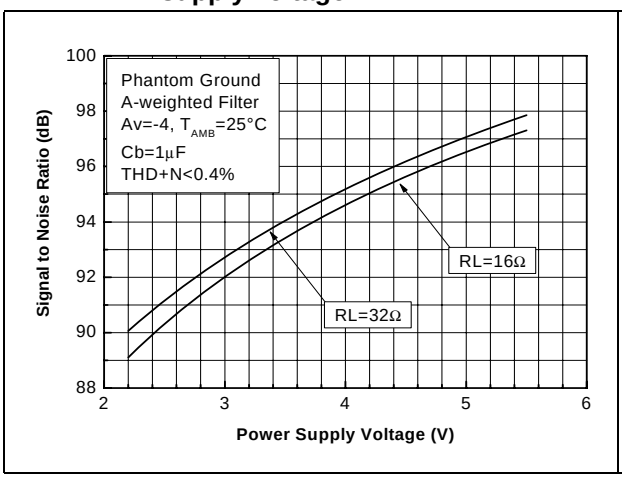


Figure 61. Signal to noise ratio vs. power supply voltage

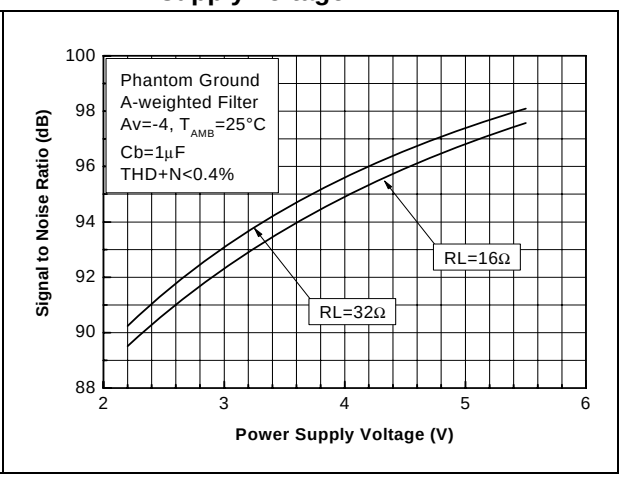


Figure 62. Power supply rejection ratio vs. frequency

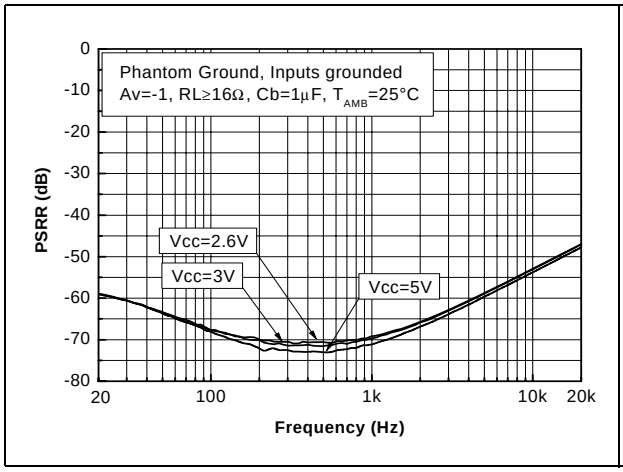


Figure 63. Power supply rejection ratio vs. frequency

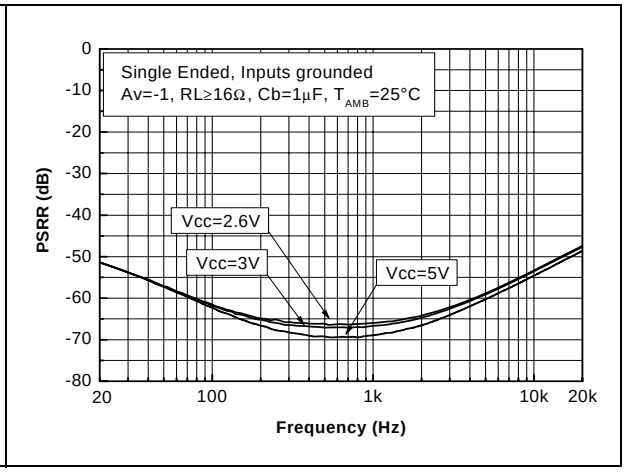


Figure 64. Power supply rejection ratio vs. frequency

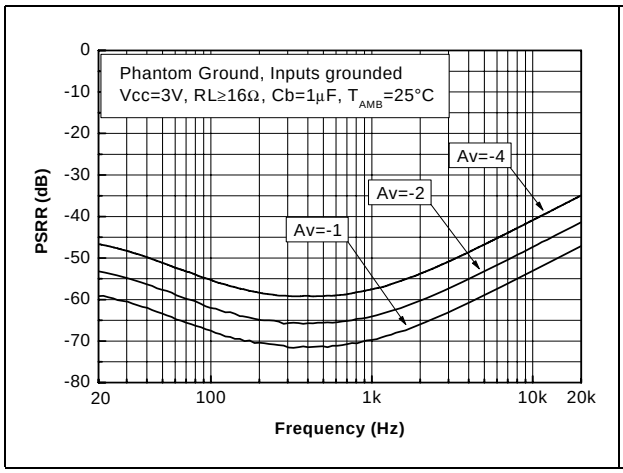


Figure 65. Power supply rejection ratio vs. frequency

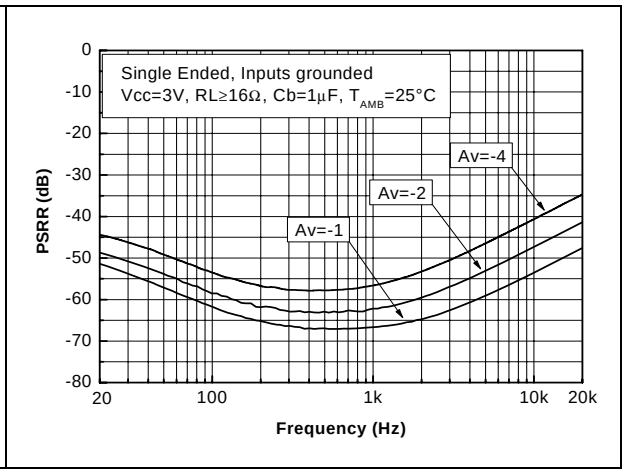


Figure 66. Power supply rejection ratio vs. frequency

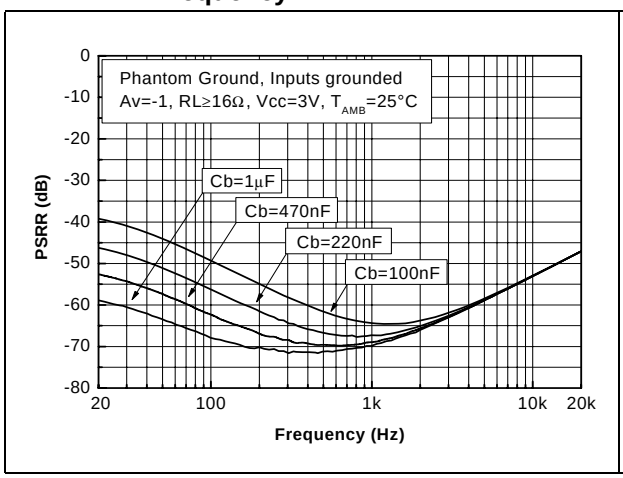


Figure 67. Power supply rejection ratio vs. frequency

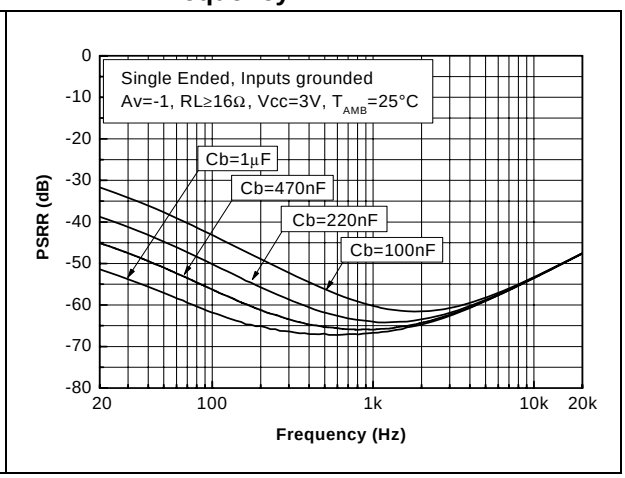


Figure 68. Current consumption vs. power supply voltage

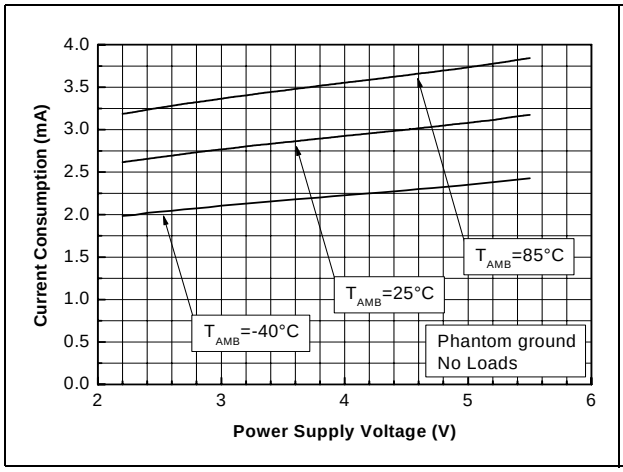


Figure 69. Current consumption vs. power supply voltage

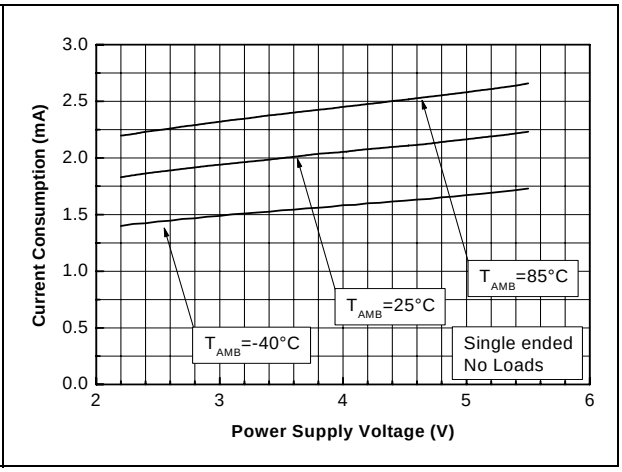


Figure 70. Current consumption vs. standby voltage

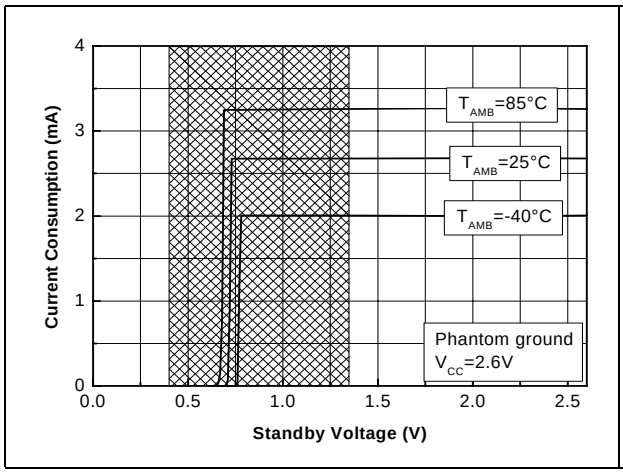


Figure 71. Current consumption vs. standby voltage

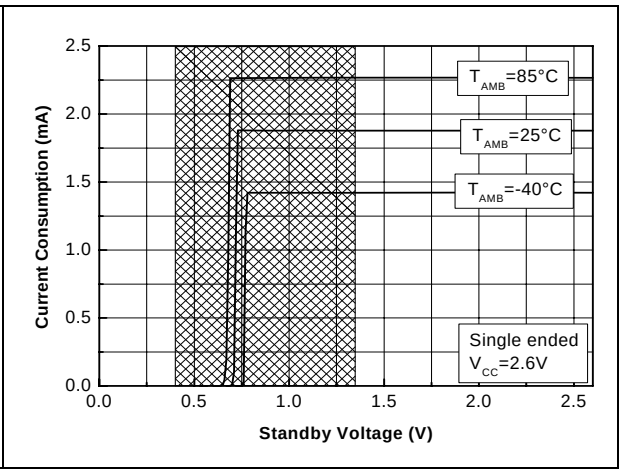


Figure 72. Current consumption vs. standby voltage

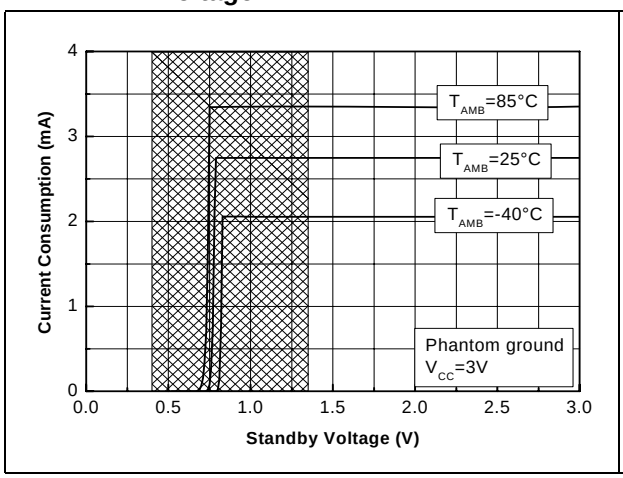


Figure 73. Current consumption vs. standby voltage

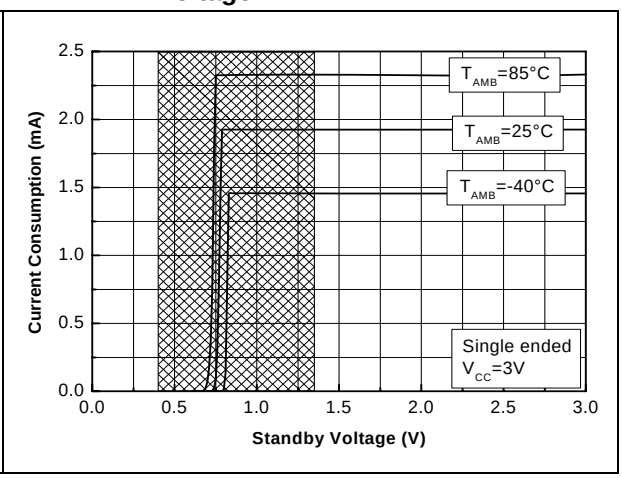


Figure 74. Current consumption vs. standby voltage

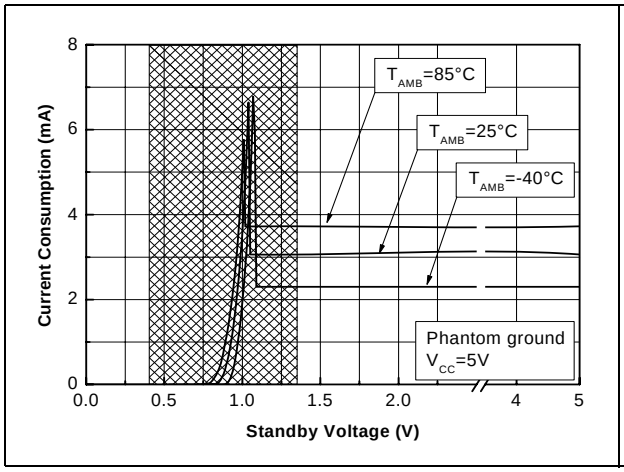


Figure 75. Current consumption vs. standby voltage

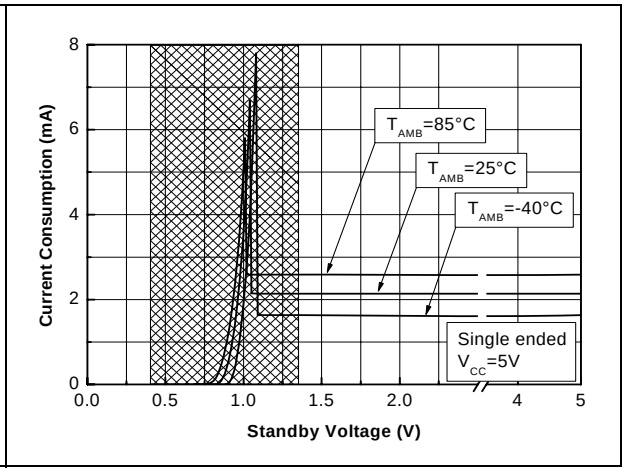
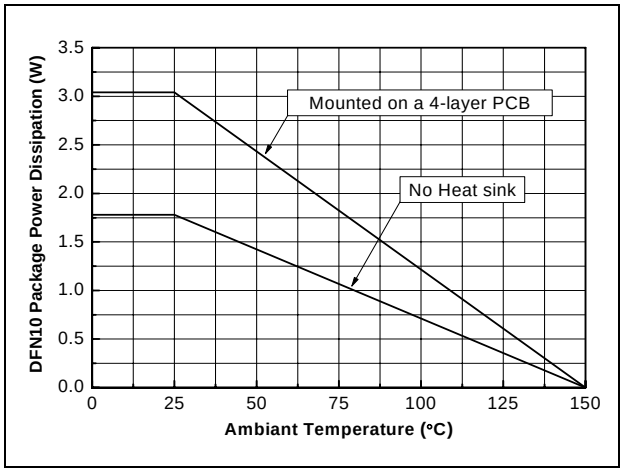


Figure 76. Power derating curves



4 Application information

4.1 General description

The TS4909 integrates two monolithic power amplifiers. The amplifier output can be configured to provide either single-ended (SE) capacitively-coupled output or phantom ground (PHG) capacitor-less output. *Figure 1: Typical applications for the TS4909 on page 3* shows schematics for each of these configurations.

Single-ended configuration

In the single-ended configuration, an output coupling capacitor, C_{out}, on the output of the power amplifier (V_{out1} and V_{out2}) is mandatory. The output of the power amplifier is biased to a DC voltage equal to $V_{CC}/2$ and the output coupling capacitor blocks this reference voltage.

Phantom ground configuration

In the phantom ground configuration, an internal buffer (V_{out3}) maintains the $V_{CC}/2$ voltage and the output of the power amplifiers are also biased to the $V_{CC}/2$ voltage. Therefore, no output coupling capacitors are needed. This is of primary importance in portable applications where space constraints are continually present.

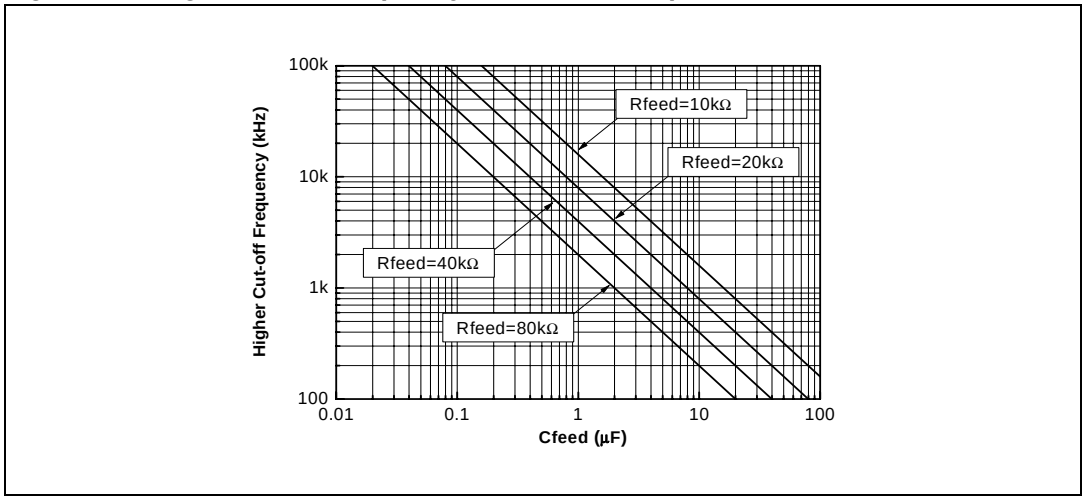
4.2 Frequency response

Higher cut-off frequency

In the high frequency region, you can limit the bandwidth by adding a capacitor C_{feed} in parallel with R_{feed}. It forms a low-pass filter with a -3dB cut-off frequency F_{CH}. Assuming that F_{CH} is the highest frequency to be amplified (with a 3dB attenuation), the maximum value of C_{feed} is:

$$F_{CH} = \frac{1}{2\pi \cdot R_{feed} \cdot C_{feed}}$$

Figure 77. Higher cut-off frequency vs. feedback capacitor



Lower cut-off frequency

The lower cut-off frequency F_{CL} of the TS4909 depends on input capacitors $C_{in1,2}$. In the single-ended configuration, F_{CL} depends on output capacitors $C_{out1,2}$ as well.

The input capacitor C_{in} in series with the input resistor R_{in} of the amplifier is equivalent to a first-order high-pass filter. Assuming that F_{CL} is the lowest frequency to be amplified (with a 3dB attenuation), the minimum value of C_{in} is:

$$C_{in} = \frac{1}{2\pi \cdot F_{CL} \cdot R_{in}}$$

In the single-ended configuration, the capacitor C_{out} in series with the load resistor R_L is equivalent to a first-order high-pass filter. Assuming that F_{CL} is the lowest frequency to be amplified (with a 3dB attenuation), the minimum value of C_{out} is:

$$C_{out} = \frac{1}{2\pi \cdot F_{CL} \cdot R_L}$$

Figure 78. Lower cut-off frequency vs. input capacitor

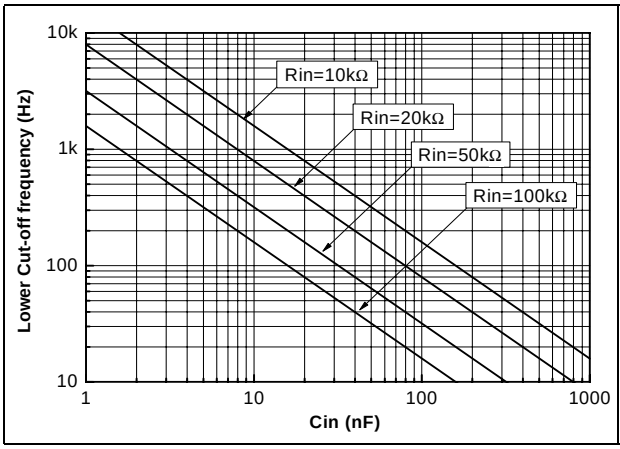
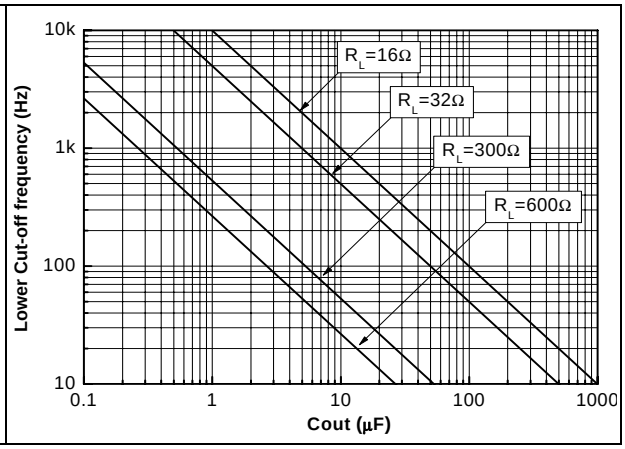


Figure 79. Lower cut-off frequency vs. output capacitor



Note: If F_{CL} is kept the same for calculation purposes, it must be taken in account that the 1st-order high-pass filter on the input and the 1st-order high-pass filter on the output create a 2nd-order high-pass filter in the audio signal path with an attenuation 6dB on F_{CL} and a roll-off of 40db／ decade.

4.3 Gain using the typical application schematics

In the flat region (no C_{in} effect), the output voltage of a channel is:

$$V_{OUT} = V_{IN} \cdot \left(-\frac{R_{feed}}{R_{in}}\right) = V_{IN} \cdot A_V$$

The gain A_V is:

$$A_V = -\frac{R_{feed}}{R_{in}}$$

Note: The configuration (either single-ended or phantom ground) has no effect on the value of the gain.

4.4 Power dissipation and efficiency

Hypotheses:

- Voltage and current (V_{out} and I_{out}) in the load are sinusoidal.
- Supply voltage (V_{CC}) is a pure DC source.

Regarding the load we have:

$$V_{OUT} = V_{PEAK}\sin\omega t(V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L}(A)$$

and

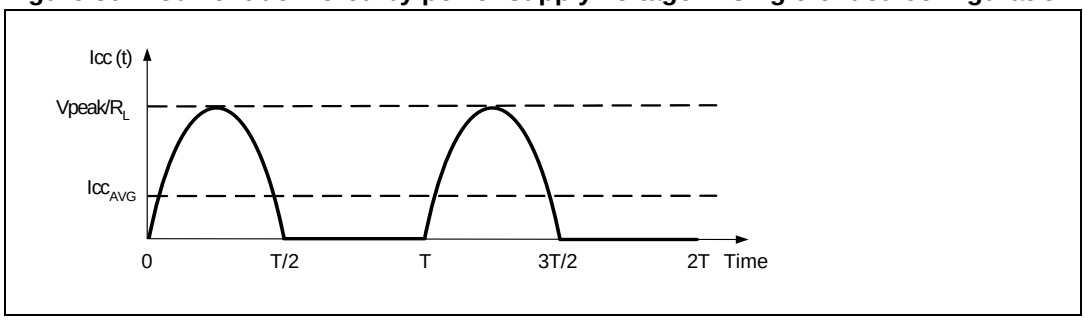
$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L}(A)$$

4.4.1 Single-ended configuration

The average current delivered by the power supply voltage is:

$$Icc_{AVG} = \frac{1}{2\pi}\int_0^{\pi}\frac{V_{PEAK}}{R_L}\sin(t)dt = \frac{V_{PEAK}}{\pi R_L}(A)$$

Figure 80. Current delivered by power supply voltage in single-ended configuration



The power delivered by the power supply voltage is:

$$P_{supply} = V_{CC}I_{CC_{AVG}}(W)$$

Therefore, the power dissipation by each power amplifier is

$$P_{diss} = P_{supply} - P_{OUT}(W)$$

$$P_{diss} = \frac{\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT}(W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{V_{CC}^2}{\pi^2 R_L}(W)$$

Note: This maximum value depends only on the power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{2V_{CC}}$$

The **maximum theoretical value** is reached when $V_{PEAK} = V_{CC}/2$, so:

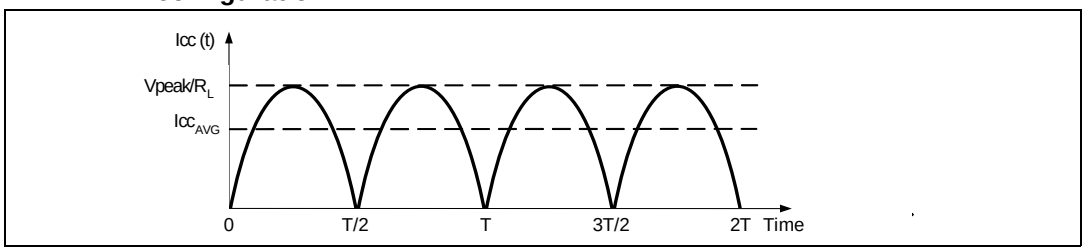
$$\eta = \frac{\pi}{4} = 78.5\%$$

4.4.2 Phantom ground configuration

The average current delivered by the power supply voltage is:

$$Icc_{AVG} = \frac{1}{\pi}\int_0^{\pi} \frac{V_{PEAK}}{R_L}\sin(t)dt = \frac{2V_{PEAK}}{\pi R_L}(A)$$

Figure 81. Current delivered by power supply voltage in phantom ground configuration



The power delivered by the power supply voltage is:

$$P_{supply} = V_{CC}I_{CC_{AVG}}(W)$$

Therefore, the power dissipation by each amplifier is

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT}(W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{2V_{CC}^2}{\pi^2 R_L}(W)$$

Note: This maximum value depends only on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The **maximum theoretical value** is reached when $V_{PEAK} = V_{CC}/2$, so:

$$\eta = \frac{\pi}{8} = 39.25\%$$

4.4.3 Total power dissipation

The TS4909 is a stereo (dual channel) amplifier. It has two independent power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows:

- $P_{diss\ 1}$ = power dissipation due to the first channel power amplifier (V_{out1}).
- $P_{diss\ 2}$ = power dissipation due to the second channel power amplifier (V_{out2}).
- Total $P_{diss} = P_{diss\ 1} + P_{diss\ 2}$ (W)

In most cases, $P_{diss\ 1} = P_{diss\ 2}$, giving:

$$TotalP_{diss} = 2P_{diss1} = 2P_{diss2}$$

Single-ended configuration:

$$TotalP_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - 2P_{OUT}$$

Phantom ground configuration:

$$TotalP_{diss} = \frac{4\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - 2P_{OUT}$$

4.5 Decoupling of the circuit

Two capacitors are needed to properly bypass the TS4909 — a power supply capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has a strong influence on the THD+N at high frequencies (above 7kHz) and indirectly on the power supply disturbances. With 1 µF, you could expect the THD+N performance to be similar to the values shown in this datasheet. If C_s is lower than 1 µF, THD+N increases at high frequencies and disturbances on the power supply rail are less filtered. On the contrary, if C_s is higher than 1 µF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N at lower frequencies, but its value is critical on the final result of PSRR with inputs grounded in lower frequencies:

- If C_b is lower than 1 µF, THD+N increases at lower frequencies and the PSRR worsens (increases).
- If C_b is higher than 1 µF, the benefit on THD+N and PSRR in the lower frequency range is small.

4.6 Wake-up time

When the standby is released to turn the device ON, the bypass capacitor C_b is charged immediately. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage plus a time delay of 40ms (pop precaution) is called the wake-up time or t_{WU}. It is specified in the electrical characteristics tables with C_b=1µF (see *Section 3: Electrical characteristics on page 5*).

If C_b has a value other than 1µF, you can calculate t_{WU} by using the following formulas, or read it directly from the graph in *Figure 82*.

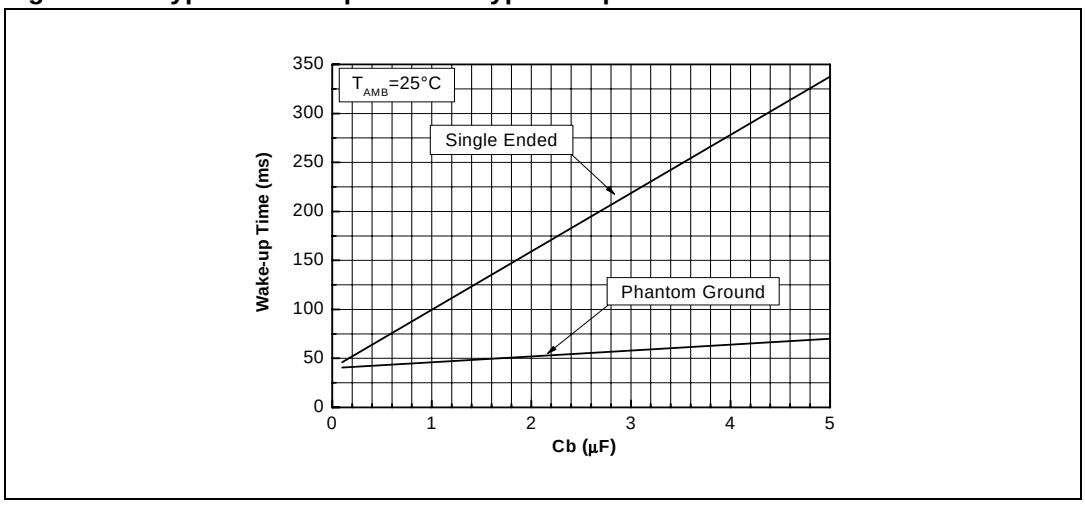
- Single-ended configuration

$$t_{WU} = \frac{Cb \cdot 2.5}{0.042} + 40 \quad [ms;\mu F]$$

- Phantom ground configuration

$$t_{WU} = \frac{Cb \cdot 2.5}{0.417} + 40 \quad [ms;\mu F]$$

Figure 82. Typical wake-up time vs. bypass capacitance



Note: It is assumed the C_b voltage is equal to 0 V. If the C_b voltage is not equal 0 V, the wake-up time is lower.

4.7 Pop performance

Pop performance in the phantom ground configuration is closely linked with the size of the input capacitor C_{in}. The size of C_{in} is dependent on the lower cut-off frequency and PSRR values requested.

In order to reach low pop, C_{in} must be charged to $V_{CC}/2$ in less than 40ms. To follow this rule, the equivalent input constant time ($R_{in}C_{in}$) should be less then 8ms:

$$\tau_{in} = R_{in} \times C_{in} < 0.008 \text{ s}$$

By following the previous rules, the TS4909 can reach low pop even with a high gain such as 20dB.

Example calculation:

With R_{in} = 20kΩ and F_{CL} = 20Hz, -3db low cut-off frequency, C_{in} = 398nF. So, C_{in} = 390nF with standard value which gives a lower cut-off frequency equal to 20.4Hz.

In this case,

$$\tau_{in} = R_{in} \times C_{in} = 7.8ms$$

This value is sufficient with regards to the previous formula, so we can state that the pop will be imperceptible.

Connecting the headphones

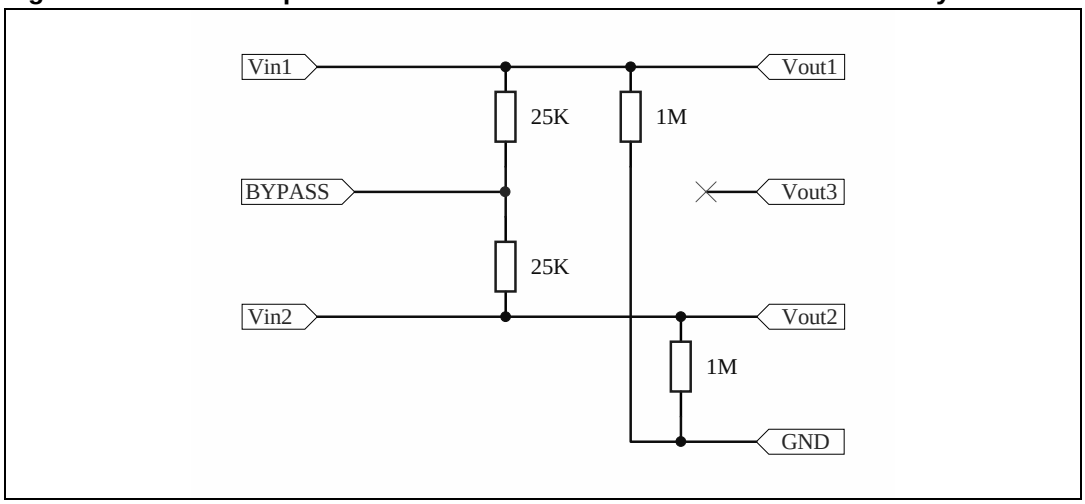
Generally headphones are connected using a jack connector. To prevent pop in the headphones while plugging in the jack, a pulldown resistor should be connected in parallel with each headphone output. This allows the capacitors C_{out} to be charged even when no headphones are plugged in.

A resistor of 1 kΩ is high enough to be a negligible load, and low enough to charge the capacitors C_{out} in less than one second.

4.8 Standby mode

When the TS4909 is in standby mode, the time required to put the output stages (V_{out1}, V_{out2} and V_{out3}) into a high impedance state with reference to ground, and the internal circuitry in standby mode, is a few microseconds.

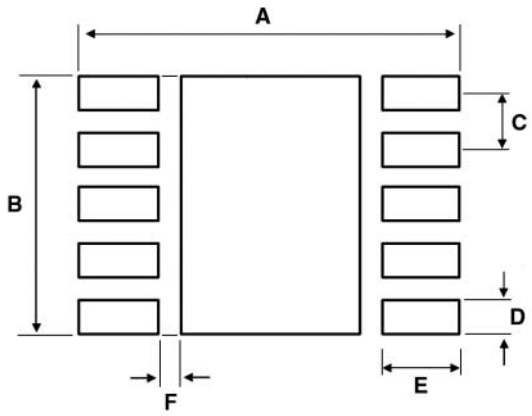
Figure 83. Internal equivalent circuit schematics of the TS4909 in standby mode



5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

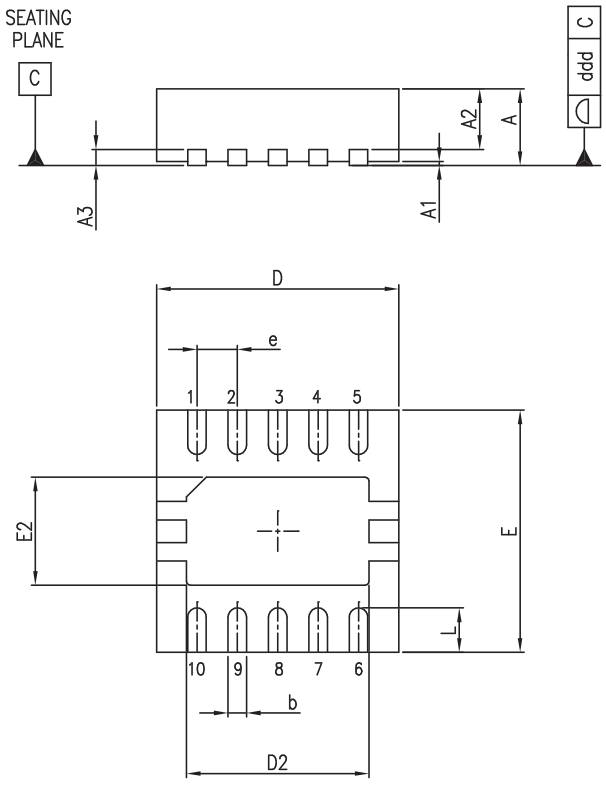
Figure 84. TS4909 footprint recommendation



FOOTPRINT DATA	
	mm
A	3.40
B	2.30
C	0.50
D	0.30
E	0.70
F	0.20

Figure 85. DFN10 3x3 exposed pad package mechanical data

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			25.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.21	2.26	2.31	87.0	89.0	91.0
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.3	0.4	0.5	11.8	15.7	19.7



6 Ordering information

Table 8. Order code

Part number	Temperature range	Package	Packing	Marking
TS4909IQT	-40°C to +85°C	DFN10	Tape & reel	K909

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
1-Dec-2006	6	Release to production of the device.
2-Jan-2007	7	Correction of revision number of December revision (revision 6 instead of revision 5).
26-Sep-2007	8	Updated *Table 2: Absolute maximum ratings*.

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