Features

- **EE Programmable 1,048,576 x 1-bit Serial Memory Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **Very Low-power CMOS EEPROM Process**
- **In-System Programmable (ISP) via Two-Wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with AT40K Devices**
- **Cascadable Read-back to Support Additional Configurations or Higher-density Arrays**
- **Programmable Reset Polarity**
- **Low-power Standby Mode**
- **High-reliability**
  - **Endurance: 5,10^4 Read Cycles**
  - **Data Retention: 10 Years**
- **No Single Event Latch-up below a LET Threshold of 80 MeV/mg/cm^2**
- **Tested up to a Total Dose of (according to MIL STD 883 Method 1019)**
  - **20 krads (Si) Read-only mode when Biased**
  - **60 krads (Si) Read-only mode when Unbiased**
- **Operating Range: 3.0V to 3.6V, -55°C to +125°C**
- **Available in 400 mils Wide 28 Pins DIL Flat Pack**

Description

The AT17LV010-10DP is a FPGA Configuration Serial EEPROM provides an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. It is packaged in the 28-pin 400 mils wide FP package. Configurator uses a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes. The device also supports a write-protection mechanism within its programming mode.

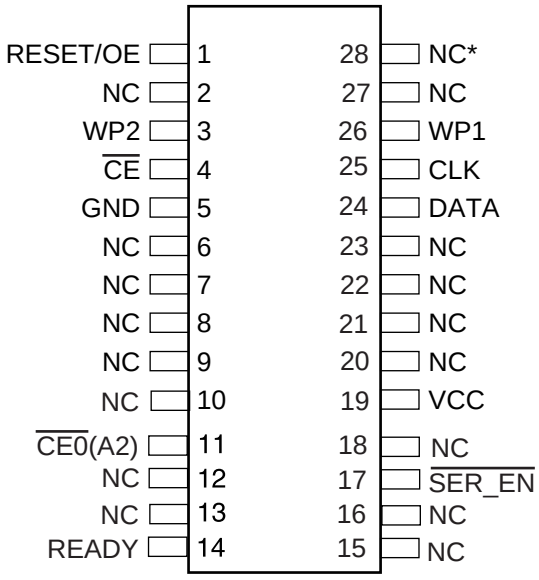
Space FPGA Configuration EEPROM

AT17LV010-10DP

Rev. 4265C–AERO–05/05

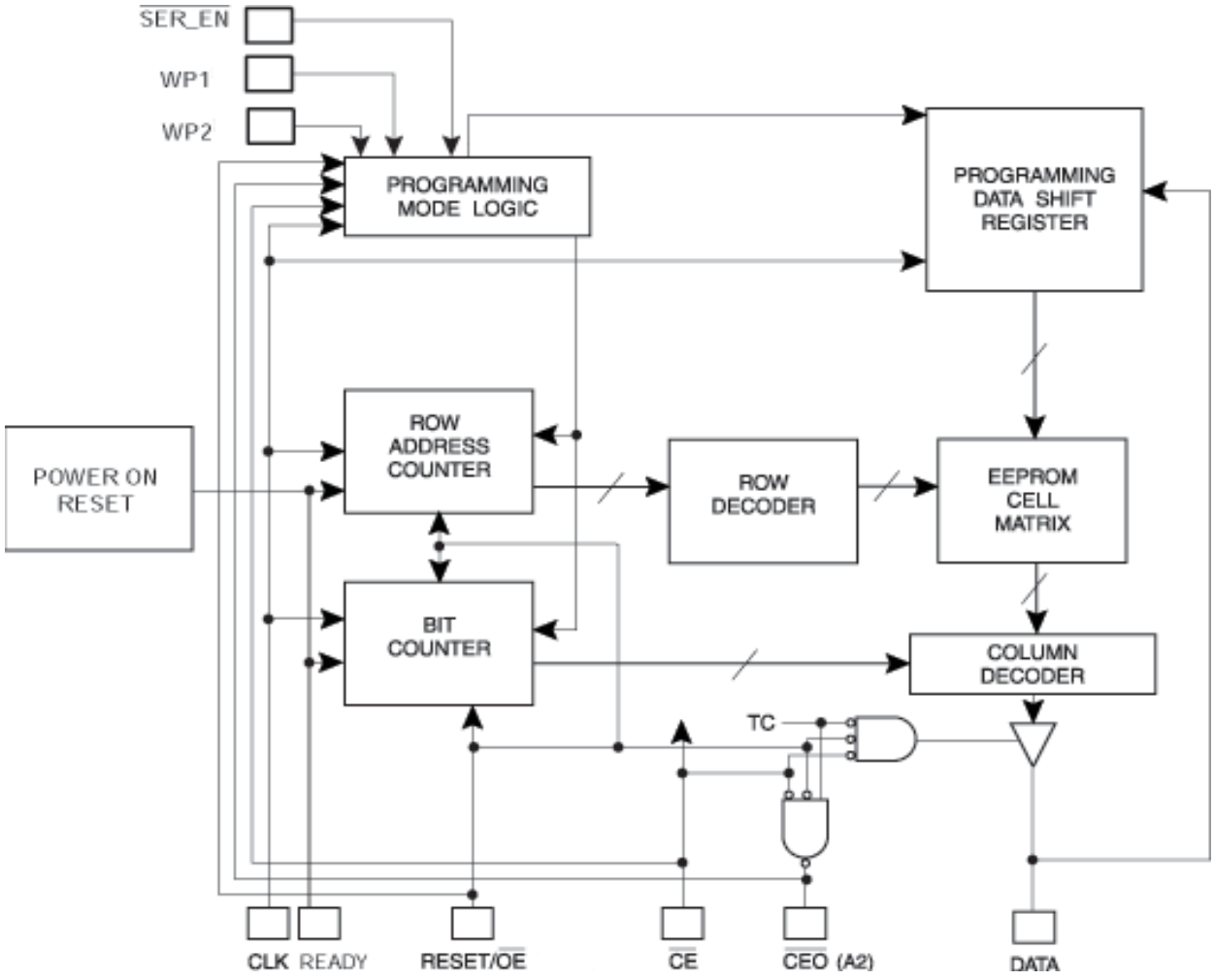
Pin Configuration

Figure 1. 28-pin Flat Pack



Note: * indicates this pin must not be used.

Block Diagram



Device Description

The control signals for the configuration EEPROM ($\overline{CE}$, RESET/$\overline{OE}$ and CCLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM RESET/$\overline{OE}$ and $\overline{CE}$ pins control the tri-state buffer on the DATA output pin and enable the address counter. When RESET/$\overline{OE}$ is driven High, the configuration EEPROM resets its address counter and tri-states its DATA pin. The $\overline{CE}$ pin also controls the output of the AT17LV010-10DP configurator. If $\overline{CE}$ is held High after the RESET/$\overline{OE}$ reset pulse, the counter is disabled and the DATA output pin is tri-stated. When $\overline{OE}$ is subsequently driven Low, the counter and the DATA output pin are enabled. When RESET/$\overline{OE}$ is driven High again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of $\overline{CE}$.

When the configurator has driven out all of its data and $\overline{CEO}$ is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This is the default setting for the device. Since almost all FPGAs use RESET Low and OE High, this document will describe $\overline{RESET}$/OE.

Pin Description

DATA Tri-state DATA output for configuration. Open-collector bi-directional pin for programming.

CLK Clock input. Used to increment the internal address and bit counter for reading and programming.

WP1 WRITE PROTECT (1). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations.

RESET/$\overline{OE}$ Output Enable (active High) and RESET (active Low) when $\overline{SER\_EN}$ is High. A Low level on RESET/OE resets both the address and bit counters. A High level (with $\overline{CE}$ Low) enables the data output driver. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. For most applications, RESET should be programmed active Low. This document describes the pin as $\overline{RESET}$/OE.

WP2 WRITE PROTECT (2). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations.

$\overline{CE}$ Chip Enable input (active Low). A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the Two-Wire Serial Programming mode ($\overline{SER\_EN}$ Low).

GND Ground pin. A 0.2 µF decoupling capacitor between V_{CC} and GND is recommended.

$\overline{CEO}$ Chip Enable Output (active Low). This output goes Low when the address counter has reached its maximum value. In a daisy chain of AT17LV010-10DP devices, the $\overline{CEO}$ pin of one device must be connected to the $\overline{CE}$ input of the next device in the chain. It will stay Low as long as $\overline{CE}$ is Low and OE is High. It will then follow CE until OE goes Low; thereafter, $\overline{CEO}$ will stay High until the entire EEPROM is read again.

A2 Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{SER\_EN}$ is Low). A2 has an internal pull-down resistor.

READY Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. It is recommended to use a 4.7 kΩ pull-up resistor when this pin is used.

$\overline{SER\_EN}$ Serial enable must be held High during FPGA loading operations. Bringing $\overline{SER\_EN}$ Low enables the Two-Wire Serial Programming Mode. For non-ISP applications, $\overline{SER\_EN}$ should be tied to V_{CC}.

V_{CC} 3.3V (±0.3V).

FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17LV Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

This document discusses the Atmel AT40KEL applications.

Control of Configuration

Most connections between the FPGA device and the AT17LV Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17LV010-10DP configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17LV010-10DP configurator.
- The $\overline{CEO}$ output of any AT17LV010-10DP configurator drives the $\overline{CE}$ input of the next configurator in a cascaded chain of EEPROMs.
- $\overline{SER\_EN}$ must be connected to V_{CC} (except during ISP).
- The READY pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.

Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the clock signal to the configurator asserts its $\overline{CEO}$ output Low and disables its DATA line driver. The second configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the $\overline{RESET}$/OE on each configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the $\overline{RESET}$/OE input can be tied to its inactive (High) level.

AT17LV010-10DP Reset Polarity

The AT17LV010-10DP configurator allows the user to program the reset polarity as either $\overline{RESET}$/OE or RESET/$\overline{OE}$. This feature is supported by industry-standard programmer algorithms.

Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ Low. In this mode the chip can be programmed by the Two-Wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. For more information see application note:

http://www.atmel.com/dyn/resources/prod_documents/doc0437.pdf

Standby Mode

The AT17LV010-10DP configurator enter a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the AT17LV010-10DP configurator consumes less than 100 µA of current at 3.3V. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Electrical Characteristics

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{DD} +0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Conditions

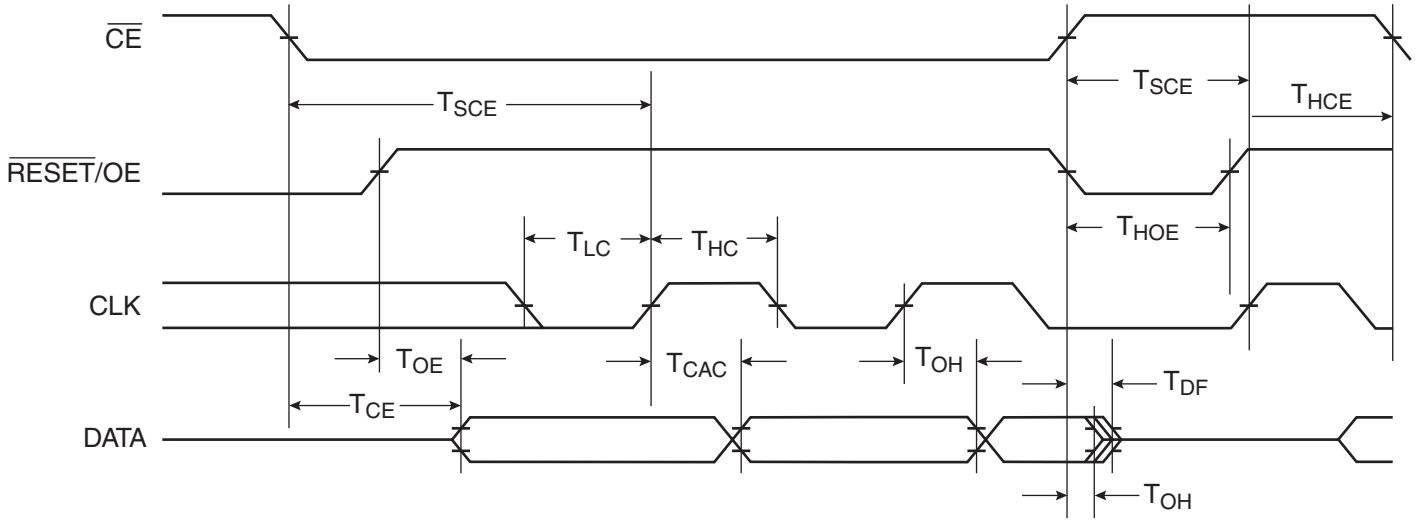
Symbol	Description	3.3V		Units
		Min	Max	
V_{DD}	-55 to +125°C	3.0	3.6	V

DC Characteristics

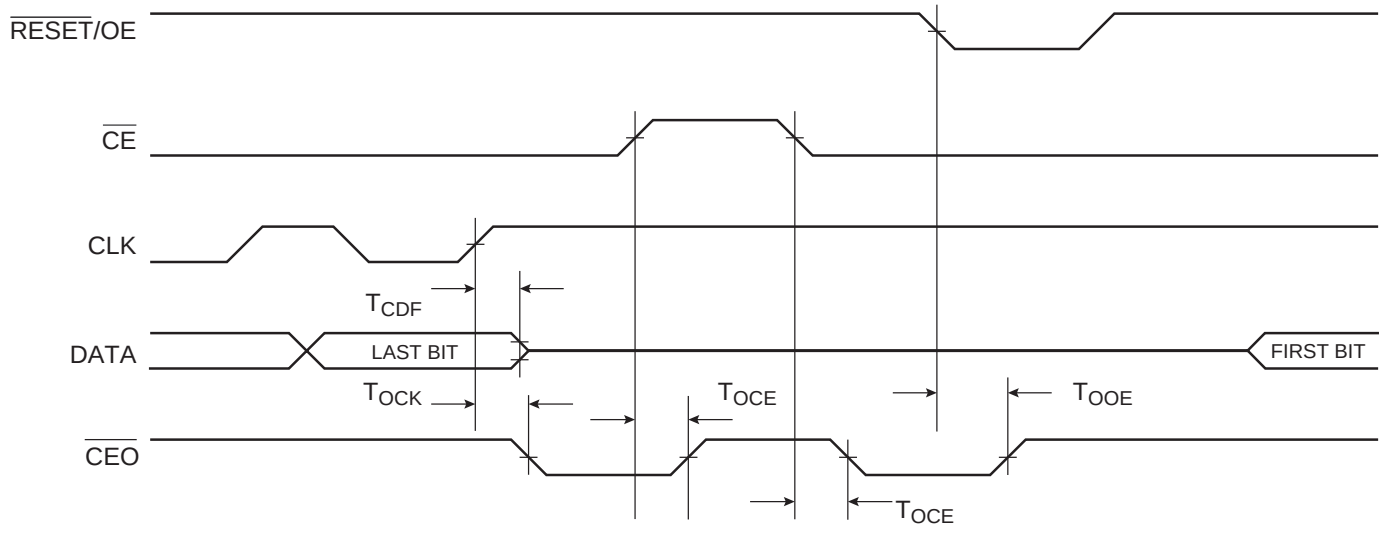
V_{DD} = 3.3V ± 0.3V

Symbol	Description	AT17LV010-10DP		Units
		Min	Max	
V_{IH}	High-level Input Voltage	2.0	V_{DD}	V
V_{IL}	Low-level Input Voltage	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)		0.4	V
I_{CCOP}	Supply Current, Active Mode		5	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{DD} or GND)	-10	10	µA
I_{CCS}	Supply Current, Standby Mode		150	µA

AC Characteristics



AC Characteristics when Cascading



AC Characteristics

V_{CC} = 3.3V ± 0.3V

Symbol	Description	Military		Units
		Min	Max	
T_{OE}[1]	OE to Data Delay		55	ns
T_{CE}[1]	$\overline{CE}$ to Data Delay		60	ns
T_{CAC}[1]	CLK to Data Delay		60	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		ns
T_{DF}[2]	$\overline{CE}$ or OE to Data Float Delay		50	ns
T_{LC}	CLK Low Time	25		ns
T_{HC}	CLK High Time	25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	25		ns
F_{MAX}	Maximum Clock Frequency		10	MHz

Notes: 1. AC test lead = 60 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics when Cascading

V_{CC} = 3.3V ± 0.3V

Symbol	Description	Military		Units
		Min	Max	
T_{CDF}[2]	CLK to Data Float Delay		50	ns
T_{OCK}[1]	CLK to $\overline{CEO}$ Delay		55	ns
T_{OCE}[1]	$\overline{CE}$ to $\overline{CEO}$ Delay		40	ns
T_{OOE}[1]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		40	ns
F_{MAX}	Maximum Clock Frequency		10	MHz

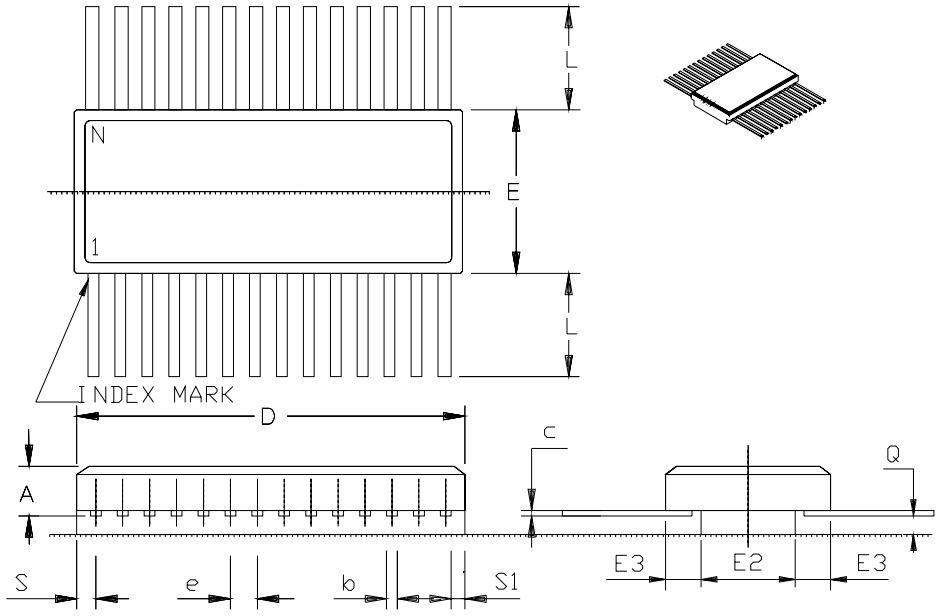
Notes: 1. AC test lead = 60 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

Ordering Information

Memory Size	Ordering Code	Package	Operation Range
1 Mbit	AT17LV010-10DP-E	28-pin Flat Pack	Engineering Samples
1 Mbit	AT17LV010-10DP-MQ	28-pin Flat Pack	Military Level B
1 Mbit	AT17LV010-10DP-SV	28-pin Flat Pack	Space Level B

Packaging Information

DP (FP28.4)



	MM		INCH	
	Min	Max	Min	Max
A	2.29	3.30	.090	.130
b	0.38	0.48	.015	.019
c	0.08	0.15	.003	.006
D	---	18.80	---	.740
E	9.65	10.67	.380	.420
E2	4.57	---	.180	---
E3	0.76	---	.030	---
e	1.27 BSC		.050 BSC	
L	6.35	9.40	.250	.370
Q	0.66	---	.026	---
S	---	1.30	---	.051
S1	0.00	---	.000	---
N	28		28	

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