Ordering number : ENA0945

SANYO Semiconductors
DATA SHEET

LA5751 — Monolithic Linear IC
Separately-excited Step-down Switching Regulator (3.3V)

Overview

The LA5751 is a separately-excited step-down switching regulator (3.3V).

Features

- High efficiency
- Four external parts
- Time-base generator (60kHz) incorporated
- Current limiter incorporated
- Thermal shutdown circuit incorporated
- Soft start circuit incorporated

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{IN} max		30	V
Output current	I_O max		3	A
SW pin application reverse voltage	Vsw		-1	V
Allowable power dissipation	Pd max1	Infinite heat sink.	7.5	W
	Pd max2	No heat sink.	1.75	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-30 to +125	°C
Storage temperature	Tstg		-40 to +150	°C

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage range	V_{IN}		5.5 to 28	V
Operating junction temperature range	Tj op		-30 to +150	°C

Electrical Characteristics at Ta = 25°C

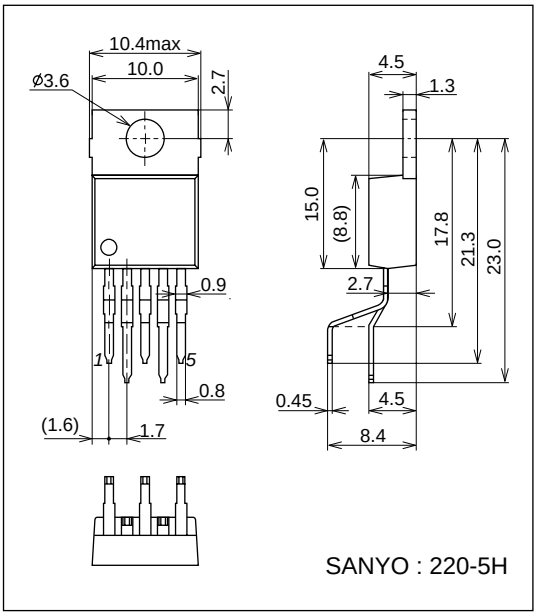
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output voltage	V_O	V_{IN} = 15V, I_O = 1.0A	3.17	3.30	3.43	V
Efficiency	η	V_{IN} = 15V, I_O = 1.0A		79		%
Switching frequency	f	V_{IN} = 15V, I_O = 1.0A	48	60	72	kHz
Line regulation	ΔVOLINE	V_{IN} = 8 to 20V, I_O = 1.0A		25	80	mV
Load regulation	ΔVOLOAD	V_{IN} = 15V, I_O = 0.5 to 1.5A		10	30	mV
Output voltage temperature coefficient	ΔVO/ΔTa			±0.5		mV/°C
Ripple attenuation factor	RREJ	f = 100 to 120Hz		45		dB
Current limiter operating voltage	IS	V_{IN} = 15V	3.1			A
Thermal shutdown operating temperature	TSD	Designed target value*		165		°C
Thermal shutdown hysteresis width	ΔTSD	Designed target value*		15		°C

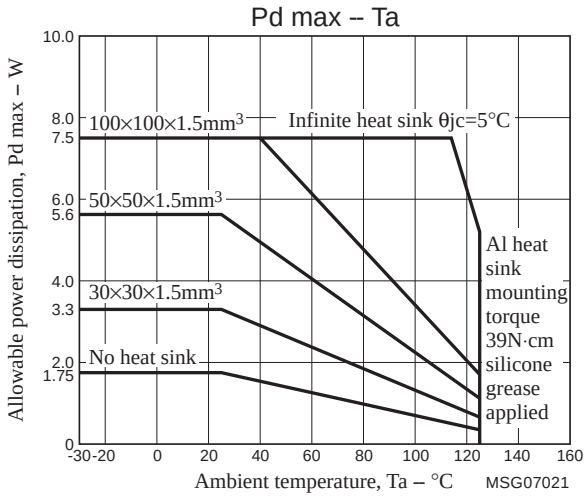
* Designed target value: No measurement made.

Package Dimensions

unit : mm (typ)

3079C

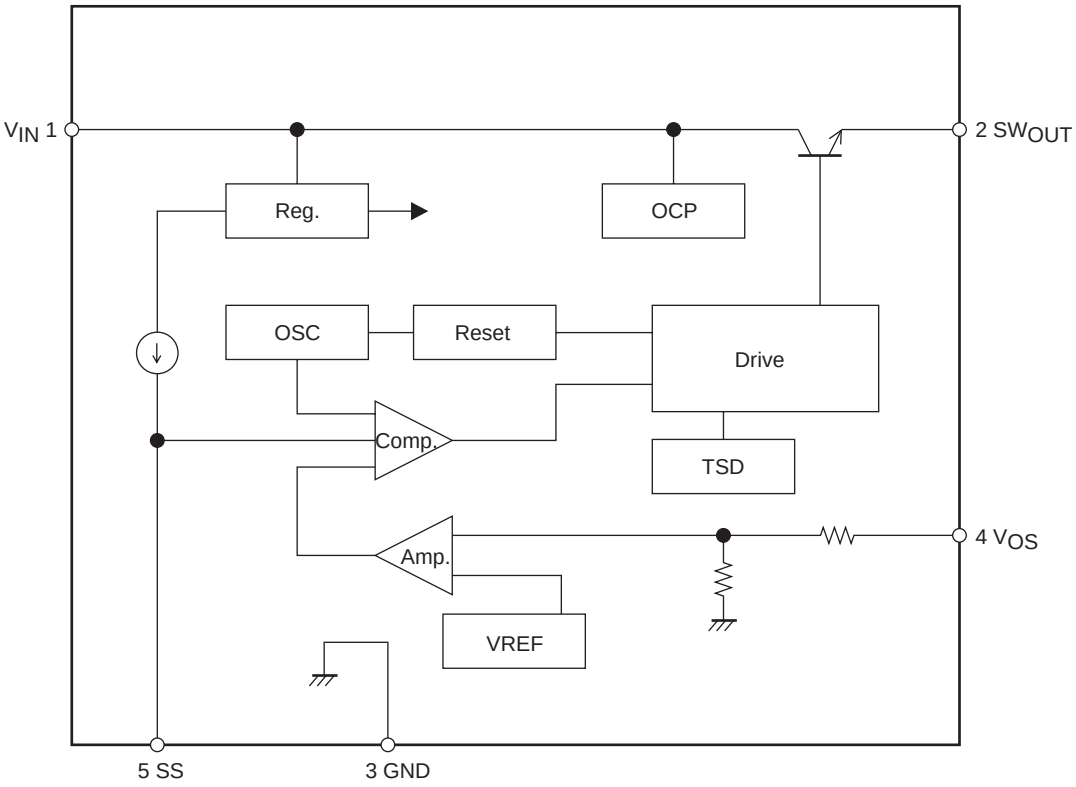




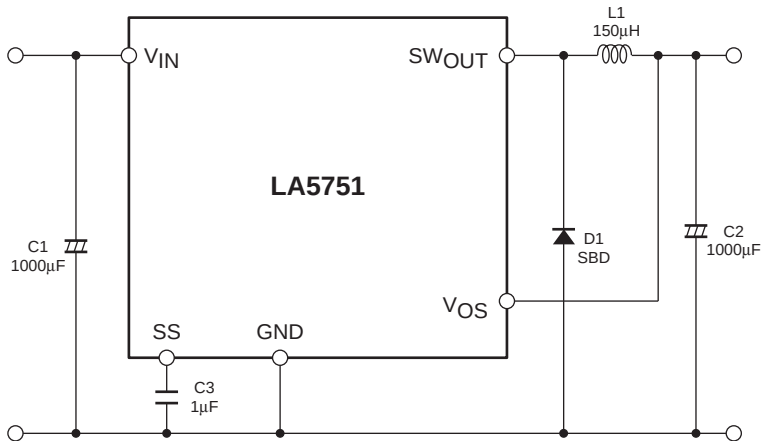
Pin Assignment

(1)V_{IN} (2)SW_{OUT} (3)GND (4)V_{OS} (5)SS

Block Diagram



Application Circuit Example



Notes: C3 is for the soft start function. Delete C3 and keep the SS pin open when the soft function is not necessary.

Description of Functional Settings

1.Start delay function

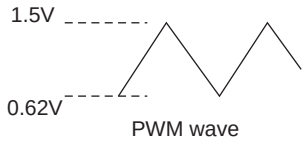
The SS pin has the internally-connected 22μA (typ) constant-current supply. When the voltage of SS pin exceeds the threshold voltage, the regulator starts operation. As the threshold is 0.62V(typ), the start delay time can be calculated as follows:

ex. For setting at 1μF

$$Td = \frac{C \times V}{i} = \frac{1\mu \times 0.62}{22\mu} = 28.2\ msec$$

2.Soft start function

The internal PWM waveform has the voltage value as shown in the right.
If down-conversion from the voltage of V_{IN} = 15V to 3.3V output to be made, for example, the PWM-ON duty has the value as shown below.



$$PWMduty = \frac{V_{OUT} + VF}{V_{IN} - Vsat + VF} = 25\%$$

(Note that calculation is made with Vsat = 1V and VF = 0.2V)

The output voltage of error amplifier, which is 3.3V, is the value with PWM = 25%, as calculated in the above equation, so that this voltage is determined as follows:

$$Ver = (\Delta VPWM) \times PWMduty + VPWML = 0.88V \times 0.25 + 0.62V = 0.84V$$

(ΔVPWM is the PWM amplitude value or 0.88V(typ) while VPWML is the lower limit voltage of PWM waveform or 0.62V(typ))

SS pin and error amplifier output voltages are designed to prefer the lower voltages, so that V_{OUT} will reach the designed regulation voltage in timing when the SS pin voltage exceeds the error amplifier output. Therefore, the soft strt time is calculated as follows:

$$Tss = \frac{C \times \Delta VPWM \times PWMduty}{i} = \frac{C \times 0.88 \times PWMduty}{22\mu A}$$

For the set conditions of C = 1μF and PWMduty = 25%:

$$Tss = \frac{1\mu \times 0.88V \times 0.25}{22\mu A} = 10msec$$

Timing Chart