

V_{SM}	=	6500 V
I_{TAVM}	=	1580 A
I_{TRMS}	=	2480 A
I_{TSM}	=	29700 A
V_{T0}	=	1.2 V
r_T	=	0.458 mΩ

Bi-Directional Control Thyristor

5STB 18U6500

Doc. No. 5SYA1037-02 Apr. 02

- Two thyristors integrated into one wafer
- Patented free-floating silicon technology
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate.

The electrical and thermal data are valid for one thyristor half of the device.

Blocking Maximum rated values

Symbol	Conditions	5STB 18U6500	5STB 18U6200	5STB 18U5800
V_{SM}	$f = 5 \text{ Hz}$, $t_p = 10 \text{ ms}$	6500 V	6200 V	5800 V
V_{RM}	$f = 50 \text{ Hz}$, $t_p = 10 \text{ ms}$	5600 V	5300 V	4900 V
I_{RM}	V_{RM} , $T_j = 110^\circ\text{C}$	$\leq 600 \text{ mA}$		
dV/dt_{crit}	Exp. to $0.67 \times V_{DRM}$, $T_j = 110^\circ\text{C}$	2000 V/ μs		

Mechanical data

Parameter	Symbol	Conditions	min	typ.	max	Unit
Mounting force	F_M		120	135	160	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2
Weight	m			3.6		kg
Surface creepage distance	D_S		53			mm
Air strike distance	D_a		22			mm

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On-state

Parameter	Symbol	Conditions	min	typ.	max	Unit
Max. average on-state current	I_{TAVM}	Half sine wave, $T_c = 70^\circ\text{C}$	1580			A
Max. RMS on-state current	I_{TRMS}		2480			A
Max. peak non-repetitive surge current	I_{TSM}	$t_p = 10\text{ ms}$, $T_j = 110^\circ\text{C}$, $V = V_R = 0\text{ V}$	29700			A
Limiting load integral	$I^2 t$		4400			kA^2s
Max. peak non-repetitive surge current	I_{TSM}	$t_p = 8.3\text{ ms}$, $T_j = 110^\circ\text{C}$, $V = V_R = 0\text{ V}$	31800			A
Limiting load integral	$I^2 t$		4190			kA^2s
On-state voltage	V_T	$I_T = 1600\text{ A}$, $T_j = 110^\circ\text{C}$			1.93	V
Threshold voltage	V_{T0}	$I_T = 1000\text{ A} - 3000\text{ A}$, $T_j = 110^\circ\text{C}$			1.2	V
Slope resistance	r_T	$T_j = 110^\circ\text{C}$			0.458	$\text{m}\Omega$
Holding current	I_H	$T_j = 25^\circ\text{C}$			125	mA
		$T_j = 110^\circ\text{C}$			75	mA

Switching

Parameter	Symbol	Conditions	min	typ.	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	$T_j = 110^\circ\text{C}$, $I_{TRM} = 2000\text{ A}$, $V_D \leq 0.67 \cdot V_{RM}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$	Cont. $f = 50\text{ Hz}$		250	$\text{A}/\mu\text{s}$
Critical rate of rise of on-state current	di/dt_{crit}			Cont. $f = 1\text{ Hz}$	1000	$\text{A}/\mu\text{s}$
Delay time	t_d	$V_D = 0.4 \cdot V_{RM}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$			3	μs
Turn-off time	t_q	$T_j = 110^\circ\text{C}$, $I_{TRM} = 2000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1.5\text{ A}/\mu\text{s}$, $V_D \leq 0.67 \cdot V_{RM}$, $dv_D/dt = 20\text{ V}/\mu\text{s}$,			800	μs
Recovery charge	Q_{rr}	$T_j = 110^\circ\text{C}$, $I_{TRM} = 2000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1.5\text{ A}/\mu\text{s}$	2100		3200	μAs

Triggering

Parameter	Symbol	Conditions	min	typ.	max	Unit
Gate trigger voltage	V_{GT}	$T_j = 25^\circ\text{C}$			2.6	V
Gate trigger current	I_{GT}	$T_j = 25^\circ\text{C}$			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \times V_{RM}$, $T_{vjmax} = 110^\circ\text{C}$	0.3			V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \times V_{RM}$	10			mA
Peak forward gate voltage	V_{FGM}				12	V
Max. rated peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Max. rated gate power loss	P_G	For DC gate current			3	W
Max. rated peak forward gate power	P_{GM}		see Fig. 9			

Thermal

Parameter	Symbol	Conditions	min	typ.	max	Unit
Operating junction temperature range	T_j				110	°C
Storage temperature range	T_{stg}		-40		140	°C
Thermal resistance junction to case	R_{thJC}	Double side cooled			8	K/kW
		Anode side cooled			16	K/kW
		Cathode side cooled			16	K/kW
Thermal resistance case to heatsink	R_{thCH}	Double side cooled			1.6	K/kW
		Single side cooled			3.2	K/kW

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i (K/kW)	5.11	1.63	0.85	0.45
τ_i (s)	0.9531	0.1541	0.0211	0.0068

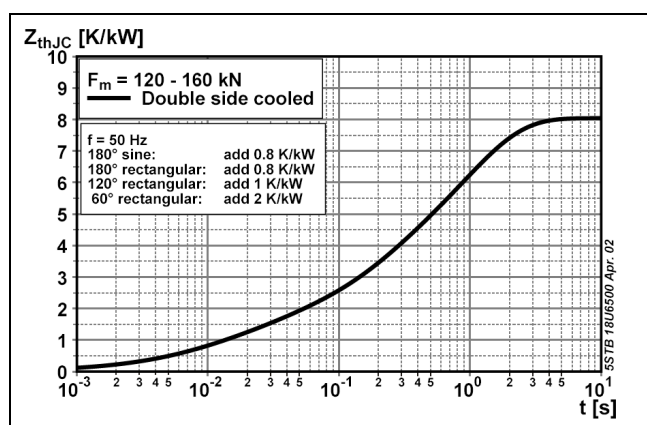


Fig. 1 Transient thermal impedance junction to case

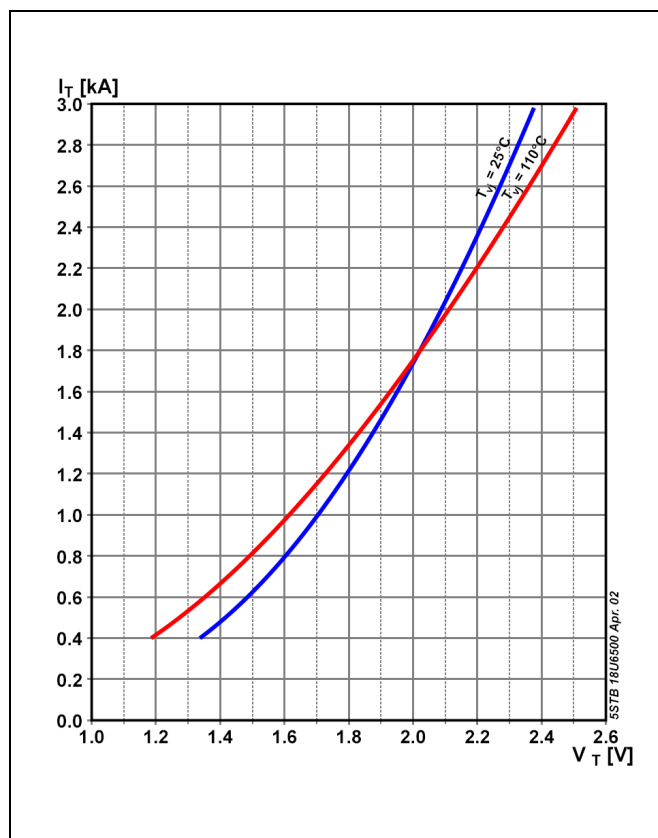


Fig. 2 Isothermal on-state characteristics

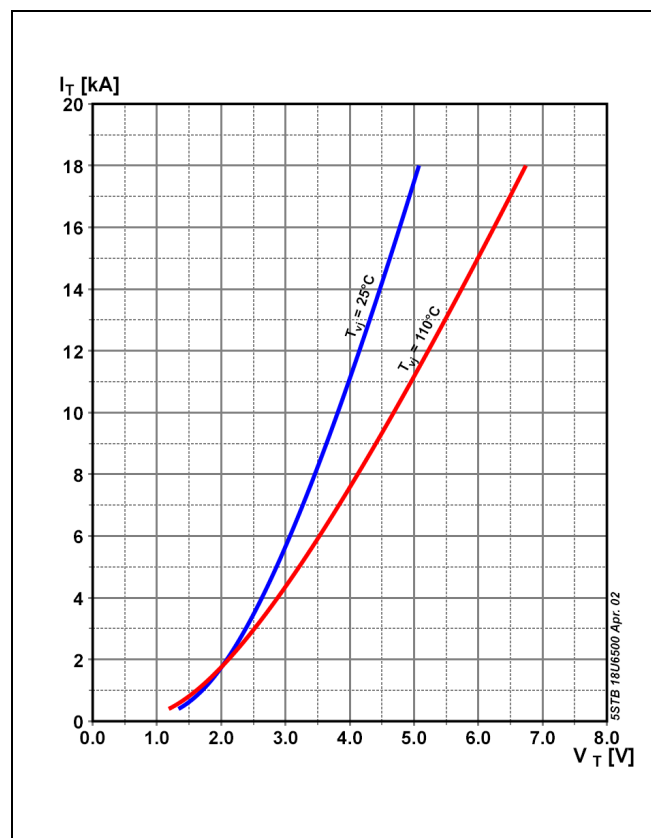


Fig. 3 Isothermal on-state characteristics

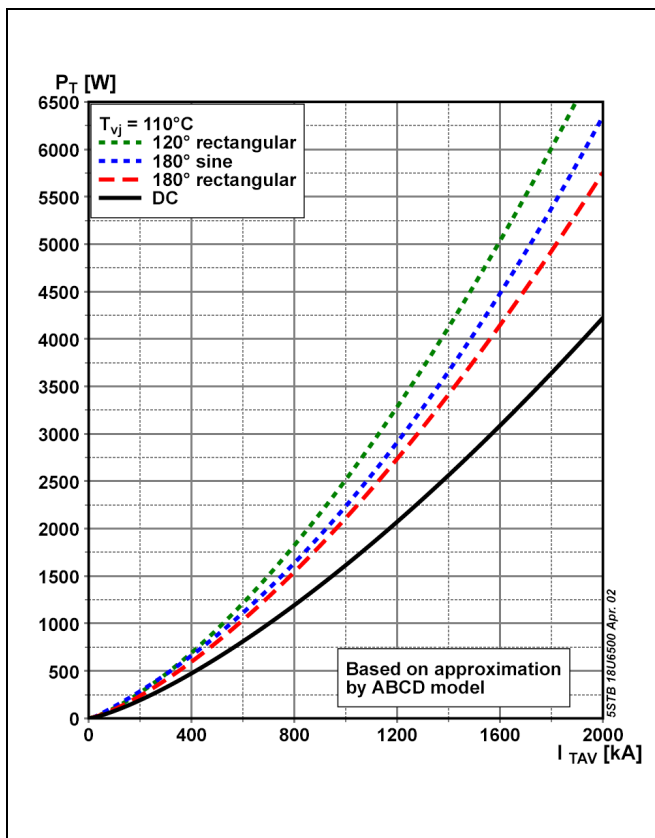


Fig. 4 On-state power dissipation vs. mean on-state current. Switching losses excluded.

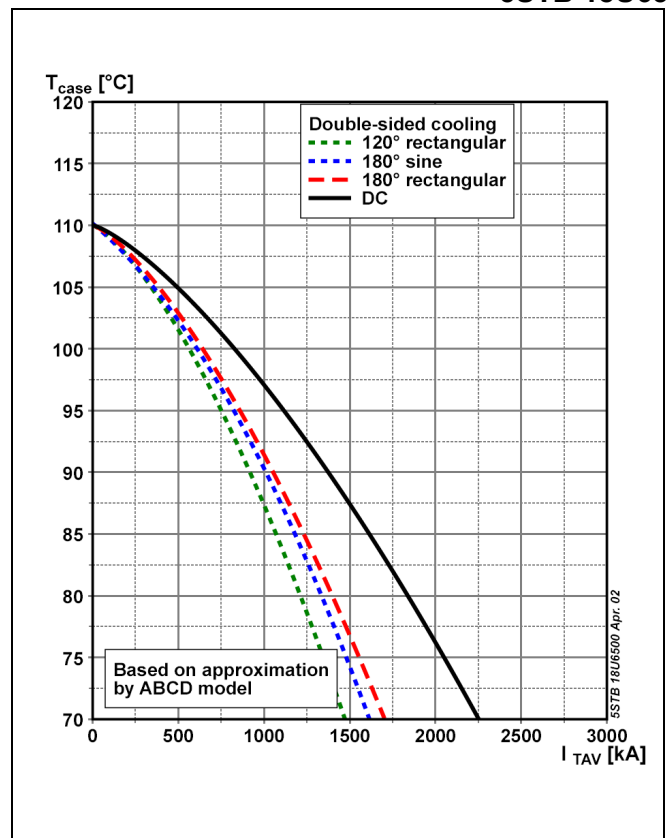


Fig. 5 Max. permissible case temperature vs. mean on-state current.

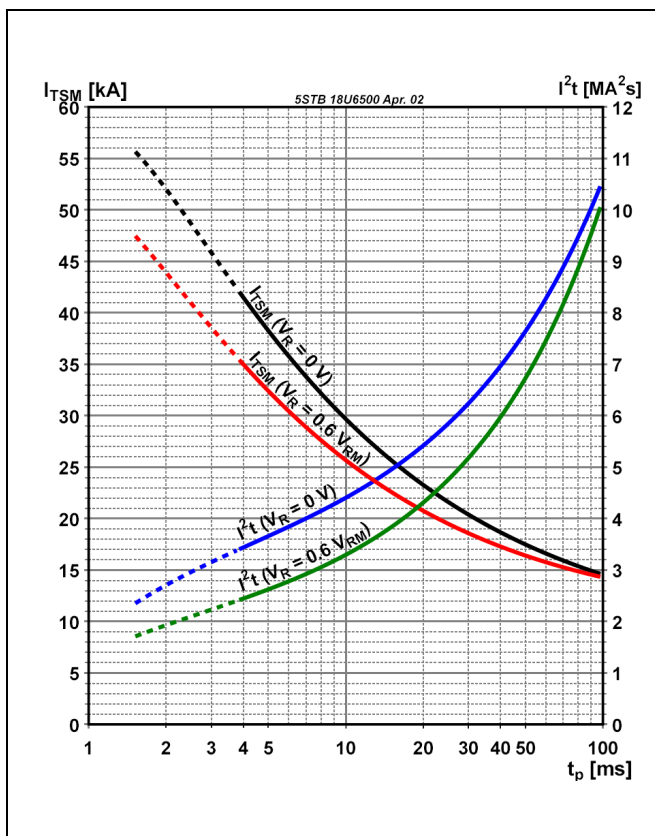


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

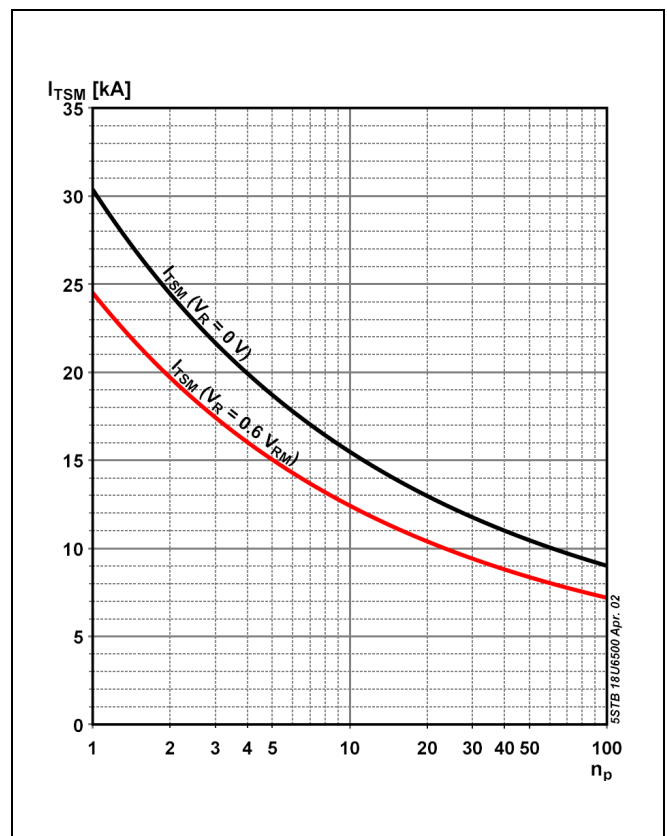


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

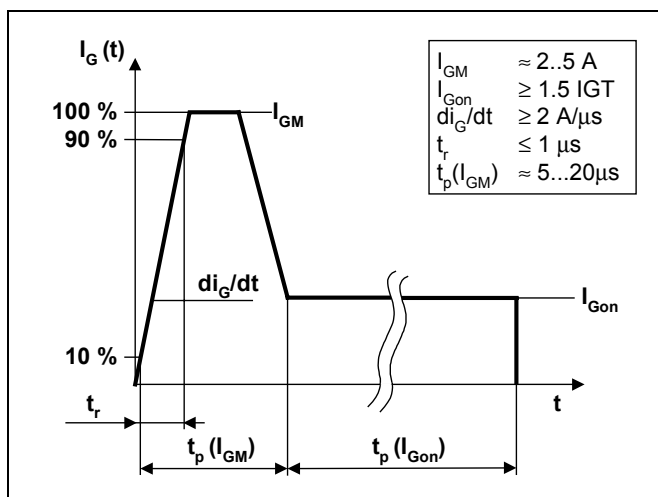


Fig. 8 Recommended gate current waveform.

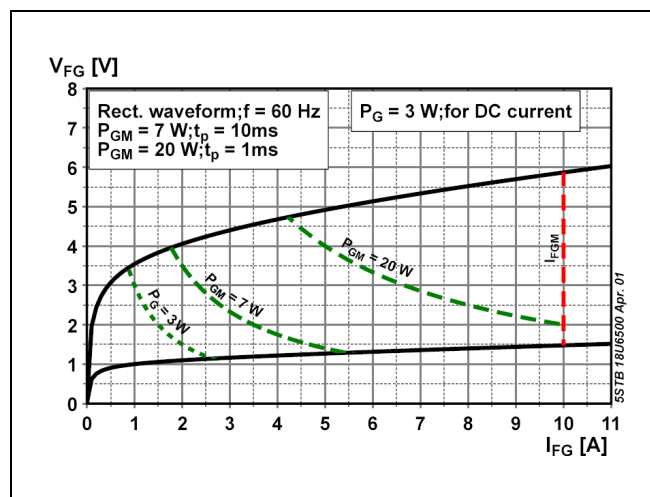


Fig. 9 Max. rated peak gate power loss.

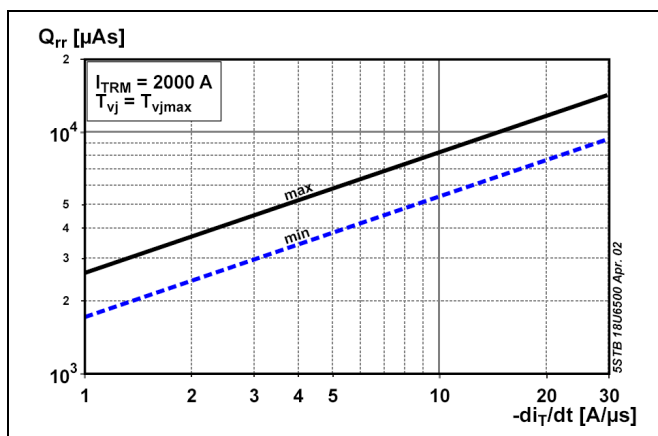


Fig. 10 Recovery charge vs. decay rate of on-state current.

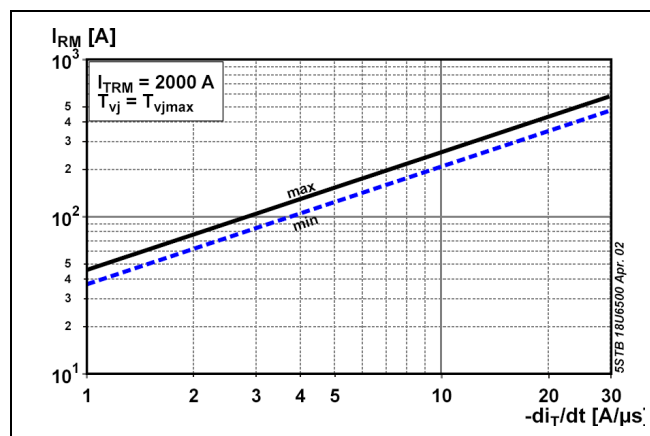


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

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