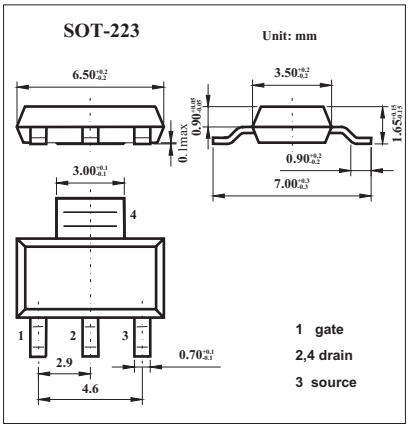
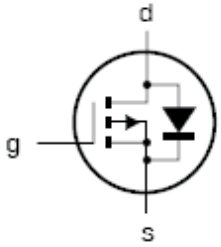
P-Channel Enhancement Mode Vertical D-MOS Transistor

KSP230

■ Features

- Direct interface to C-MOS,TTL,etc
- High-speed switching
- No secondary breakdown





■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain-source voltage (DC)	V_{DS}	-300	V
Gate-source voltage (DC) open drain	V_{GSO}	±20	V
Drain current (DC)	I_D	-210	mA
Peak drain current	I_{DM}	-0.75	A
Total power dissipation *	P_{tot}	1.5	W
Storage temperature	T_{stg}	-65 to +150	℃
Operating junction temperature	T_j	150	℃
thermal resistance from junction to ambient *	$R_{th\ j\text{-}a}$	83.3	K/W

*Device mounted on an epoxy printed-circuit board, 40 X 40 X 1.5 mm;
mounting pad for drain lead minimum 6 cm^2.

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D= -10 μA, V_{GS} = 0V	-300			V
Gate-source threshold voltage	V_{GSth}	V_{DS} = V_{GS}, I_D= -1 mA	-1.7		-2.55	V
Drain-source leakage current	I_{DSS}	V_{DS} = -240 V, V_{GS} = 0V			-100	μA
Gate leakage current	I_{GSS}	V_{GS} = ±20V,V_{DS}=0			±100	nA
Drain-source on-state resistance	$R_{DS(on)}$	I_D = -170 mA, V_{GS} = -10 V			17	Ω
Forward transfer admittance	| yfs |	V_{DS} = -25 V , I_D = -170 mA	100			mS
Input capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz		60	90	pF
Output capacitance	C_{oss}			15	30	
Reverse transfer capacitance	C_{rss}			5	15	
Turn-on time (See Fig.1and Fig.2)	t_{on}	V_{GS} = 0 V to -10 V,I_D = -250 mA, V_{DD} = -50 V,		5	10	ns
Turn-off time (See Fig.1and Fig.2)	t_{off}	V_{GS} = -10V to 0 V,I_D = -250 mA, V_{DD} = -50 V,		15	30	

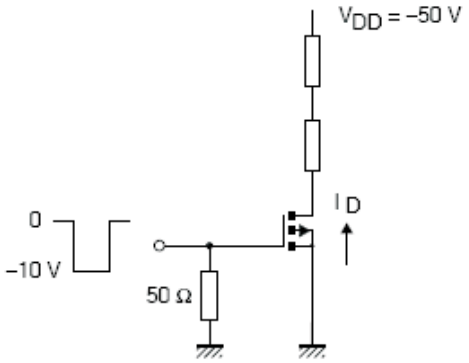

Fig.1Switching time test circuit.

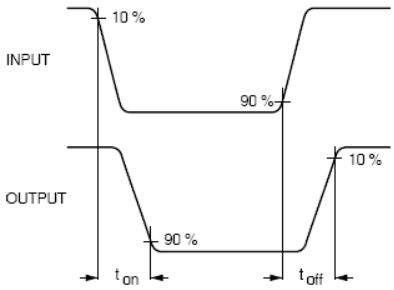

Fig.2 Input and output waveforms.