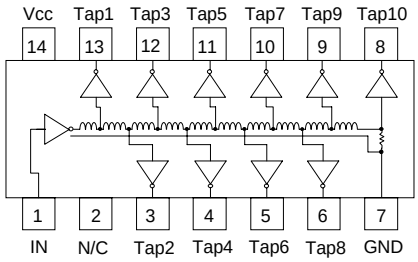
LVITD Series LVC Low Voltage Logic 10-Tap Delay Modules

Inputs accept voltages up to 5.5 V

74LVC type input can be driven from either 3.3V or 5V devices. This allows delay module to serve as a translator in a mixed 3.3V / 5V system environment.

- *Operating Temp. -40°C to +85°C*
- *Low Profile 14-Pin Package*
  Two Surface Mount Versions
- *For 5-Tap 8-Pin Versions see LVMDM Series*

LVITD Schematic



Electrical Specifications at 25°C

LVC Logic 10 Tap P/N	Tap Delay Tolerances +/- 5% or 2ns (>15ns +/- 1.0ns)										Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8	Tap 9	Total - Tap 10	
LVITD-12	3	4	5	6	7	8	9	10	11	12 ± 2.5	1.0 ± 0.4
LVITD-21	3	5	7	9	11	13	15	17	19	21 ± 2.5	2.0 ± 0.6
LVITD-30	3	6	9	12	15	18	21	24	27	30 ± 2.5	3.0 ± 0.8
LVITD-50	5	10	15	20	25	30	35	40	45	50 ± 2.5	5.0 ± 1.8
LVITD-60	6	12	18	24	30	36	42	48	54	60 ± 3.0	6.0 ± 2.0
LVITD-75	7.5	15	22.5	30	37.5	45	52.5	60	67.5	75 ± 3.75	7.5 ± 2.0
LVITD-80	8	16	24	32	40	48	56	64	72	80 ± 4.0	8.0 ± 2.0
LVITD-100	10	20	30	40	50	60	70	80	90	100 ± 5.0	10.0 ± 2.0
LVITD-125	12.5	25	37.5	50	62.5	75	87.5	100	112.5	125 ± 6.25	12.5 ± 3.0
LVITD-150	15	30	45	60	75	90	105	120	135	150 ± 7.5	15.0 ± 3.0

TEST CONDITIONS -- Low Voltage CMOS, LVC

V_{CC} Supply Voltage 3.30VDC
Input Pulse Voltage 2.70V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 50pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

Supply Voltage, V_{CC} ..... 3.3 ± 0.3 VDC
Supply Current, I_{CC} ..... 10 mA typ., 30 mA max.
Supply Current, I_{CCL}: V_{IN} = GND ..... 22 mA max.
Supply Current, I_{CCH}: V_{IN} = V_{CC} ..... 10 µA max.
Input Voltage, V_I ..... 0 V min., 5.5 V max.
Logic "1" Input, V_{IH} ..... 2.0 V min.
Logic "0" Input, V_{IL} ..... 0.8 V max.
Logic "1" Out, V_{OH}: V_{CC} = 3V & I_{OH} = -24 mA ..... 2.0 V min.
Logic "0" Out, V_{OL}: V_{CC} = 3V & I_{OL} = 24 mA ..... 0.55 V max.
Input Capacitance, C_I ..... 5 pF, typ.
Input Pulse Width, P_{WI} ..... 40% of Delay min.
Operating Temperature Range ..... -40° to +85°C
Storage Temperature Range ..... -65° to +150°C

P/N Description *LVITD - XXX X*

LVC Buffered 10 Tap Delay
Molded Package Series:
14-pin DIP: LVITD
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD
J = "J" Bend SMD

Examples: LVITD-30G = 30ns (3ns per tap) 74LVC, 14-Pin G-SMD
LVITD-100 = 100ns (10ns per tap) 74LVC, 14-Pin DIP

Dimensions in Inches (mm)