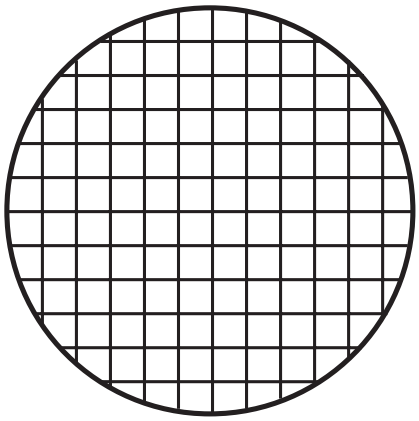
M29W800FB-KGD

Known good die, 8-Mbit (1 Mbit x 8 or 512 Kbits x 16), boot block, 3 V supply Flash memory

Preliminary Data

Features

- Supply voltage
  - V_{CC} = 2.7 V to 3.6 V for program, erase and read
- Access times: 90 ns
- Programming time
  - 10 µs per byte/word typical
- 19 memory blocks
  - 1 boot block (top or bottom location)
  - 2 parameter and 16 main blocks
- Program/erase controller
  - Embedded byte/word program algorithms
- Erase suspend and resume modes
  - Read and program another block during erase suspend
- Unlock bypass program command
  - Faster production/batch programming
- Temporary block unprotection mode
- Common flash interface
  - 64-bit security code
- Low power consumption
  - Standby and automatic standby
- 100,000 program/erase cycles per block
- Electronic signature
  - Manufacturer code: 0020h
  - Bottom device code M29W800FB: 225Bh



Wafer

Contents

List of tables

List of figures

1 Description

The M29W800F is available as known good dice.

Numonyx defines known good dice as standard products offered as dice and tested for functionality and speed. Numonyx's known good die products are as reliable and of the same quality as products delivered in packages.

This datasheet describes the features specific to parts sold as known good dice. It should be read in conjunction with the M29W800F datasheet that detailfully describes the device operation. The M29W800F datasheet is available from the Numonyx website: *www.numonyx.com*.

The M29W800FB-KGD is a 8-Mbit non-volatile Flash memory that can be erased electrically at the block level and programmed in-system on a single-word basis using a 2.7 V to 3.6 V. On power-up the memory defaults to its read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental program or erase commands from modifying the memory. Program and erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged. The first or last 64 Kbytes have been divided into four additional blocks. The 16-Kbyte boot block can be used for small initialization code to start the microprocessor, the two 8-Kbyte parameter blocks can be used for parameter storage and the remaining 32-Kbyte is a small main block where the application may be stored.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

For information on how to order these options refer to *Table 5: Ordering information scheme*.

Figure 1. Logic diagram

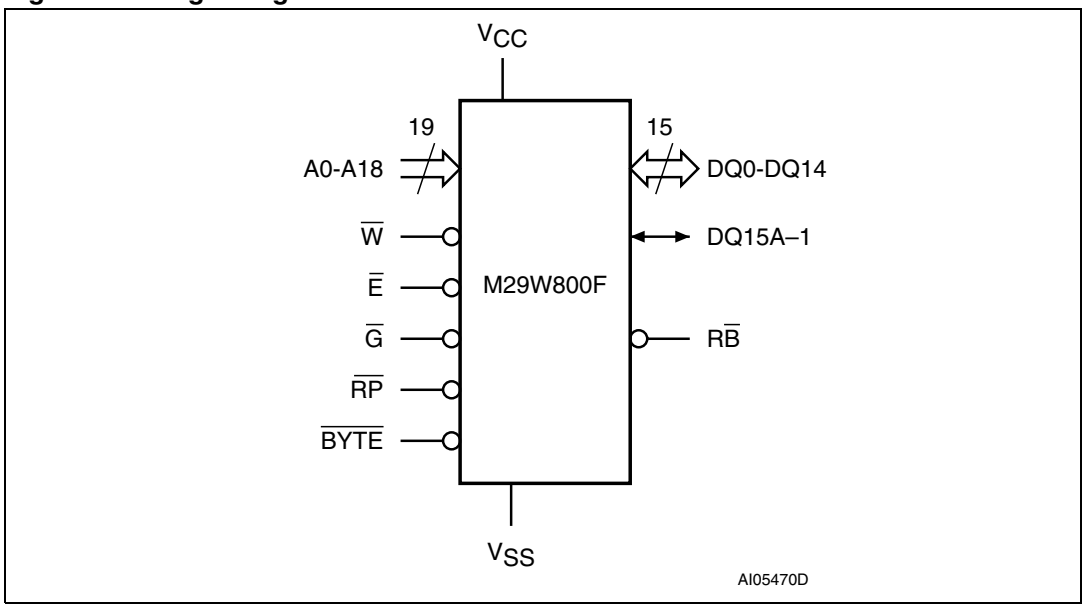


Table 1. Signal names

Signal	Description	Direction
A0-A18	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15A–1	Data input/output or address input	I/O
$\overline{E}$	Chip Enable	Input
$\overline{G}$	Output Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{RP}$	Reset/block temporary unprotect	Input
$R\overline{B}$	Ready/Busy output	Output
$\overline{BYTE}$	Byte/word organization select	Input
V_{CC}	Supply voltage	Supply
V_{SS}	Ground	–
NC	Not connected internally	–

2 KGD-specific DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics that differ from those of the packaged device.
The parameters in the tables that follow are derived from tests performed under the measurement conditions specified in the full datasheet M29W800F. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 2. Operating and AC measurement conditions

Parameter		Value		Units
		Min	Max	
Ambient temperature (T_A)	Grade 3	–40	125	°C

3 Die specifications

3.1 Functional specification

Refer to the M29W800F datasheet for the full functional and electrical specifications of the product.

3.2 Physical specification

The physical specifications are shown in *Table 3*, while the die is illustrated in *Figure 2*, and the pad coordinates are given in *Table 4*.

Table 3. Physical specifications

Name	Value	Unit
Wafer diameter	200	mm
Die dimensions, X by Y (with scribe line)	3337(X) × 1640(Y)	µm
Die dimensions, X by Y (without scribe line)	3257(X) × 1560(Y)	µm
Wafer thickness	240	µm
Die backside (material)	silicon	–
Die backside potential	ground	–
Number of bond pads per die	50	–
Bond pad opening	65	µm (min)
Bond pad metallization	AlCu	–
Bond pad metallization thickness	710	nm
Passivation	HDP / SiN	–
Passivation thickness	0.8 / 0.55	µm
Maximum junction temperature (T_J) under bias	125	°C

Figure 2. Die pad identification

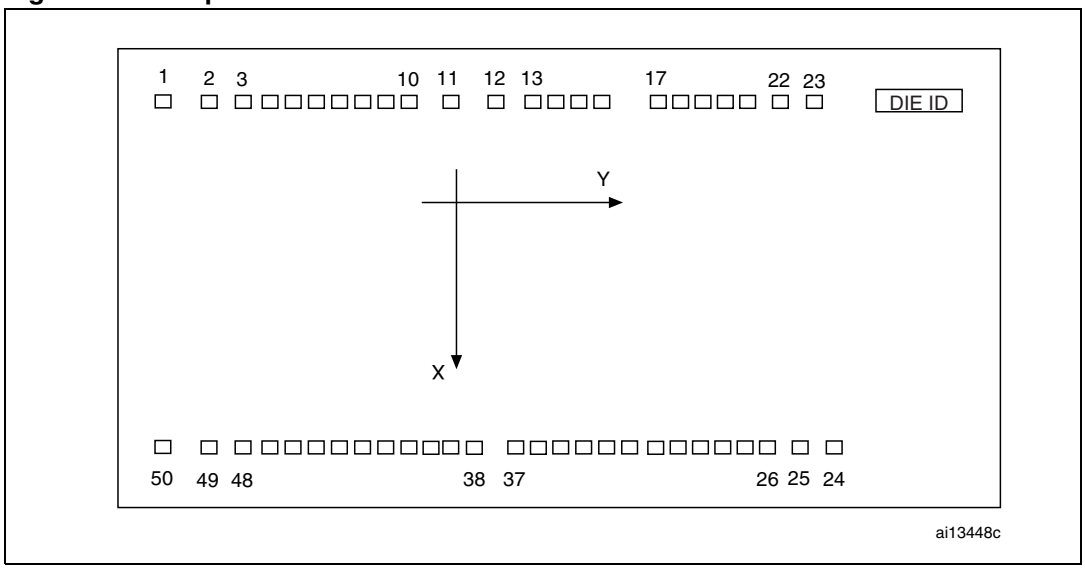


Table 4. Pad numbers and coordinates

Pad name	Pad #	X (µm)	Y (µm)	Pad name	Pad #	X (µm)	Y (µm)
A0	1	–1400.921	679.567	GND(1)	26	1138.242	–633.273
A1	2	–1250.041	679.567	GND(1)	27	1038.238	–633.273
A2	3	–1124.921	679.567	DQ15	28	933.579	–633.273
A3	4	–1024.917	679.567	DQ7	29	833.575	–633.273
A4	5	–924.913	679.567	DQ14	30	733.571	–633.273
A5	6	–824.909	679.567	DQ6	31	633.567	–633.273
A6	7	–724.905	679.567	DQ13	32	533.563	–633.273
A7	8	–624.901	679.567	DQ5	33	433.559	–633.273
A17	9	–524.897	679.567	DQ12	34	333.555	–633.273
A18	10	–424.893	679.567	DQ4	35	233.551	–633.273
$R\overline{B}$	11	–284.574	679.567	V_{DD}	36	128.892	–633.273
$\overline{RP}$	12	–78.531	679.567	V_{DD}	37	28.888	–633.273
$\overline{W}$	13	280.067	679.567	DQ11	38	–112.81	–633.273
NC(2)	14	380	679.567	DQ3	39	–212.814	–633.273
A8	15	480.074	679.567	DQ10	40	–312.818	–633.273
A9	16	580.078	679.567	DQ2	41	–412.822	–633.273
A10	17	733.369	679.567	DQ9	42	–512.826	–633.273
A11	18	833.373	679.567	DQ1	43	–612.83	–633.273
A12	19	933.377	679.567	DQ8	44	–712.834	–633.273
A13	20	1033.381	679.567	DQ0	45	–812.838	–633.273
A14	21	1133.385	679.567	$\overline{G}$	46	–917.498	–633.273
A15	22	1258.505	679.567	GNDQ	47	–1017.502	–633.273
A16	23	1409.385	679.567	GNDQ	48	–1117.506	–633.273
A16	24	1414.242	–633.273	$\overline{E}$	49	–1254.549	–633.273
$\overline{BYTE}$	25	1263.362	–633.273	A0	50	–1405.778	–633.273

1. This pin must be grounded.
2. NC means that the pad is not connected.

4 Product test flow

Numonyx implements quality assurance procedures throughout the product test flow. In addition, an off-line quality monitoring program is implemented to ensure that Numonyx's KGD devices have the same level of reliability as the standard packaged devices.

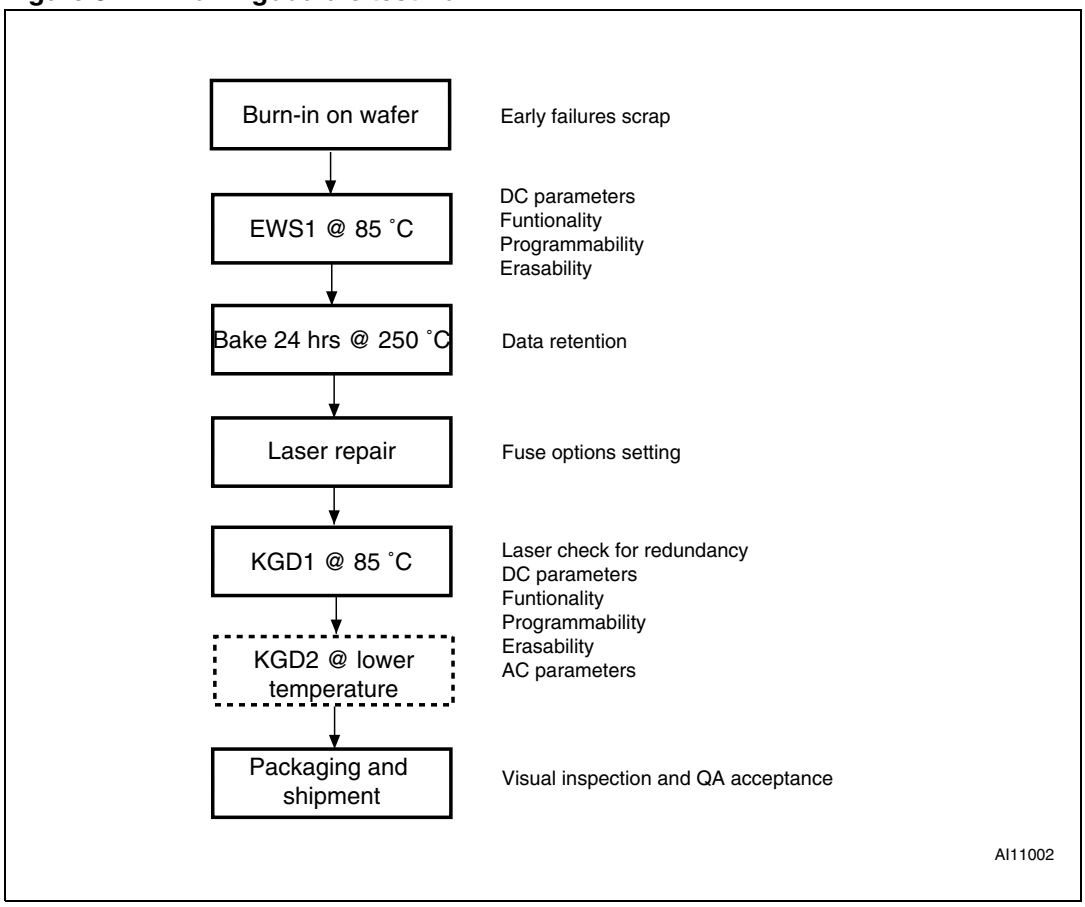
Figure 3 gives an overview of Numonyx's known good die test flow.

The burn-in step performs an electrical stress on the devices by executing write/erase cycles at 125 °C. This ensures that all the devices that fail early are removed from the population before proceeding to the following steps.

The electrical wafer sort 1 (EWS1) step applies the same test procedure for both packaged and KGD devices. After EWS1, only wafers with a minimum yield are accepted for the following steps (minimum yield rule).

The KGD1 test emulates the final test of packaged devices and is validated after correlating the results with standard test flow for packaged devices, to ensure the same reliability level for both test flows. The same test can be reproduced at a lower temperature (KGD2).

Figure 3. Known good die test flow



1. EWS = electrical wafer sort.

5 Handling instructions

5.1 Processing instructions

Known good die products should not be exposed to ultraviolet light or be processed at temperatures greater than 250 °C. Failure to adhere to these processing instructions may cause permanent damage to the device.

For best yield, Numonyx recommends assembly in a class 10K (or better) designated clean room.

All standard ESD (electrostatic discharge) handling procedures should be observed. The die should be kept in an ESD-protected environment at all times during inspection and assembly.

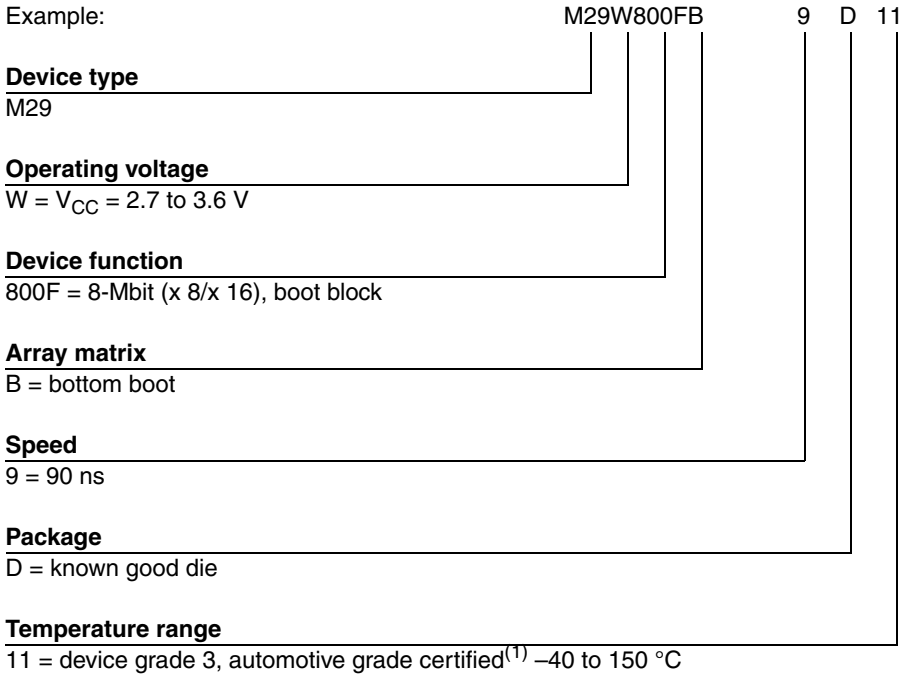
5.2 Storage instructions

Known good die products should be stored in a nitrogen purged atmosphere cabinet or in a vacuum-sealed bag.

Moisture content of the storage facility should be maintained at 30% ± 10% relative humidity.

6 Ordering information

Table 5. Ordering information scheme



1. Qualified & characterized according to AEC Q100 & Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Numonyx Sales Office.

7 Revision history

Table 6. Document revision history

Date	Version	Revision Details
20-Mar-2008	1	Initial release.
28-Mar-2008	2	Applied Numonyx branding.

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