1.2 Gb, DDR - SDRAM Integrated Module (IMOD)

FEATURES

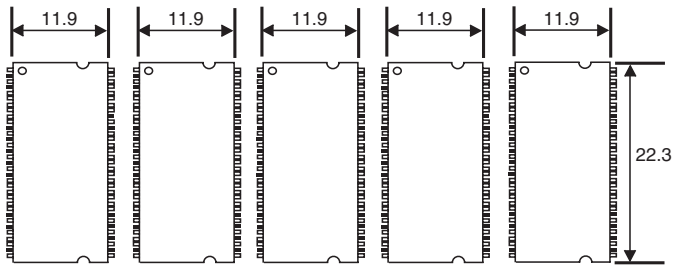
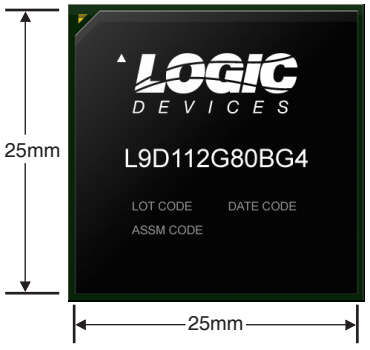
- DDR SDRAM Data Rate = 200, 250, 266, and 333 Mbps
- Package:
  - 25mm x 25mm, Encapsulated Plastic Ball Grid array (PBGA), 219 balls, 1.27mm pitch.
- 2.5V ±0.2V Core Power supply
- 2.5V ±0.2V I/O Power supply (SSTL_2 compatible)
- Differential Clock inputs (CLKx, CLKx\)
- Commands entered on each positive CLKx edge
- Internal pipelined double-data-rate (DDR) Architecture; two data accesses per clock cycle
- Programmable Burst Length: 2, 4, or 8
- Bidirectional data strobe (DQSLx, DQsHx) per byte transmitted/ received with data i.e. source-synchronous data capture
- DQS edge-aligned with data for READ; center-aligned with data for WRITE
- DLL to align DQx and DQSLx, DQSHx transitions with CLKx
- Four internal banks for concurrent operation
- One data mask per byte, IMOD contains (10) bytes
- Programmable IOL/IOH Option
- Auto PRECHARGE option
- Auto REFRESH and SELF REFRESH Modes
- Available in INDUSTRIAL, EXTENDED and Mil-Temp ranges
- Organized as 16M x 72/80
- Weight: LOGIC Devices, Inc. L9D112G80BG4 = 2.75 grams typical

Benefits

- 53% SPACE savings vs. Monolithic, TSOPII-66 solution
- Reduced I/O routing (34%)
- Reduced trace length providing improved/reduced parasitic capacitance
- Impedance matched (60ohm) packaging
- High TCE organic laminate interposer
- Suitable for High Reliability applications
- Upgradable to 32M x 72/80: L9D125G80BG4

*Note: This integrated product and/or its specifications are subject to change without notice.

Latest document should be retrieved from LDI prior to your design consideration.

OPTIONS	MONOLITHIC SOLUTION	IMOD SOLUTION	SAVINGS
			
AREA	5 X 265mm² = 1328mm² PLUS	625mm²	53%
I/O	5 X 66 pins = 320 pins total	219 Balls/Locations	34%

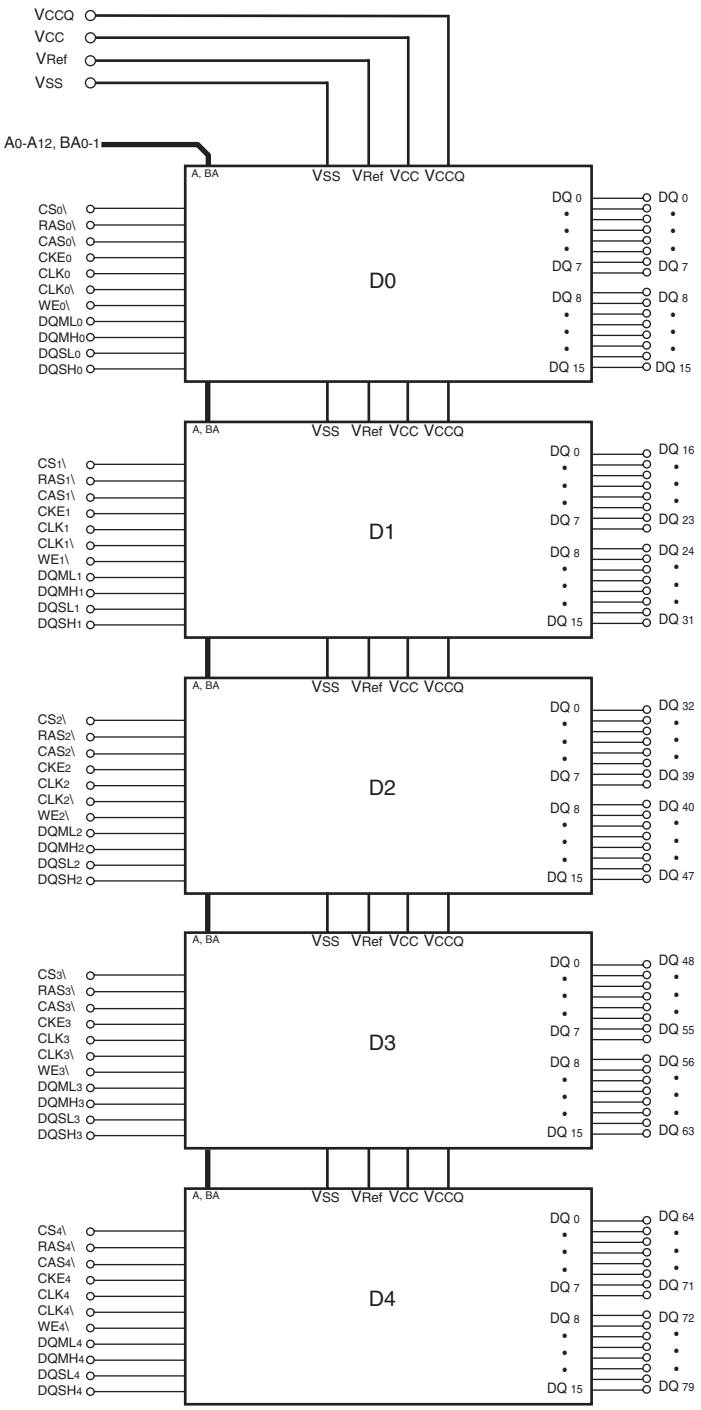
L9D112G80BG4, DDR1 SIGNAL LOCATION DIAGRAM

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		DQ0	DQ14	DQ15	VSS	VSS	A9	A10	A11	A8	VCCQ	VCCQ	DQ16	DQ17	DQ31	VSS	A
B	DQ1	DQ2	DQ12	DQ13	VSS	VSS	A0	A7	A6	A1	VCC	VCC	DQ18	DQ19	DQ29	DQ30	B
C	DQ3	DQ4	DQ10	DQ11	VCC	VCC	A2	A5	A4	A3	VSS	VSS	DQ20	DQ21	DQ27	DQ28	C
D	DQ6	DQ5	DQ8	DQ9	VCCQ	VCCQ	A12	RFU	RFU	RFU	VSS	VSS	DQ22	DQ23	DQ26	DQ25	D
E	DQ7	DQML0	VCC	DQMH0	DQSH3	DQSL0	DQSH0	BA0	BA1	DQSL1	DQSH1	Vref	DQML1	VSS	NC	DQ24	E
F	CAS0\	WE0\	VCC	CLK0	DQSL3							RAS1\	WE1\	VSS	DQMH1	CLK1	F
G	CS0\	RAS0\	VCC	CKE0	CLK0\							CAS1\	CS1\	VSS	CLK1\	CKE1	G
H	VSS	VSS	VCC	VCCQ	VSS							VCC	VSS	VSS	VCCQ	VCC	H
J	VSS	VSS	VCC	VCCQ	VSS							VCC	VSS	VSS	VCCQ	VCC	J
K	CLK3\	CKE3	VCC	CS3\	DQSL4							CLK2\	CKE2	VSS	RAS2\	CS2\	K
L	NC	CLK3	VCC	CAS3\	RAS3\							DQSL2	CLK2	VSS	WE2\	CAS2\	L
M	DQ56	DQMH3	VCC	WE3\	DQML3	CKE4	DQMH4	CLK4	CAS4\	WE4\	RAS4\	CS4\	DQMH2	VSS	DQML2	DQ39	M
N	DQ57	DQ58	DQ55	DQ54	DQSH4	CLK4\	DQ73	DQ72	DQ71	DQ70	DQML4	DQSH2	DQ41	DQ40	DQ37	DQ38	N
P	DQ60	DQ59	DQ53	DQ52	VSS	VSS	DQ75	DQ74	DQ69	DQ68	VCC	VCC	DQ43	DQ42	DQ36	DQ35	P
R	DQ62	DQ61	DQ51	DQ50	VCC	VCC	DQ77	DQ76	DQ67	DQ66	VSS	VSS	DQ45	DQ44	DQ34	DQ33	R
T	VSS	DQ63	DQ49	DQ48	VCCQ	VCCQ	DQ79	DQ78	DQ65	DQ64	VSS	VSS	DQ47	DQ46	DQ32	VCC	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

VSS | V + (Core Power) | V + (I/O Power) | UNPOPULATED | Address

Data IO | CNTRL | NC | Level REF

Functional Block Diagram



Pin/Ball Locations/Definitions and Functional Description

BGA Locations	Symbol	Type	Description
F4, F16, G5, G15, K1, K12, L2, L13, N6, M8	**CKx,CKx**	**CNTL. Input**	Clock: CKx and CKx\ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CKx and negative edge of CKx\. Output data (DQ's and DQS) is referenced to the crossings of the differential clock inputs.
G4, G16, K2, K13, M6	**CKEx**	**CNTL. Input**	Clock Enable: CKE controls the clock inputs. CKE High enables, CKE Low disables the clock input pins. Driving CKE Low provides PRECHARGE POWER-DOWN. CKE is synchronous for POWER-DOWN entry and exit, and for SELF-REFRESH entry CKE is asynchronous for SELF-REFRESH exit and disabling the outputs. CKE must be maintained High throughout READ and WRITE accesses. Input buffers are disabled during POWER-DOWN, input buffers are disabled during SELF-REFRESH. CKE is an SSTL-2 input but will detect an LVCMOS LOW level after V_{CC} is applied.
G1, G13, K4, K16, M12	**CSx**	**CNTL. Input**	Chip Select: CSx\ enables the COMMAND register(s) of each of the five (5) integrated words. All commands are masked (registered) HIGH with CSx\ driven true. CSx\ provides for external word/bank selection on systems with multiple banks. CSx\ is considered part of the COMMAND CODE.
F12, G2, K15, L5, M11	**RASx**	**CNTL. Input**	Row Address Strobe: Command input along with CASx\ and WEx\
F1, G12, L4, L16, M9	**CASx**	**CNTL. Input**	Column Address Strobe: Command input along with RASx\ and WEx\
F2, F13, L15, M4, M10	**WEx**	**CNTL. Input**	WRITE (word): Command input along with CASx\ and RASx\
E2, E4, E13, F15, M2, M5, M7, M13, M15, N11	**DQMLx, DQMHx**	**CNTL. Input**	Input Data Mask: DQM is an input mask signal for WRITE operations. Input Data is masked when DQML/Hx is sampled HIGH at time of a WRITE access DQML/Hx is sampled on both edges of DQSL/Hx.
E5, E6, E7, E10, E11, F5, K5, L12, N5, N12	**DQSLx, DQSHx**		Data Strobe: Output flag on READ data and Input flag on WRITE data. DQS is edge-aligned with READ data, centered in WRITE data operations.
E12	**Vref**	**Level REF**	Reference Voltage
A7, A8, A9, A10, B7, B8, B9, B10, C7, C8, C9, C10, D7	**A_0-A_{12}**	**Input**	Address input: Provide the ROW address for ACTIVE commands and the COLUMN address and AUTO PRE-CHARGE bit (A_{10}) for READ/WRITE commands to select one location out of the total array within a selected bank A_{10} sampled during a PRE-CHARGE command determines whether the PRE-CHARGE applies to one bank or all banks. The address inputs also provide the OP-CODE during a MODE REGISTER SET command.
E8, E9	**BA_0, BA_1**	**Input**	Bank Address input: define which BANK is active during a READ, WRITE, or PRE-CHARGE command.

Pin/Ball Locations/Definitions and Functional Description Continued

BGA Locations	Symbol	Type	Description
D8, D9, D10	**RFU**	**Input**	Reserved Future Use: Pins reserved for future Address and Bank Select inputs
A2, A3, A4, A13, A14, A15, B1, B2, B3, B4, B13, B14, B15, B16, C1, C2, C3, C4, C13, C14, C15, C16, D1, D2, D3, D4, D13, D14, D15, D16, E1, E16, M1, M16, N1, N2, N3, N4, N7, N8, N9, N10, N13, N14, N15, N16, P1, P2, P3, P4, P7, P8, P9, P10, P13, P14, P15, P16, R1, R2, R3, R4, R7, R8, R9, R10, R13, R14, R15, R16, T2, T3, T4, T7, T8, T9, T10, T13, T14, T15	**DQ_0-DQ_{79}**	**Input/Output**	Data I/O
B11, B12, C5, C6, E3, F3, G3, H3, H12, H16, J3, J12, J16, K3, L3, M3, P11, P12, R5, R6, T16	**V_{CC}**	**Supply**	Core Power
A11, A12, D5, D6, H4, H15, J4, J15, T5, T6	**V_{CCQ}**	**Supply**	I/O Power
A5, A6, A16, B5, B6, C11, C12, D11, D12, E14, F14, G14, H1, H2, H5, H13, H14, J1, J2, J5, J13, J14, K14, L14, M14, P5, P6, R11, R12, T1, T11, T12	**V_{SS}**	**Supply**	Ground (Digital)

GENERAL DESCRIPTION

The LOGIC Devices, 1.2Gb, DDR SDRAM IMOD, is one member of its Integrated Module family. This family of Integrated memory modules contains DDR3/DDR2 and DDR device definitions in three package footprints including this 25mm2, a 16mm x 22mm package and a 25mm x 32mm footprint. This device, a high speed CMOS random-access, integrated memory device based on use of (5) silicon devices each containing 268,435,456 bits. Each chip is internally configured as a quad-bank SDRAM. Each of the chips 67,108,864 bit banks is organized as 8,192 rows by 512 columns by 16bits. Each of the Silicon devices equates to a WORD or DUAL-BYTES, each BYTE containing Data Mask and Data Strobes.

The 1.2Gb DDR IMOD uses the double-data-rate (DDR) architecture to achieve high-speed operation. The double-data-rate architecture is a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle via the I/O pins. A single READ or WRITE access for the 1.2Gb DDR IMOD effectively consists of a single 2n-bit wide, one clock cycle transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock cycle data transfers at the DQ (I/O) pins.
A bidirectional data strobe (DQSLx, DQSHx) is transmitted externally, along with data, for use in data capture at the end-point receiver. DQSLx, DQSHx are strobes transmitted by the DDR SDRAM during READ operations and by the memory controller during WRITE operations. Each strobe, DQSLx, DQSHx control each of two bytes contained within each of the (5) silicon chips contained in LDI's IMOD.

The 1.2Gb DDR SDRAM operated from a differential clock (CLKx, CLKx\); the crossing of CLKx going HIGH and CLKx\ going LOW will be referred to as the positive edge of CLK. Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

READ and WRITE accesses to the DDR memory are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR IMOD provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An AUTO-PRECHARGE function may be enabled to provide a self-timed row PRECHARGE that is initiated at the end of the burst access.

The pipelined, multi-banked architecture of the DDR SDRAM architecture allows for concurrent operations, therefore providing high effective bandwidth, by hiding row PRECHARGE and activation time.

An AUTO REFRESH mode is provided, along with a power-saving power-down mode.

FUNCTIONAL DESCRIPTION

READ and WRITE accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA_0 and BA_1 select the bank, A_0-A_{12} select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the IMOD must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to V_{CC} and V_{CCQ} simultaneously, and then to V_{REF} (and to the System V_{TT}). V_{TT} must be applied after V_{CCQ} to avoid device latch-up, which may cause permanent damage to the device. V_{REF} can be applied after V_{CCQ} but is expected to be nominally coincident with V_{TT}. Except for CKE, inputs are not recognized as valid until after F_{REF} is applied. CKE during power-up is required to ensure that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a READ access). After all power supply and reference voltages are stable, and the clock is stable, the IMOD requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a LOAD MODE REGISTER command should be issued for the extended mode register (BA_1 LOW and BA_0 HIGH) to enable the DLL, followed by another LOAD MODE REGISTER command to the mode register (BA_0/BA_1 both LOW) to reset the DLL and to program the operating parameters. Two-hundred clock cycles are required between the DLL reset and any READ command. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO PRECHARGE cycles must be performed (^tRFC must be satisfied). Additionally, a LOAD MODE REGISTER command for the mode register with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) is required. Following these requirements, the DDR IMOD is ready for normal operation.

REGISTER DEFINITION

Mode Register

The MODE REGISTER is used to define the specific mode of operation of the DDR IMOD. This definition includes the selection of a burst length, a burst type, a CAS latency as shown in Figure 2 and the operating mode, as shown in Figure 3. The MODE REGISTER is programmed via the MODE REGISTER SET command (with BA_0=0 and BA_1=0) and will retain the stored information until it is programmed again or the device realizes a loss of power (except for bit A_8 which is self clearing).

Reprogramming the MODE REGISTER will not alter the contents of the memory, provided it is performed correctly. The MODE REGISTER must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation. MODE REGISTER bits A_0-A_2 specify the burst length, A_3 specifies the type of burst (sequential or interleaved), A_4-A_6 specify the CAS latency, and A_7-A_{12} specify the operating mode.

Burst Length

READ and WRITE accesses to the DDR IMOD are burst oriented, with the burst length being programmable, as shown in Figure 3. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility issues with future version may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A_1-A_i when the burst length is set to two; by A_2-A_i when the burst length is set to four and by A_3-A_i when the burst length is set to eight. The remaining (least significant) address bits are used to select the starting location within the block. The programmed burst length applies to both the READ and WRITE bursts.

Burst type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

Table 1: Burst Definition

Burst Length	Starting Column Address			Order of Accesses within a Burst		Notes
				Type = Sequential	Type = Interleaved	
2			A_0			1. For a burst length of two, A_1-A_i selects a two-data-element block; A_0 selects the starting column within the block. 2. For a burst length of four, A_2-A_i selects a four-data-element block; A_0-1 selects the starting column within the block. 3. For a burst length of eight, A_3-A_i selects an eight-data-element block; A_0-2 selects the starting column within the block. 4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
			0	0-1	0-1	
			1	1-0	1-0	
4		A_1	A_0			
		0	0	0-1-2-3	0-1-2-3	
		0	1	1-2-3-0	1-0-3-2	
		1	0	2-3-0-1	2-3-0-1	
		1	1	3-0-1-2	3-2-1-0	
8	A_2	A_1	A_0			
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	

READ LATENCY

The READ latency is the delay in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks.

If a READ command is registered at clock edge [n], and the latency is [m] clocks, the data will be available by clock edge [n+m]. Table 2 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Table 2 - CAS LATENCY

	Allowable Operating Frequency (MHz)	
Speed	CAS Latency = 2	CAS Latency = 2.5
-10	≤83	≤100
-8	≤100	≤125
-75	≤125	≤133
-6	NA	≤166

OPERATING MODE

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A_7-A_{12}, each set to zero, and bits A_0-A_6, set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A_7 and A_9-A_{12}, each set to zero, bit A_8 set to one, and bits A_0-A_6, set to the desired values. Although not required, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A_7-A_{12} are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility from future versions may result.

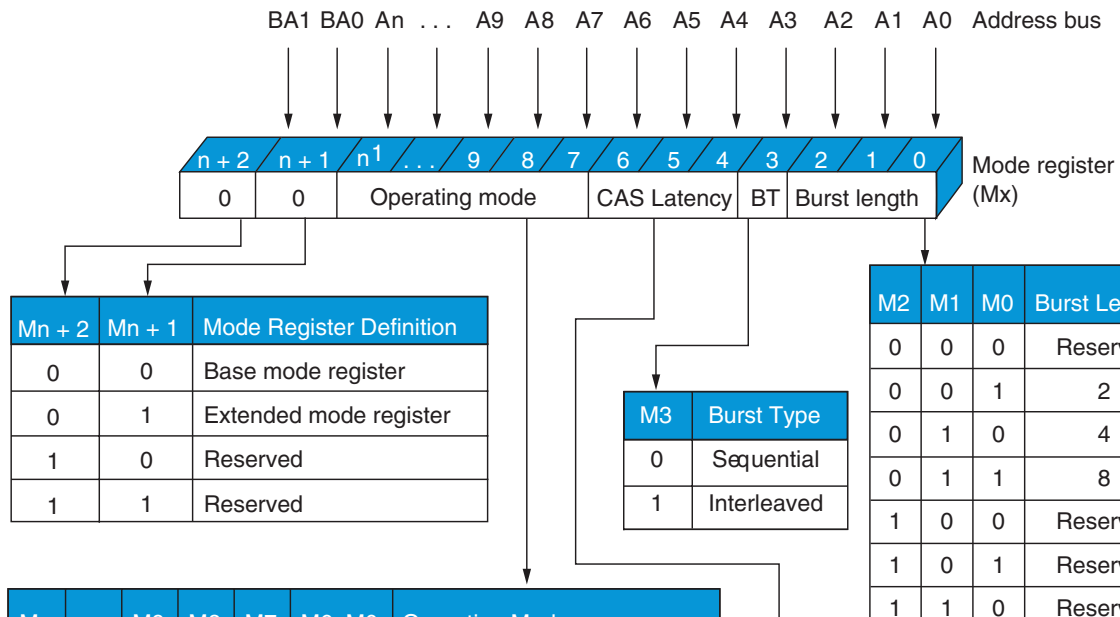
EXTENDED MODE REGISTER

The EXTENDED MODE REGISTER controls functions beyond those controlled by the MODE REGISTER; these additional functions are DLL enable/disable, output drive strength, and QFC#. These functions are controlled via the bits shown in Figure 4. The EXTENDED MODE REGISTER command to the MODE REGISTER (with BA_0=1, BA_1=0) and the register will retain the stored information until it is programmed again or the device realizes loss of power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the MODE REGISTER (BA_0=BA_1=LOW) to reset the DLL.

The EXTENDED MODE REGISTER must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

REGISTER DEFINITION

FIGURE 1 - MODE REGISTER DEFINITION



Mn + 2	Mn + 1	Mode Register Definition
0	0	Base mode register
0	1	Extended mode register
1	0	Reserved
1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

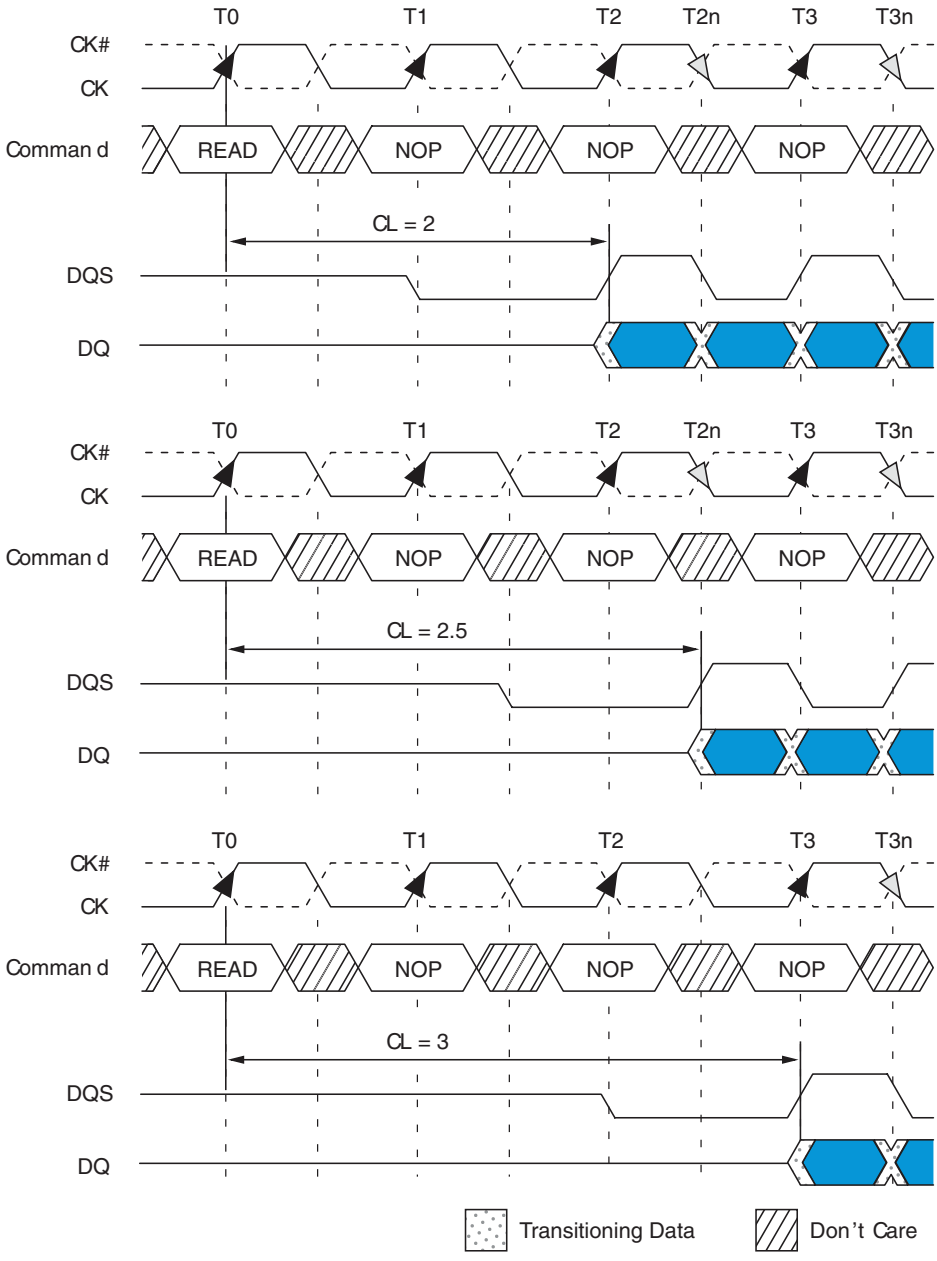
Mn	. . .	M9	M8	M7	M6–M0	Operating Mode
0	0	0	0	0	Valid	Normal operation
0	0	0	1	0	Valid	Normal operation/reset DLL
–	–	–	–	–	–	All other states reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (-5B only)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

Note: 1. n is the most significant row address bit

REGISTER DEFINITION

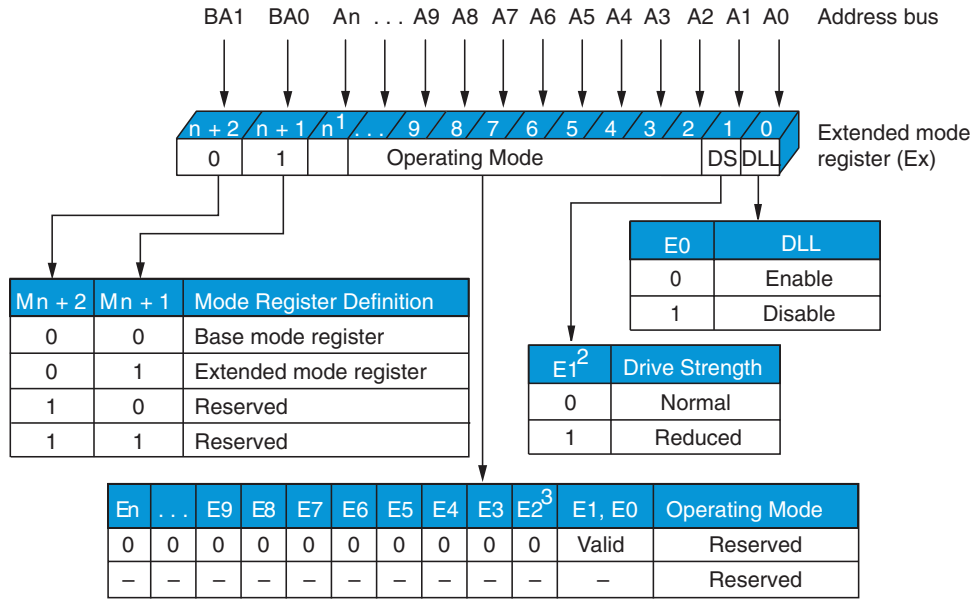
FIGURE 2 - CASE LATENCY



Note: BL = 4 in the cases shown; shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

REGISTER DEFINITION

FIGURE 3 - EXTENDED MODE REGISTER



Mn + 2	Mn + 1	Mode Register Definition
0	0	Base mode register
0	1	Extended mode register
1	0	Reserved
1	1	Reserved

E0	DLL
0	Enable
1	Disable

E1[2]	Drive Strength
0	Normal
1	Reduced

En	. . .	E9	E8	E7	E6	E5	E4	E3	E2[3]	E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	Reserved

Notes:
1. n is the most significant row address bit.
2. The reduced drive strength option is available only on Design Revision F and K.
3. The QFC# option is not supported.

OUTPUT DRIVE STRENGTH

The normal full drive strength for all outputs are specified to be SSTL2, Class II. The DDR IMOD supports an option for reduced drive. This option is intended for the support of the lighter load and/or point-to-point environments. The selection of the reduced drive strength will alter the DQs and DQSs from SSTL2, Class II drive strength to a reduced drive strength, which is approximately 54% of the SSTL, Class II drive strength.

DLL ENABLE/DISABLE

The DLL must be enabled for normal operation. The DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. When the device exits SELF REFRESH mode, the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

REGISTER DEFINITION

COMMANDS

The TRUTH TABLE (below) provides a quick reference of available commands, followed by a written description of each command.

TRUTH TABLE

Name (Function)	CSx\	RASx\	CASx\	WEx\	ADDR	Notes
Deselect (NOP)	H	X	X	X	X	1,9
No Operation (NOP)	L	H	H	H	X	1,9
ACTIVE (select bank and activate row)	L	L	H	H	Bank/Row	1,3
READ (select bank and column, and start READ burst)	L	H	L	H	Bank/Column	1,4
WRITE (select bank and column and start WRITE burst)	L	H	L	L	Bank/Column	1,4
BURST TERMINATE	L	H	H	L	X	1,8
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	1,5
AUTO REFRESH or SELF REFRESH (enter soft refresh mode)	L	L	L	H	X	6,7
LOAD MODE REGISTER	L	L	L	L	OP Code	1,2

TRUTH TABLE - DM OPERATION

Name (Function)	DQMLx, DQMHx	DQSLx, DQSHx	Notes
WRITE ENABLE	L	Valid	1,10
WRITE INHIBIT	H	X	1,10

NOTES:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A_0-A_{12} define the op-code to be written to the selected MODE REGISTER BA_0, BA_1 select either the MODE REGISTER or the EXTENDED MODE REGISTER.
3. A_0-A_{12} provide row addresses, and BA_0, BA_1 provide bank addresses.
4. A_0-A_8 provide column address; A_{10} HIGH enables the AUTO PRECHARGE feature (non-persistent), while A_{10} LOW disables the AUTO PRECHARGE feature; BA_0, BA_1 provide bank address.
5. A_{10} LOW; BA_0, BA_1 determine the bank being PRECHARGED. A_{10} HIGH all banks PRECHARGED and BA_0, BA_1 or "Don't Care".
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal REFRESH counter controls row addressing; all inputs and I/Os are "Don't Care" except for CLE.
8. Applies only to READ bursts with AUTO PRECHARGE disabled. This command is undefined (and should not be used) for READ burst with AUTO PRECHARGE enabled.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask WRITE data; provided coincident with the corresponding data.

DESELECT

The DESELECT function (CSx\=HIGH) prevents new commands from being executed by the DDR IMOD. The IMOD is effectively deselected. Operations already in progress are not affected.

REGISTER DEFINITION

No Operation (NOP)

The NO OPERATION command is used to perform a NOP to the selected DDR Silicon within the IMOD (CSx\=LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

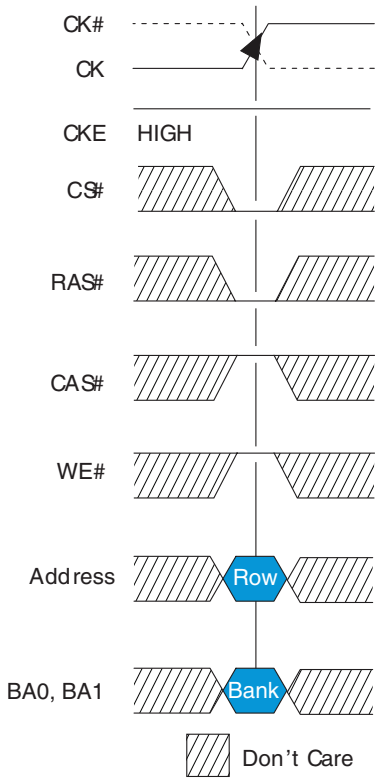
Load Mode Register

The MODE REGISTER is loaded via inputs A_0-A_{12}. The LOAD MODE REGISTER command can only be issued when all banks idle and a subsequent executable command cannot be issued until ^{t}MRD is met.

Active

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA_0, BA_1 inputs selects the bank and the address provided on inputs A_0-A_{12}, selects the row. This row remains active (or opens) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

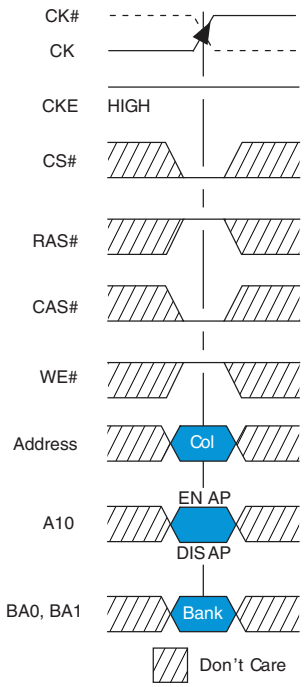
Activating a Specific Row in a Specific Bank



READ

The READ command is used to initiate a burst READ access to an active row. The value on the BA_0, BA_1 inputs selects the bank, and the address provided on inputs A_0-A_8 selects the starting column location. The value on input A_{10} determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be PRECHARGED at the end of the READ burst; If AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

READ COMMAND

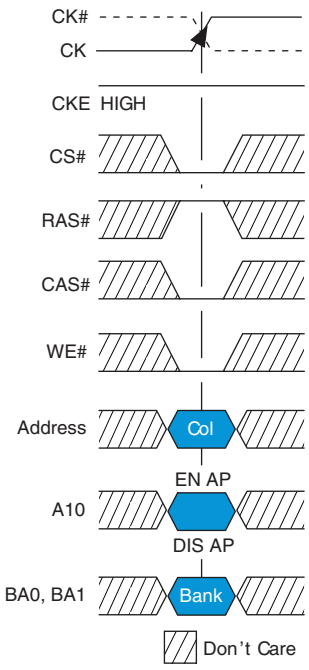


Note:
EN AP = enable auto precharge
DIS AP = disable auto precharge.

WRITE

The WRITE command is used to initiate a burst WRITE access to an active row. The value on the BA_0, BA_1 inputs selects the bank, and the address provided on inputs A_0-A_8 selects the starting column location. The value on the input A_{10} determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be AUTO PRECHARGED at the end of the WRITE burst; If AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ lines is written to the memory array subject to DQMLx, DQMHx for each WORD. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte column location.

WRITE COMMAND

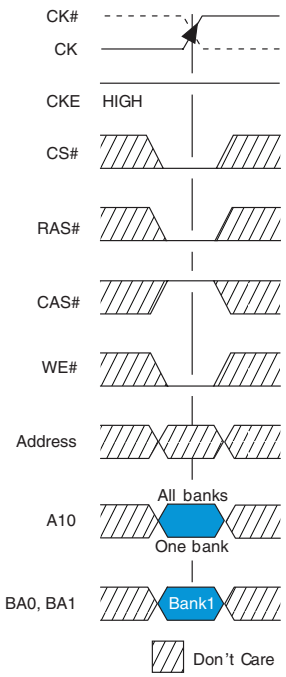


Note:
EN AP = enable auto precharge
DIS AP = disable auto precharge..

Precharge

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank or banks will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Except in the case of concurrent auto PRECHARGE, where a READ or WRITE command to a different bank is allowed as long as it does not violate any other timing parameters. Input A10 determines whether one or all banks are to be PRECHARGED and in the case where only one bank is to be PRECHARGED, inputs BA0, BA1 select the bank. In all other cases BA0, BA1 are treated as "Don't Care". Once a bank has been PRECHARGED, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of PRECHARGING.

PRECHARGE Command



Note:
1. If A10 is HIGH, bank address becomes "Don't Care."

Auto Precharge

AUTO PRECHARGE is a feature which performs the same individual bank PRECHARGE function described prior, but without requiring an explicit command. This is accomplished by using A10 to enable the command/function in conjunction with a specific READ or WRITE command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is non-persistent in that it is either enabled or disabled for each individual READ or WRITE command. The device supports concurrent AUTO PRECHARGE if the command to the other bank does not interrupt the data transfer to the current bank.

AUTO PRECHARGE ensures that the PRECHARGE is initiated at the earliest valid stage within a burst. This earliest valid stage is determined as if an explicit PRECHARGE command was issued at the earliest possible time without violating ^{t}RAS (MIN).

Burst Terminate

The BURST TERMINATE command is used to truncate READ bursts. The most recently registered READ command prior to the BURST TERMINATE command will be truncated. The open page which the READ burst was terminated from, remains open.

Auto Refresh

AUTO REFRESH is used during normal operations of the IMOD and is analogous to CASx\-BEFORE-RASx\ (CBR) REFRESH in conventional DRAMs. This command is non-persistent so it must be issued each time a REFRESH is required.

The addressing is generated by the internal REFRESH controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. Each DDR die within the IMOD, requires AUTO REFRESH cycles at an average of 7.8125 us (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute REFRESH interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR die, meaning that the maximum absolute interval between any AUTO REFRESH command is 9 x 7.8125uS (70.3uS). This maximum absolute interval is to allow future support for DLL updates internal to the DDR SDRAM die.

Although not a JEDEC requirement, to provide for future functionality enhancements, CKEx must be active (HIGH) during the AUTO REFRESH period. The AUTO REFRESH period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

Self Refresh

The SELF REFRESH command can be used to retain data in the DDR IMOD even if the rest of the system is powered down. When in the SELF REFRESH mode, the DDR IMOD retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKEx is disabled (LOW). The DLL is automatically enabled upon entering SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CLEx are “Don’t Care” during SELF REFRESH.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CLKx must be stable prior to CKEx going back to HIGH. Once CLEx is HIGH, the DDR die must have a NOP command issued for ^{t}XSNR, because time is required for the completion of any internal REFRESH in progress.

A simple algorithm for meeting both REFRESH and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

Absolute Maximum Ratings

Parameter	MIN	MAX	UNITS
V_{CC} Supply Voltage relative to V_{SS}	-1.0V	+3.6V	V
V_{CCQ} I/O Supply Voltage relative to V_{SS}	-1.0V	+3.6V	V
V_{REF} and inputs Voltage relative to V_{SS}	-1.0V	+3.6V	V
I/O pins Voltage relative to V_{SS}	-0.5V	V_{CCQ} + 0.5V	V
Storage Temperature	-55	+150	C
Short circuit current	––	50	mA

Capacitance

Parameter	SYMBOL	MAX	UNITS
Input Capacitance [CKx\CKx\]	C_{I1}	5	pF
Addresses, BA_0-1	C_A	30	pF
Input Capacitance [All other Input Pins]	C_{12}	7	pF
DQ line	C_{10}	8	pF

DC Electrical Characteristics and Operating Conditions (Notes 1, 6)

V_{CC}, V_{CCQ}=+2.5V±0.2V;-55°C ≤ T_A ≤ +125°C

Parameter	Symbol	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	2.3	2.5	2.7	V
I/O Supply Voltage	V_{CCQ}	2.3	2.5	2.7	V
I/O Reference Voltage	V_{REF}	0.49 x V_{CCQ}	0.50 x V_{CCQ}	0.51 x V_{CCQ}	V
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
Input High Voltage	V_{IH}				
Input Low Voltage	V_{IL}				
Input Leakage Current: Any input 0V ≤ V_{IN} ≤ V_{CC}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V All other pins not under test = 0V	I_I	-2		+2	uA
Output Leakage Current: DQ lines disabled; 0V ≤ V_{OUT} ≤ V_{CCQ}	I_{OZ}	-5		+5	uA
Full Drive Output Option	I_{OH}	-16.8		––	mA
	I_{OL}	+16.8		––	mA
Reduced Drive Output Option	I_{OH}	-9		––	mA
	I_{OL}	+9		––	mA
Ambient Operating Temperature					
Industrial = "I"	T_A	-40	25	85	°C
Extended = "E"	T_A	-40	25	105	°C
Mil-Temp = "M"	T_A	-55	25	125	°C

ICC OPERATING SPECIFICATION LIMITS AND CONDITIONS (NOTES 1-5, 10, 12, 14)

VCC, VCCQ=+2.5V±0.2V;-55°C ≤ TA ≤ +125°C

Parameter		Symbol	333 Mbps @CL=2.5	266/250 Mbps @CL=2	200 Mbps @CL=2	Units
OPERATING current: One bank active - precharge $^tCL=^tCK(MIN)$, $^tRC=^tRC(MIN)$, $^tRAS=^tRAS$ MIN(ICC); DQ, DQM, DQS inputs changing once per clock cycle; Address and Control inputs changing once every two clock cycles		ICC0	625	575	520	mA
OPERATING current: One bank active - READ - precharge current Active-Read-Precharge; Burst=2; $^tRC=^tRC(MIN)$; $^tCK=^tCK(MIN)$; IOUT=0mA; Address and control inputs changing once per clock cycle (notes: 22, 48)		ICC1	775	700	650	mA
Precharge POWER-DOWN current All banks idle; POWER-DOWN mode; $^tCK=^tCK(MIN)$, CKE=LOW (notes: 23, 32, 50)		ICC2P	25	25	25	mA
IDLE STANDBY current CS\=HIGH; All banks idle; POWER-DOWN mode; $^tCK=^tCK(MIN)$; CKE=HIGH; Address and other Control inputs changing once per clock cycle; VSS=VREF for DQ, DQS and DM (note: 51)		ICC2F	225	225	195	mA
ACTIVE POWER-DOWN, STANDBY current One bank active; POWER-DOWN mode; $^tCK=^tCK(MIN)$, CKE=LOW (notes: 23, 32, 50)		ICC3P	175	175	150	mA
ACTIVE STANDBY current CS\=HIGH; CKE=HIGH; One bank Active Precharge; $^tRC=^tRAS(MAX)$; $^tCK=^tCK(MIN)$; DQ, DQM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per cycle (note: 22)		ICC3N	225	225	200	mA
OPERATING current Burst=2 READS Continuous Burst; One bank active; Address and Control inputs changing once per clock cycle; $^tCK=^tCK(MIN)$; IOUT=0mA cycle (notes: 22, 48)		ICC4R	350	300	245	mA
OPERATING current Burst=2 WRITES Continuous Burst; One bank active; Address and Control inputs changing once per clock cycle; $^tCK=^tCK(MIN)$; DQ, DQM and DQS inputs changing twice per clock cycle (note: 22)		ICC4W	1250	1025	775	mA
AUTO REFRESH current	$^tREF=^tRC$ (MIN) (notes: 27, 50)	ICC5	1450	1450	1400	mA
	^tREF=7.8125us (notes: 27, 50) =^tRC (MIN)	ICC5A	50	50	50	mA
SELF REFRESH current; CKE= ≤ 0.2V		ICC6	25	25	25	mA
OPERATING current Four bank interleaving READS (BL=4) with AUTO PRECHARGE; $^tRC=^tRC$ (MIN); $^tCK=^tCK$ (MIN); Address and Control inputs change only during ACTIVE READ or WRITE commands (notes: 22, 49)		ICC7	2000	1925	1700	mA

AC Electrical Specifications and Recommend Operating Characteristics (Notes 1-5, 14-17, 33)

			-6, 333 Mbps 167 MHz, CLKx CL = 2.5		-75, 266 [250]Mbps 133 MHz CLKx CL = 2.5 [2]		-8, 250 [200]Mbps 125 MHz CLKx CL = 2.5 [2]		-10, 200 [167] Mbps 100 MHz CLKx CL = 2.5 [2]		
Parameter		**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Access window of DQs from CLKx / CLKx\		^{t}AC	-0.7	0.7	-0.75	0.75	-0.8	0.8	-0.8	0.8	ns
CLKx High level Width		^{t}CH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CLK
CLKx Low level Width		^{t}CL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CLK
Clock Cycle Time	CL=2.5	^{t}CK	6	13	7.5	13	8	13	10	13	ns
	CL=2	^{t}CK	7.5	13	10	13	10	13	13	15	ns
DQ and DM Input Hold Time relative to DQS		^{t}DH	0.45		0.5		0.6			0.6	ns
DQ and DM Input Setup Time relative to DQS		^{t}DS	0.45		0.5		0.6			0.6	ns
DQ and DM Input Pulse Width		^{t}DIPW	1.75		1.75		2		2		ns
Access window of DQs from CLKx / CLKx\		^{t}DQSCK	-0.6	0.6	-0.75	0.75	-0.8	0.8	-0.8	0.8	ns
DQS Input HIGH Pulse Width		^{t}DQSH	0.35		0.35		0.35		0.35		^{t}CLK
DQS Input LOW Pulse Width		^{t}DQSL	0.35		0.35		0.35		0.35		^{t}CLK
DQS-DQ Skew, DQS to last DQ valid, per grp.		^{t}DQSQ		0.45		0.5		0.6		0.6	ns
WRITE command to first DQS latching transition		^{t}DQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	^{t}CLK
DQS falling edge to CLKx rising - setup time		^{t}DSS	0.2		0.2		0.2		0.2		^{t}CLK
DQS falling edge to CLKx rising - hold time		^{t}DSH	0.2		0.2		0.2		0.2		^{t}CLK
Half Clock period		^{t}HP	^{t}CH,^{t}CL		^{t}CH,^{t}CL		^{t}CH,^{t}CL		^{t}CH,^{t}CL		ns
Data-Out HIGH impedance window from CLKx / CLKx\		^{t}HZ		0.7		0.75		0.8		0.8	ns
Data-Out LOW impedance window from CLKx / CLKx\		^{t}LZ	-0.70		-0.75		-0.8		-0.8		ns
Address and Control Input hold time		^{t}IHF	0.75		0.9		1.1		1.1		ns
Address and Control Input setup time		^{t}ISF	0.75		0.9		1.1		1.1		ns
Address and Control Input hold time		^{t}HIS	0.8		1		1.1		1.1		
Address and Control Input setup time		^{t}ISS	0.8		1		1.1		1.1		
Load Mode Register		^{t}MRD	12		15		16		16		ns
DQ-DQS hold. DQS to first DQ to go non-valid		^{t}QH	^{t}HP-^{t}QHS		^{t}HP-^{t}QHS		^{t}HP-^{t}QHS		^{t}HP-^{t}QHS		ns
Data Hold skew factor		^{t}QHS		0.55		0.75		1		1	ms
ACTIVE to PRECHARGE command		^{t}RAS	42	70000	40	120000	40	120000	40	120000	ms
ACTIVE to READ with AUTO PRECHARGE command		^{t}RAP	15		20		20		20		ms
ACTIVE to ACTIVE/AUTO REFRESH command per.		^{t}RC	60		65		70		70		ns
AUTO REFRESH command period		^{t}RFC	72		75		80		80		ns
ACTIVE to READ or WRITE delay		^{t}RCD	15		20		20		20		ns
PRECHARGE command period		^{t}RP	15		20		20		20		ns
DQS READ Preamble		^{t}RPRC	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CLK
DQS READ Postamble		^{t}RPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CLK
ACTIVE bank to ACTIVE bank b command		^{t}RRD	12		15		15		15		ns
DQS WRITE Preamble		^{t}WPRC	0.25		0.25		0.25		0.25		^{t}CLK
DQS READ Preamble Setup Time		^{t}WPRCS	0		0		0		0		ns

AC Electrical Specifications and Recommend Operating Characteristics (Notes 1-5, 14-17, 33)

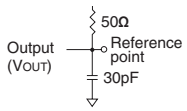
		-6, 333 Mbps 167 MHz, CLKx CL = 2.5		-75, 266 [250]Mbps 133 MHz CLKx CL = 2.5 [2]		-8, 250 [200]Mbps 125 MHz CLKx CL = 2.5 [2]		-10, 200 [167] Mbps 100 MHz CLKx CL = 2.5 [2]		
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
DQS WRITE Postamble	^{t}WPST	0.4		0.4		0.4	0.6	0.4	0.6	^{t}CLK
WRITE Recovery Time	^{t}WR	12		15		15		15		ns
Internal WRITE to READ command delay	^{t}WTR	1		1		1		1		^{t}CLK
Data Valid Output Window	na	^{t}QH-^{t}DQSQ		^{t}QH-^{t}DQSQ		^{t}QH-^{t}DQSQ		^{t}QH-^{t}DQSQ		us
REFRESH to REFRESH command Interval (Industrial)	^{t}REFC		70.3		70.3		70.3		70.3	us
REFRESH to REFRESH command Interval (Extended)	^{t}REFC		35		53		53		53	us
REFRESH to REFRESH command Interval (Mil-Temp)	^{t}REFC		7.8		35		35		35	us
Average Periodic REFRESH Interval (Industrial)	^{t}REFI		3.9		7.8		7.8		7.8	us
Average Periodic REFRESH Interval (Extended)	^{t}REFI		5.9		5.9		5.9		5.9	us
Average Periodic REFRESH Interval (Mil-Temp)	^{t}REFI		3.9		3.9		3.9		3.9	us
Terminating delay reference to V_{DD}	^{t}VTD	0		0		0		0		ns
Exit Self REFRESH to non-READ Command	^{t}XSNR	75		75		80		80		ns
Exit Self REFRESH to READ Command	^{t}XSRD	200		200		200		200		^{t}CLK

AC Specification Notes

1.All voltages referenced to V_{SS}

2.Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and the device operation are guaranteed for the full voltage range specified.

3. Outputs (except for I_{DD} measurements) measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.

5. The AC and DC input level specifications are as defined in the SSTL_2 standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. All speeds may not be offered on all device grades. Refer to "Ordering Information" for availability.

7. V_{REF} is expected to equal $V_{DDQ/2}$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on V_{REF} may not exceed ±2% of the DC value. Thus, from $V_{DDQ/2}$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.

8. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, it is expected to be set equal to V_{REF}, and it must track variations in the DC level of V_{REF}.

9. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

10. The value of V_{IX} and V_{MP} is expected to equal $V_{DDQ/2}$ of the transmitting device and must track variations in the DC level of the same.

11. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle times.

12. Enables on-chip refresh and address counters.

13. I_{DD} specifications are tested after the device is properly initialized and is averaged at the defined cycle rate.

14. This parameter is sampled. V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100MHz, T_A= 25°C, $V_{OUT(DC)}$ = $V_{DDQ/2}$, V_{OUT} (peak-to-peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.

15. For slew rates less than 1 V/ns and greater than or equal to 0.5 V/ns. If the slew rate is less than 0.5 V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100 mV/ns reduction in slew rate from the 500 mV/ns. ^{t}IH has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain.

16. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.

17. Inputs are not recognized as valid until V_{REF} stabilizes. Once initialized, including self refresh mode, V_{REF} must be powered within specified range. Exception: during the period before V_{REF} stabilizes, CKE < 0.3 × V_{DD} is recognized as LOW.

18. The output timing reference level, as measured at the timing reference point (indicated in Note 3), is V_{TT}.

19. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as data valid transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (High-Z) or begins driving (Low-Z).

20. The intent of the "Don't Care" state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW, or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above $V_{IH[DC]}$ MIN) then it must not transition LOW (below $V_{IH[DC]}$ prior to $^{t}DQSH$ [MIN]).

21. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.

22. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on $^{t}DQSS$.

23. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

24. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs (15.625µs for 128Mb DDR). However, an AUTO REFRESH command must be asserted at least once every 70.3µs (140.6µs for 128Mb DDR); burst refreshing or posting by the DRAM controller greater than 8 REFRESH cycles is not allowed.

25. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

26. The data valid window is derived by achieving other specifications: ^{t}HP ($^{t}CK/2$), $^{t}DQSQ$, and ^{t}QH ($^{t}QH = {}^{t}HP - {}^{t}QHS$). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, because functionality is uncertain when operating beyond a 45/55 ratio. 27. Referenced to each output group: x4 = DQS with DQ_0–DQ_3; x8 = DQS with DQ_0–DQ_7; x16 = LDQS with DQ_0–DQ_7 and UDQS with DQ_8–DQ_{15}.

28. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during the REFRESH command period (^{t}RFC [MIN]), else CKE is LOW (that is, during standby).

AC Specification Notes

29. To maintain a valid level, the transitioning edge of the input must:

a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.

b. Reach at least the target AC level.

c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.

30. The input capacitance per pin group will not differ by more than this maximum amount for any given device.

31. CK and CK# input slew rate must be ≥1 V/ns (≥2 V/ns if measured differentially).

32. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100 mV/ns reduction in slew rate.

33. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.

34. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.

35. ^{t}HP (MIN) is the lesser of ^{t}CL (MIN) and ^{t}CH (MIN) actually applied to the device CK and CK# inputs, collectively, during bank active.

36. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.

37. Any positive glitch must be less than 1/3 of the clock cycle and not more than +400mV or 2.9V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either –300mV or 2.2V, whichever is more positive. The average cannot be below the +2.5V minimum.

38. Normal output drive curves:

a. The full driver pull-down current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 4.

b. The driver pull-down current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 4.

c. The full driver pull-up current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 5.

d. The driver pull-up current variation within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 5.

e. The full ratio variation of MAX to MIN pull-up and pull-down current should be between 0.71 and 1.4 for drain-to-source voltages from 0.1V to 1.0V at the same voltage and temperature.

f. The full ratio variation of the nominal pull-up to pull-down current should be unity ±10% for device drain-to-source

Figure 4 - Full Drive Pull-Down Characteristics

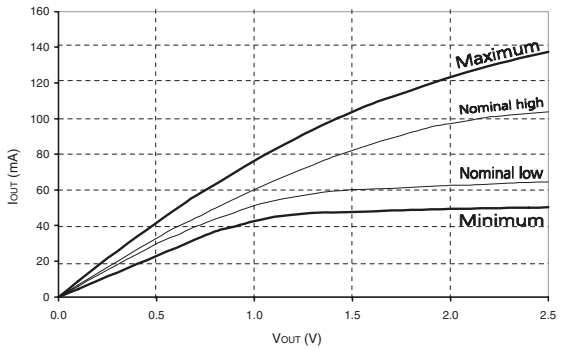
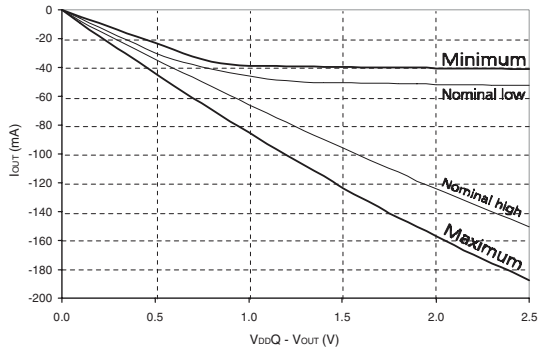


Figure 5 - Full Drive Pull-Up Characteristics



39. Reduced output drive curves:

a. The full driver pull-down current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 6.

b. The driver pull-down current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 6.

c. The full driver pull-up current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 7.

d. The driver pull-up current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 7.

e. The full ratio variation of the MAX-to-MIN pull-up and pull-down current should be between 0.71 and 1.4 for device drain-to-source voltages from 0.1V to 1.0V at the same voltage and temperature.

AC Specification Notes

f. The full ratio variation of the nominal pull-up to pull-down current should be unity ±10%, for device drain-to-source voltages from 0.1V to 1.0V.

Figure 6 - Reduced Drive Pull-Down Characteristics

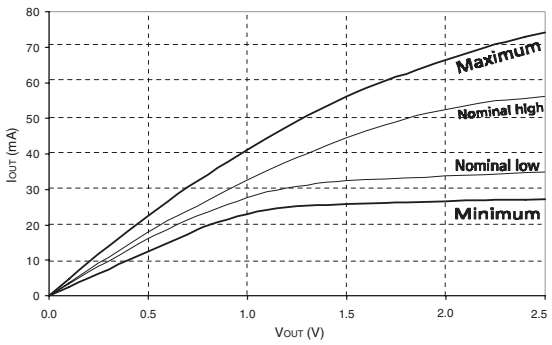
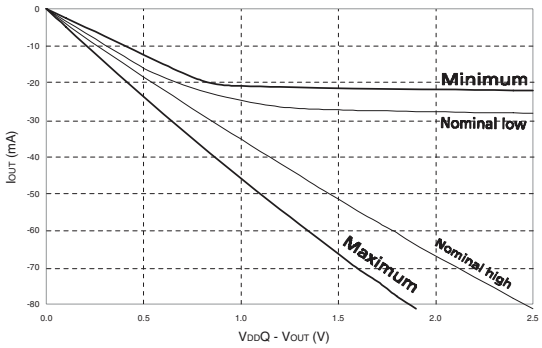


Figure 7 - Reduced Drive Pull-Up Characteristics



40. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.

41. VIH overshoot: VIH (MAX) = VDDQ + 1.5V for a pulse width ≤ 3ns, and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL (MIN) = –1.5V for a pulse width ≤ 3ns, and the pulse width can not be greater than 1/3 of the cycle rate.

42. VDD and VDDQ must track each other.

43. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition. ^{t}LZ (MIN) will prevail over ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.

44. ^{t}RPST end point and ^{t}RPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (^{t}RPST) or begins driving (^{t}RPRE).

45. During initialization, VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power-up, even if VDD/VDDQ are 0V, provided a minimum of 42Ω of series resistance is used between the VTT supply and the input pin.

46. The current LDI part operates below 83 MHz (slowest specified JEDEC operating frequency). As such, future die may not reflect this option.

47. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or LOW.

48. Random address is changing; 50% of data is changing at every transfer.

49. Random address is changing; 100% of data is changing at every transfer.

50. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}RFC has been satisfied.

51. IDD2N specifies the DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is “worst case.”

52. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset followed by 200 clock cycles before any READ command.

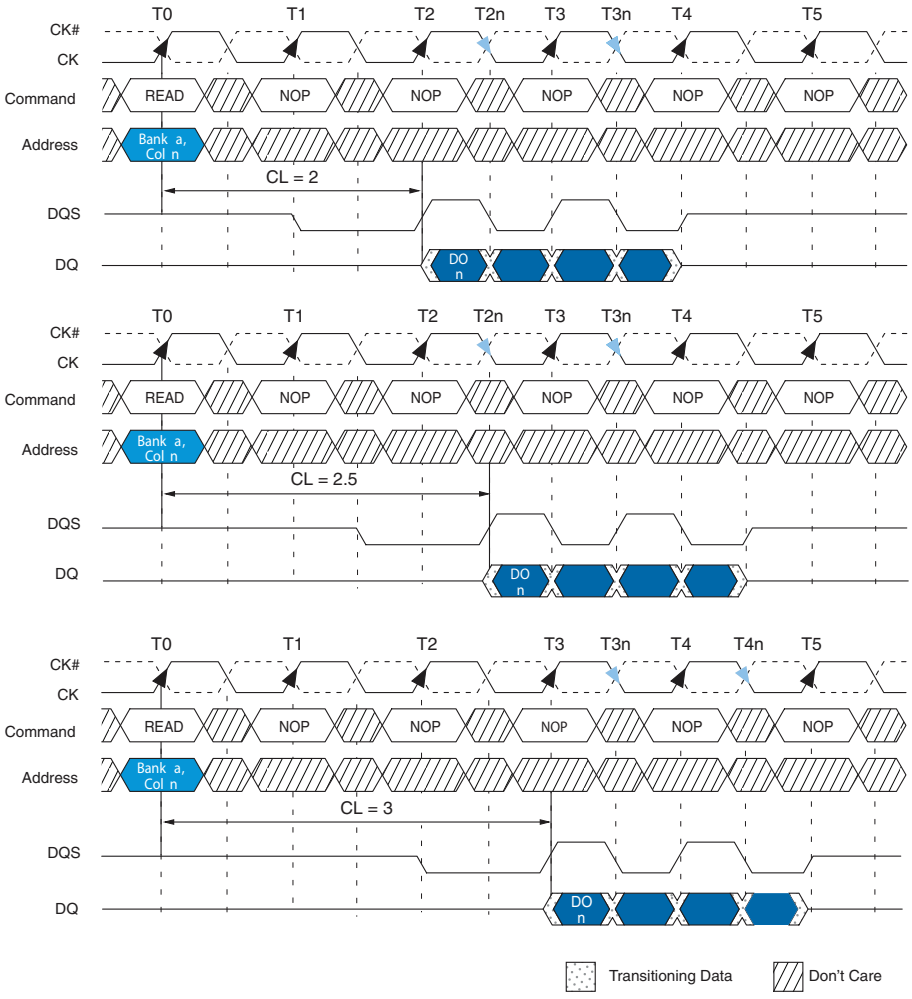
53. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz. Any noise above 20 MHz at the DRAM generated from any source other than that of the DRAM itself may not exceed the DC voltage range of 2.6V ±100mV.

54. The -6 speed grades will operate with ^{t}RAS (MIN) = 40ns and ^{t}RAS (MAX) = 120,000ns at any slower frequency.

AC SWITCHING DIAGRAMS

AC Switching diagrams reference 16 bits, LDI's IMOD contains (5) 16 bit devices totaling 80 bits

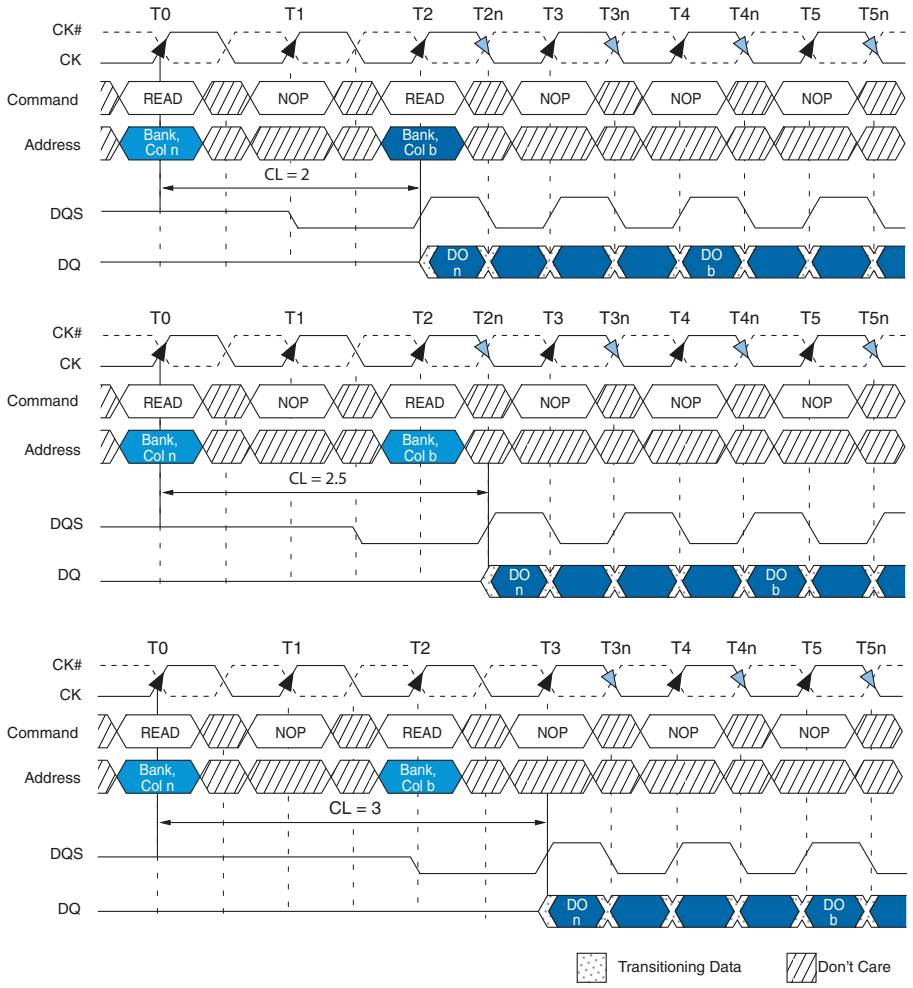
FIGURE 8 - READ BURST



Notes:
1. DO n = data-out from column n.
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

AC SWITCHING DIAGRAMS

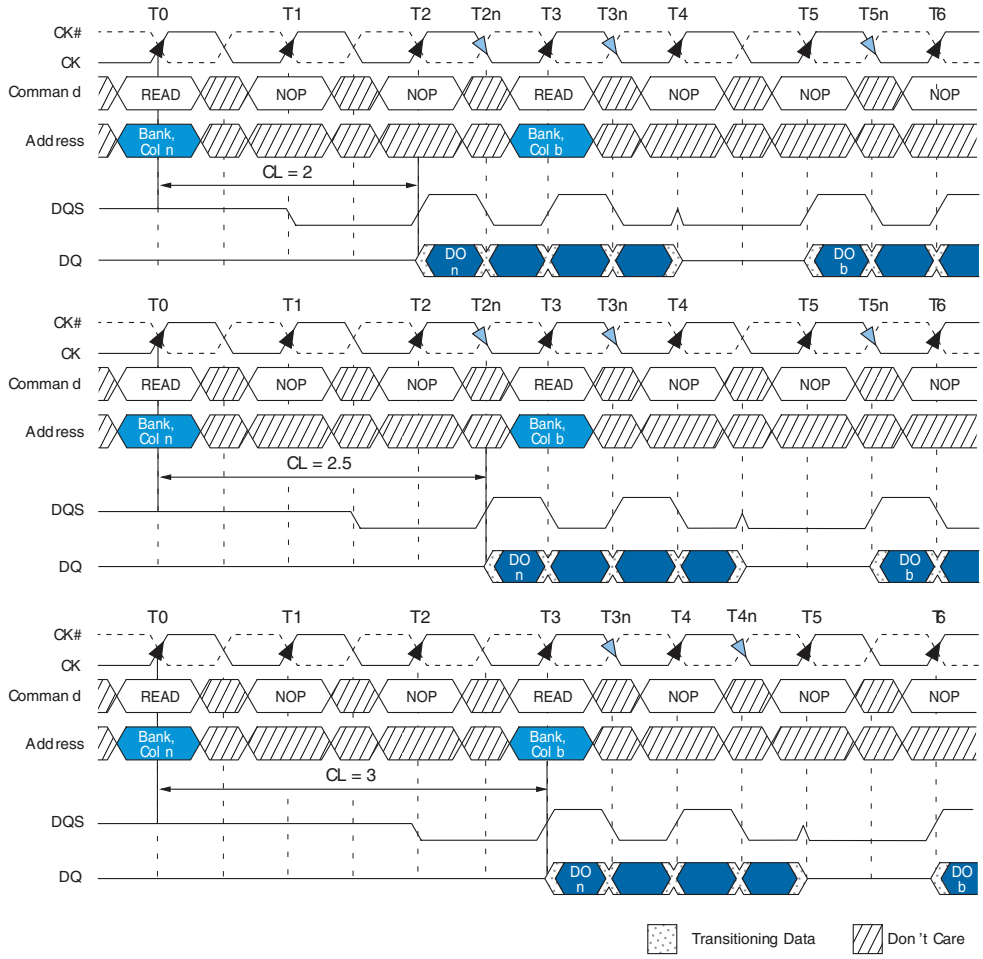
FIGURE 9 - CONSECUTIVE READ BURST



Notes:
1. DO n (or b) = data-out from column n (or column b).
2. BL = 4 or BL = 8 (if BL = 4, the bursts are concatenated; if BL = 8, the second burst interrupts the first).
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO b.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies only when READ commands are issued to same device.

AC SWITCHING DIAGRAMS

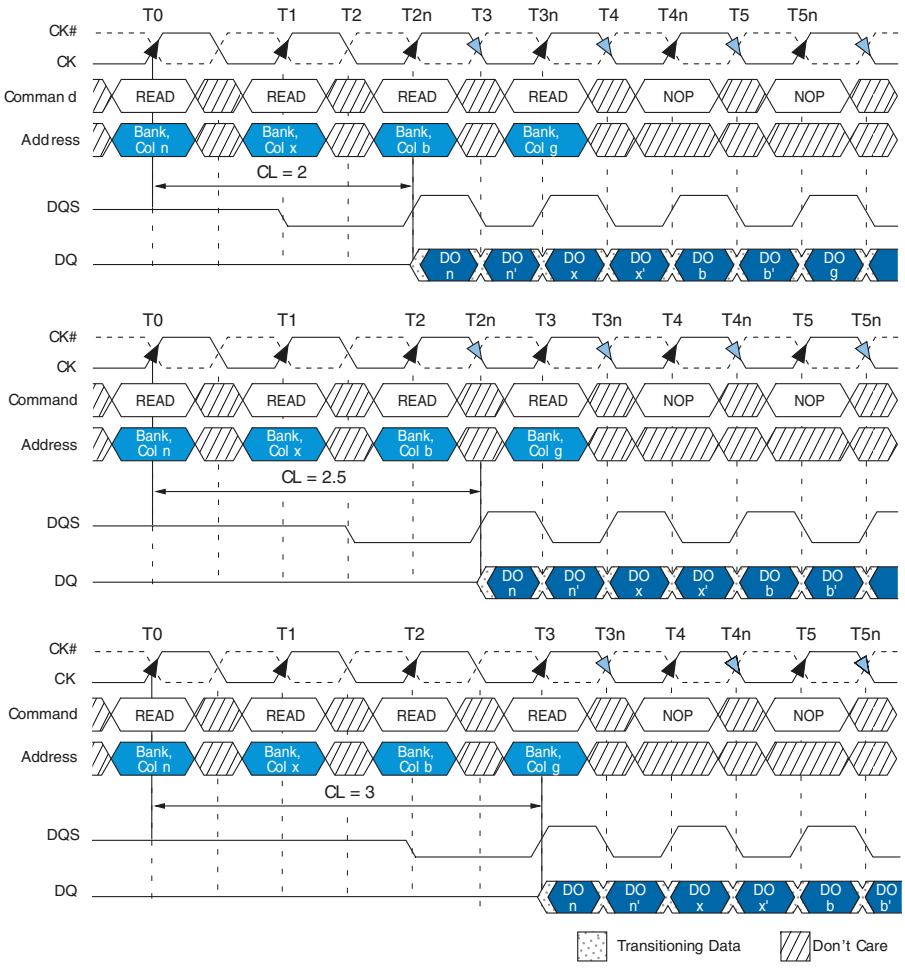
FIGURE 10 - NONCONSECUTIVE READ BURST



Notes:
1. DO n (or b) = data-out from column n (or column b).
2. BL = 4 or BL = 8 (if BL = 4, the bursts are concatenated; if BL = 8, the second burst interrupts the first).
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO b.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

AC SWITCHING DIAGRAMS

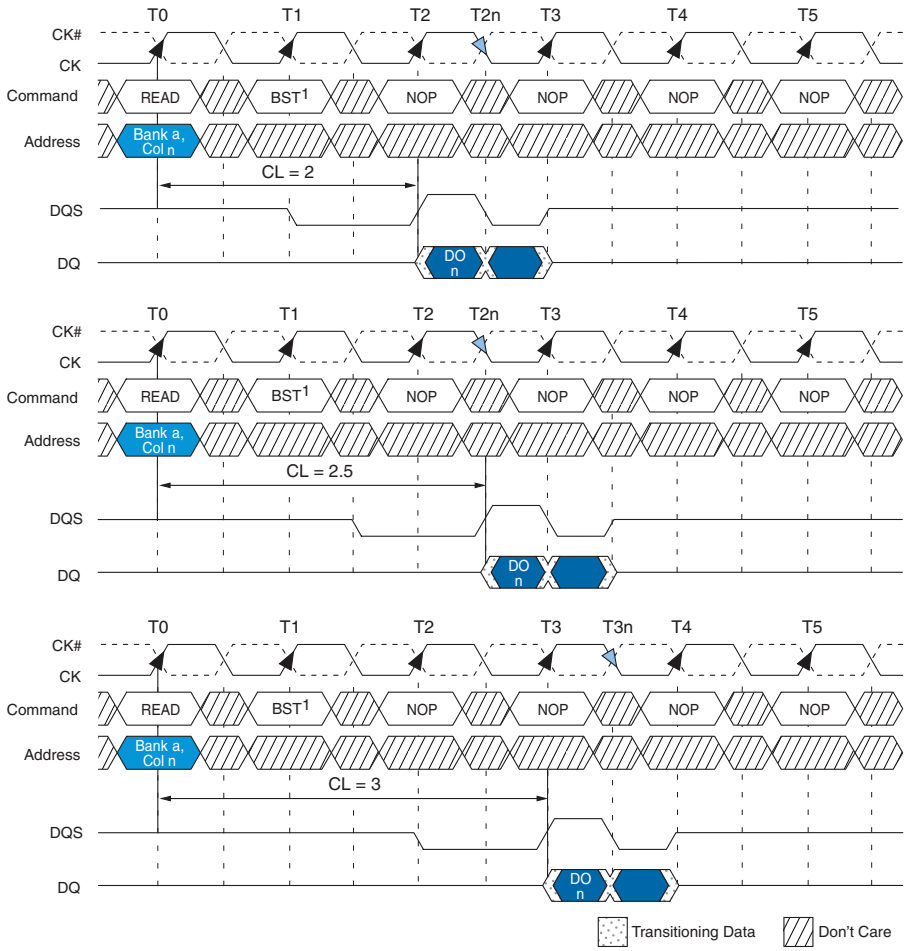
FIGURE 11 - RANDOM READ ACCESSES



Notes:
1. DO n (or x or b or g) = data-out from column n (or column x (or column b or column g).
2. BL = 2, BL = 4, or BL = 8 (if BL = 4 or BL = 8, the following burst interrupts the previous).
3. n', x', b', or g' indicate the next data-out following DO n, DO x, DO b, or DO g, respectively.
4. READs are to an active row in any bank .
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

AC SWITCHING DIAGRAMS

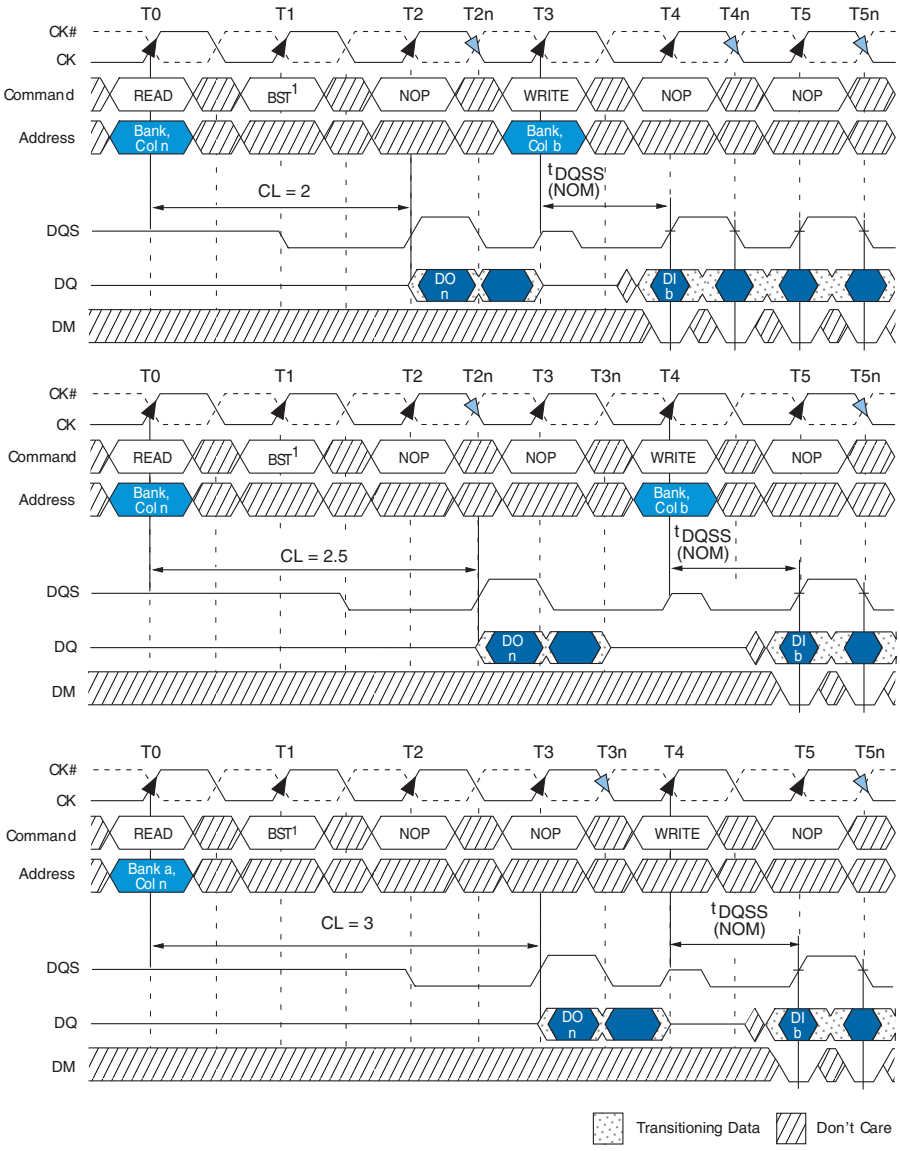
FIGURE 12 - TERMINATING A READ BURST



Notes:
1. Page remains open.
2. DO n = data-out from column n.
3. BL = 4.
4. Subseqent element of data-out appears in the programmed order following DO n.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

AC SWITCHING DIAGRAMS

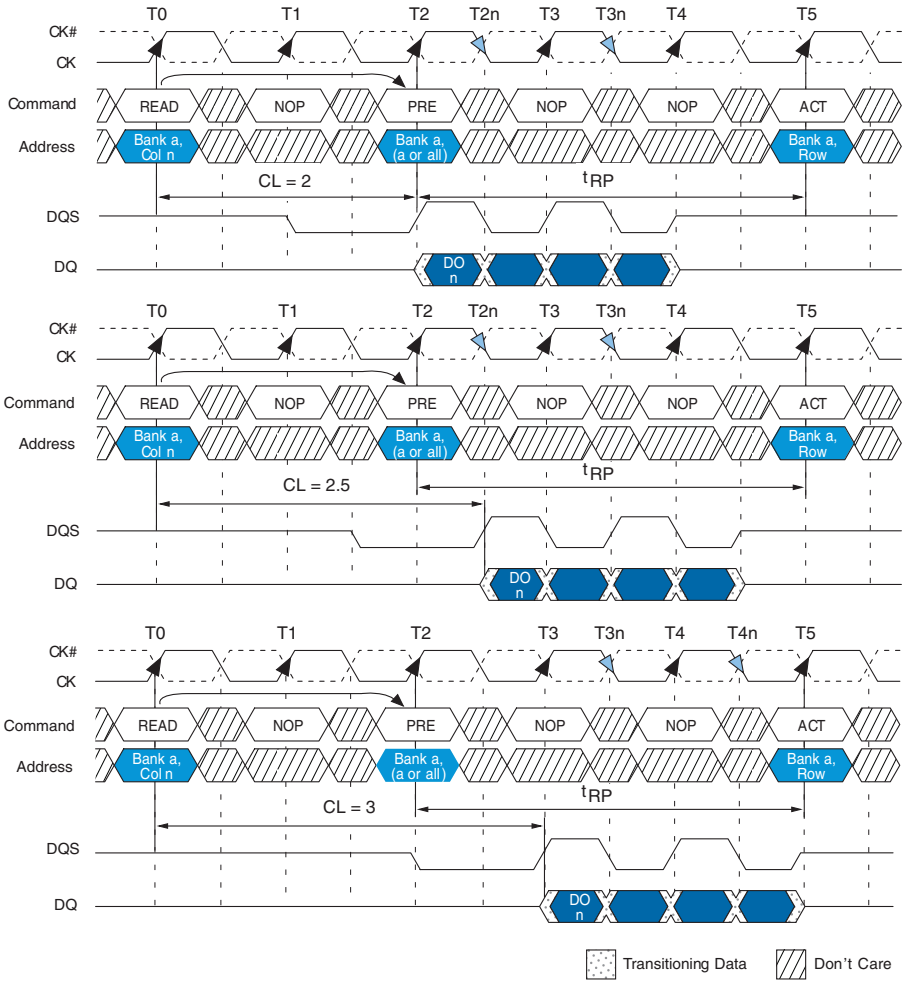
FIGURE 13 - READ TO WRITE



Notes:
1. Page remains open.
2. DO n = data-out from column n; DI b = data-in from column b.
3. BL = 4 (applies for bursts of 8 as well; if BL = 2, the BURST command shown can be NOP).
4. One subsequent element of data-out appears in the programmed order following DO n.
5. Data-in elements are applied following DI b in the programmed order.
6. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

AC SWITCHING DIAGRAMS

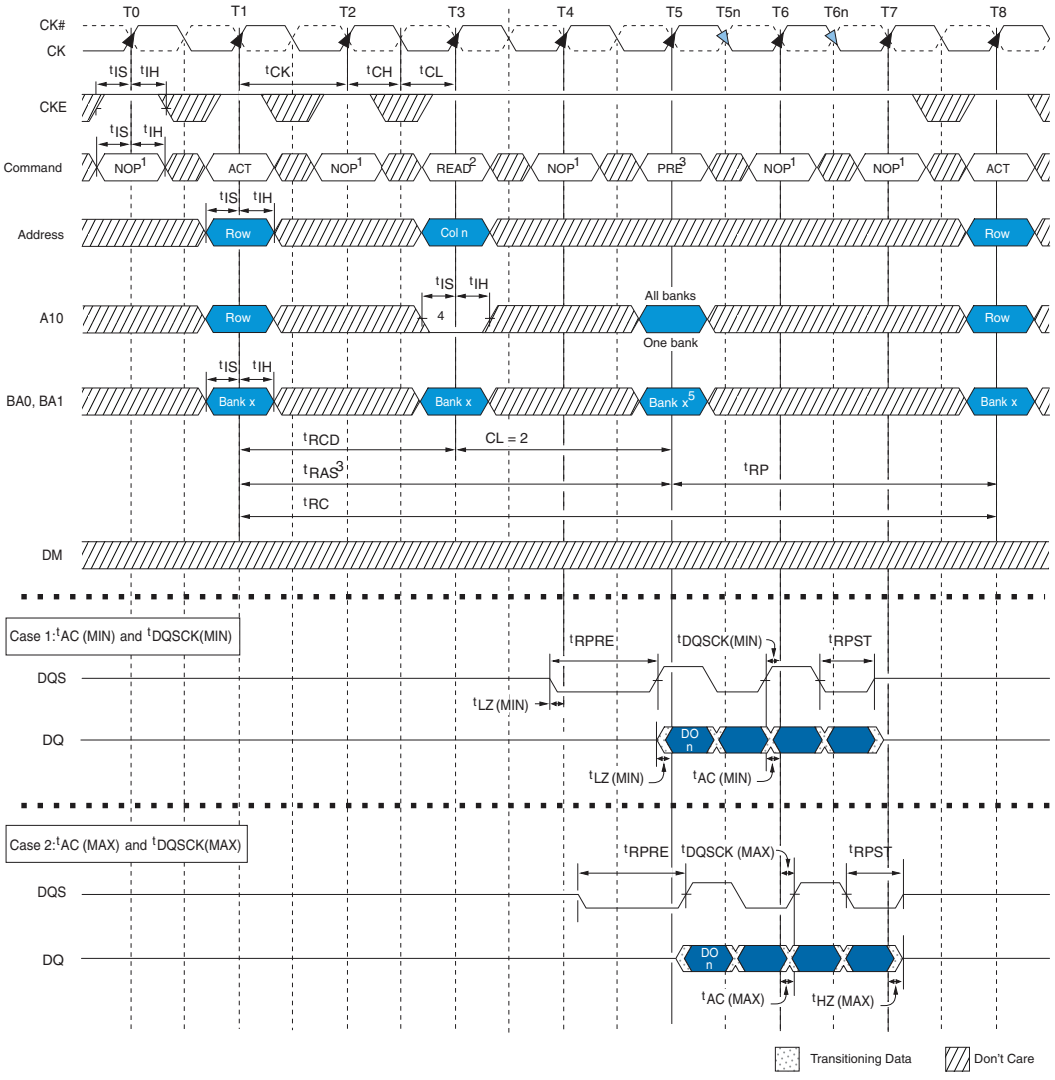
FIGURE 14 - READ TO PRECHARGE



Notes:
1. Provided ^{t}RAS (MIN) is met, a READ command with auto precharge enabled would cause a precharge to be performed at x number of clock cycles after the READ command, where x = BL/2.
2. DO n = data-out from column n.
3. BL = 4 or an interrupted burst of 8.
4. Three subsequent elements of data-out appear in the programmed order following DO n.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. READ-to-PRECHARGE equals two clocks, which allows two data pairs of data-out; it is also assumed that ^{t}RAS (MIN) is met.
7. An ACTIVE command to the same bank is only allowed if ^{t}RC (MIN) is met.

AC SWITCHING DIAGRAMS

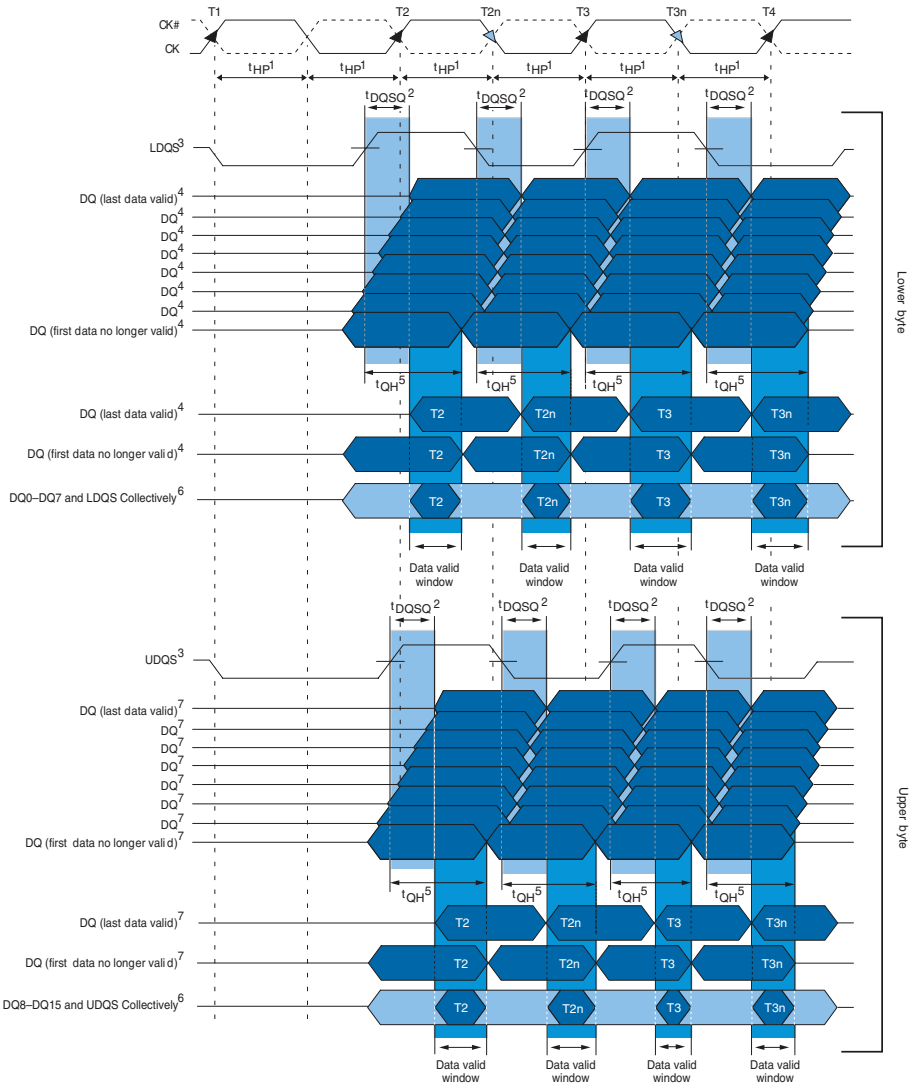
FIGURE 15 - BANK READ WITHOUT PRECHARGE



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4.
3. The PRECHARGE command can only be applied at T5 if ^{t}RAS (MIN) is met.
4. Disable auto precharge.
5. "Don't Care" if A10 is HIGH at T5.
6. DO n (or b) = data-out from column n (or column b); subsequent elements are provided in the programmed order.

AC SWITCHING DIAGRAMS

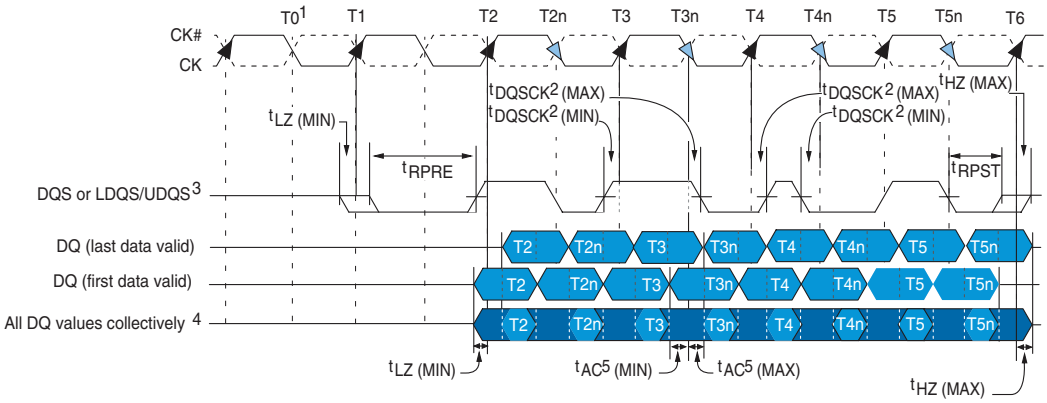
FIGURE 16 - DATA OUTPUT TIMING – ^{t}DQSQ, ^{t}QH, AND DATA VALID WINDOW



Notes:
1. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
2. ^{t}DQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transition, and ends with the last valid DQ transition.
3. DQ transitioning after DQS transition define the ^{t}DQSQ window. LDQS defines the lower byte, and UDQS defines the upper byte.
4. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
5. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
6. The data valid window is derived for each DQS transition and is ^{t}QH - ^{t}DQSQ.
7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

AC SWITCHING DIAGRAMS

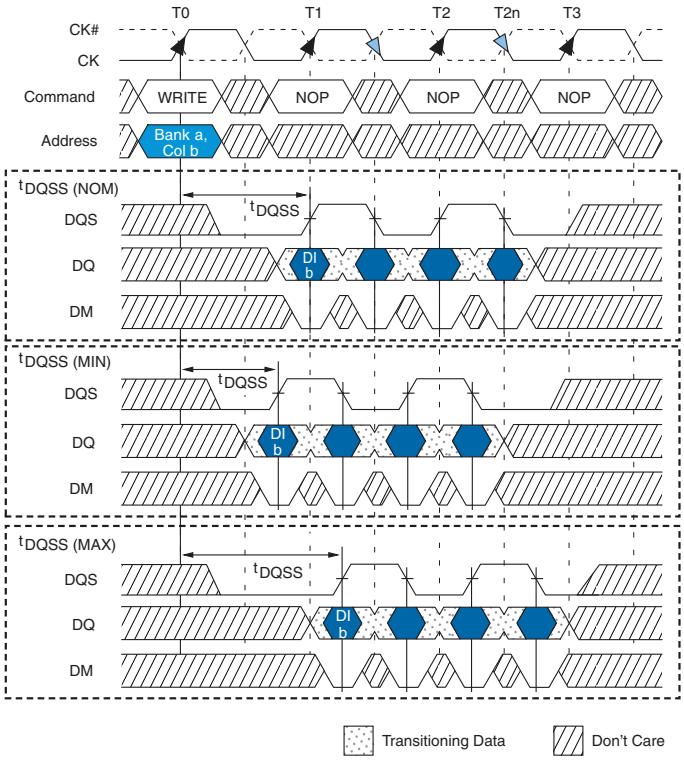
FIGURE 17 - DATA OUTPUT TIMING - tAC AND tDQSCK



Notes:
1. READ command with CL = 2 issued at T0.
2. tDQSCK is the DQS output window relative to CK and is the “long term” component of the DQS skew.
3. DQ transitioning after DQS transition define the tDQSQ window.
4. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
5. tAC is the DQ output window relative to CK and is the “long term” component of DQ skew.
6. tLZ (MIN) and tAC (MIN) are the first valid signal transitions.
7. tHZ (MAX) and tAC (MAX) are the latest valid signal transitions.

AC SWITCHING DIAGRAMS

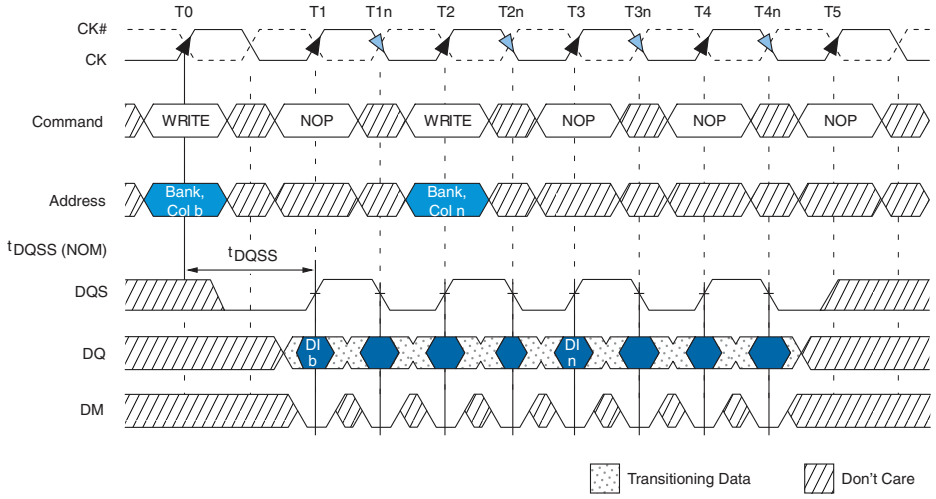
FIGURE 18 - WRITE BURST



Notes:
1. DI b = data-in for column b.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. An uninterrupted burst of 4 is shown.
4. A10 is LOW with the WRITE command (auto precharge is disabled).

AC SWITCHING DIAGRAMS

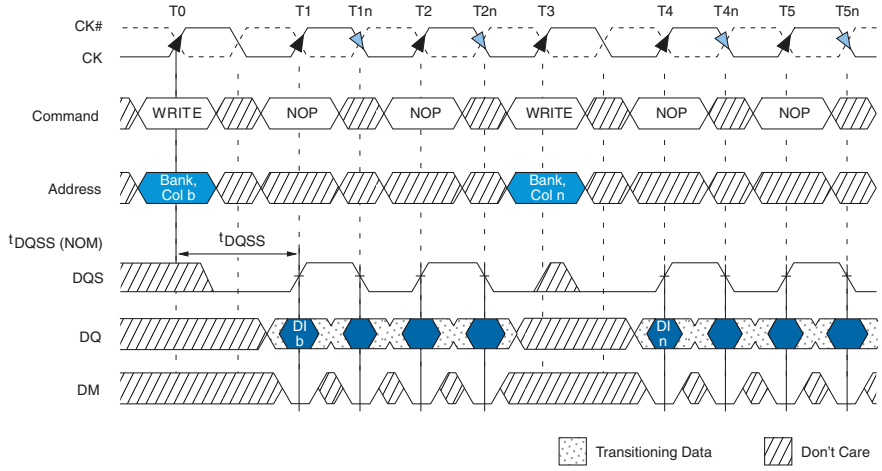
FIGURE 19 - CONSECUTIVE WRITE TO WRITE



Notes:
1. DI b (or n) = data-in from column b (or column n).
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. Three subsequent elements of data-in are applied in the programmed order following DI n.
4. An uninterrupted burst of 4 is shown.
5. Each WRITE command may be to any bank.

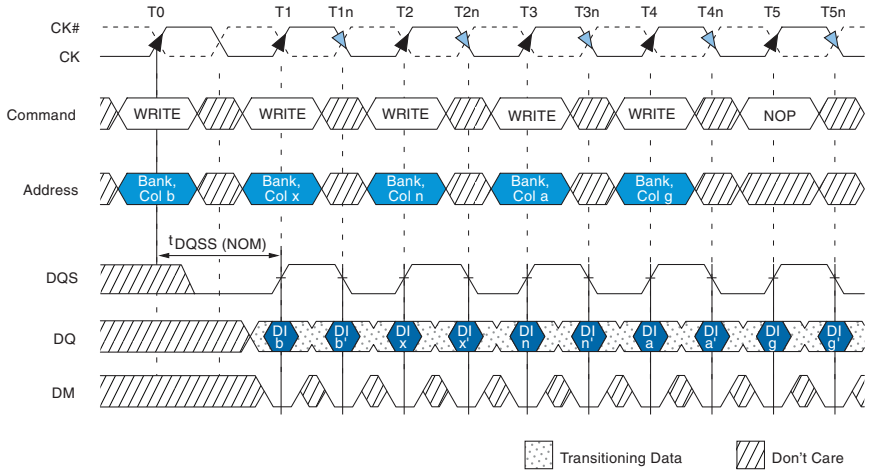
AC SWITCHING DIAGRAMS

FIGURE 20 - NONCONSECUTIVE WRITE TO WRITE



Notes:
1. DI b (or n) = data-in from column b (or column n).
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. Three subsequent elements of data-in are applied in the programmed order following DI n.
4. An uninterrupted burst of 4 is shown.
5. Each WRITE command may be to any bank.

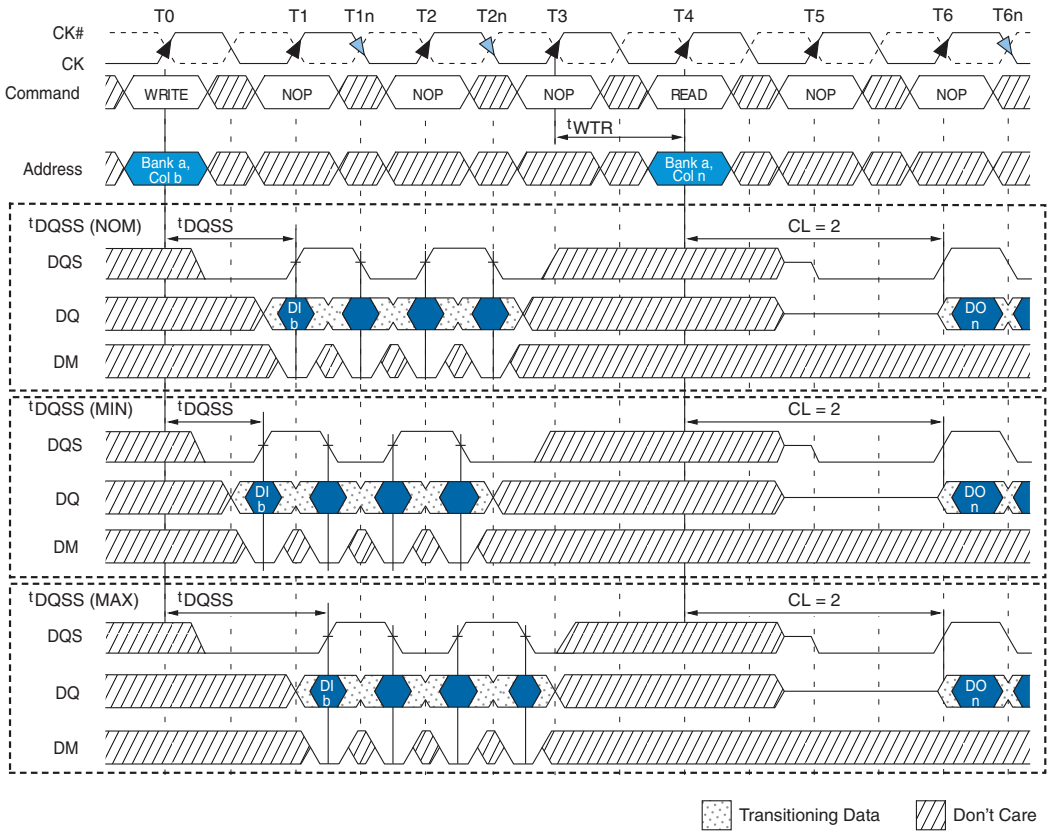
FIGURE 21 - RANDOM WRITE CYCLES



Notes:
1. DI b (or x or n or a or g) = data-in from column b (or column x, or column n, or column a, or column g).
2. b', x', n', a' or g' indicate the next data-in following DO b, DO x, DO n, DO a, or DO g, respectively.
3. Programmed BL = 2, BL = 4, or BL = 8 in cases shown.
4. Each WRITE command may be to any bank.

AC SWITCHING DIAGRAMS

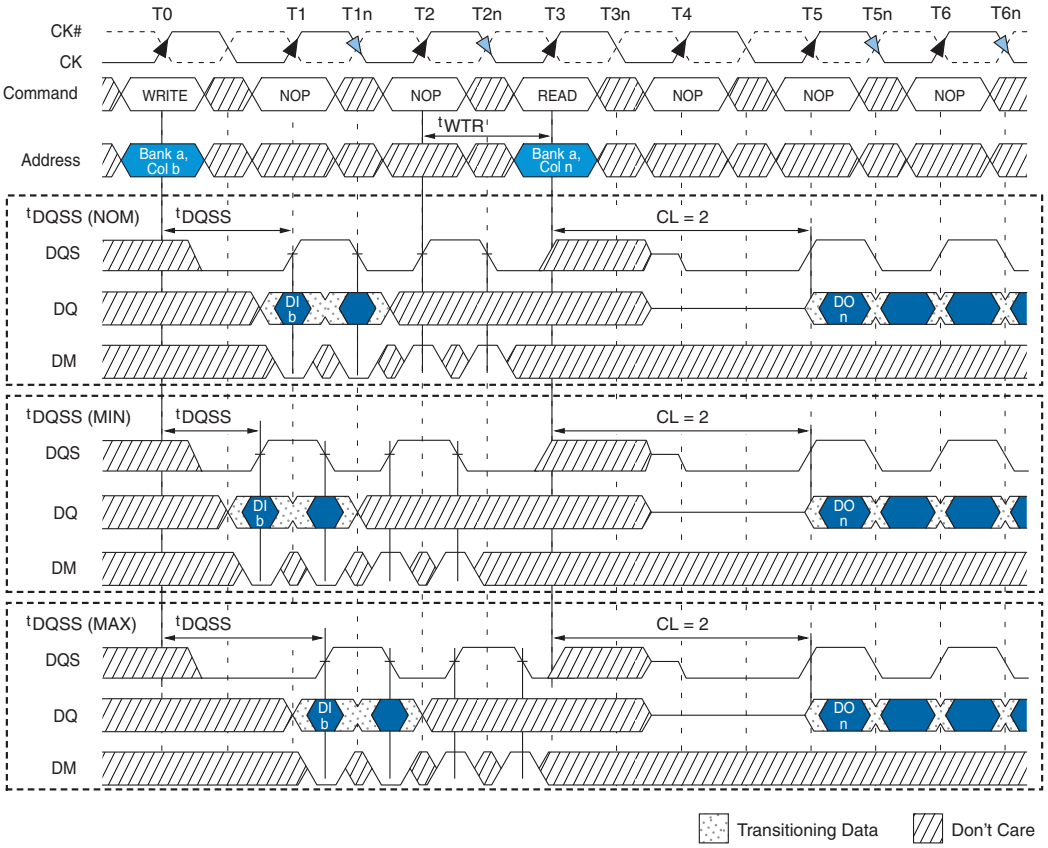
FIGURE 22 - WRITE TO READ UNINTERRUPTED



Notes:
1. DI b = data-in for column b; DO n = data-out for column n.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. An uninterrupted burst of 4 is shown.
4. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case ^{t}WTR is not required, and the READ command could be applied earlier.
6. A10 is LOW with the WRITE command (auto precharge is disabled).

AC SWITCHING DIAGRAMS

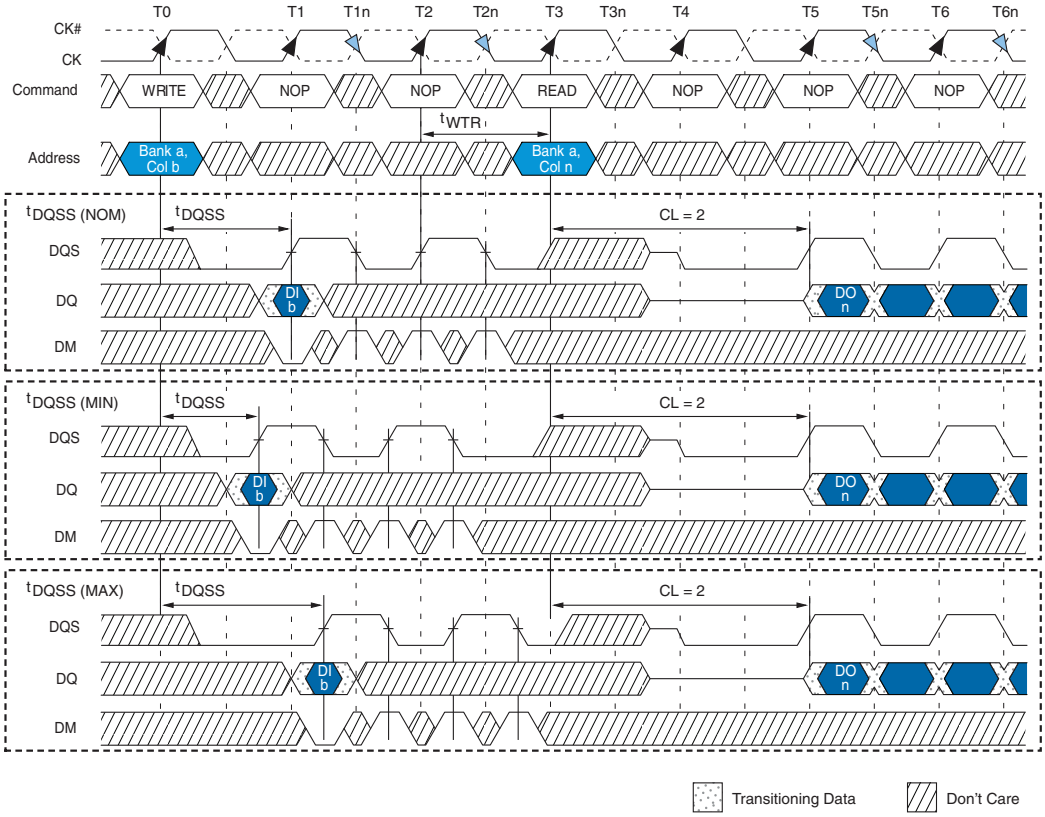
FIGURE 23 - WRITE TO READ INTERRUPTING



Notes:
1. DI b = data-in for column b; DO n = data-out for column n.
2. An interrupted burst of 4 is shown; two data elements are written.
3. One subsequent element of data-in is applied in the programmed order following DI b.
4. tWTR is referenced from the first positive CK edge after the last data-in pair.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. DQS is required at T2 and T2n (nominal case) to register DM.
7. If the burst of 8 is used, DM and DQS are required at T3 and T3n because the READ command will not mask these two data elements.

AC SWITCHING DIAGRAMS

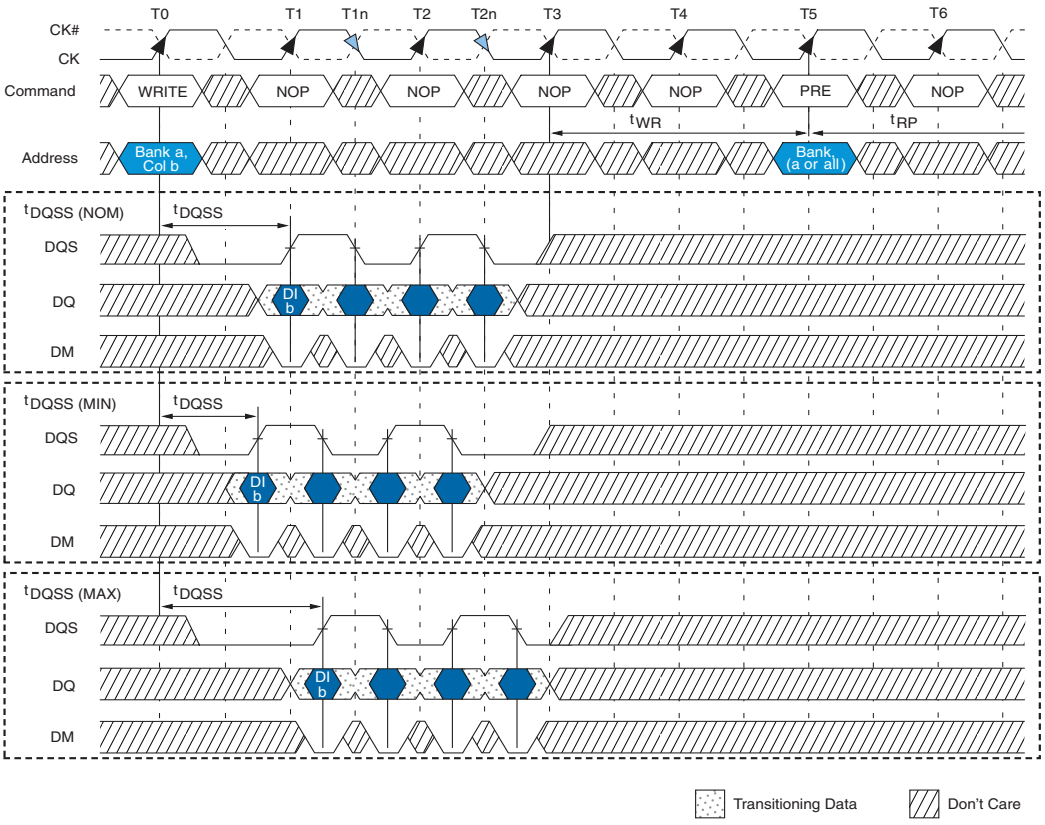
FIGURE 24 - WRITE TO READ, ODD NUMBER OF DATA, INTERRUPTING



Notes:
1. DI b = data-in for column b; DO n = data-out for column n.
2. An interrupted burst of 4 is shown; one data element is written.
3. ^{t}WTR is referenced from the first positive CK edge after the last desired data-in pair (not the last two data elements).
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T1n, T2, and T2n (nominal case) to register DM.
6. If the burst of 8 is used, DM and DQS are required at T3–T3n because the READ command will not mask these data elements.

AC SWITCHING DIAGRAMS

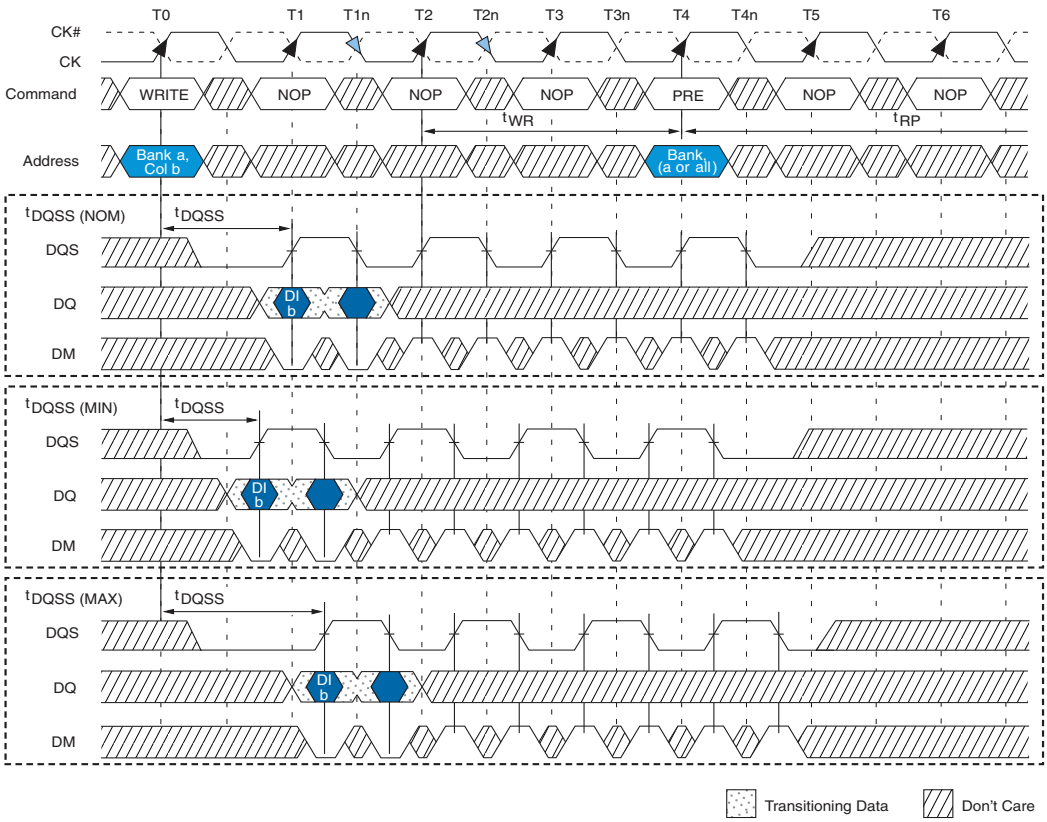
FIGURE 25 - WRITE TO PRECHARGE - UNINTERRUPTED



Notes:
1. DI b = data-in for column b.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. An uninterrupted burst of 4 is shown.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case ^{t}WR is not required and the PRECHARGE command could be applied earlier.
6. A10 is LOW with the WRITE command (auto precharge is disabled).

AC SWITCHING DIAGRAMS

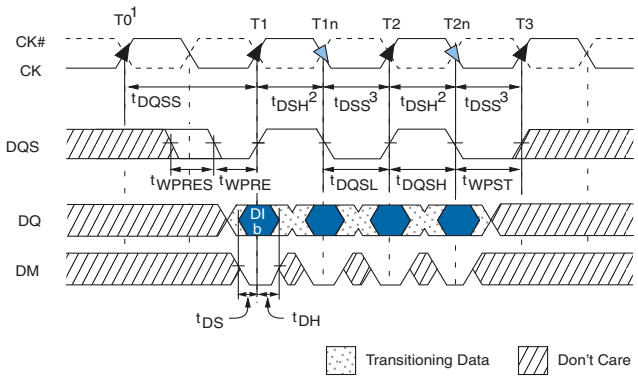
FIGURE 26 - WRITE TO PRECHARGE - INTERRUPTING



Notes:
1. DI b = data-in for column b.
2. Subsequent element of data-in is applied in the programmed order following DI b.
3. An interrupted burst of 8 is shown; two data elements are written.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. DQS is required at T4 and T4n (nominal case) to register DM.
7. If the burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.

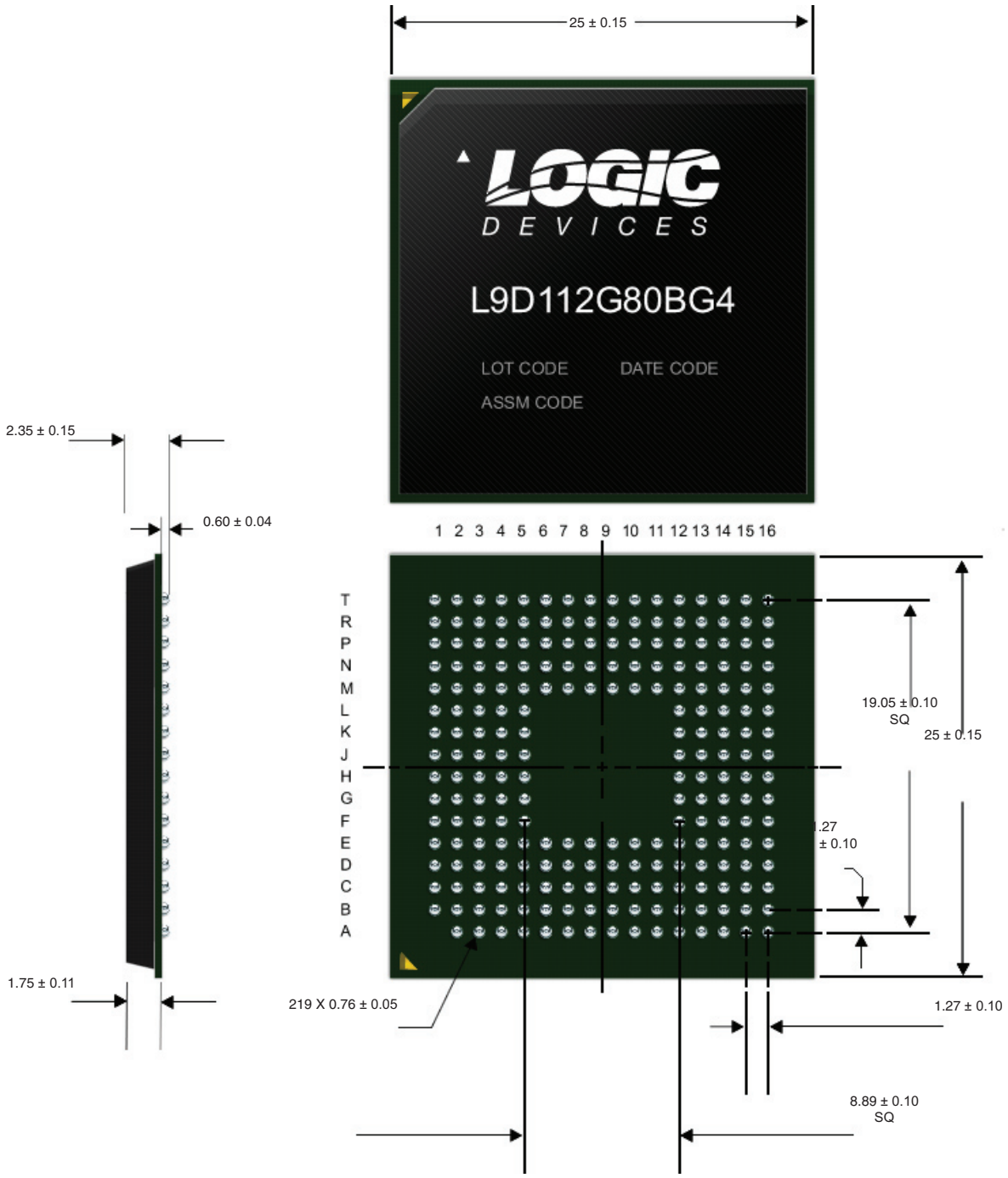
AC SWITCHING DIAGRAMS

FIGURE 27 - DATA INPUT TIMING



Notes:
1. WRITE command issued at T0.
2. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
3. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
4. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
5. DI b = data-in from column b.

Mechanical Drawing



Ordering Information

Part Number	Core FREQ.	Data Transfer Rate	Package	Grade
L9D112G80BG4I6	166 MHz	333 Mbps	25mm2-219 PBGA	INDUSTRIAL
L9D112G80BG4E6	166 MHz	333 Mbps	25mm2-219 PBGA	EXTENDED
L9D112G80BG4M6	166 MHz	333 Mbps	25mm2-219 PBGA	MIL-TEMP
L9D112G80BG4I75	133 MHz	266 Mbps	25mm2-219 PBGA	INDUSTRIAL
L9D112G80BG4E75	133 MHz	266 Mbps	25mm2-219 PBGA	EXTENDED
L9D112G80BG4M75	133 MHz	266 Mbps	25mm2-219 PBGA	MIL-TEMP
L9D112G80BG4I8	125 MHz	250 Mbps	25mm2-219 PBGA	INDUSTRIAL
L9D112G80BG4E8	125 MHz	250 Mbps	25mm2-219 PBGA	EXTENDED
L9D112G80BG4M8	125 MHz	250 Mbps	25mm2-219 PBGA	MIL-TEMP
L9D112G80BG4I10	100 MHz	200 MHz	25mm2-219 PBGA	INDUSTRIAL
L9D112G80BG4E10	100 MHz	200 MHz	25mm2-219 PBGA	EXTENDED
L9D112G80BG4M10	100 MHz	200 MHz	25mm2-219 PBGA	MIL-TEMP

Revision History

Revision	Engineer	Issue Date	Description Of Change
A	DH/JM	11/7/2008	INITIATE
B	DH/JM	01/21/2009	Pgs 1, 45: Change all incidences of “LBGA” to “PBGA”, revise wording to Plastic Ball Grid Array Pgs 4,5: Revision to include ball E12, Vref in Pin/Ball Locations/Definitions Section Pg 8 : Changes to allowable frequency parameters (CAS =2) in CAS latency table (speed -10 changes from ≤75 to ≤83, -75 changes from ≤100 to ≤125, -6 changes from ≤133 to NA) Pg 19: Revise CL parameter (333 Mbps: change CL from 2 to 2.5) Pg 20, 21: AC chart specs changes for 167 MHz, correct tLZ min. from -0.07 to -0.70
C	CM/JM	02/02/2009	Pg 44: Correction to mechanical drawing