HD74AC194

4-bit Bidirectional Unviersal Shift Register

REJ03D0259–0200Z
(Previous ADE-205-379 (Z))
Rev.2.00
Jul.16.2004

Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four destinct modes of operation: parallel (broadside) load, shift right (in the direction Q_0 toward Q_3); shift left; inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1, high. The data are loaded into their respective flip-flops and appear at the output after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial date for this mode is entered at the shift right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shifts left serial input. Clocking of the flip-flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the clock input is high.

Features

- Asynchronous Master Reset
- Hole (Do Nothing) Mode
- Outputs Source/Sink 24 mA

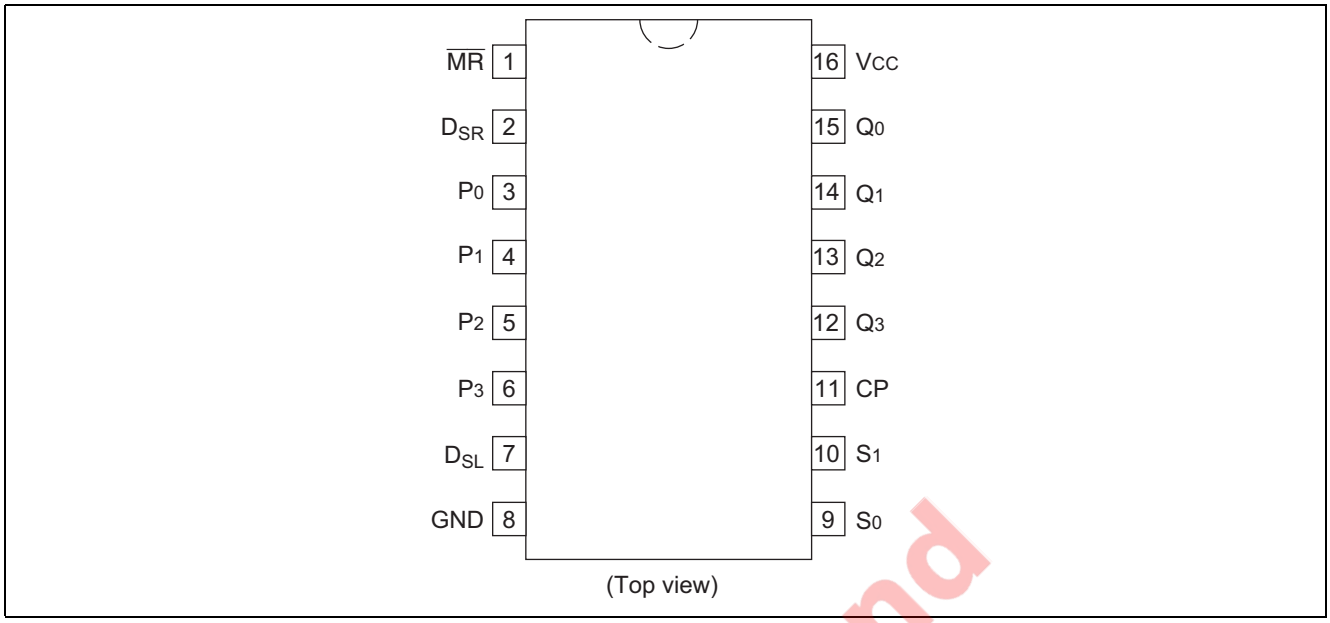
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC194FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC194RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

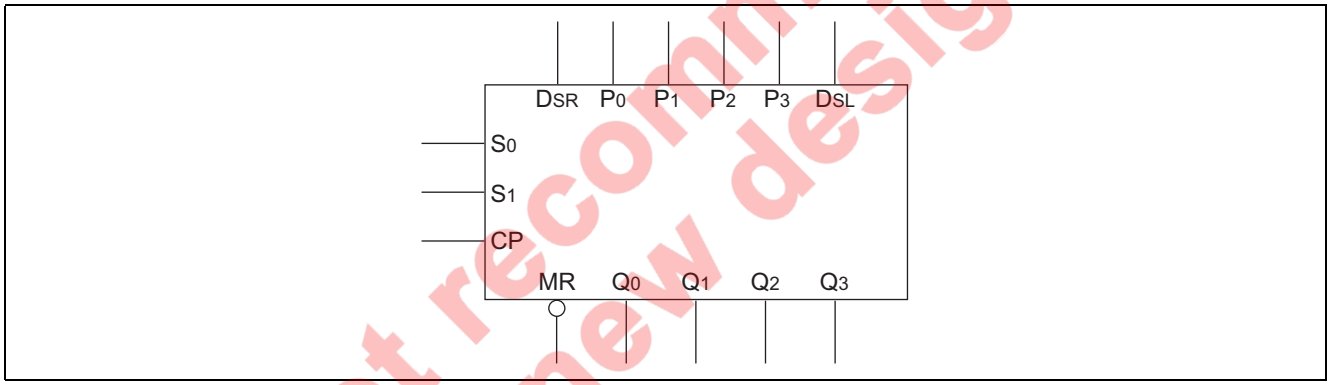
Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Not recommend for new design

Pin Arrangement



Logic Symbol



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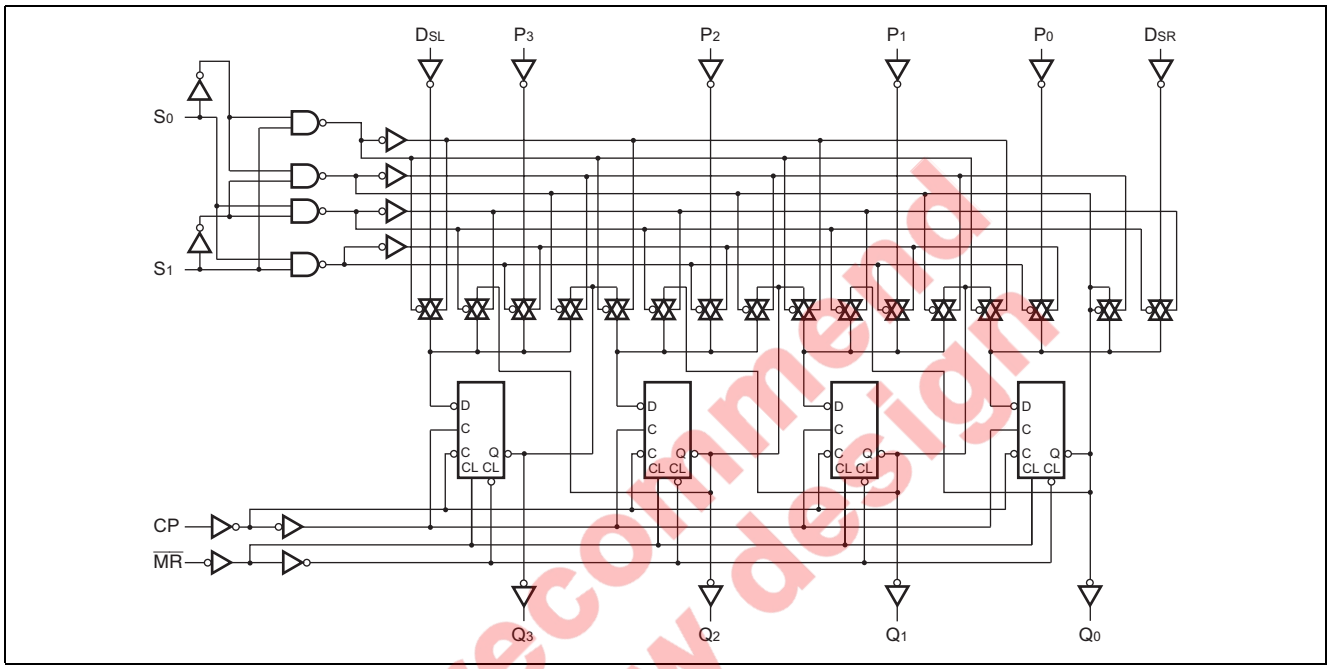
Pin Names

S_0, S_1	Mode Control Inputs
P_0 to P_3	Parallel Data Inputs
D_{SR}	Serial Data Input (Shift Right)
D_{SL}	Serial Data Input (Shift Left)
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
Q_0 to Q_3	Parallel Outputs

Logic Diagram



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Mode Select Table

Operating Mode	Inputs						Output			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	L	L	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	H	L	X	L	X	q_1	q_2	q_3	L
	H	H	L	X	H	X	q_1	q_2	q_3	H
Shift Right	H	L	H	L	X	X	L	q_0	q_1	q_2
	H	L	H	H	X	X	H	q_0	q_1	q_2
Parallel Load	H	H	H	X	X	p_n	p_0	p_1	p_2	p_3

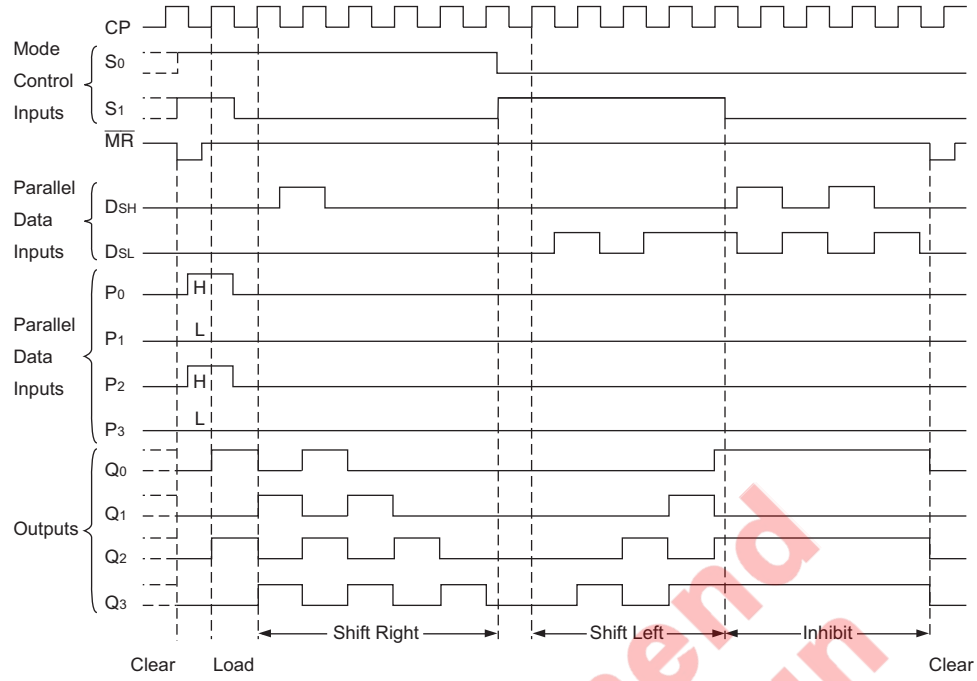
H : HIGH Voltage Level

L : LOW Voltage Level

p_n (q_n) : Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition

X : Immaterial

Timing Diagram



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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	75	—		65		MHz
		5.0	100	—		85		
Propagation delay CP to Q_n	t_{PLH}	3.3	1.0	—	13.0	1.0	15.0	ns
		5.0	1.0	—	10.0	1.0	11.5	
Propagation delay CP to Q_n	t_{PHL}	3.3	1.0	—	13.0	1.0	15.0	ns
		5.0	1.0	—	10.0	1.0	11.5	
Propagation delay $\overline{MR}$ to Q_n	t_{PHL}	3.3	1.0	—	10.5	1.0	12.5	ns
		5.0	1.0	—	8.0	1.0	9.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Not recommend for new design

AC Operating Requirements

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF		Ta = –40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW Pn or D_{SR} or D_{SL} to CP	t_{su}	3.3	—	5.5	7.0	ns
		5.0	—	4.0	5.0	
Hold time, HIGH or LOW Pn or D_{SR} or D_{SL} to CP	t_h	3.3	—	2.0	3.0	ns
		5.0	—	1.5	2.0	
Setup time, HIGH or LOW S_n to CP	t_{su}	3.3	—	6.0	7.5	ns
		5.0	—	4.5	5.5	
Hold time, HIGH or LOW S_n to CP	t_h	3.3	—	0.0	0.0	ns
		5.0	—	0.0	0.0	
Recovery time $\overline{MR}$ to CP	t_{rec}	3.3	—	0.5	0.5	ns
		5.0	—	0.5	0.5	
Pulse width	t_w	3.3	—	5.5	7.0	ns
		5.0	—	4.5	5.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	100	pF	V_{CC} = 5.0 V

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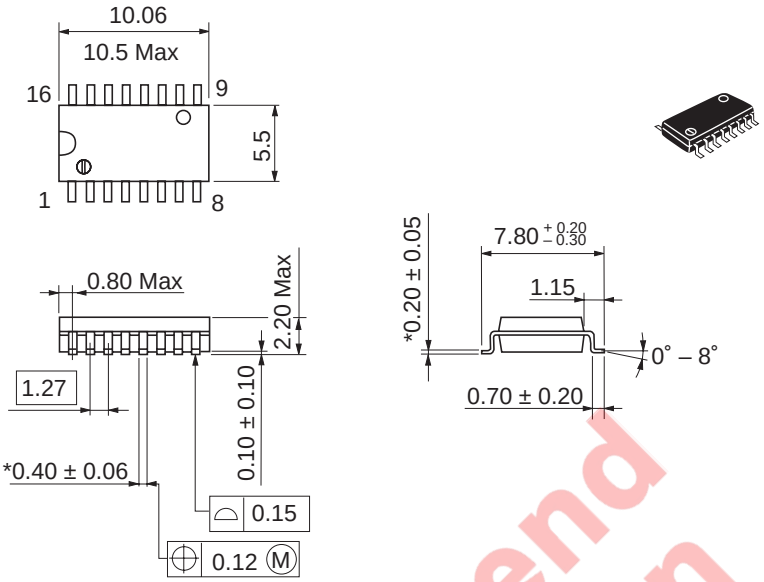
Package Dimensions

As of January, 2003

Unit: mm

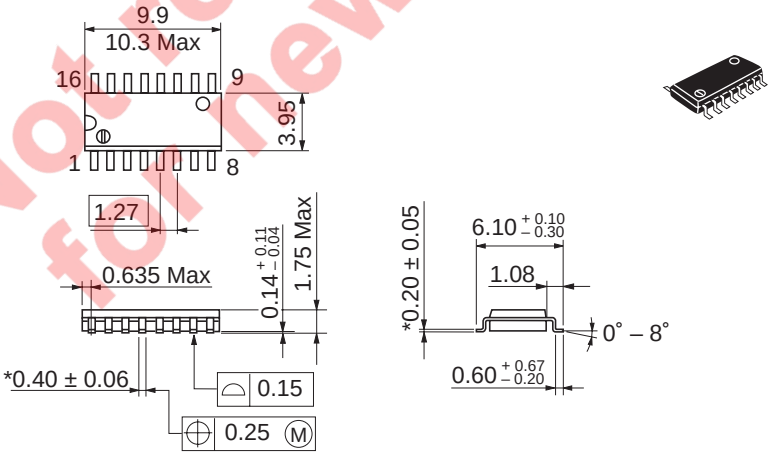


Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm



Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

*Ni/Pd/Au plating

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