

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

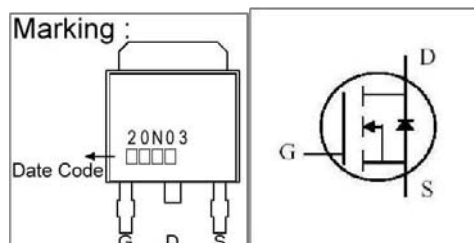
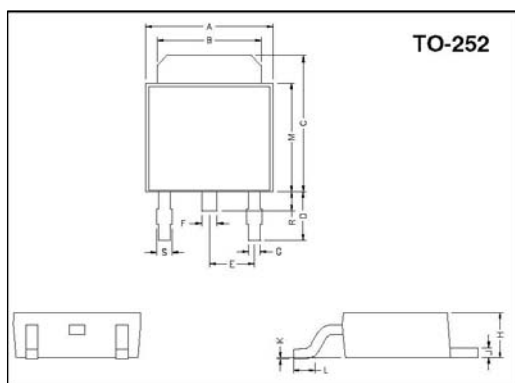
The SSD20N03 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-252 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

FEATURES

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Simple Drive Requirement
- Fast Switching

PACKAGE DIMENSIONS



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.40	6.80	G	0.50	0.70
B	5.20	5.50	H	2.20	2.40
C	6.80	7.20	J	0.45	0.55
D	2.40	3.00	K	0	0.15
E	2.30 Ref.		L	0.90	1.50
F	0.70	0.90	M	5.40	5.80
S	0.60	0.90	R	0.80	1.20

ABSOLUTE MAXIMUM RATINGS at Ta = 25°C

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_D @ T_C=25^\circ C$	20	A
Continuous Drain Current	$I_D @ T_C=100^\circ C$	13	A
Pulsed Drain Current ¹	I_{DM}	53	A
Total Power Dissipation	$P_D @ T_a=25^\circ C$	31	W
Linear Derating Factor		0.25	W/°C
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55 ~ +150	°C

THERMAL DATA

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-case Max.	$R_{\theta j-case}$	4.0	°C / W
Thermal Resistance Junction-ambient Max.	$R_{\theta j-amb}$	110	°C / W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	30	-	-	V	V _{GS} =0, I _D = 250uA
Breakdown Voltage Temperature	ΔBV _{DSS} /ΔT _j	-	0.037	-	V / °C	Reference to 25°C, I _D = 1mA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D = 250uA
Forward Transconductance	g _{fs}	-	3	-	S	V _{DS} = 10V, I _D = 10A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	1	uA	V _{DS} = 30V, V _{GS} =0
Drain-Source Leakage Current(T _j =150°C)		-	-	100	uA	V _{DS} = 24V, V _{GS} = 0
Static Drain-Source On-Resistance	R _{DS(ON)}	-	-	52	mΩ	V _{GS} = 10V, I _D = 10A
		-	-	85		V _{GS} = 4.5V, I _D = 8A
Total Gate Charge ²	Q _g	-	6.1	-	nC	I _D = 10 A V _{DS} = 24 V V _{GS} = 5 V
Gate-Source Charge	Q _{gs}	-	1.4	-		
Gate-Drain ("Miller") Change	Q _{gd}	-	4	-		
Turn-on Delay Time ²	T _{d(on)}	-	4.9	-	ns	V _{DS} =15 V I _D = 20 A V _{GS} = 10 V R _G = 3.3 Ω R _D = 0.75 Ω
Rise Time	T _r	-	29	-		
Turn-off Delay Time	T _{d(off)}	-	14.3	-		
Fall Time	T _f	-	3.6	-		
Input Capacitance	C _{iss}	-	290	-	pF	V _{GS} =0 V V _{DS} =25 V f=1.0 MHz
Output Capacitance	C _{oss}	-	160	-		
Reverse Transfer Capacitance	C _{rss}	-	45	-		

SOURCE-DRAIN DIODE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	1.3	V	I _S =20 A, V _{GS} =0 V, T _J = 25°C
Continuous Source Current (Body Diode)	I _S	-	-	20	A	V _D = V _G = 0V, V _S = 1.3 V
Pulsed Source Current (Body Diode) ¹	I _{SM}	-	-	53	A	

Notes: 1. Pulse width limited by safe operating area.
2. Pulse width ≤ 300us, duty cycle ≤ 2%.

CHARACTERISTIC CURVES

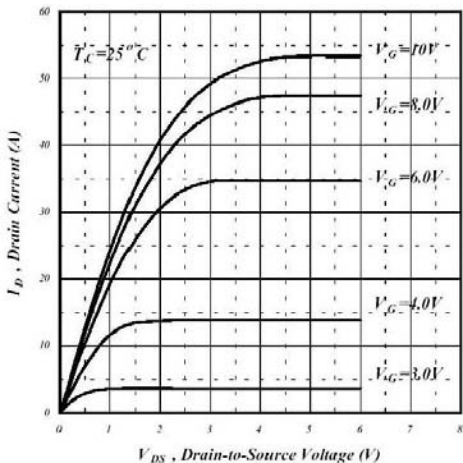


Fig 1. Typical Output Characteristics

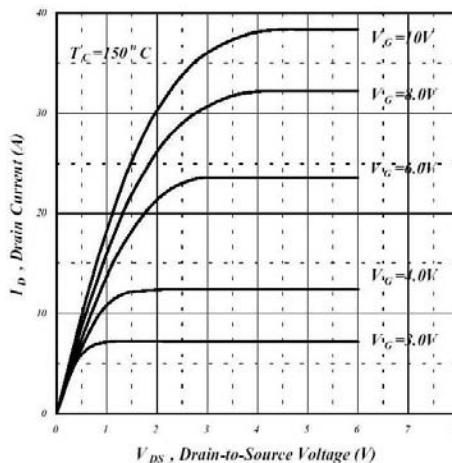


Fig 2. Typical Output Characteristics

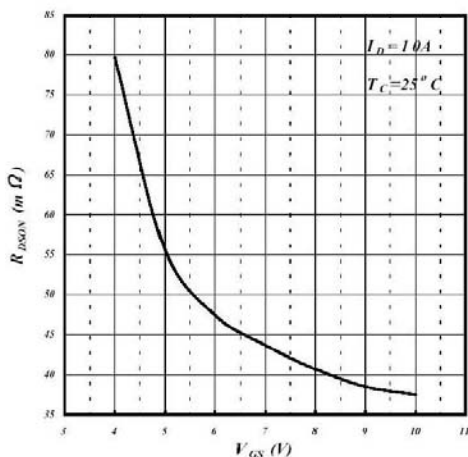


Fig 3. On-Resistance v.s. Gate Voltage

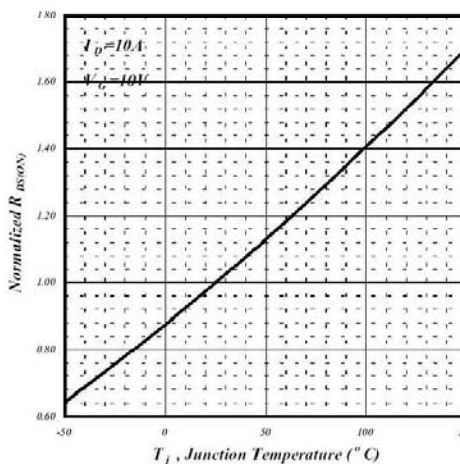


Fig 4. Normalized On-Resistance v.s. Junction Temperature

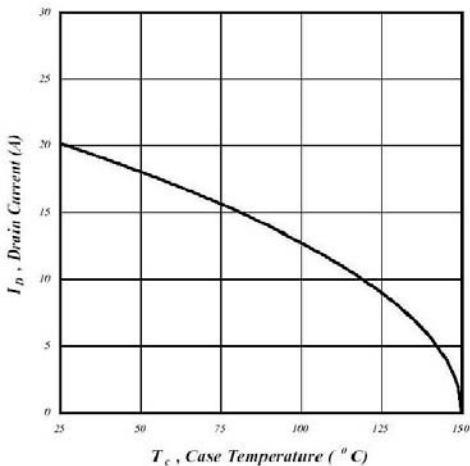


Fig 5. Maximum Drain Current v.s. Case Temperature

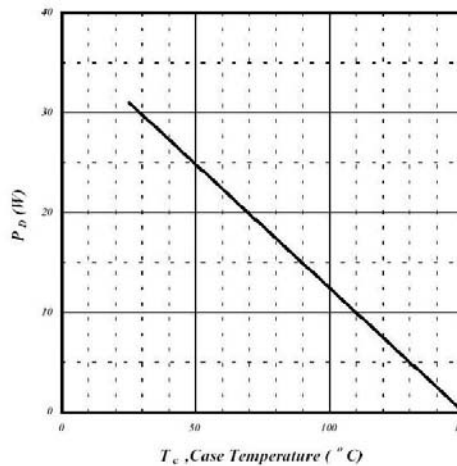


Fig 6. Type Power Dissipation

CHARACTERISTIC CURVES (cont'd)

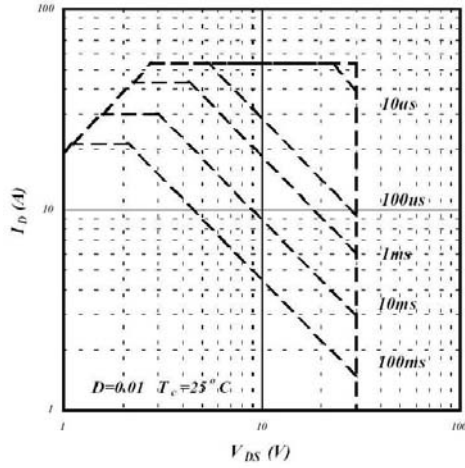


Fig 7. Maximum Safe Operating Area

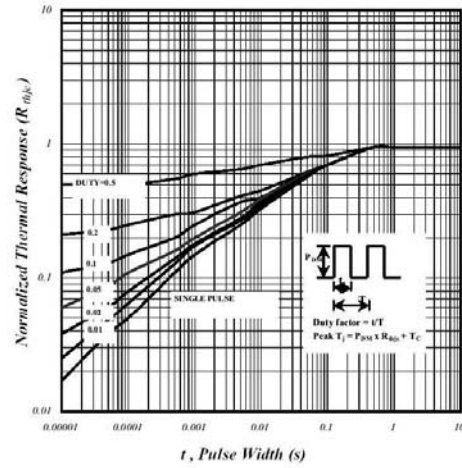


Fig 8. Effective Transient Thermal Impedance

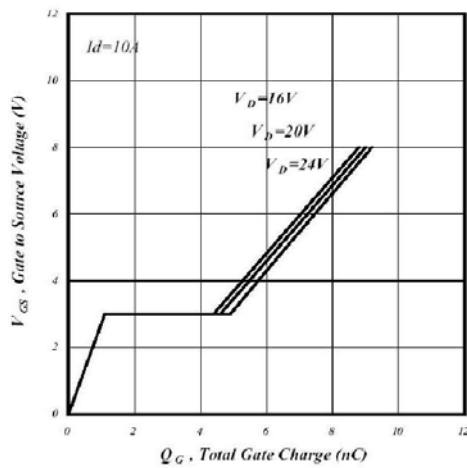


Fig 9. Gate Charge Characteristics

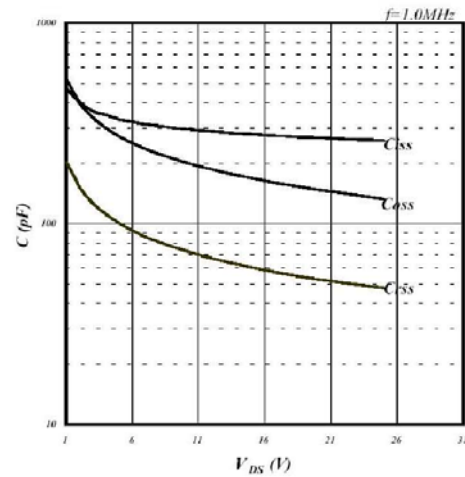


Fig 10. Typical Capacitance Characteristics

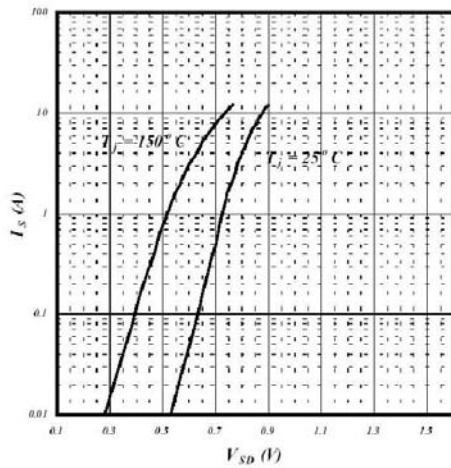


Fig 11. Forward Characteristics of Reverse Diode

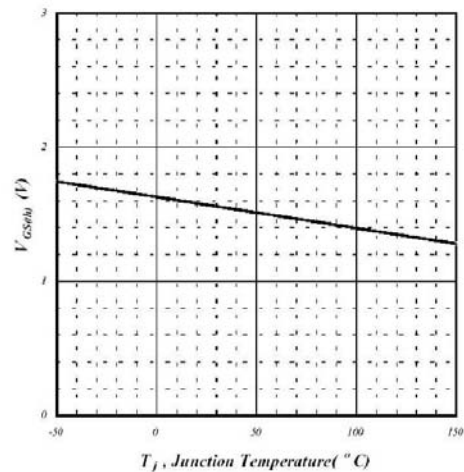


Fig 12. Gate Threshold Voltage vs. Junction Temperature

CHARACTERISTIC CURVES (cont'd)

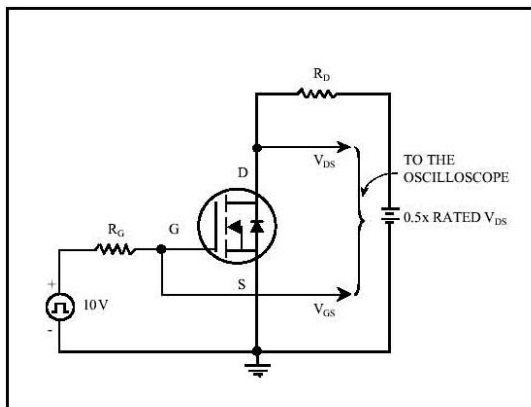


Fig 13. Switching Time Circuit

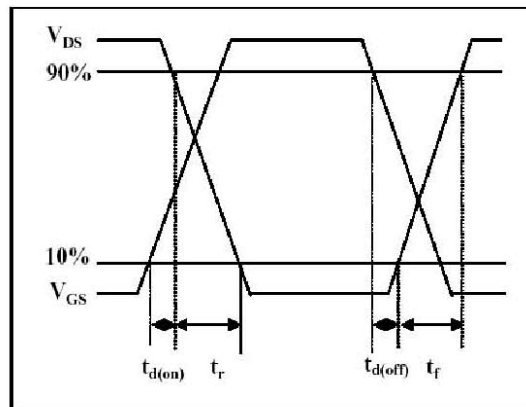


Fig 14. Switching Time Waveform

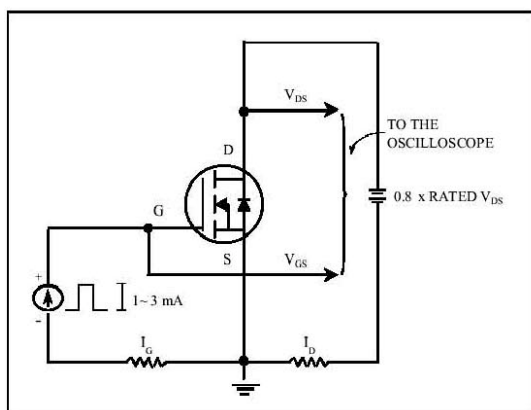


Fig 15. Gate Charge Circuit

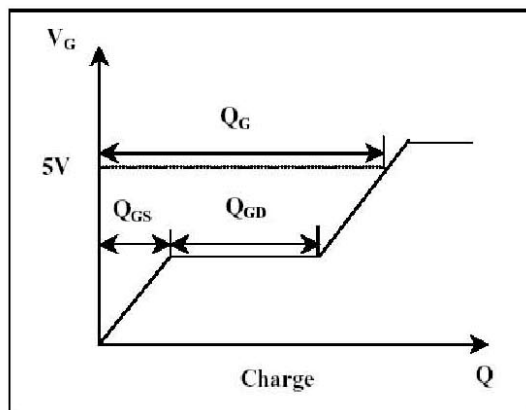


Fig 16. Gate Charge Waveform