



## 128K X 8 BIT LOW POWER CMOS SRAM

### FEATURES

- Access time :55ns
- Low power consumption:  
Operating current:10 mA (TYP.)  
Standby current: 1  $\mu$ A (TYP)
- Single 2.7V ~ 5.5V power supply
- Fully Compatible with all Competitors 5V product
- Fully Compatible with all Competitors 3.3V product
  
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- All products are ROHS Compliant
- Package : 32-pin 450 mil SOP  
32-pin 600 mil P-DIP  
32-pin 8mm x 20mm TSOP-I  
32-pin 8mm x 13.4mm sTSOP  
36-ball 6mm x 8mm TFBGA

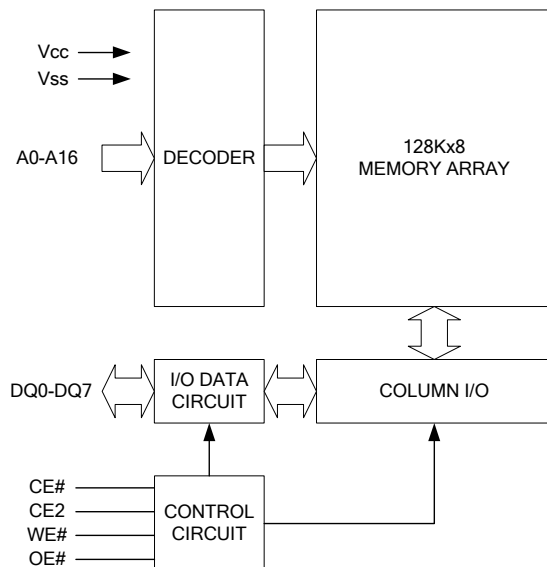
### GENERAL DESCRIPTION

The AS6C1008 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C1008 is well designed for very low power system applications, and particularly well suited for battery back-up non-volatile memory application.

The AS6C1008 operates from a single power supply of 2.7V ~ 5.5V.

### FUNCTIONAL BLOCK DIAGRAM



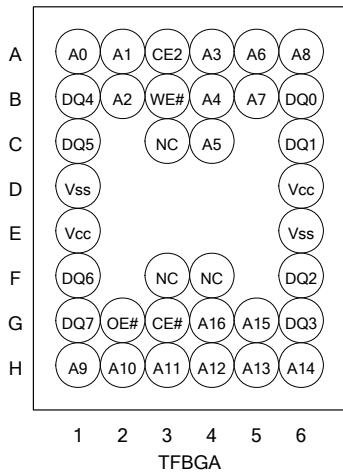
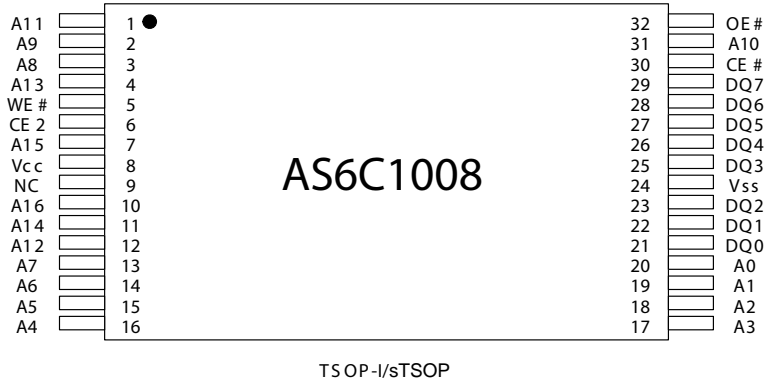
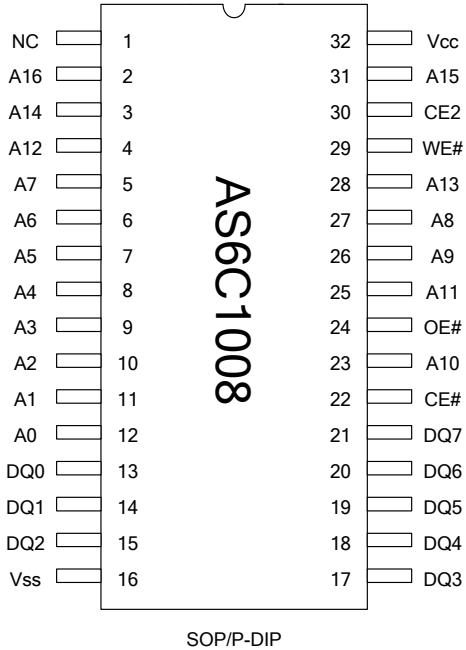
### PIN DESCRIPTION

| SYMBOL    | DESCRIPTION         |
|-----------|---------------------|
| A0 - A16  | Address Inputs      |
| DQ0 - DQ7 | Data Inputs/Outputs |
| CE#, CE2  | Chip Enable Inputs  |
| WE#       | Write Enable Input  |
| OE#       | Output Enable Input |
| Vcc       | Power Supply        |
| Vss       | Ground              |
| NC        | No Connection       |



128K X 8 BIT LOW POWER CMOS SRAM

PIN CONFIGURATION





## 128K X 8 BIT LOW POWER CMOS SRAM

**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER  | SYMBOL              | RATING             | UNIT |
|--|---------------------|--------------------|------|
| Terminal Voltage with Respect to V <sub>SS</sub> | V <sub>TERM</sub>   | -0.5 to 7.0        | V    |
| Operating Temperature                            | T <sub>A</sub>      | 0 to 70(C grade)   | °C   |
|  |                     | -40 to 85(I grade) |      |
| Storage Temperature                              | T <sub>STG</sub>    | -65 to 150         | °C   |
| Power Dissipation                                | P <sub>D</sub>      | 1                  | W    |
| DC Output Current                                | I <sub>OUT</sub>    | 50                 | mA   |
| Soldering Temperature (under 10 sec)             | T <sub>SOLDER</sub> | 260                | °C   |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

| MODE           | CE# | CE2 | OE# | WE# | I/O OPERATION    | SUPPLY CURRENT                     |
|----------------|-----|-----|-----|-----|------------------|------------------------------------|
| Standby        | H   | X   | X   | X   | High-Z           | I <sub>SB1</sub>                   |
|                | X   | L   | X   | X   | High-Z           | I <sub>SB1</sub>                   |
| Output Disable | L   | H   | H   | H   | High-Z           | I <sub>CC</sub> , I <sub>CC1</sub> |
| Read           | L   | H   | L   | H   | D <sub>OUT</sub> | I <sub>CC</sub> , I <sub>CC1</sub> |
| Write          | L   | H   | X   | L   | D <sub>IN</sub>  | I <sub>CC</sub> , I <sub>CC1</sub> |

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

| PARAMETER                              | SYMBOL                       | TEST CONDITION   | MIN.                | TYP. <sup>4</sup> | MAX.                 | UNIT |    |
|--|------------------------------|--|---------------------|-------------------|----------------------|------|----|
| Supply Voltage                         | V <sub>CC</sub>              |  | 2.7                 | 3.0               | 5.5                  | V    |    |
| Input High Voltage                     | V <sub>IH</sub> <sup>1</sup> |  | 0.7*V <sub>CC</sub> | -                 | V <sub>CC</sub> +0.3 | V    |    |
| Input Low Voltage                      | V <sub>IL</sub> <sup>2</sup> |  | -0.2                | -                 | 0.6                  | V    |    |
| Input Leakage Current                  | I <sub>LI</sub>              | V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>  | -1                  | -                 | 1                    | μA   |    |
| Output Leakage Current                 | I <sub>LO</sub>              | V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> ,<br>Output Disabled  | -1                  | -                 | 1                    | μA   |    |
| Output High Voltage                    | V <sub>OH</sub>              | I <sub>OH</sub> = -1mA   | 2.2                 | 2.7               | -                    | V    |    |
| Output Low Voltage                     | V <sub>OL</sub>              | I <sub>OL</sub> = 2mA  | -                   | -                 | 0.4                  | V    |    |
| Average Operating Power supply Current | I <sub>CC</sub>              | Cycle time = Min.<br>CE# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> ,<br>I <sub>I/O</sub> = 0mA   | -                   | 10                | 60                   | mA   |    |
|  | I <sub>CC1</sub>             | Cycle time = 1μs<br>CE# ≤ 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V,<br>I <sub>I/O</sub> = 0mA<br>other pins at 0.2V or V <sub>CC</sub> -0.2V | -                   | 1                 | 10                   | mA   |    |
| Standby Power Supply Current           | I <sub>SB1</sub>             | CE# ≥ V <sub>CC</sub> -0.2V  | C*                  | -                 | 1                    | 20   | μA |
|  |                              | or CE2 ≤ 0.2V  | I*                  | -                 | 1                    | 50   | μA |

\*C=Commercial temperature/I= Industrial temperature



## 128K X 8 BIT LOW POWER CMOS SRAM

### Notes:

1.  $V_{IH(max)} = V_{CC} + 3.0V$  for pulse width less than 10ns.
2.  $V_{IL(min)} = V_{SS} - 3.0V$  for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at  $V_{CC} = V_{CC(TYP)}$  and  $T_A = 25^\circ C$

### CAPACITANCE ( $T_A = 25^\circ C, f = 1.0MHz$ )

| PARAMETER                | SYMBOL    | MIN. | MAX | UNIT |
|--------------------------|-----------|------|-----|------|
| Input Capacitance        | $C_{IN}$  | -    | 6   | pF   |
| Input/Output Capacitance | $C_{I/O}$ | -    | 8   | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

### AC TEST CONDITIONS

|  |   |
|--|---|
| Input Pulse Levels                       | 0.2V to $V_{CC} - 0.2V$                       |
| Input Rise and Fall Times                | 3ns   |
| Input and Output Timing Reference Levels | 1.5V  |
| Output Load                              | $C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA$ |

### AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

| PARAMETER                          | SYM.        | AS6C1008-55 |      | UNIT |
|------------------------------------|-------------|-------------|------|------|
|                                    |             | MIN.        | MAX. |      |
| Read Cycle Time                    | $t_{RC}$    | 55          | -    | ns   |
| Address Access Time                | $t_{AA}$    | -           | 55   | ns   |
| Chip Enable Access Time            | $t_{ACE}$   | -           | 55   | ns   |
| Output Enable Access Time          | $t_{OE}$    | -           | 30   | ns   |
| Chip Enable to Output in Low-Z     | $t_{CLZ}^*$ | 10          | -    | ns   |
| Output Enable to Output in Low-Z   | $t_{OLZ}^*$ | 5           | -    | ns   |
| Chip Disable to Output in High-Z   | $t_{CHZ}^*$ | -           | 20   | ns   |
| Output Disable to Output in High-Z | $t_{OHZ}^*$ | -           | 20   | ns   |
| Output Hold from Address Change    | $t_{OH}$    | 10          | -    | ns   |

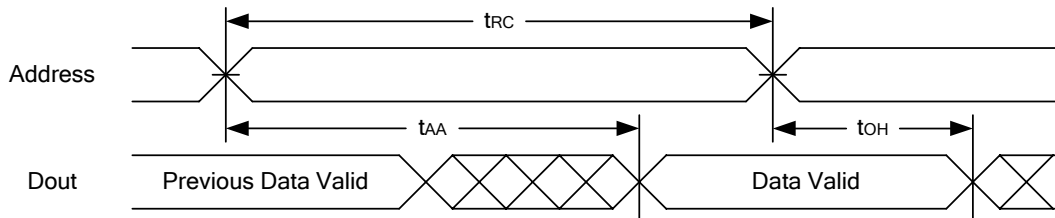
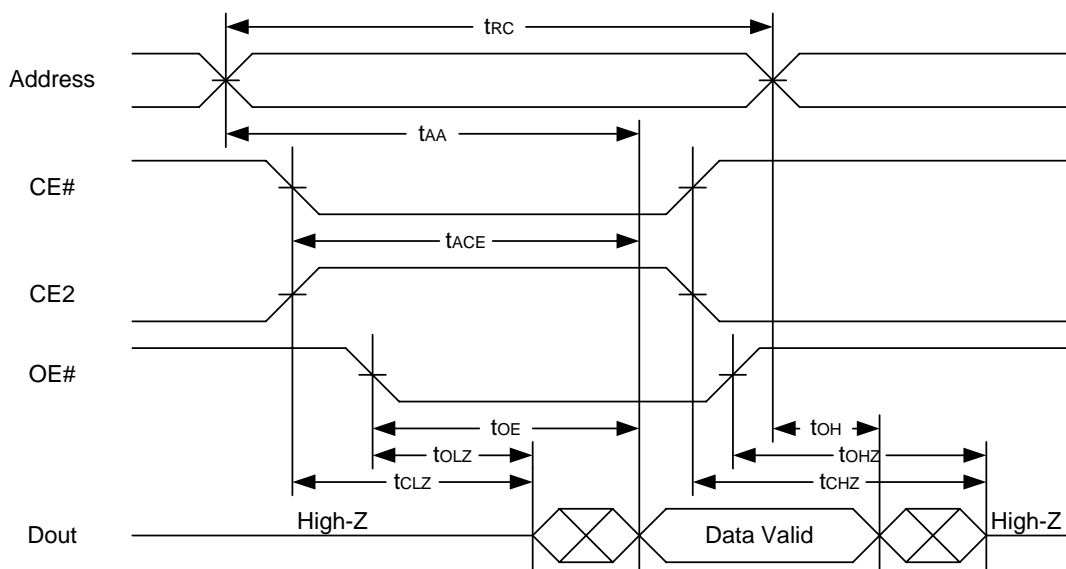
#### (2) WRITE CYCLE

| PARAMETER                        | SYM.        | AS6C1008-55 |      | UNIT |
|----------------------------------|-------------|-------------|------|------|
|                                  |             | MIN.        | MAX. |      |
| Write Cycle Time                 | $t_{WC}$    | 55          | -    | ns   |
| Address Valid to End of Write    | $t_{AW}$    | 50          | -    | ns   |
| Chip Enable to End of Write      | $t_{CW}$    | 50          | -    | ns   |
| Address Set-up Time              | $t_{AS}$    | 0           | -    | ns   |
| Write Pulse Width                | $t_{WP}$    | 45          | -    | ns   |
| Write Recovery Time              | $t_{WR}$    | 0           | -    | ns   |
| Data to Write Time Overlap       | $t_{DW}$    | 25          | -    | ns   |
| Data Hold from End of Write Time | $t_{DH}$    | 0           | -    | ns   |
| Output Active from End of Write  | $t_{OW}^*$  | 5           | -    | ns   |
| Write to Output in High-Z        | $t_{WHZ}^*$ | -           | 20   | ns   |

\*These parameters are guaranteed by device characterization, but not production tested.



## 128K X 8 BIT LOW POWER CMOS SRAM

**TIMING WAVEFORMS****READ CYCLE 1 (Address Controlled) (1,2)****READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)**

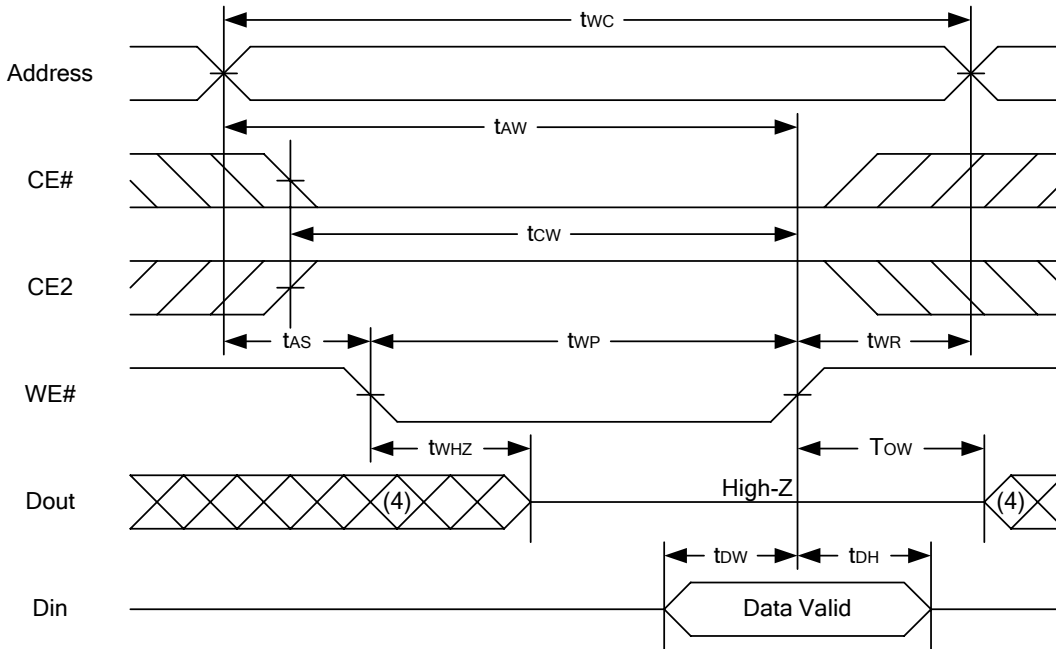
## Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

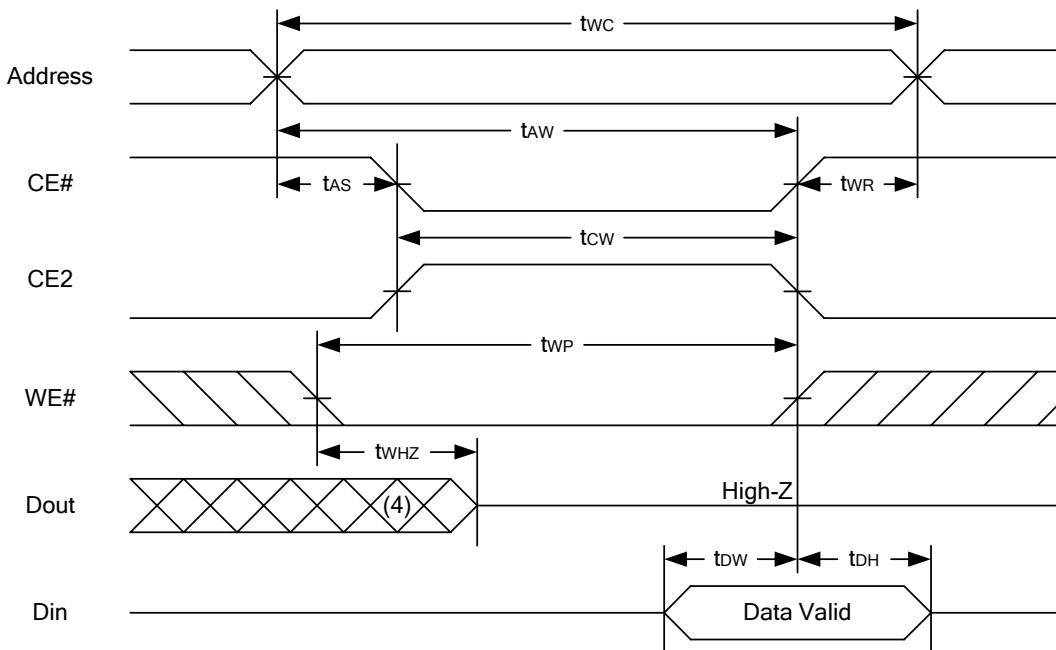


128K X 8 BIT LOW POWER CMOS SRAM

**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**



**WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)**



Notes :

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low,  $t_{wp}$  must be greater than  $t_{whz} + t_{dw}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.  $t_{ow}$  and  $t_{whz}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

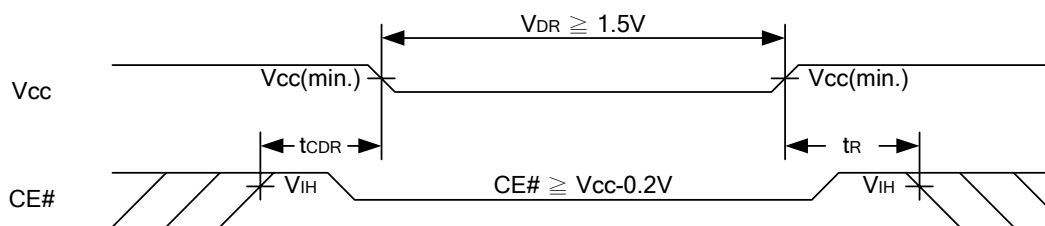
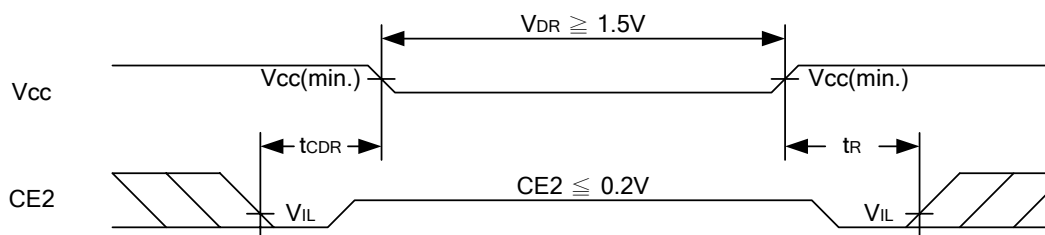


## 128K X 8 BIT LOW POWER CMOS SRAM

**DATA RETENTION CHARACTERISTICS**

| PARAMETER                           | SYMBOL           | TEST CONDITION  | MIN.             | TYP. | MAX. | UNIT |         |
|-------------------------------------|------------------|---|------------------|------|------|------|---------|
| V <sub>CC</sub> for Data Retention  | V <sub>DR</sub>  | CE# $\geq$ V <sub>CC</sub> - 0.2V<br>or CE2 $\leq$ 0.2V                           | 1.5              | -    | 5.5  | V    |         |
| Data Retention Current              | I <sub>DR</sub>  | V <sub>CC</sub> = 1.5V<br>CE# $\geq$ V <sub>CC</sub> - 0.2V<br>or CE2 $\leq$ 0.2V | C**              | -    | 0.5  | 1    | $\mu$   |
|                                     |                  |   | I**              |      | 0    | 3    | $\mu$ A |
| Chip Disable to Data Retention Time | t <sub>CDR</sub> | See Data Retention Waveforms (below)  | 0                | -    | -    | ns   |         |
| Recovery Time                       | t <sub>R</sub>   |   | t <sub>RC*</sub> | -    | -    | ns   |         |

t<sub>RC\*</sub> = Read Cycle Time C=Commercial temp/I = Industrial temp\*\*

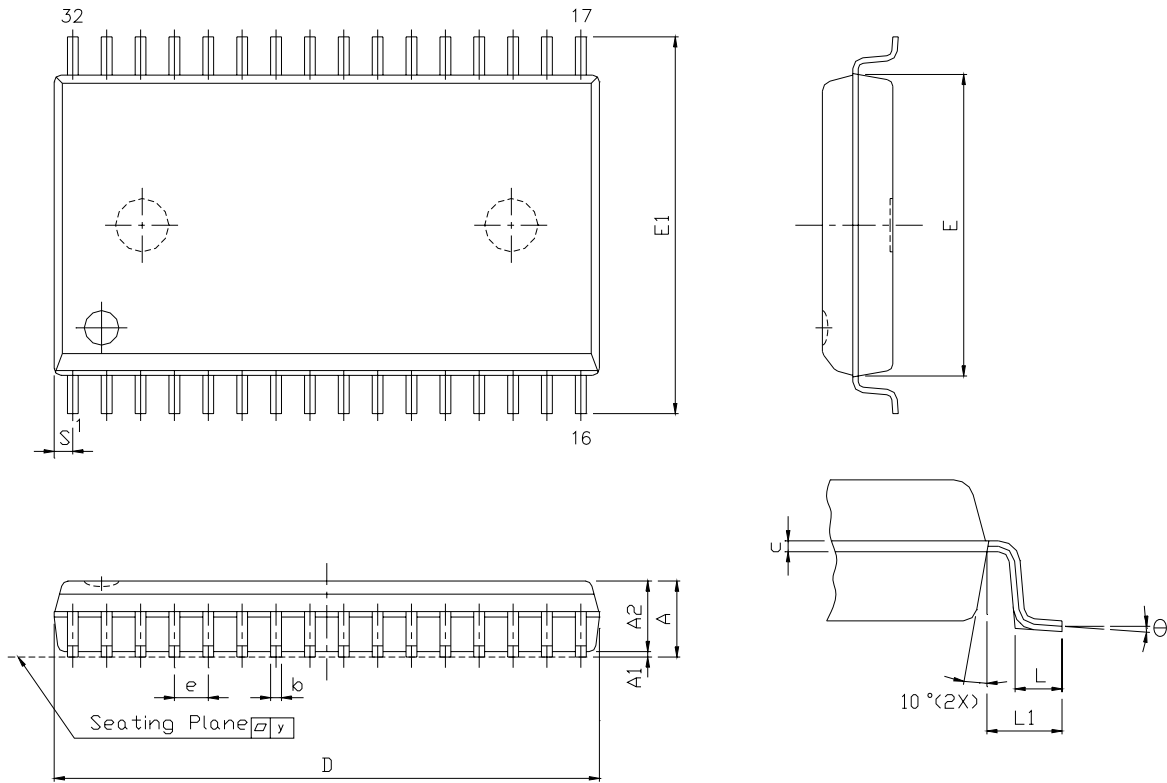
**DATA RETENTION WAVEFORM****Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)****Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)**



128K X 8 BIT LOW POWER CMOS SRAM

**PACKAGE OUTLINE DIMENSION**

**32 pin 450 mil SOP Package Outline Dimension**



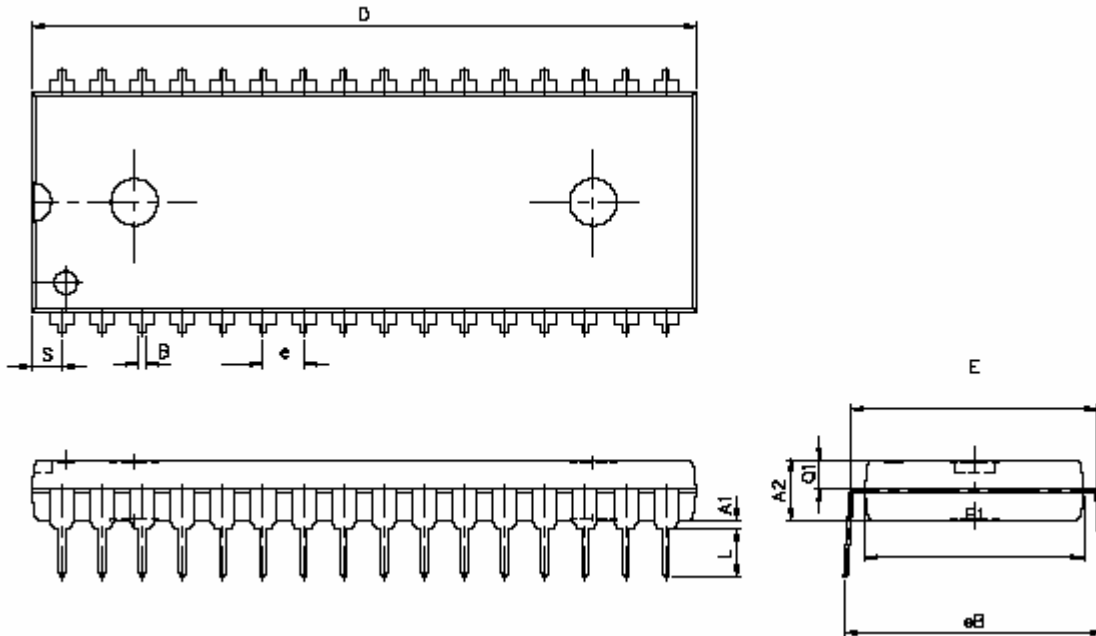
| SYM. | UNIT | INCH.(BASE)   | MM(REF)       |
|------|------|---------------|---------------|
| A    |      | 0.118 (MAX)   | 2.997 (MAX)   |
| A1   |      | 0.004(MIN)    | 0.102(MIN)    |
| A2   |      | 0.111(MAX)    | 2.82(MAX)     |
| b    |      | 0.016(TYP)    | 0.406(TYP)    |
| c    |      | 0.008(TYP)    | 0.203(TYP)    |
| D    |      | 0.817(MAX)    | 20.75(MAX)    |
| E    |      | 0.445 ±0.005  | 11.303 ±0.127 |
| E1   |      | 0.555 ±0.012  | 14.097 ±0.305 |
| e    |      | 0.050(TYP)    | 1.270(TYP)    |
| L    |      | 0.0347 ±0.008 | 0.881 ±0.203  |
| L1   |      | 0.055 ±0.008  | 1.397 ±0.203  |
| S    |      | 0.026(MAX)    | 0.660 (MAX)   |
| y    |      | 0.004(MAX)    | 0.101(MAX)    |
| Θ    |      | 0° -10°       | 0° -10°       |





128K X 8 BIT LOW POWER CMOS SRAM

32 pin 600 mil P-DIP Package Outline Dimension



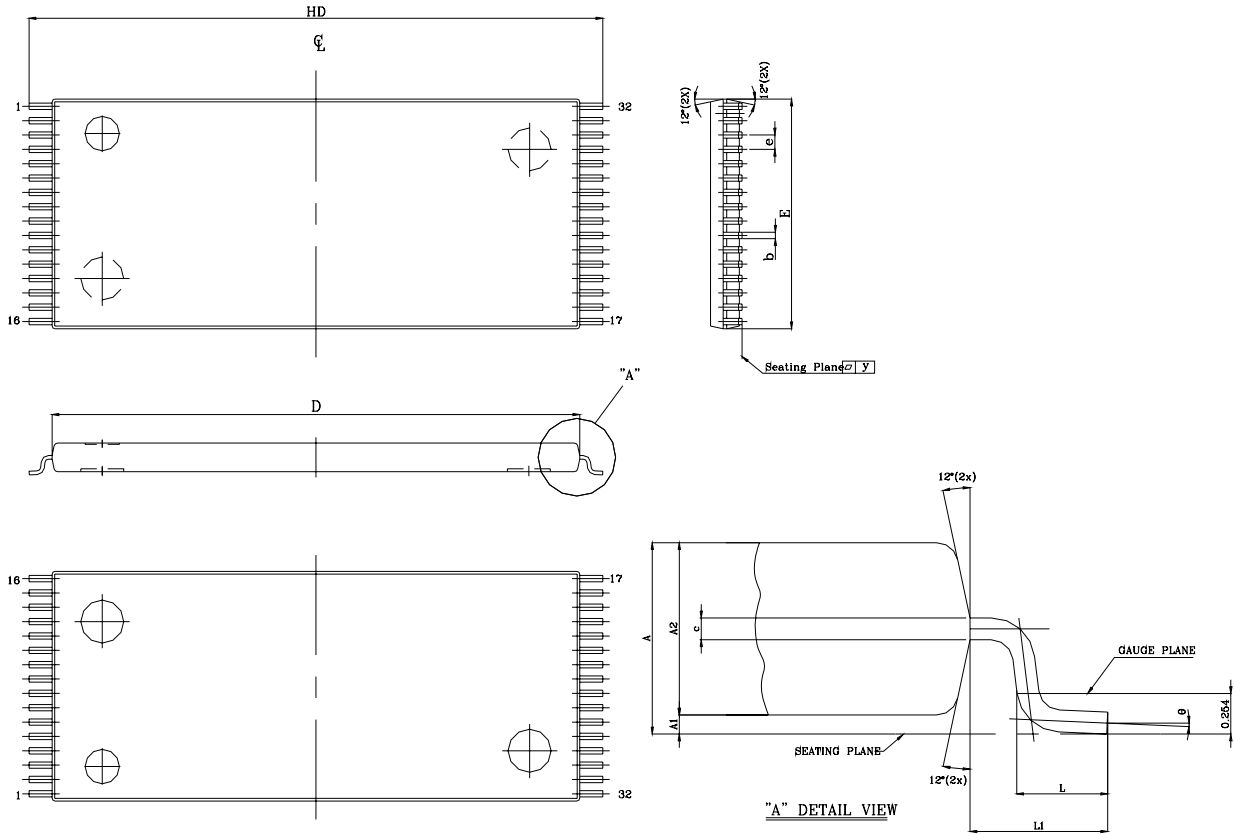
| SYM. \ UNIT | INCH(BASE)    | MM(REF)         |
|-------------|---------------|-----------------|
| A1          | 0.001 (MIN)   | 0.254 (MIN)     |
| A2          | 0.150 ± 0.005 | 3.810 ± 0.127   |
| B           | 0.018 ± 0.005 | 0.457 ± 0.127   |
| D           | 1.650 ± 0.005 | 41.910 ± 0.127  |
| E           | 0.600 ± 0.010 | 15.240 ± 0.254  |
| E1          | 0.544 ± 0.004 | 13.818 ± 0.102  |
| e           | 0.100 (TYP)   | 2.540 (TYP)     |
| eB          | 0.640 ± 0.020 | 16.256 ± 0.508. |
| L           | 0.130 ± 0.010 | 3.302 ± 0.254   |
| S           | 0.075 ± 0.010 | 1.905 ± 0.254   |
| Q1          | 0.070 ± 0.005 | 1.778 ± 0.127   |

Note : D/E1/S dimension do not include mold flash.



128K X 8 BIT LOW POWER CMOS SRAM

32 pin 8mm x 20mm TSOP-I Package Outline Dimension

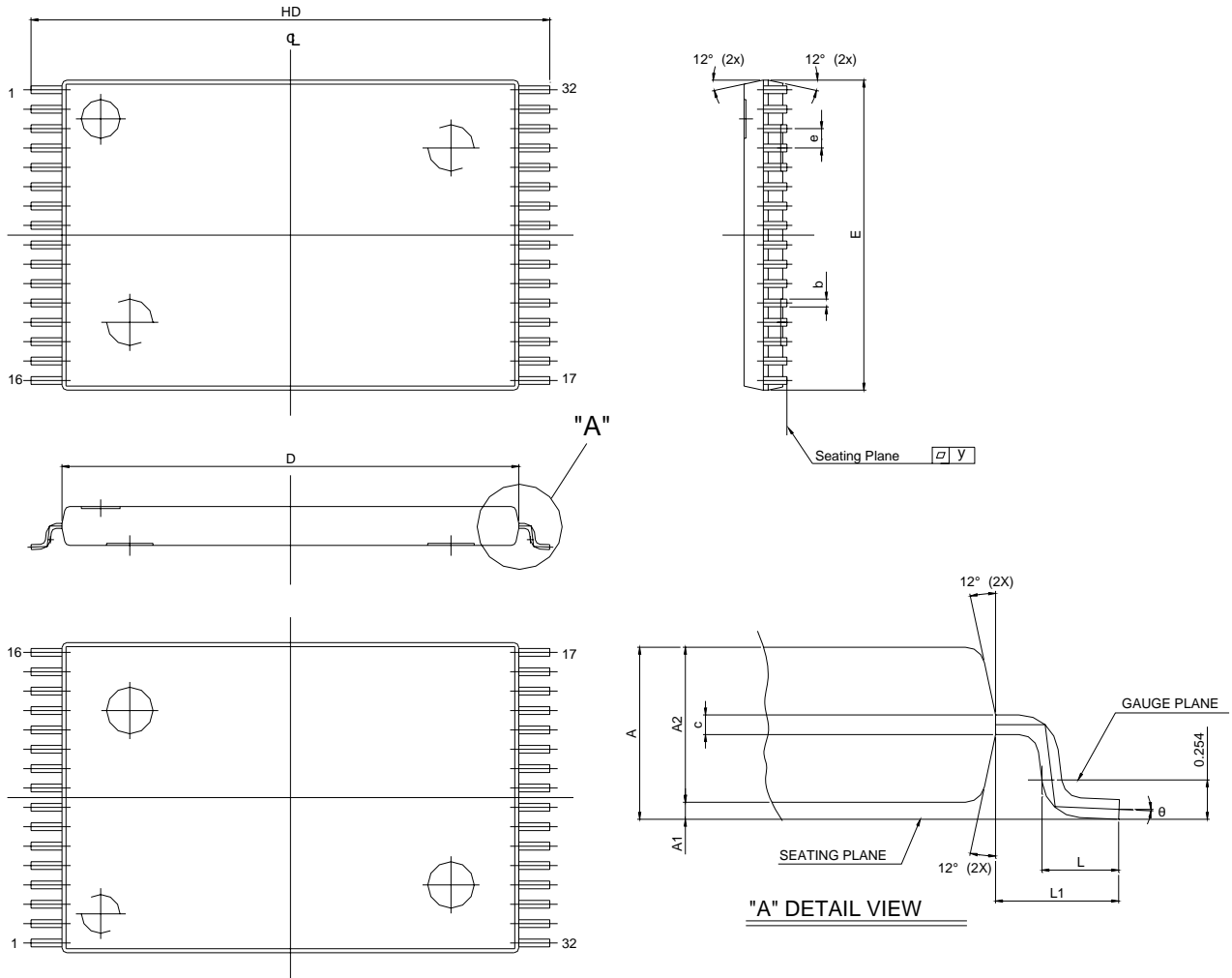


| SYM. | UNIT | INCH(BASE)               | MM(REF)               |
|------|------|--------------------------|-----------------------|
| A    |      | 0.047 (MAX)              | 1.20 (MAX)            |
| A1   |      | 0.004 ±0.002             | 0.10 ±0.05            |
| A2   |      | 0.039 ±0.002             | 1.00 ±0.05            |
| b    |      | 0.008 + 0.002<br>- 0.001 | 0.20 + 0.05<br>- 0.03 |
| c    |      | 0.005 (TYP)              | 0.127 (TYP)           |
| D    |      | 0.724 ±0.004             | 18.40 ±0.10           |
| E    |      | 0.315 ±0.004             | 8.00 ±0.10            |
| e    |      | 0.020 (TYP)              | 0.50 (TYP)            |
| HD   |      | 0.787 ±0.008             | 20.00 ±0.20           |
| L    |      | 0.0197 ±0.004            | 0.50 ±0.10            |
| L1   |      | 0.0315 ±0.004            | 0.08 ±0.10            |
| y    |      | 0.003 (MAX)              | 0.076 (MAX)           |
| θ    |      | 0° ~ 5°                  | 0° ~ 5°               |



128K X 8 BIT LOW POWER CMOS SRAM

32 pin 8mm x 13.4mm sTSSOP Package Outline Dimension

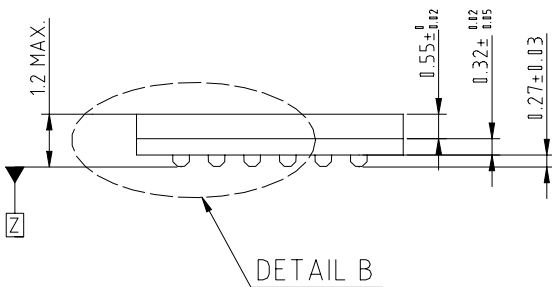
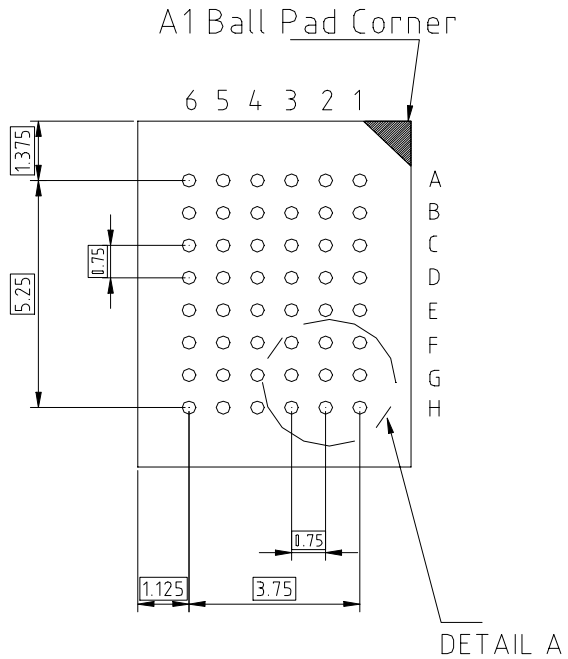
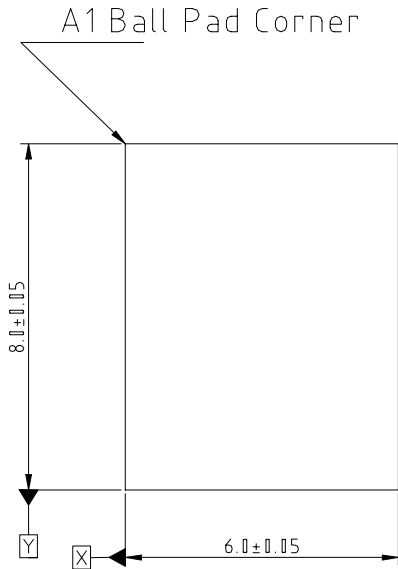


| SYM. | UNIT | INCH(BASE)    | MM(REF)      |
|------|------|---------------|--------------|
| A    |      | 0.049 (MAX)   | 1.25 (MAX)   |
| A1   |      | 0.005 ±0.002  | 0.130 ±0.05  |
| A2   |      | 0.039 ±0.002  | 1.00 ±0.05   |
| b    |      | 0.008 ±0.01   | 0.20±0.025   |
| c    |      | 0.005 (TYP)   | 0.127 (TYP)  |
| D    |      | 0.465 ±0.004  | 11.80 ±0.10  |
| E    |      | 0.315 ±0.004  | 8.00 ±0.10   |
| e    |      | 0.020 (TYP)   | 0.50 (TYP)   |
| HD   |      | 0.528±0.008   | 13.40 ±0.20. |
| L    |      | 0.0197 ±0.004 | 0.50 ±0.10   |
| L1   |      | 0.0315 ±0.004 | 0.8 ±0.10    |
| y    |      | 0.003 (MAX)   | 0.076 (MAX)  |
| Θ    |      | 0°~5°         | 0°~5°        |

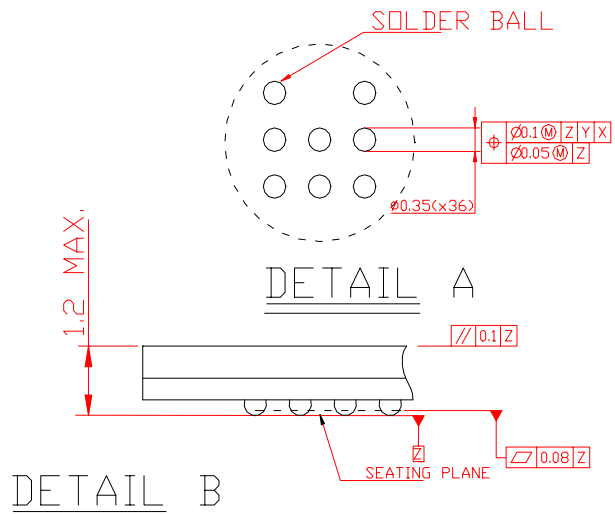


128K X 8 BIT LOW POWER CMOS SRAM

36 ball 6mm x 8mm TFBGA Package Outline Dimension



SIDE VIEW





## 128K X 8 BIT LOW POWER CMOS SRAM

**ORDERING INFORMATION**

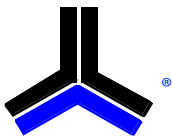
## Ordering Codes

| Alliance        | Organization | VCC range | Package                   | Operating Temp                 | Speed ns |
|-----------------|--------------|-----------|---------------------------|--------------------------------|----------|
| AS6C1008-55PCN  | 128K X 8     | 2.7-5.5V  | 32pin 600mil PDIP         | Commercial ~<br>0° C to 70° C  | 55       |
| AS6C1008-55SIN  | 128K X 8     | 2.7-5.5V  | 32pin 450mil SOP          | Industrial ~<br>-40°C to 85° C | 55       |
| AS6C1008-55TIN  | 128K X 8     | 2.7-5.5V  | 32pin TSOP-I (8 x 20 mm)  | Industrial ~<br>-40°C to 85° C | 55       |
| AS6C1008-55STIN | 128K X 8     | 2.7-5.5V  | 32pin sTSOP (8 x 13.4 mm) | Industrial ~<br>-40°C to 85° C | 55       |
| AS6C1008-55BIN  | 128K X 8     | 2.7-5.5V  | 36pin TFBGA (6mm x 8mm)   | Industrial ~<br>-40°C to 85° C | 55       |

## Part numbering system

| AS6C                           | 1008                                     | - 55           | X   | X   | N  |
|--------------------------------|--|----------------|---|---|--|
| low<br>power<br>SRAM<br>prefix | Device<br>Number<br>10 = 1M<br>08 = by 8 | Access<br>Time | Package Options:<br>P = 32 pin 600 mil P-DIP<br>S = 32 pin 450 mil SOP<br>T = 32 pin TSOP-I (8mm x 20 mm)<br>ST = 32 pin sTSOP (8 x 13.4 mm)<br>B = 36 ball 6 x 8mm TFBGA | Temperature Range:<br>C = Commercial<br>(0°C to +70° C)<br>I = Industrial<br>(-40° to +85° C) | N = Lead<br>Free ROHS<br>Compliant<br>Part |

## 128K X 8 BIT LOW POWER CMOS SRAM



Alliance Memory, Inc.  
1116 South Amphlett, #2,  
San Mateo, CA 94402  
Tel: 650-525-3737  
Fax: 650-525-0449  
[www.alliancememory.com](http://www.alliancememory.com)

Copyright © Alliance Memory  
All Rights Reserved  
Part Number: AS6C1008  
Document Version: v. 1.0

© Copyright 2003 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warranty to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as expressly agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights, mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.