Document Title

128M: 8M x 16 Mobile SDRAM

Revision History

Revision No.	Date	History
0.0	Jun 4, 2007	Initial Draft
0.1	Nov 8, 2007	- **Table9** Operating AC Parameter updated for setup & hold time - **Table9** Operating AC Parameter updated for tWR - **Table2** Bonding Pad Location and Identification table deleted - Signal names unified to /CK, /CS, /RAS, /CAS, /WE respectively (Ex.) CK#, $\overline{CK}$, CKB unified to /CK - Release date for Revision 0.0 corrected - IDD6 value in Table 6 & Table 13 modified

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128M : 8M x 16bit Mobile SDRAM

FEATURES

- 1.8V power supply.
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - CAS latency (1, 2 & 3).
  - Burst length (1, 2, 4, 8 & Full page).
  - Burst type (Sequential & Interleave).
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- EMRS cycle with address key programs.
  - PASR(Partial Array Self Refresh).
  - DS (Driver Strength)
- Internal auto TCSR (Temperature Compensated Self Refresh)
- Deep power-down(DPD) mode.
- DQM for masking.
- Auto refresh.
- 64ms refresh period (4K cycle).
- Extended Temperature Operation (-25℃ ~ 85℃).

GENERAL DESCRIPTION

This EM series is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 2,098,152 words by 16bits, fabricated with EMLSI's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

Table 1: ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
EM828164PA-60	166㎒(CL3), 111㎒(CL2)	LVCMOS	Wafer Biz.
EM828164PA-75	133㎒(CL3), 83㎒(CL2)		
EM828164PA-90	111㎒(CL3), 66㎒(CL2)		

NOTE :

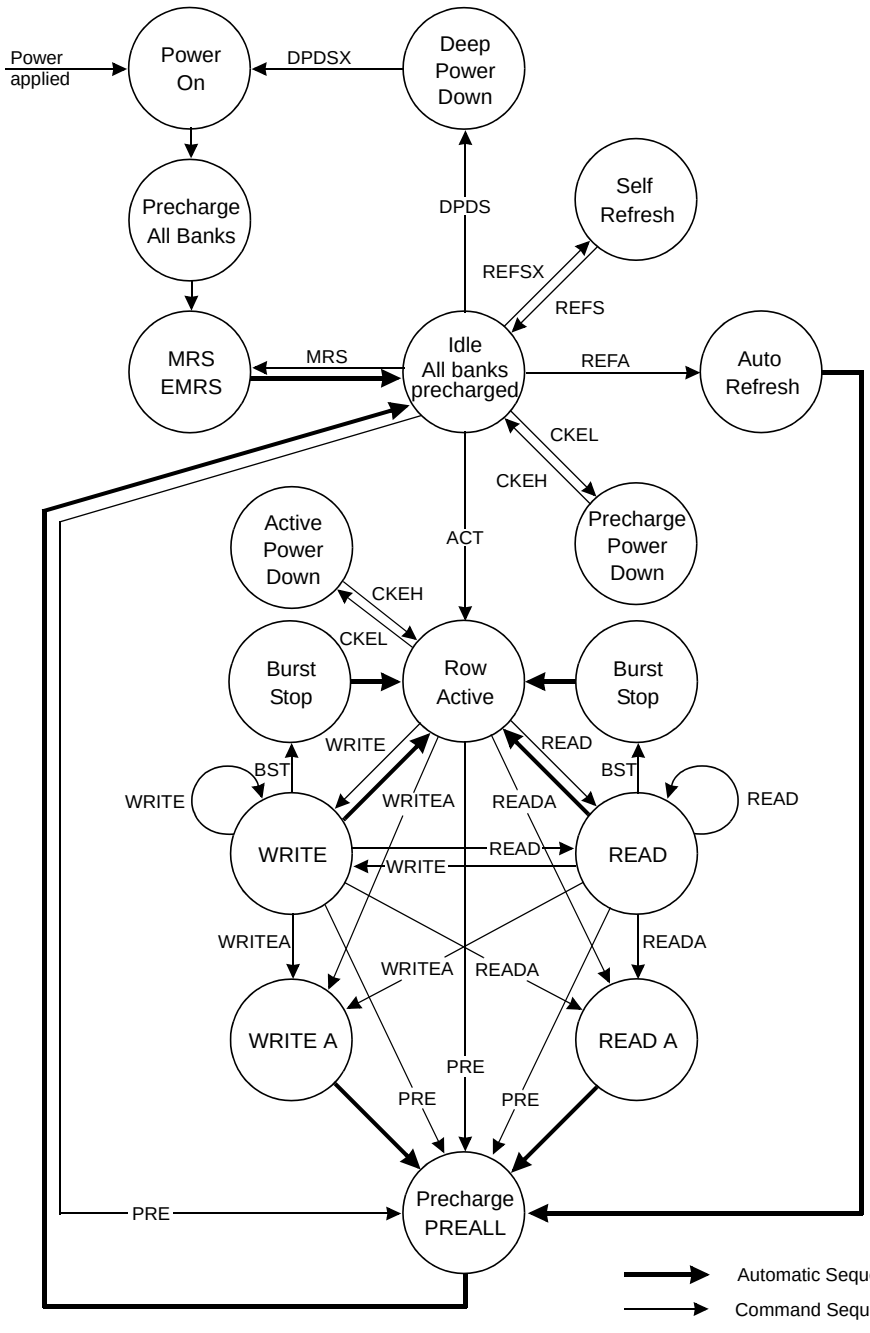
1. EMLSI are not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in emlsi electronics when considering the use of a product contained herein for any specific purpose, such as medical, aerospace, nuclear, military, vehicular or undersea repeater use.

Table 2: Pad Description

Symbol	Type	Descriptions
CLK	Input	Clock : CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable : CKE activates(HIGH) and deactivates(LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation(all banks idle), ACTIVE POWER-DOWN(row ACTIVE in any bank), DEEP POWER-DOWN (all banks idle), or CLOCK SUSPEND operation(burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
/CS	Input	Chip Select : /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	Command Inputs: /CAS, /RAS, and /WE(along with /CS) define the command being entered.
LDQM, UDQM	Input	Input/Output Mask : DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. LDQM corresponds to DQ0-DQ7, UDQM corresponds to DQ8-DQ15. LDQM and UDQM are considered same state when referenced as DQM.
BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. These balls also select between the mode register and the extended mode register.
A0 - A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command(row address A0-A11) and READ/WRITE command(column-address A0-A8; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged(A10 HIGH) or bank selected by BA0, BA1(LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0-DQ15	I/O	Data Bus: Input / Output
VDD	Supply	Power Supply
VSS	Supply	Ground
VDDQ	Supply	I/O Power Supply
VSSQ	Supply	I/O Ground

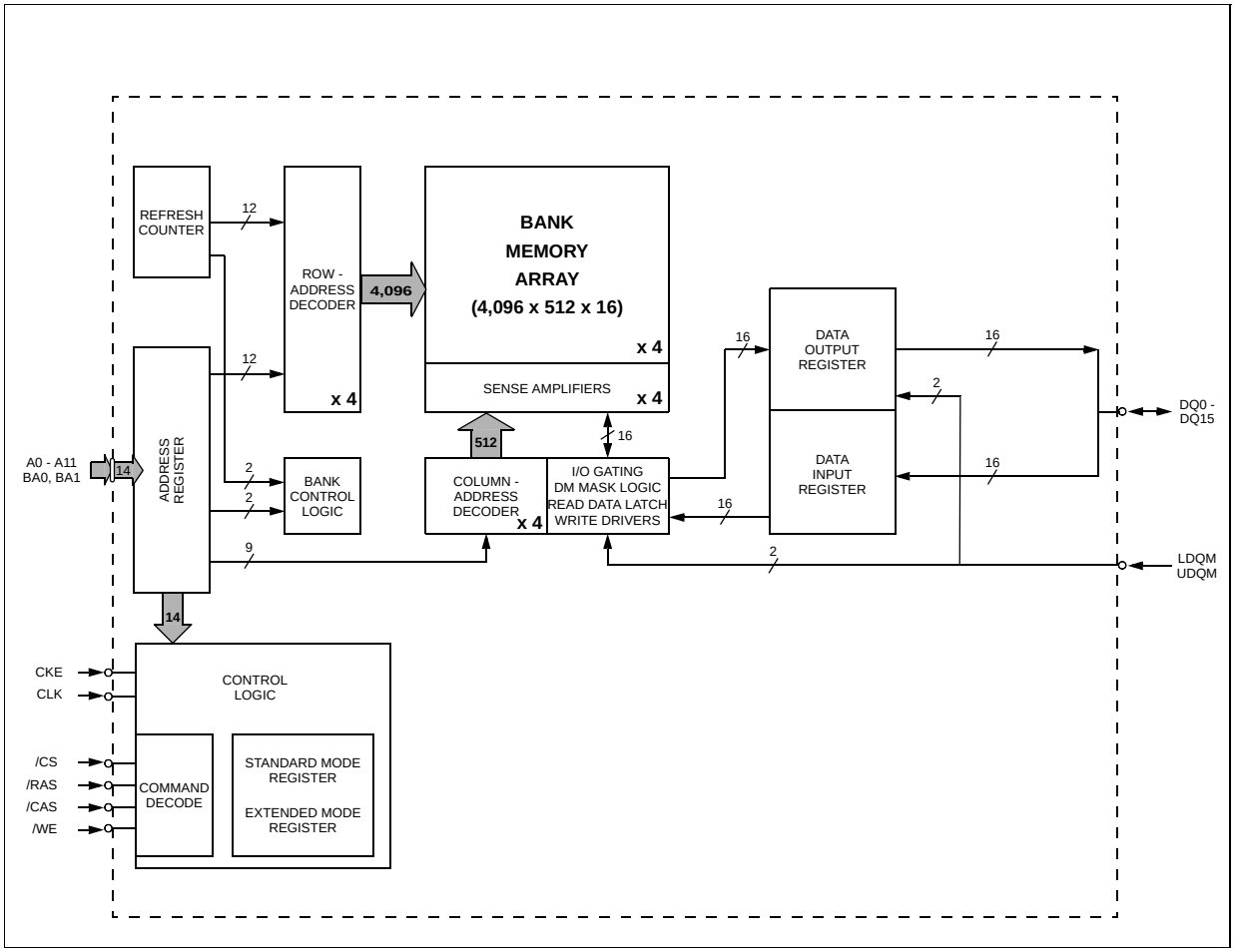
Device Operation

Simplified State Diagram



ACT = Active
BST = Burst Terminate
CKEL = Enter Power-Down
CKEH =Exit Power-Down
DPDS = Enter Deep Power-Down
DPDSX = Exit Deep Power-Down
EMRS = Ext. Mode Reg. Set
MRS = Mode Register Set
PRE = Precharge
PREALL = Precharge All Banks
REFA = Auto Refresh
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
READ = Read w/o Auto Precharge
READA = Read with Auto Precharge
WRITE = Write w/o Auto Precharge
WRITEA = Write with Auto Precharge

FUNCTIONAL BLOCK DIAGRAM



Electrical Specifications

Table 3: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 ~ 2.5	V
Voltage on V_{DD} and V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-0.5 ~ 2.5	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

NOTE :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Table 4: DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25°C~ 85°C for Extended)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	1.7	1.8	1.95	V	1
	V_{DDQ}	1.7	1.8	1.95	V	1
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	1.8	V_{DDQ} + 0.3	V	2
Input logic low voltage	V_{IL}	-0.3	0	0.3	V	3
Output logic high voltage	V_{OH}	0.9 x V_{DDQ}	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL}	-	-	0.1 x V_{DDQ}	V	I_{OL} = 0.1mA
Input leakage current	I_{LI}	-2	-	2	μA	4

NOTE :
1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VIH (max) = 2.2V AC. The overshoot voltage duration is ≤ 3ns.
3. VIL (min) = -0.1V AC. The undershoot voltage duration is ≤ 3ns.
4. Any input 0V ≤ VIN ≤ VDDQ
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
5. Dout is disabled, 0V ≤ VOUT ≤ VDDQ.

Table 5: CAPACITANCE (V_{DD} = 1.8V, T_A = 23℃, f=1㎒, Vref = 0.9V ± 50mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	1.5	3.5	pF	
/RAS, /CAS, /WE, /CS, CKE, DQM	C_{IN}	1.5	3.0	pF	
Address	C_{AD0}	1.5	3.0	pF	
DQ_0 ~ DQ_{15}	C_{OUT}	2.0	4.5	pF	

Table 6: DC CHARACTERISRICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25°C~ 85°C for Extended)

Parameter	Symbol	Test Condition	Version			Unit
			-60	-75	-90	
Operating Current (One Bank Active)	I_{DD1}	Burst length = 1 tRC ≥ tRC(min) Io = 0mA	50	40	35	mA
Precharge Standby Current in power-down mode	I_{DD2P}	CKE ≤ VIL(max), tcc =10ns	0.3			mA
	I_{DD2PS}	CKE & CLK ≤ VIL(max), tcc = ∞	0.3			
Precharge Standby Current in non power-down mode	I_{DD2N}	CKE ≥ VIH(min), /CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	10			mA
	I_{DD2NS}	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	1			
Active Standby Current in power-down mode	I_{DD3P}	CKE ≤ VIL(max), tcc = 10ns	5			mA
	I_{DD3PS}	CKE & CLK ≤ VIL(max), tcc = ∞	1			
Active Standby Current in non power-down mode (One Bank Active)	I_{DD3N}	CKE ≥ VIH(min), /CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	20			mA
	I_{DD3NS}	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	10			mA
Operationg Current (Burst Mode)	I_{DD4}	Io = 0mA Page burst 4banks activated tCCD = 2clks	80	80	45	mA mA
Refresh Current	I_{DD5}	tRFC ≥ tRFC(min)	90	90	85	mA
Self Refresh Current	I_{DD6}	CKE ≤ 0.2v	**TCSR Range**	**45*[1]**	**85**	°C
			Full Array	120	200	µA
			1/2 of Full Array	120	160	
			1/4 of Full Array	100	140	
Deep Power Down Current	I_{DD8}	CKE ≤ 0.2v	10			µA

NOTE :

1. It has ± 5℃ tolerance.
2. Refresh period is 64ms.
3. Internal TCSR can be supported.
   In extended Temp : 45°C/Max 85°C
4. DPD (Deep Power Down) function is an optional feature and it will be enabled upon request.
   Please contact EMLSI for more information.
5. Unless otherwise noted, input swing level is CMOS (VIH/VIL=VDDQ/VSSQ)

Table 7: AC OPERATING TEST CONDITIONS

(V_{DD} = 1.7V ~ 1.95V, T_A = -25°C~ 85°C for Extended)

Parameter	Value	Unit	Note
AC input levels(Vih/Vil)	0.8 × V_{DDQ} / 0.2 × V_{DDQ}	V	
Input timing measurement reference level	0.5 × V_{DDQ}	V	
Input rise and fall time	1.0	V/ns	
Output timing measurement reference level	0.5 × V_{DDQ}	V	
Output load condition	See Figure 2		

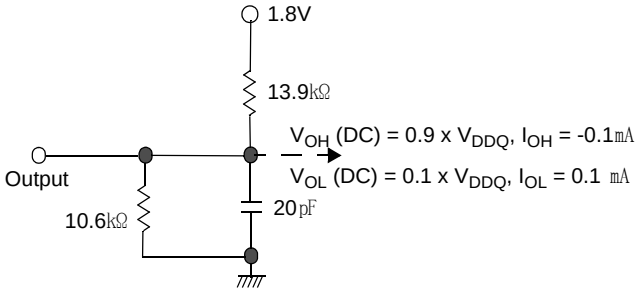


Figure 1. DC Output Load Circuit

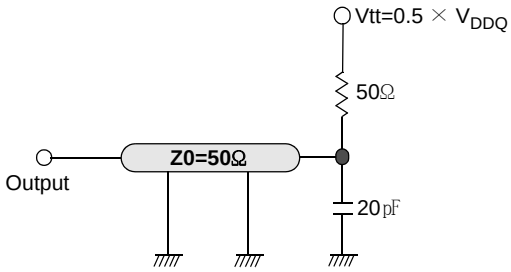


Figure 2. AC Output Load Circuit

Table 8: OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Sym-bol	-60		-75		-90		Unit	Note
			Min	Max	Min	Max	Min	Max		
DQ output access time from CLK		t_{AC}		5.4		5.4		7.0	ns	1,2
Clock high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	3
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	3
Clock half period		t_{HP}	min (t_{CL},t_{CH})		min (t_{CL},t_{CH})		min (t_{CL},t_{CH})		ns	
Clock cycle time	CL = 3	t_{CK}	6		7.5		9		ns	1
	CL = 2		9		12		15		ns	
DQ input setup time		t_{DS}	2.5		2.5		2.5		ns	
DQ input hold time		t_{DH}	1.0		1.0		1.0		ns	
Address input setup time		t_{AS}	2.5		2.5		2.5		ns	3
Address input hold time		t_{AH}	1.0		1.0		1.0		ns	3
DQ low-impedance time from CLK		t_{LZ}	1.0		1.0		1.0		ns	2
DQ high-impedance time from CLK		t_{HZ}		6.0		6.0		7.0	ns	
MODE REGISTER SET command period		t_{MRD}	2		2		2		t_{CK}	
CKE hold time		t_{CKH}	1		1		1		ns	
CKE setup time		t_{CKS}	1.5		1.5		2.5		ns	
/CS, /RAS, /CAS, /WE, DQM hold time		t_{CMH}	1.0		1.0		1.0		ns	
/CS, /RAS, /CAS, /WE, DQM setup time		t_{CMS}	2.5		2.5		2.5		ns	
Data-out hold time		t_{OH}	2.5		2.5		2.5		ns	2
ACTIVE to PRECHARGE command period		t_{RAS}	50	100,000	50	100,000	50	100,000	ns	4
ACTIVE to ACTIVE command period		t_{RC}	72.5		72.5		74		ns	4
AUTO REFRESH to ACTIVE / AUTO REFRESH command period		t_{RFC}	80		80		90		ns	7
ACTIVE to READ or WRITE delay		t_{RCD}	22.5		22.5		24		ns	4
PRECHARGE command period		t_{RP}	18		22.5		24		ns	4
ACTIVE bank A to ACTIVE bank b delay		t_{RRD}	2		2		2		t_{CK}	4
READ/WRITE command to READ/WRITE command		t_{CCD}	1		1		1		t_{CK}	
WRITE recovery time		t_{WR}	15		15		15		ns	5
Auto precharge write recovery + precharge time		t_{DAL}	t_{WR}+t_{RP}		t_{WR}+t_{RP}		t_{WR}+t_{RP}			
Self refresh exit to next valid command delay		t_{XSR}	90		112.5		120		ns	
Exit power down to next valid command delay		t_{XP}	t_{CK}+t_{CKS}		t_{CK}+t_{CKS}		t_{CK}+t_{CKS}			

NOTE :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered.
   i.e.,[(tr + tf)/2-1]ns should be added to the parameter.
4. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
5. Minimum delay is required to completed write.
6. Maximum burst refresh cycle : 8
7. All parts allow every cycle column address change.

Functional Description

In general, the 128Mb SDRAMs (2 Meg x 16 x 4 banks) are quad-bank DRAMs that operate at 1.8V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A11 select the row). The address bits (A0-A8) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power should be applied to VDD and VDDQ simultaneously. Once the power is applied to VDD and VDDQ, and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100μs delay prior to issuing any command other than a DESELECT or NOP. Starting at some point during this 100μs period and continuing at least through the end of this period, DESELECT or NOP commands should be applied.

Once the 100μs delay has been satisfied with at least one DESELECT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO refresh cycles must be performed. After the AUTO refresh cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

In order to achieve low power consumption, there are two mode registers in the mobile component, mode register and extended mode register. The mode register defines the specific mode of operation of the SDRAM, including burst length, burst type, CAS latency, operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.
Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, A7 and A8 specify the operating mode, A9 specifies the write burst mode. A10 and A11 should be set to zero. BA0 and BA1 should be set to zero to prevent extended mode register.
The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to one, two, or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n + m. The DQs will start driving as a result of the clock edge one cycle earlier (n + m - 1), and provided that the relevant access times are met, the data will be valid by clock edge n + m.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting A7 and A8 to zero; the other combinations of values for A7 and A8 are reserved for future use and/or test modes. The programmed burst length applies to both read and write bursts.
Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When A9 = 0, the burst length programmed via A0-A2 applies to both READ and WRITE bursts; when A9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

Extended Mode Register

The extended mode register controls functions specific to low power operation. These additional functions include drive strength, temperature compensated self refresh, and partial array self refresh.

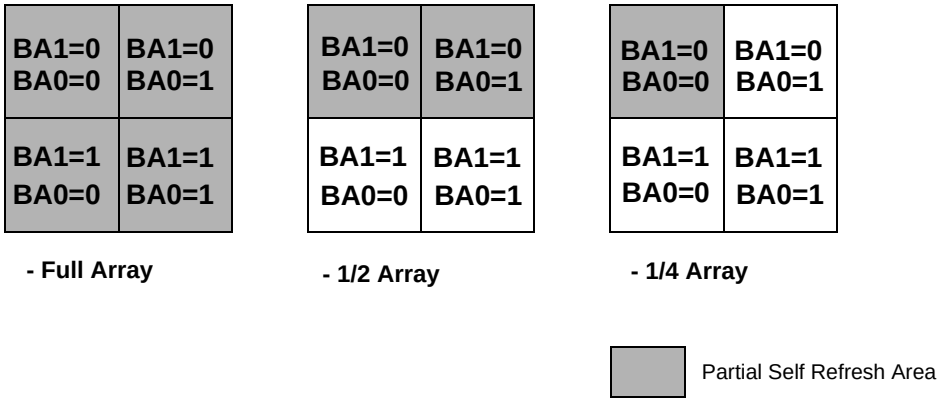
This device has default values for the extended mode register (if not programmed, the device will operate with the default values . PASR = Full Array, DS = Full Drive).

Temperature Compensated Self Refresh

On this version of the Mobile SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Programming of the temperature compensated self refresh (TCSR) bits will have no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial Array Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. Low Power SDRAM supports 3 kinds of PASR in self refresh mode : Full Array, 1/2 of Full Array and 1/4 of Full Array



Output Driver Strength

Because the Mobile SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 and A6 of the extended mode register can be used to select the driver strength of the DQ outputs.

Table 9: Mode Register Field Table to Program modes

Register Programmed with Normal MRS

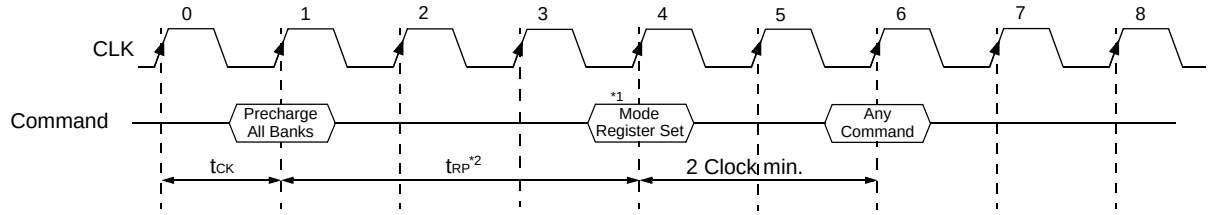
Address	BA0 ~ BA1	A11 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU*1	W.B.L	Operating Mode		CAS Latency			BT	Burst Length		

NOTE :
1. RFU(Reserved for future use) should stay “0” during MRS cycle.

Table 10: Normal Mode

Operating Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select		0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	Setting for Normal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page	Reserved

Mode Register Set



NOTE :
1. MRS can be issued only at all bank precharge state.
2. Minimum tRP is required to issue MRS command.

Table 11: Register Programmed with Extended MRS

Address	BA1	BA0	A11 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Mode Select		RFU*1				DS		RFU*1		PASR		

NOTE :
1. RFU(Reserved for future use) should stay "0" during MRS and EMRS cycle.

Table 12: EMRS for PASR(Partial Array Self Refresh) & DS(Driver Strength)

Mode Select			Driver Strength			PASR			
BA1	BA0	MODE	A6	A5	Driver Strength	A2	A1	A0	Size of Refreshed Array
0	0	Normal MRS	0	0	Full	0	0	0	Full Array
0	1	Reserved	0	1	1/2	0	0	1	1/2 of Full Array
1	0	EMRS for SDRAM	1	0	1/4	0	1	0	1/4 of Full Array
1	1	Reserved	1	1	1/8	0	1	1	Reserved
Reserved Address						1	0	0	Reserved
A11~A10/AP	A9	A8	A7	A4	A3	1	0	1	Reserved
0	0	0	0	0	0	1	1	0	Reserved
						1	1	1	Reserved

Table 13: Internal Temperature Compensated Self Refresh (TCSR)

Temperature Range	Self Refresh Current (Icc 6)			Unit
	Full Array	1/2 of Full Array	1/4 of Full Array	
Max 85℃	200	160	140	μA
Max 45℃	120	120	100	

NOTE :

1. In order to save power consumption, Low power SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the two temperature range : Max 85℃, Max 45℃
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCRS is ignored.
3. It has +/- 5 ℃ tolerance.

BURST SEQUENCE

Table 14: BURST LENGTH = 2

Initial Address	Sequential		Interleave	
A0				
0	0	1	0	1
1	1	0	1	0

Table 15: BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Table 16: BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Commands

DESELECT

The DESELECT function(/CS HIGH) prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (/CS is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode register is loaded via inputs A0-A11, BA0, BA1. The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

The values of the mode register and extended mode register will be retained even when exiting deep power-down.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs 2 clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the CASe where only 1 bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time.

BURST TERMINATE

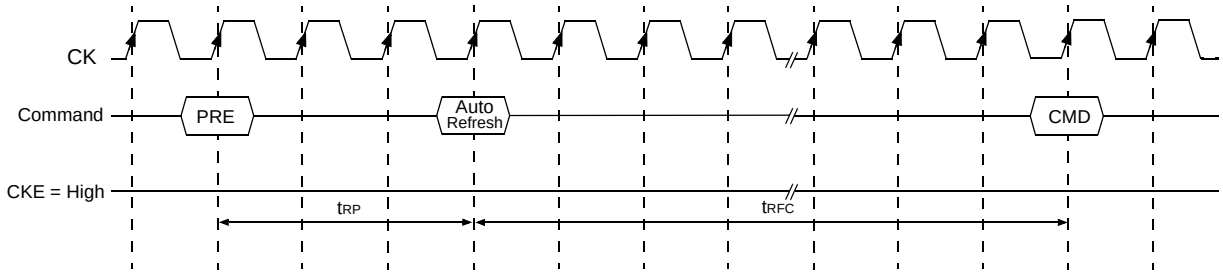
The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to /CAS BEFORE-/RAS (CBR) refresh in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum tRP has been met after the PRECHARGE command .

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The 128Mb SDRAM requires 4,096 AUTO REFRESH cycles every 64ms (tREF). Providing a distributed AUTO REFRESH command every 15.625µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRFC), once every 64ms.

Auto Refresh

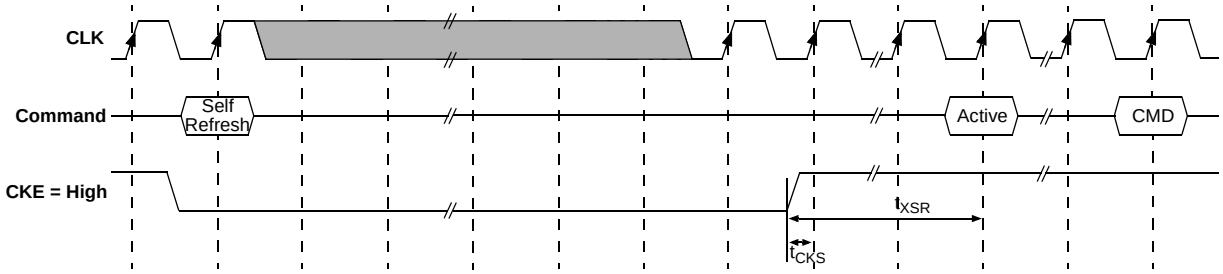


SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down, as long as power is not completely removed from the SDRAM. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to tRAS and may remain in self refresh mode for an indefinite period beyond that.

Self Refresh



DEEP POWER-DOWN

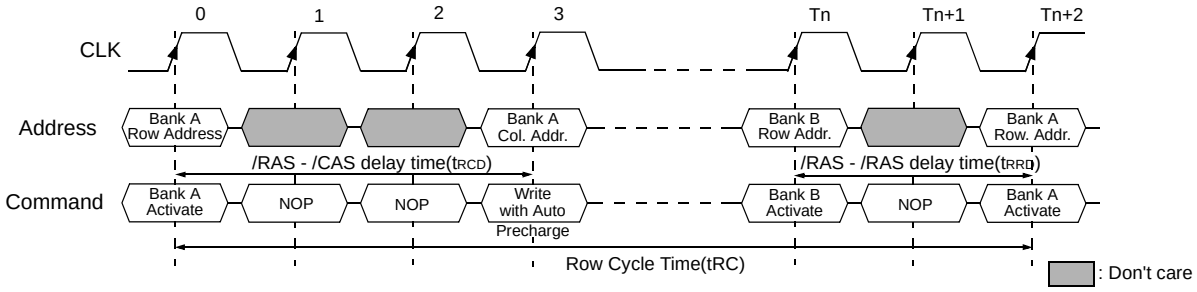
The operating mode deep power-down achieves maximum power reduction by eliminating the power of the whole memory array of the device. Array data will not be retained once the device enters deep power-down mode.
This mode is entered by having all banks idle then /CS and /WE held LOW with /RAS and /CAS held HIGH at the rising edge of the clock, while CKE is LOW. This mode is exited by asserting CKE HIGH.

Operations

Bank/Row Activation

The Bank Activation command is issued by holding /CAS and /WE high with /CS and /RAS low at the rising edge of the clock(CLK). The SDRAM has four independent banks, so two bank select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any READ or WRITE operation is executed. The delay from the Bank Activation command to the first READ or WRITE command must meet or exceed the minimum of /RAS to /CAS delay time(tRCD min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time(tRRD min).

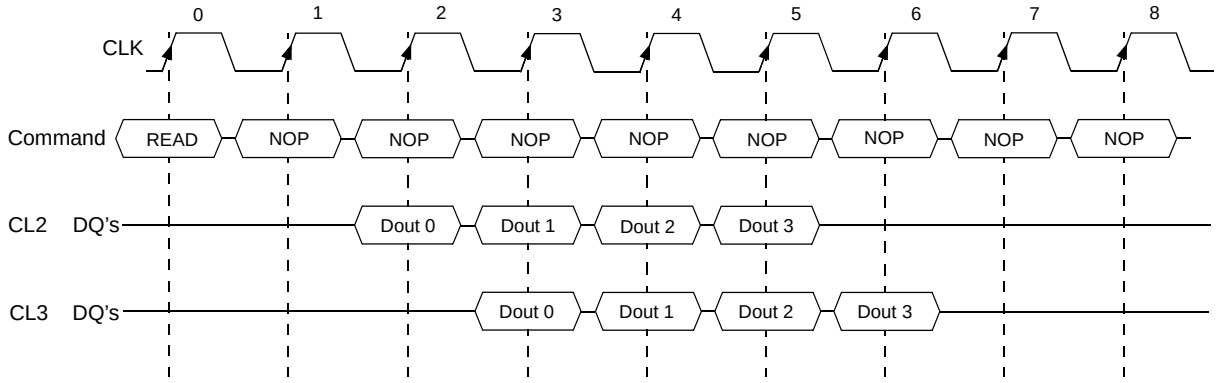
Bank Activation Command Cycle



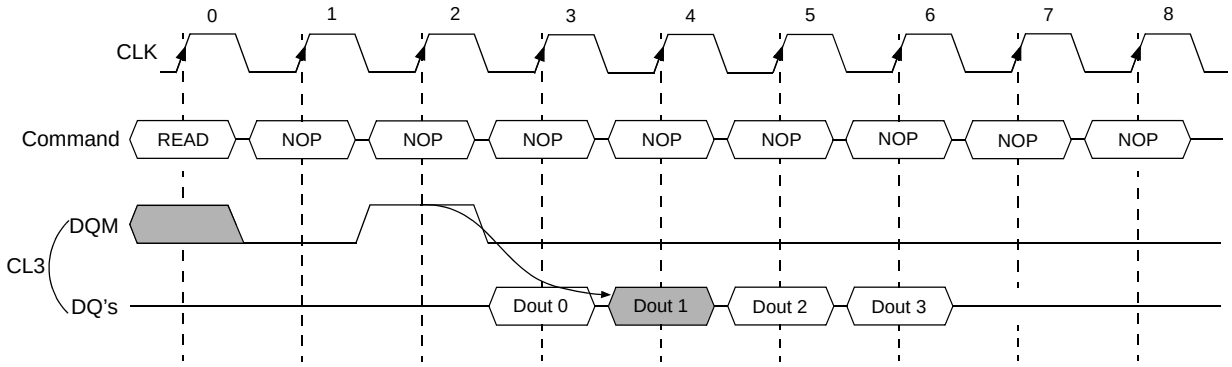
READs

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ comand. Each subsequent dataout element will be valid by the next positive clock edge. Upon completion of a burst, assuming no other comands have been initiated, the DQ will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.) Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either CASe, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ comand should be issued x cycles before the clock edge at which the last desired data element is valid, where x equals the CAS latency minus one.

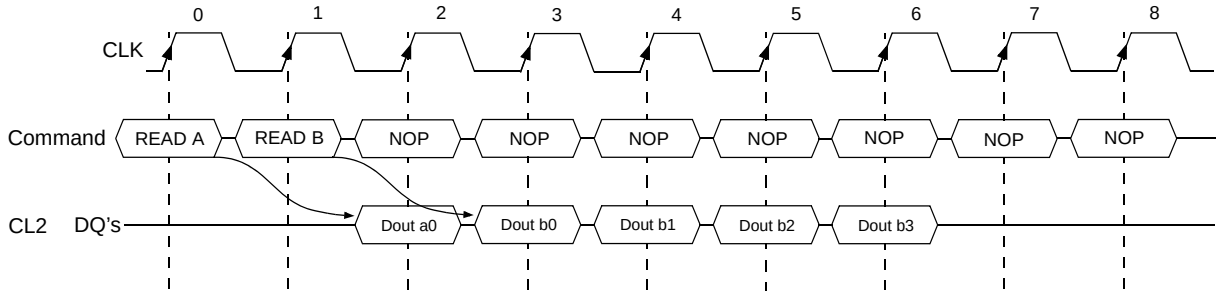
Burst Read Operation < Burst Length=4, CAS Latency=2, 3) >



DQM Masking < Burst Length = 4 >



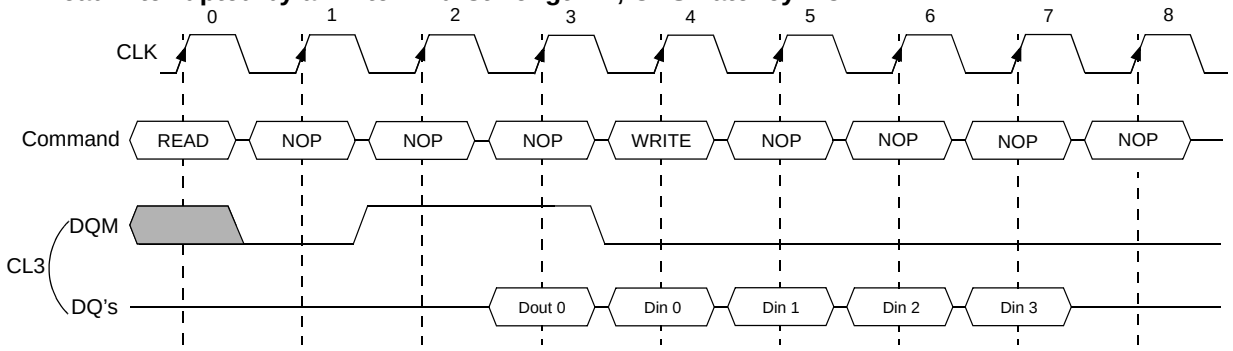
Read Interrupted by a Read < Burst Length=4, CAS Latency = 2 >



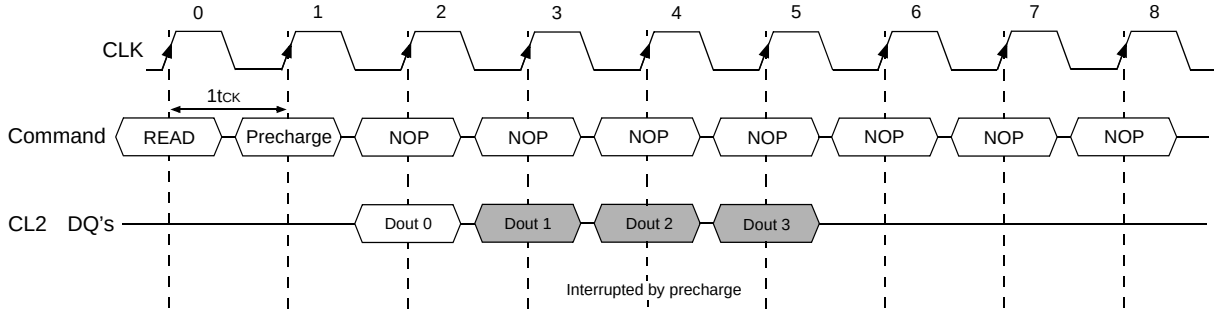
The DQM input is used to avoid I/O contention. The DQM signal must be asserted (HIGH) at least 2 clocks prior to the WRITE command (DQM latency is 2 clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQ will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked.

Read Interrupted by a Write < Burst Length=4, CAS Latency = 3 >



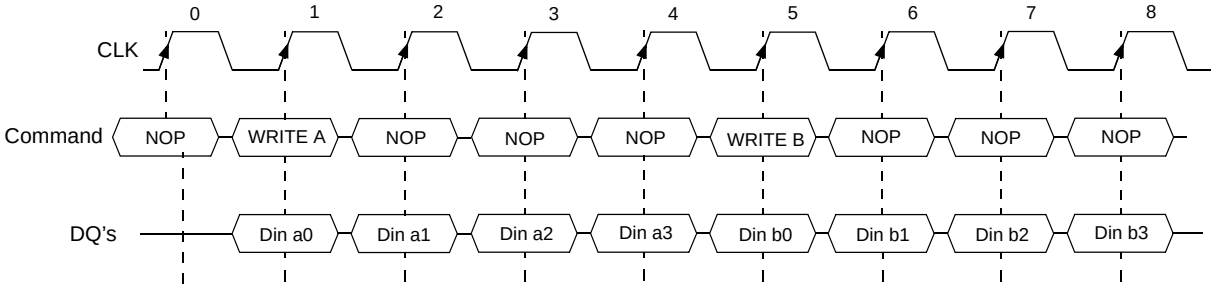
Read Interrupted by a Precharge < Burst Length=4, CAS Latency = 2 >



WRITEs

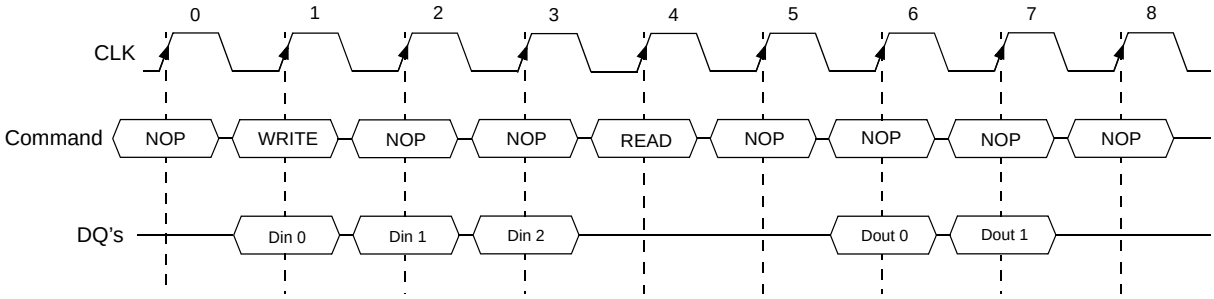
Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. Data n + 1 is either the last of a burst of two or the last desired of a longer burst. The 128Mb SDRAM uses a pipelined architecture and therefore does not require the 2n rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank or each subsequent WRITE may be performed to a different bank.

Burst Write Operation < Burst Length = 4 >

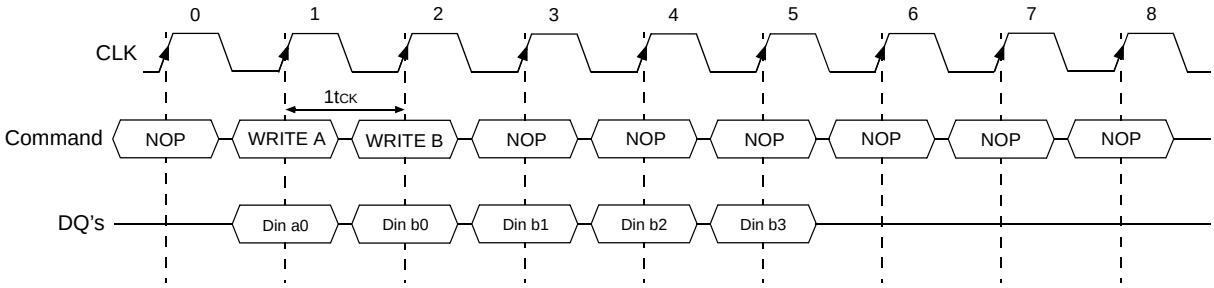


Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is registered, the data inputs will be ignored, and WRITEs will not be executed. Data n + 1 is either the last of a burst of two or the last desired of a longer burst. Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued tWR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a tWR of at least one clock plus time, regardless of frequency.

Write Interrupted by a Read < Burst Length = 4, CAS Latency = 2 >

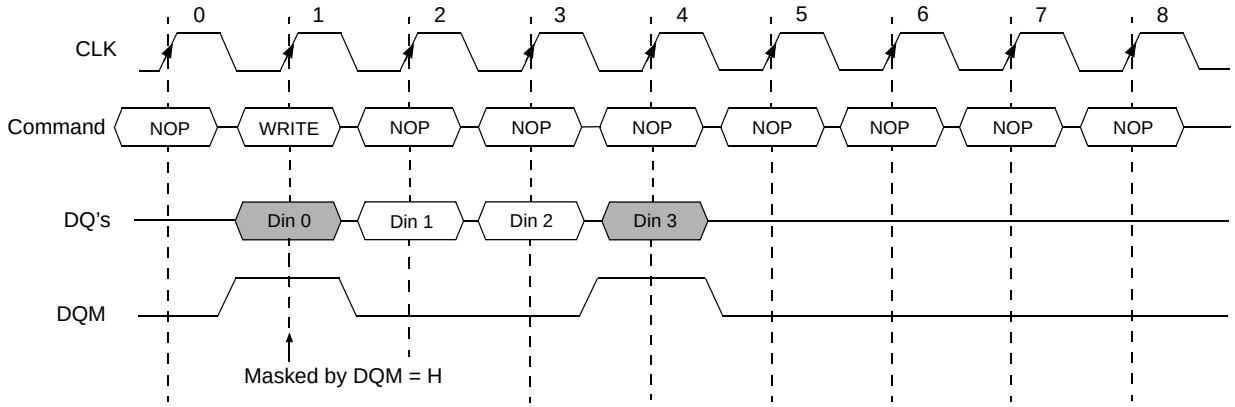


Write Interrupted by a Write < Burst Length = 4 >



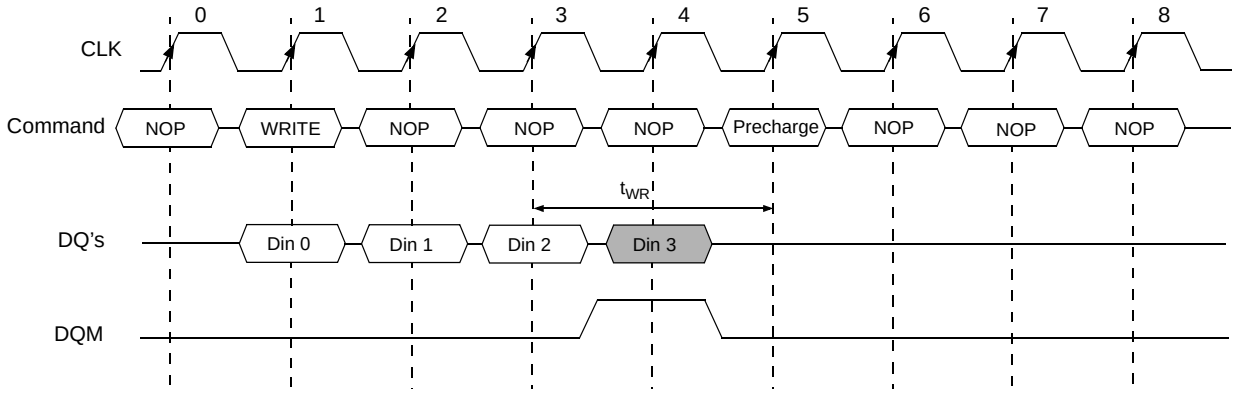
In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. Data n + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

DQM Masking < Burst Length = 4 >



In the CASe of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts. Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command.

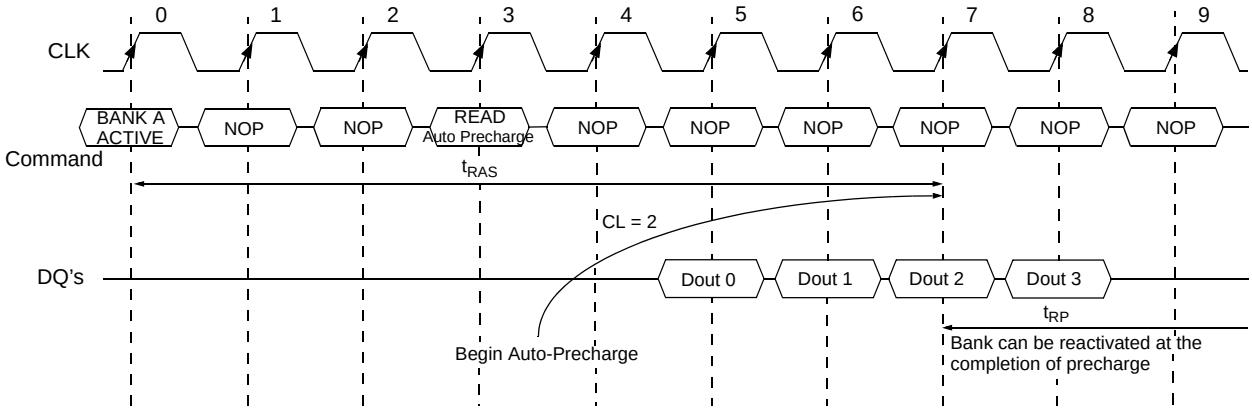
Write Interrupted by a Precharge & DQM < Burst Length = 4 >



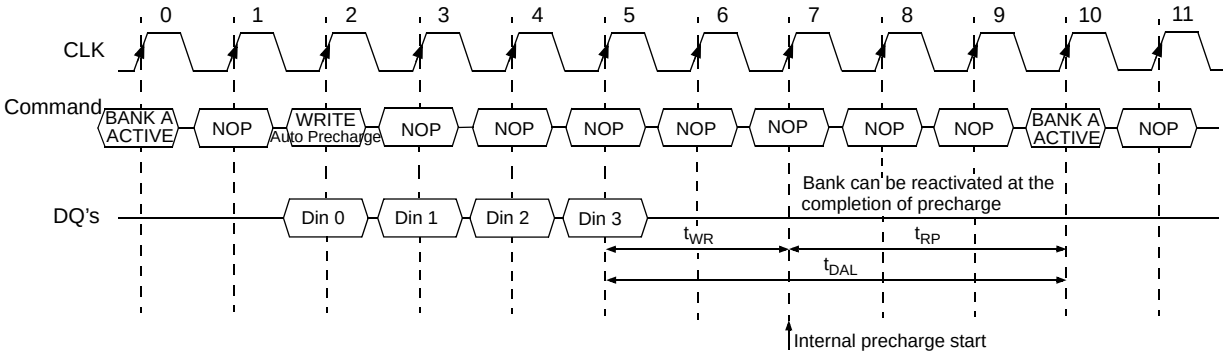
PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the CASe where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Read with Auto Precharge < Burst Length = 4, CAS Latency = 2 >



Write with Auto Precharge < Burst Length = 4 >



Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or DESELECT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or DESELECT and CKE HIGH at the desired clock edge (meeting tCKS).

Power down

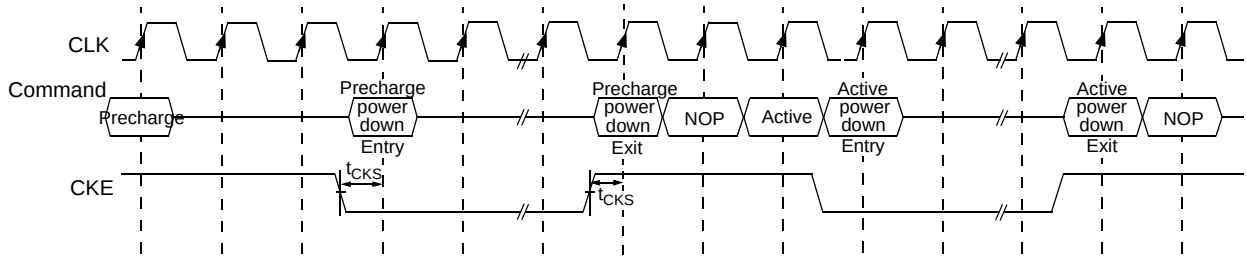


Table 17: SIMPLIFIED TRUTH TABLE

(V=Valid, X =Don't care, H=Logic High, L=Logic Low)

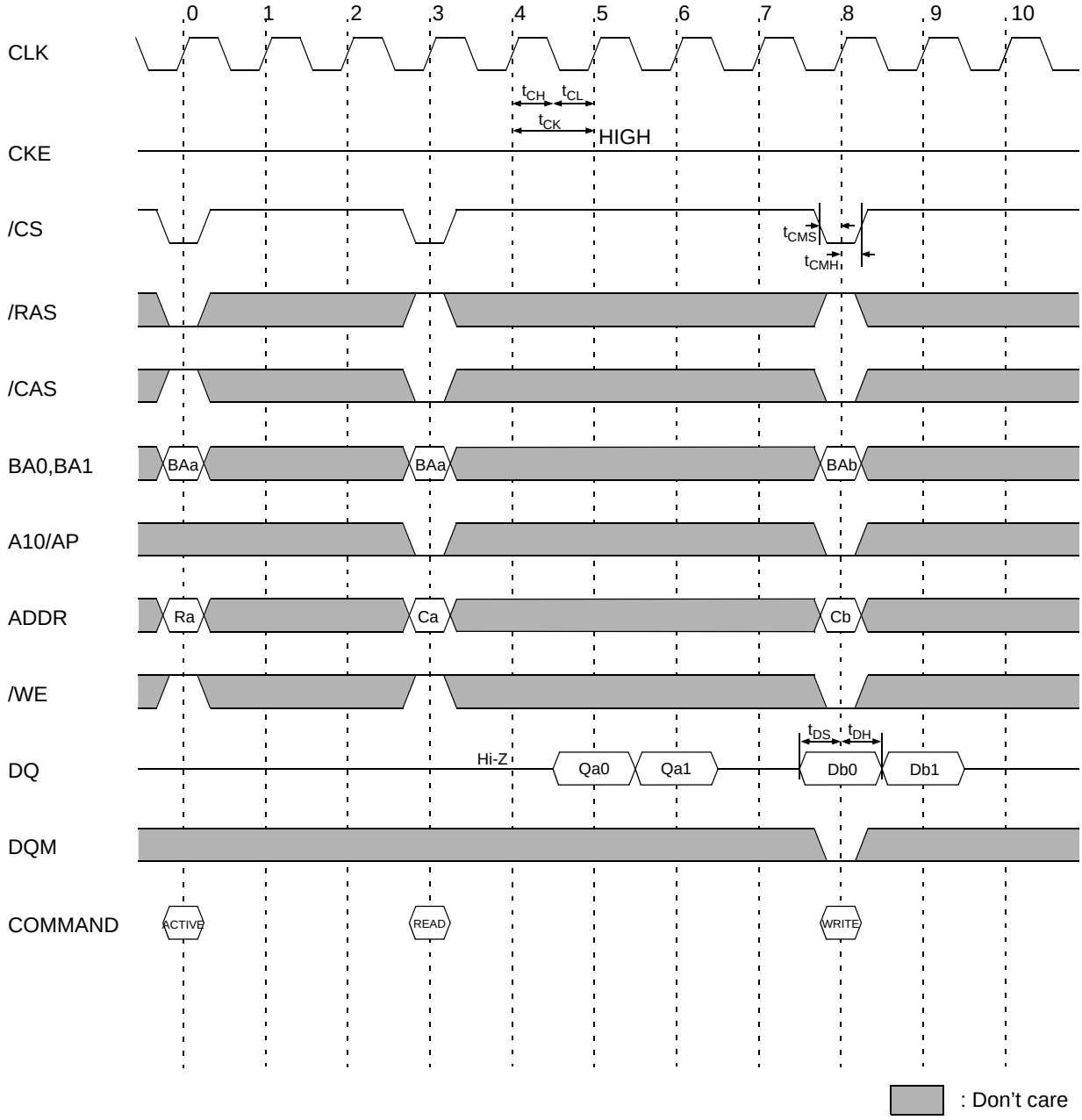
COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	BA0, 1	A10/AP	A11 A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Deep Power down		Entry	H	L	L	H	H	L	X	X			
		Exit	L	H	H	X	X	X	X				
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
DQM			H	X					V	X			7
No Operation Command(NOP)			H	X	H	X	X	X	X	X			
					L	H	H	H					

NOTE :

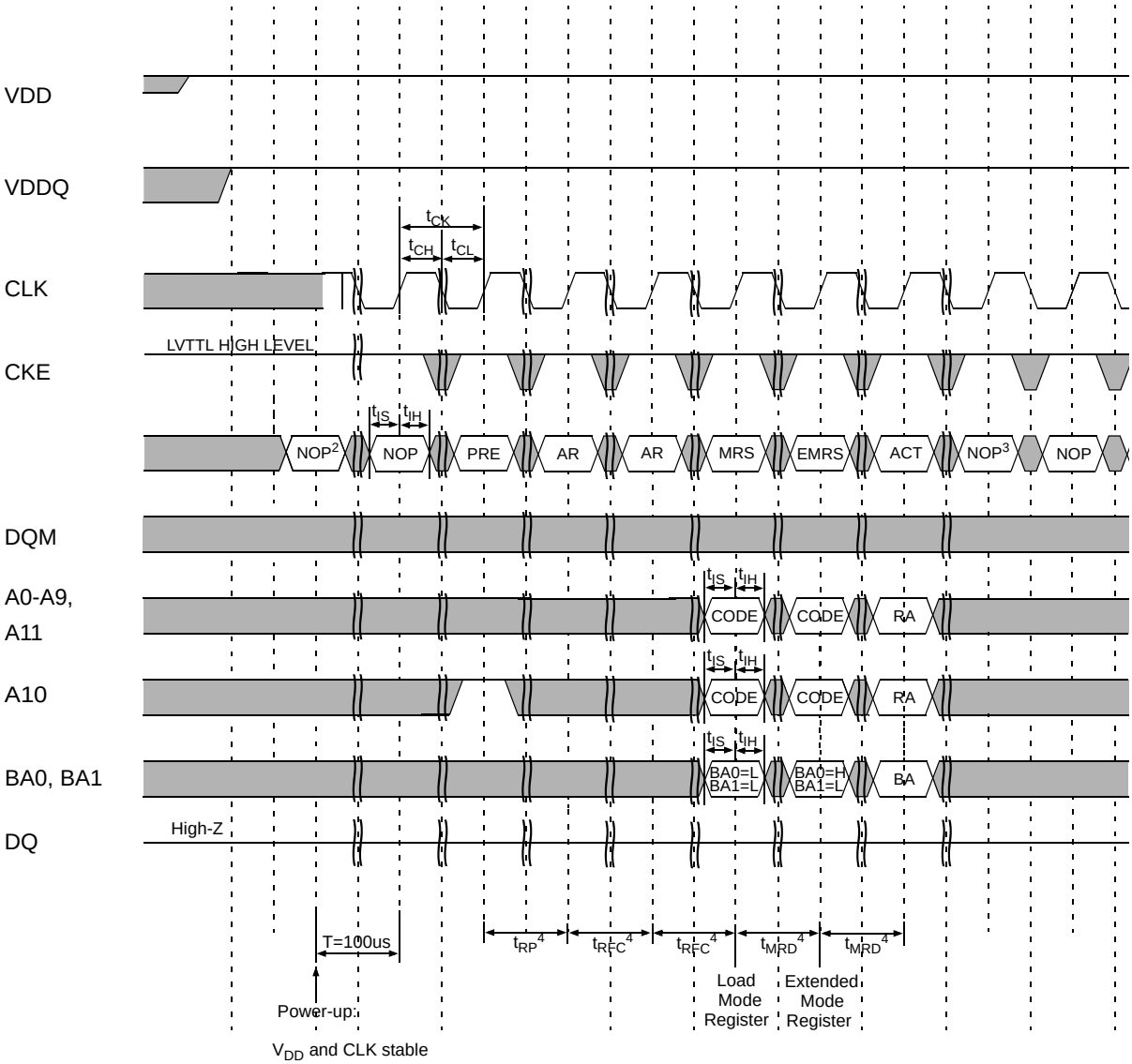
1. OP Code : Operand Code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 CLK cycles after EMRS or MRS.
3. Auto refresh functions are the same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
   Partial self refresh can be issued only at all banks precharge state.
4. BA0 ~BA1 : Bank select addresses.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation, it makes the data-out Hi-Z state after 2CLK cycles. (Read DQM latency is 2).

Timing Diagrams

Basic Timing (Setup, Hold and Access Time @ BL=2, CL=2)



Power up & Initialization Sequence



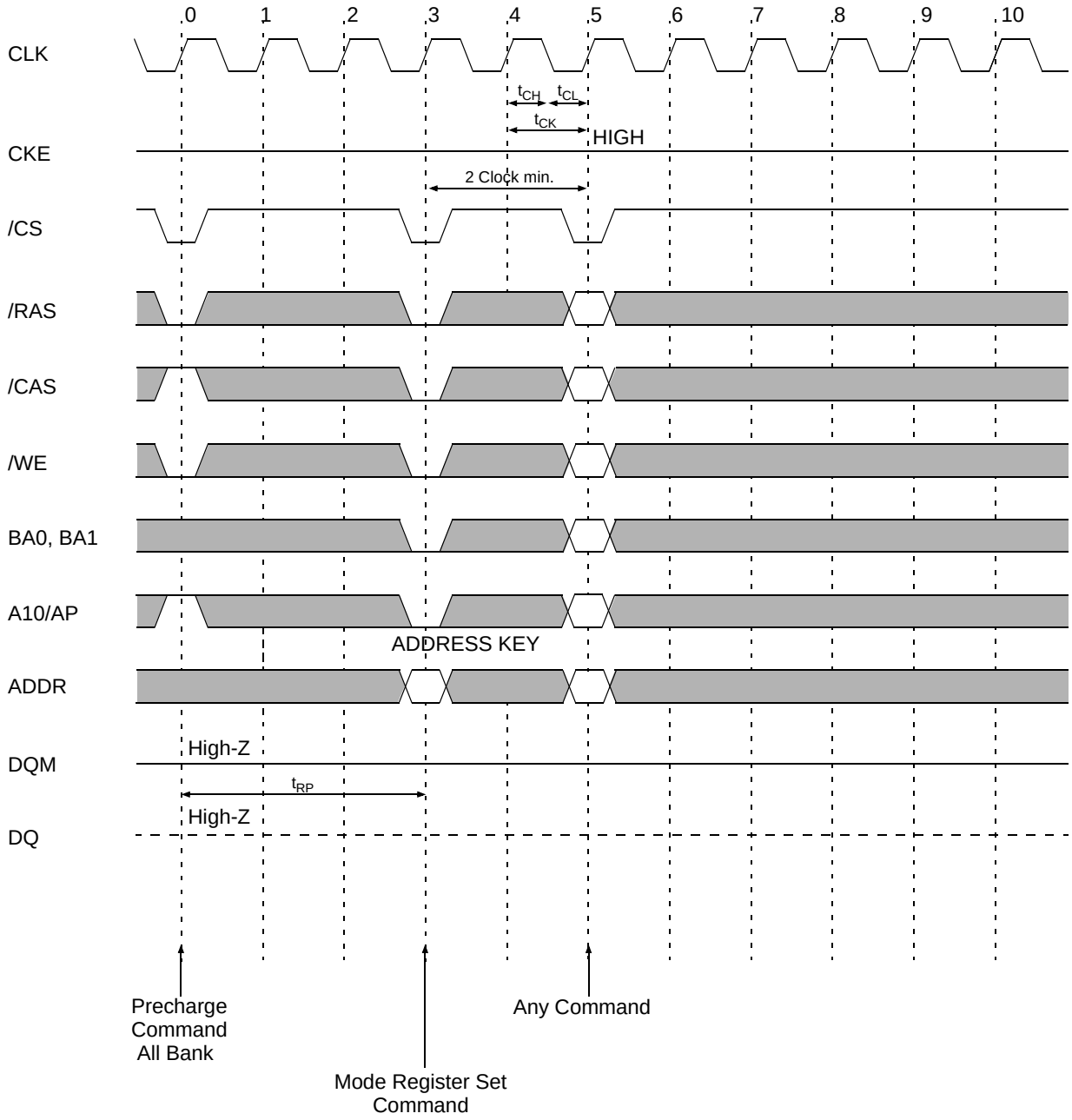
Notees: 1. PRE = PRECHARGE command, MRS = LOAD MODE REGISTER command, AR = AUTO REFRESH command
ACT = ACTIVE command, RA = Row address, BA = Bank address

2. NOP or DESELECT commands are required for at least 100us.

3. Other valid commands are possible.

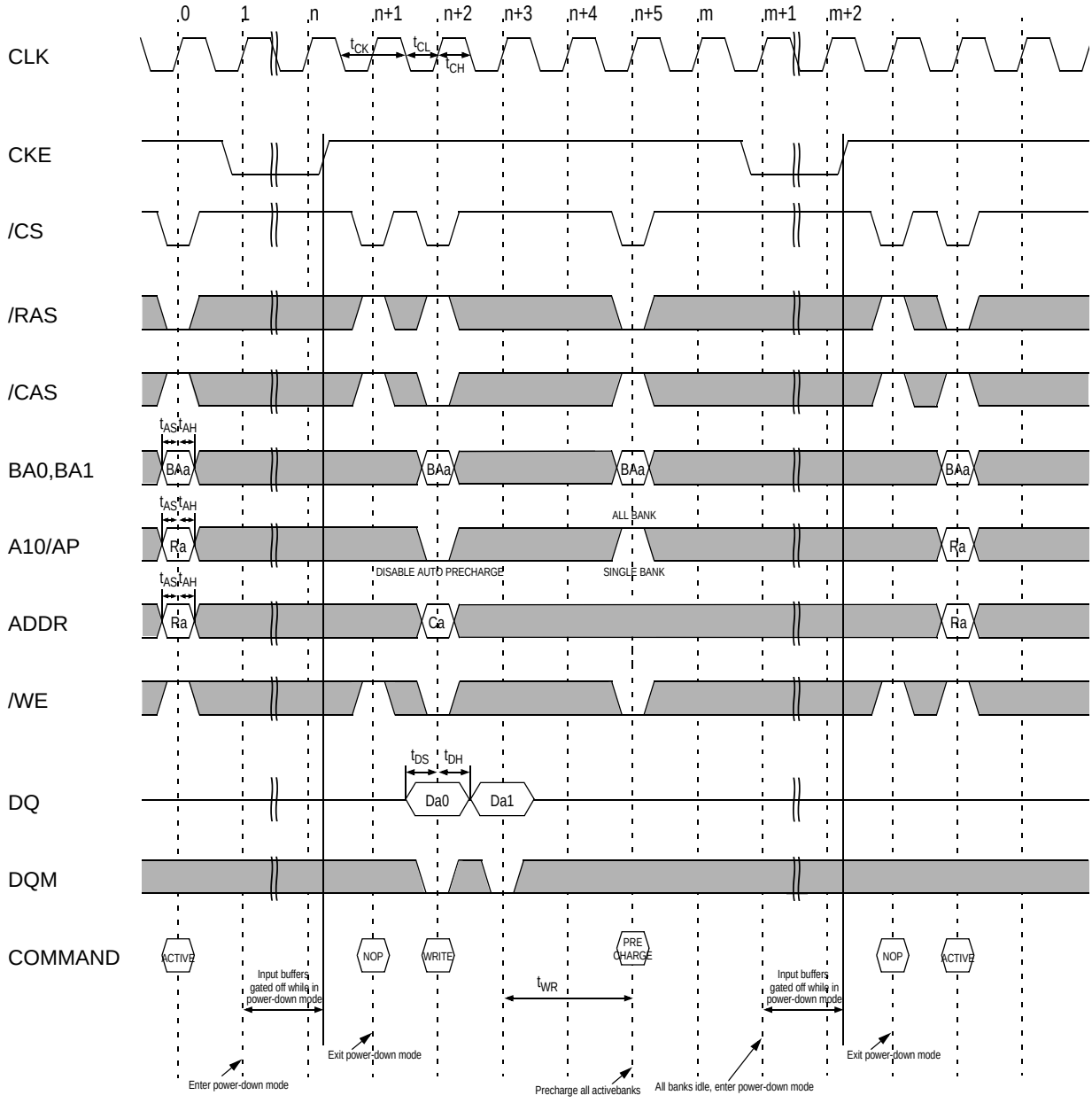
4. NOPs or DESELECTs are required during this time.

Mode Register Set



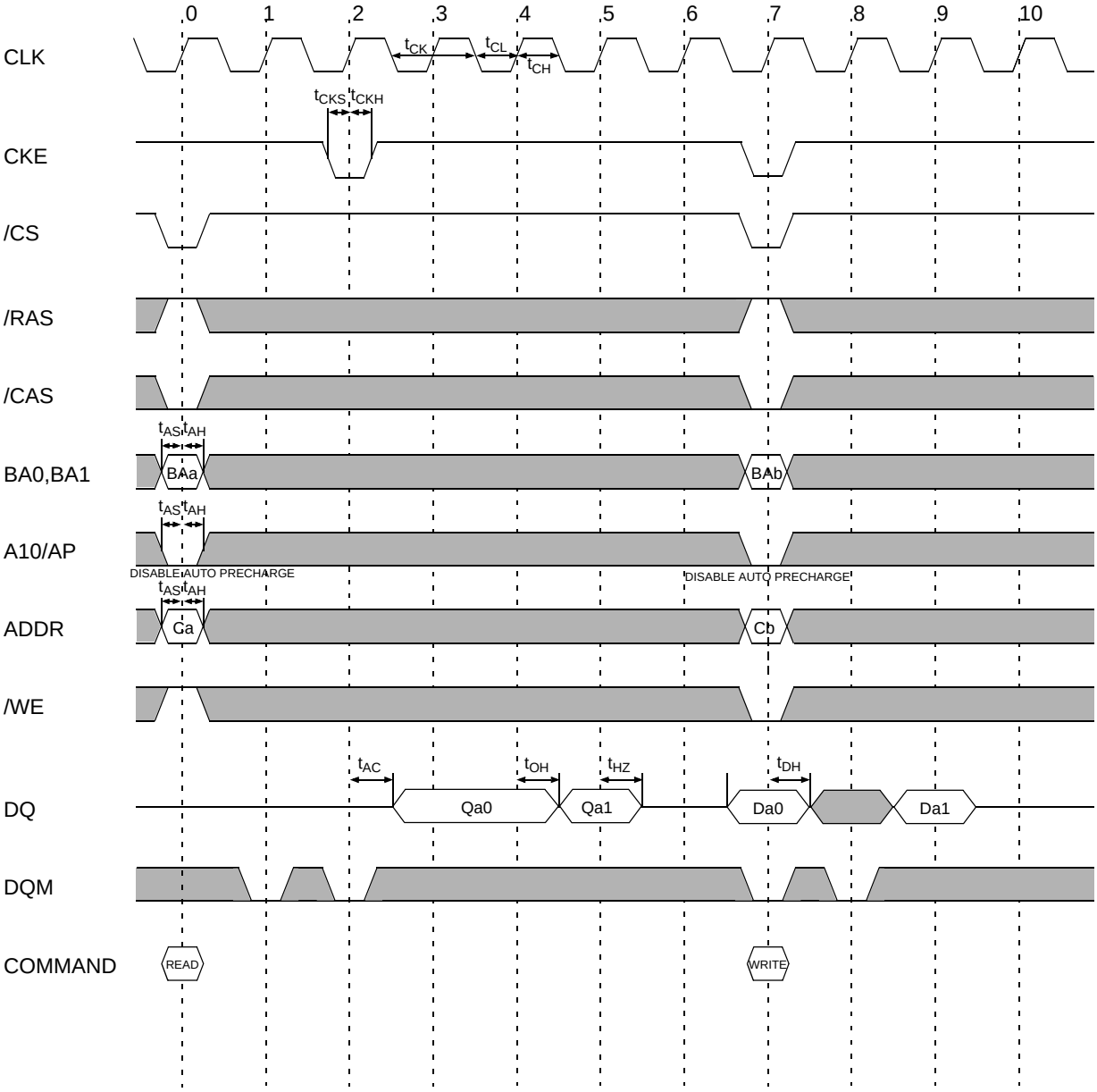
Note : Power & Clock must be stable for 100us before precharge all banks

Powerdown Mode



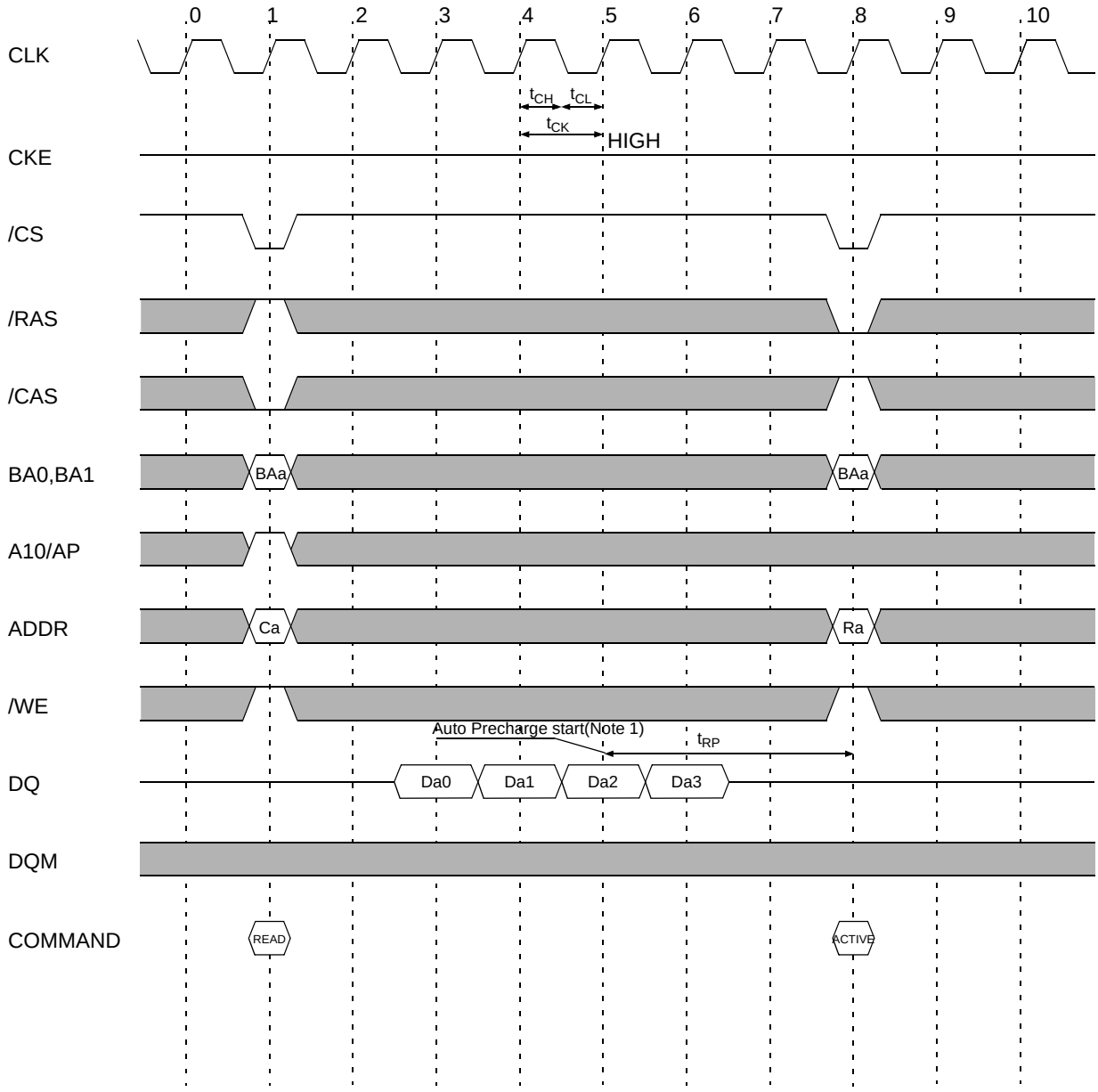
Note 1 Violating refresh requirements during power-down may result in a loss of data.

Clock Suspend Mode



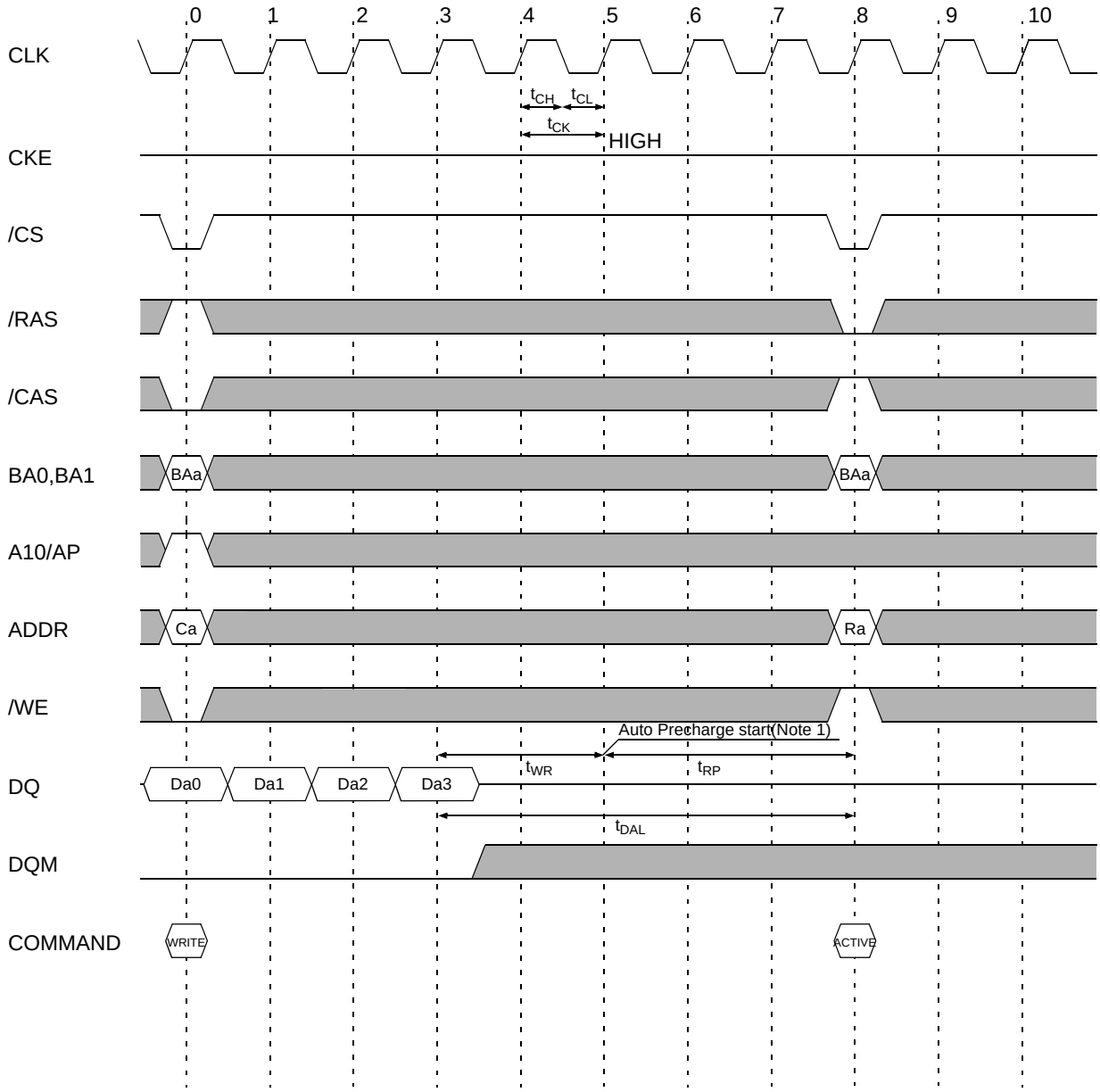
Note 1 For this example, BL=2, CL=3 and auto precharge is disabled.

READ with Auto Precharge (@ BL=4, CL=2)



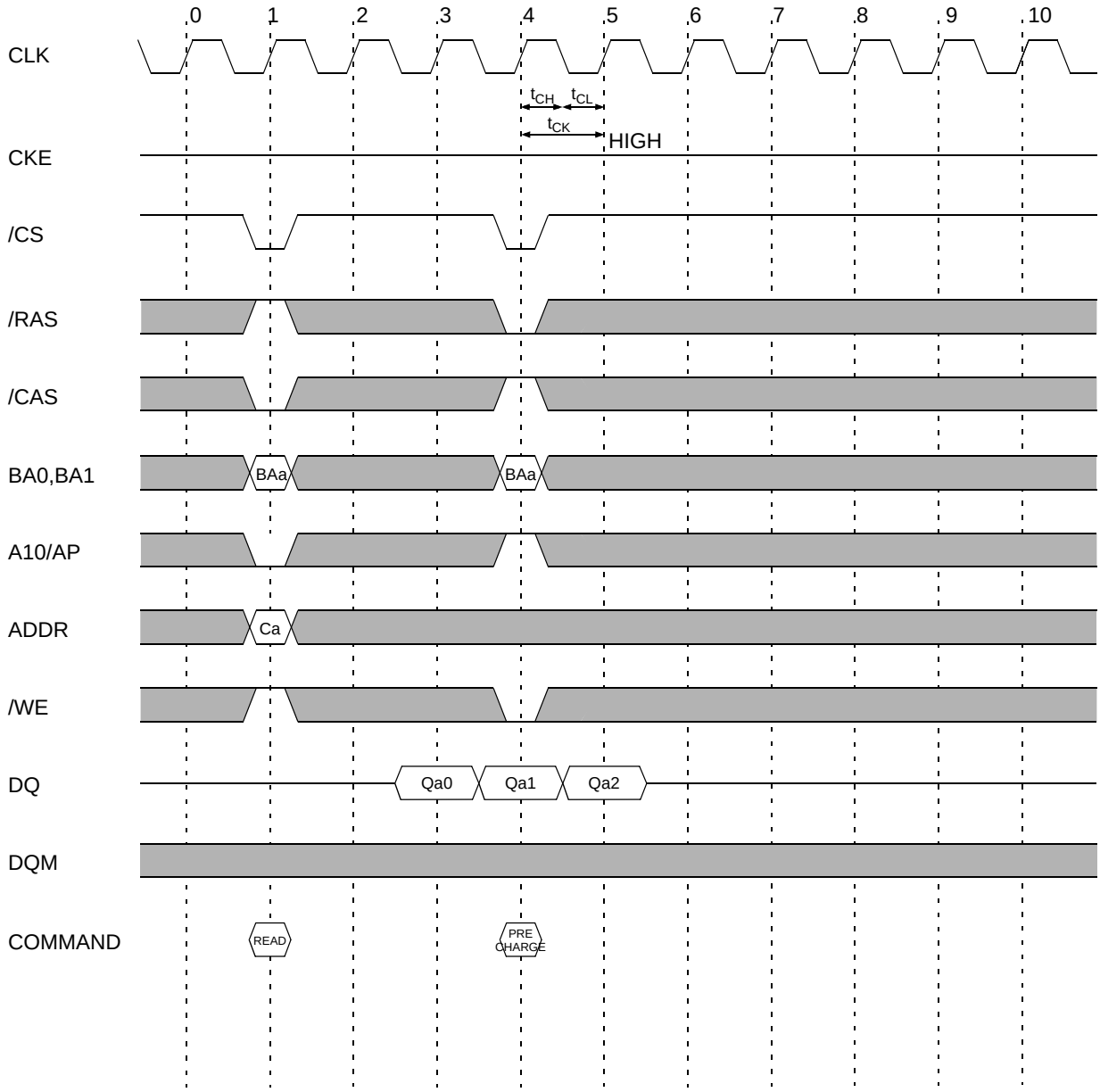
Note 1 The row active command of the precharged bank can be issued after tRP from this point.

WRITE with Auto Precharge (@ BL=4)



Note 1 The row active command of the precharged bank can be issued after tRP from this point.

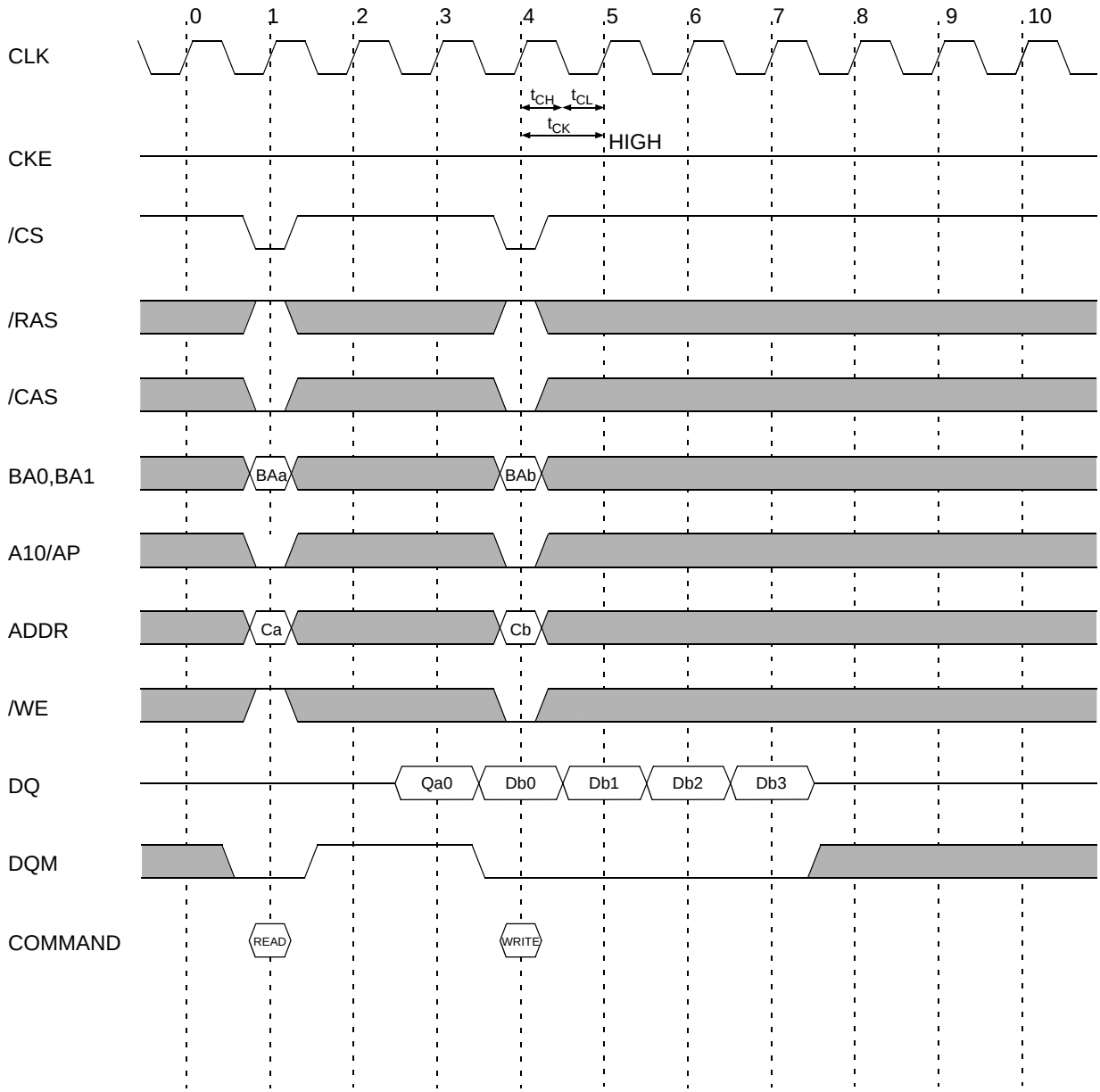
READ Interrupted by Precharge (@ BL=4, CL=2)



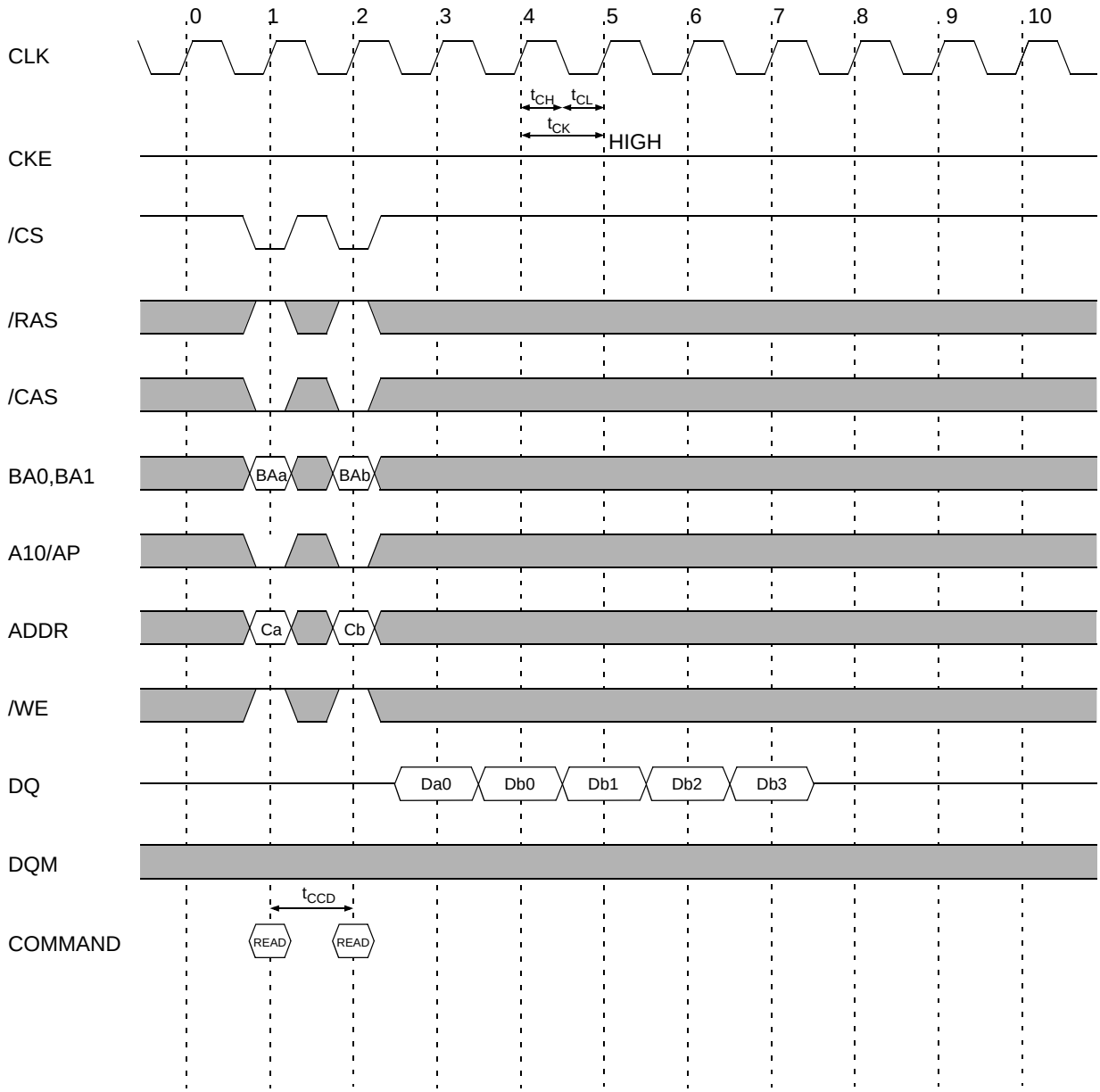
When a burst Read command is issued to a SDRAM, a Prechcrge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and When a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP(RAS Precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the CAS Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after tRP.

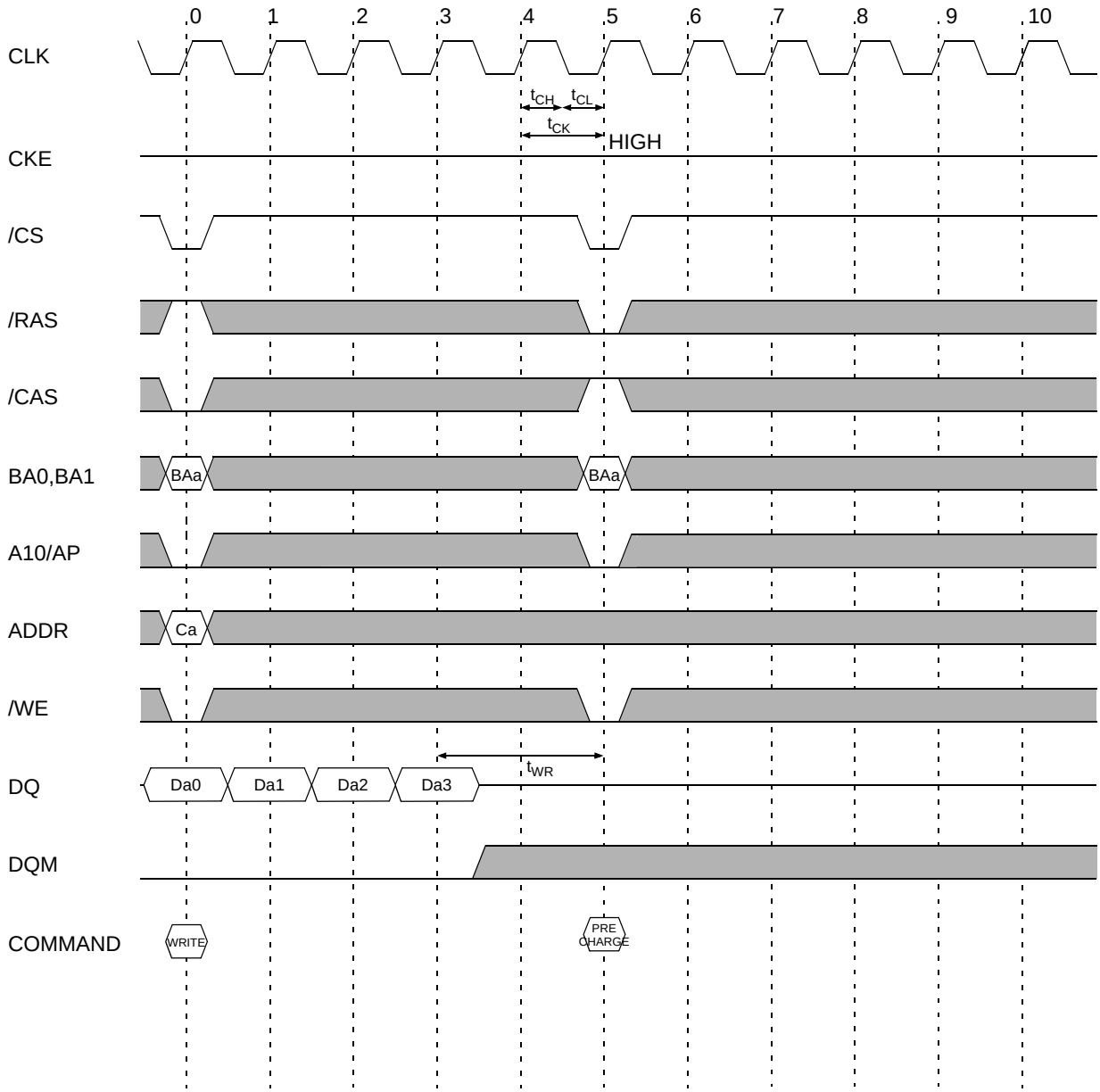
READ Interrupted by a WRITE (@ BL=4, CL=2)



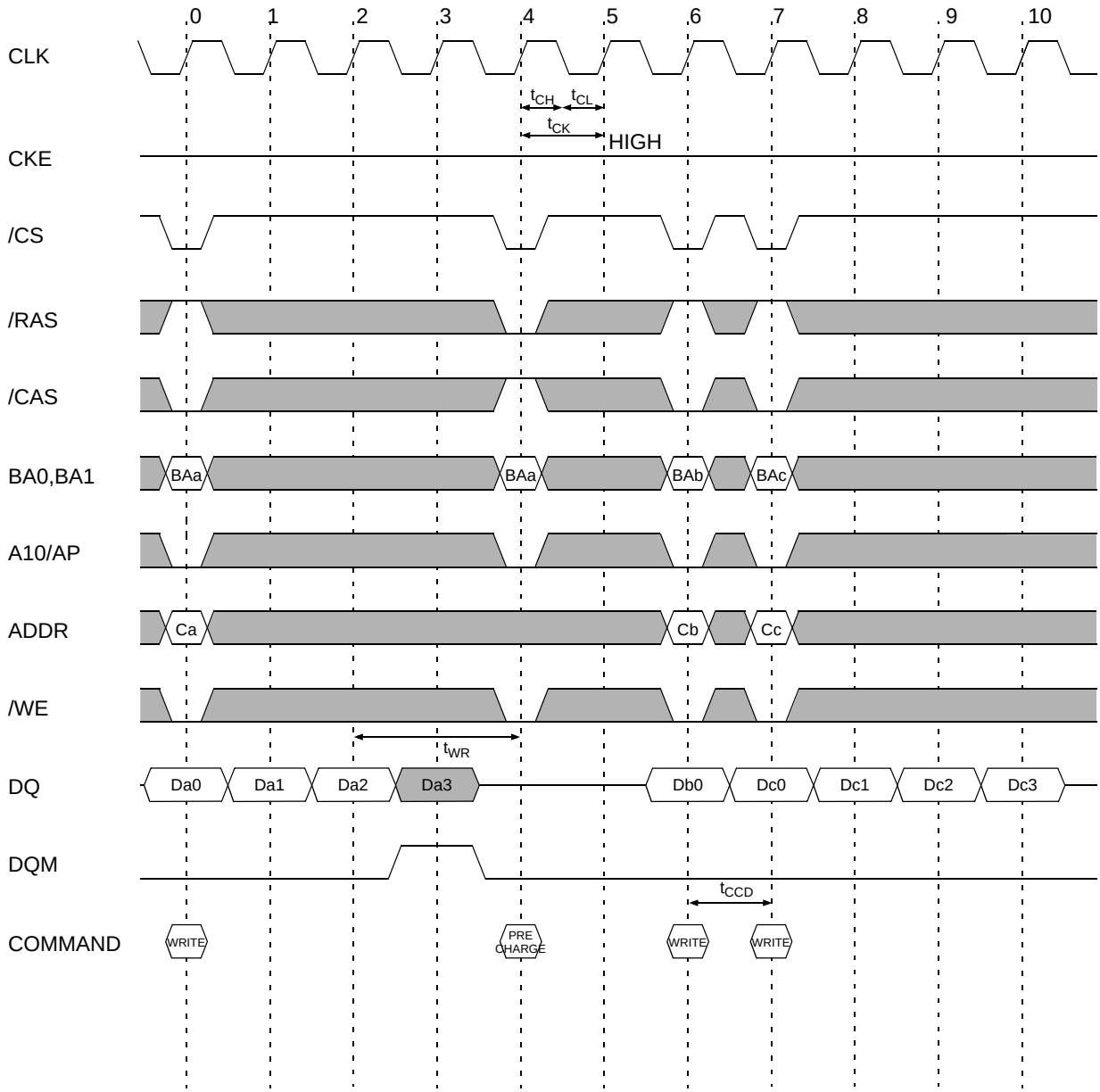
READ Interrupted by READ (@ BL=4, CL=2)



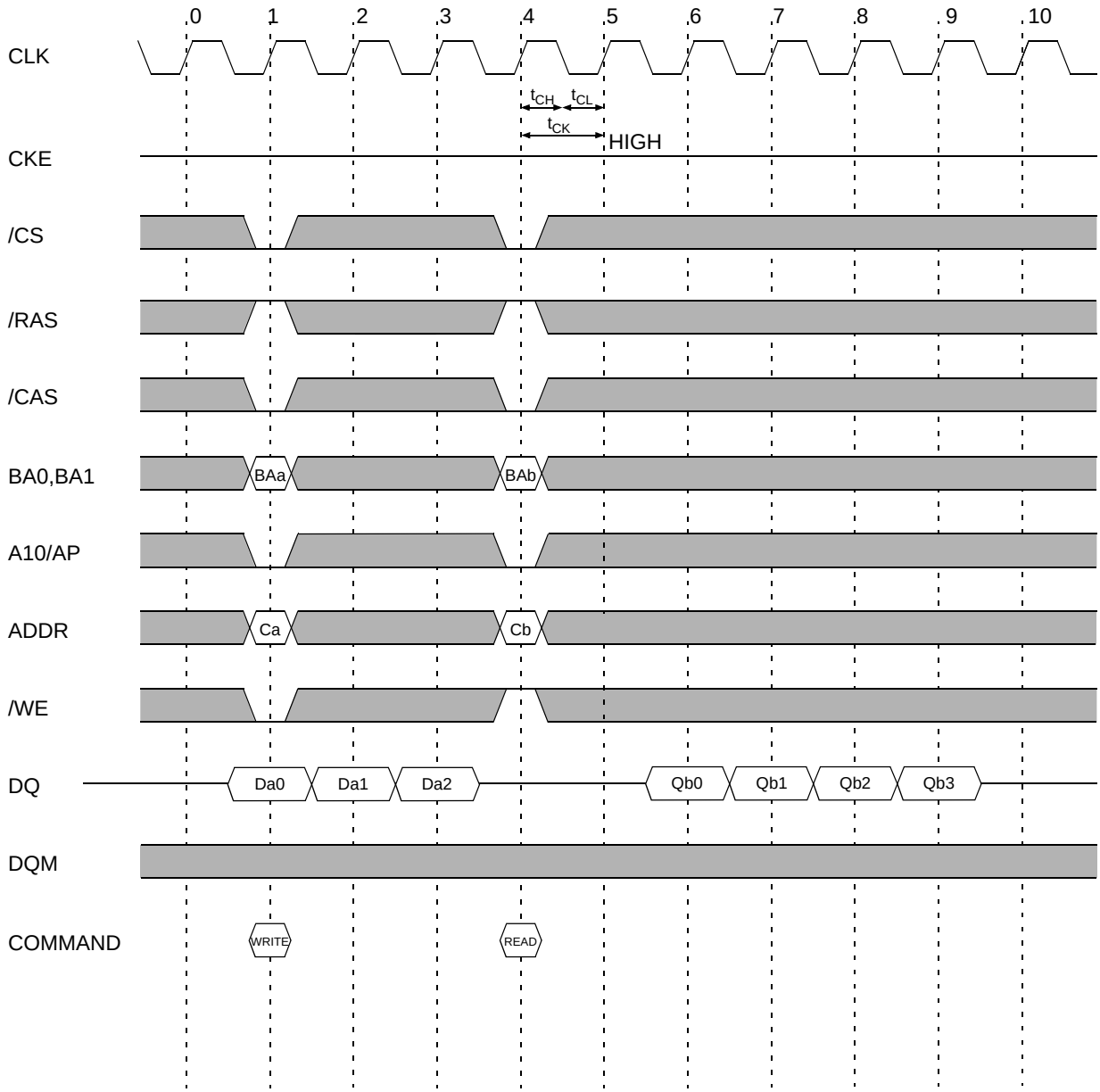
WRITE followed by Precharge (@ BL=4)



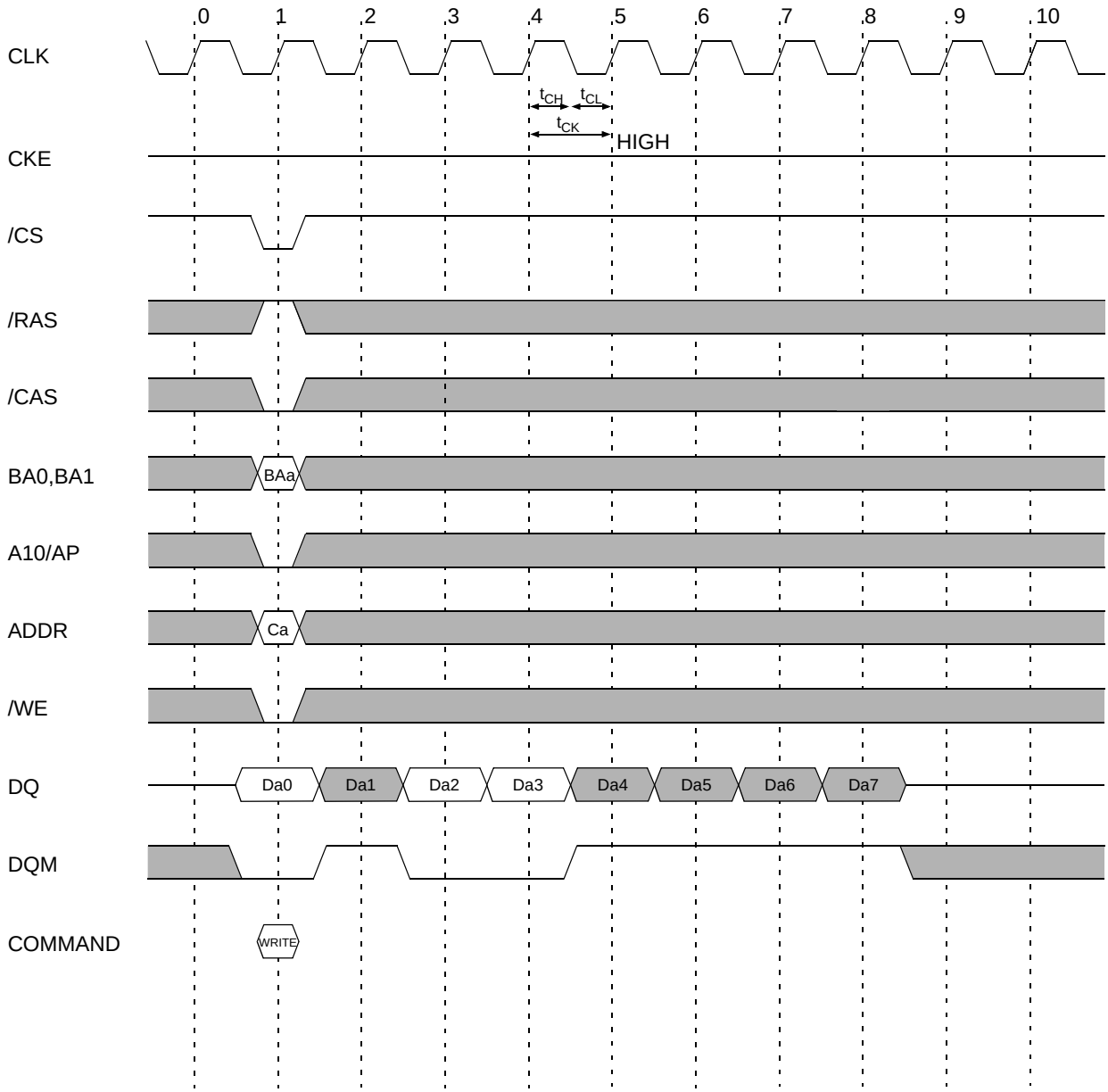
WRITE Interrupted by Precharge & DQM (@ BL=4)



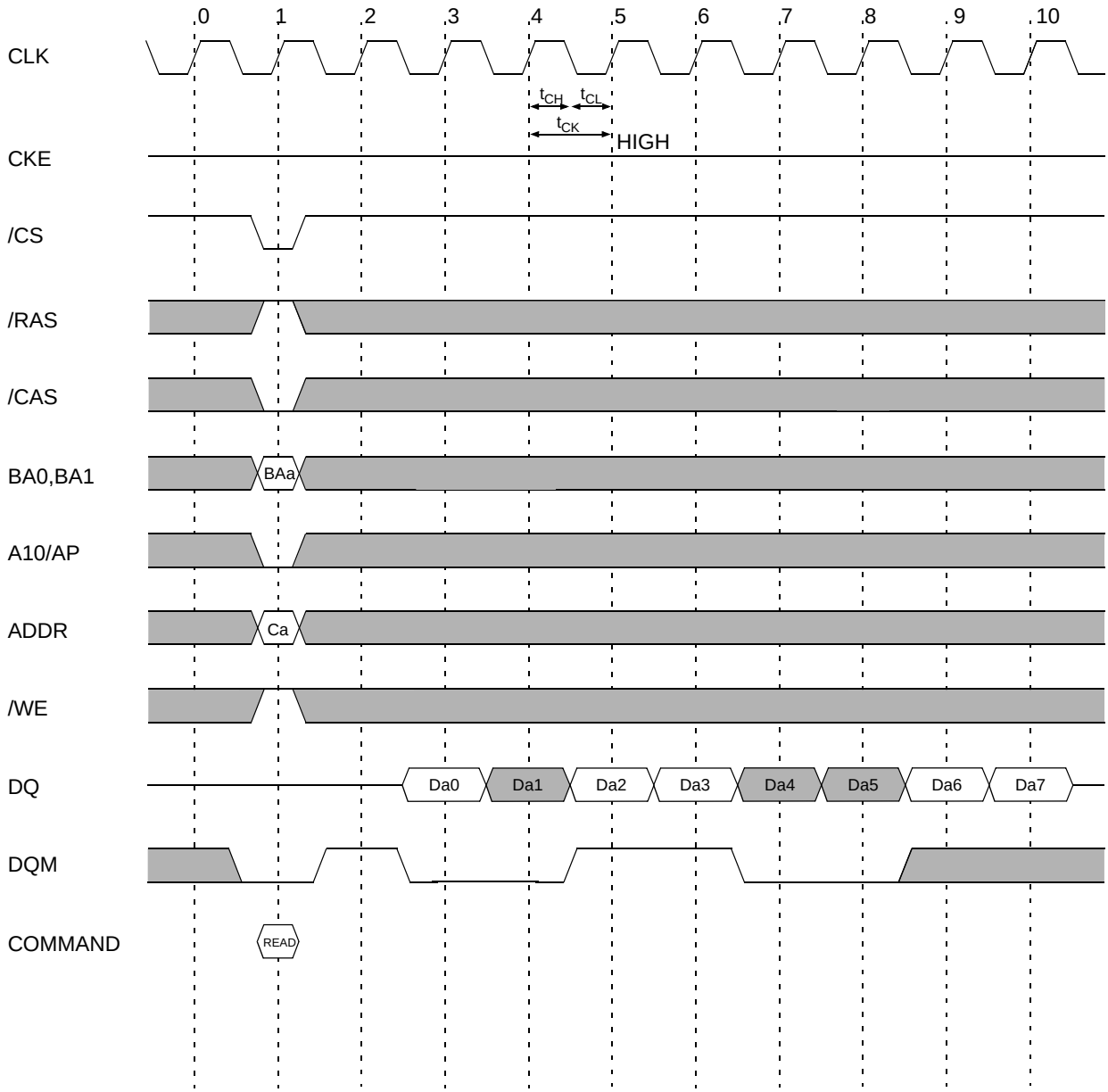
WRITE Interrupted by a READ (@ BL=4, CL=2)



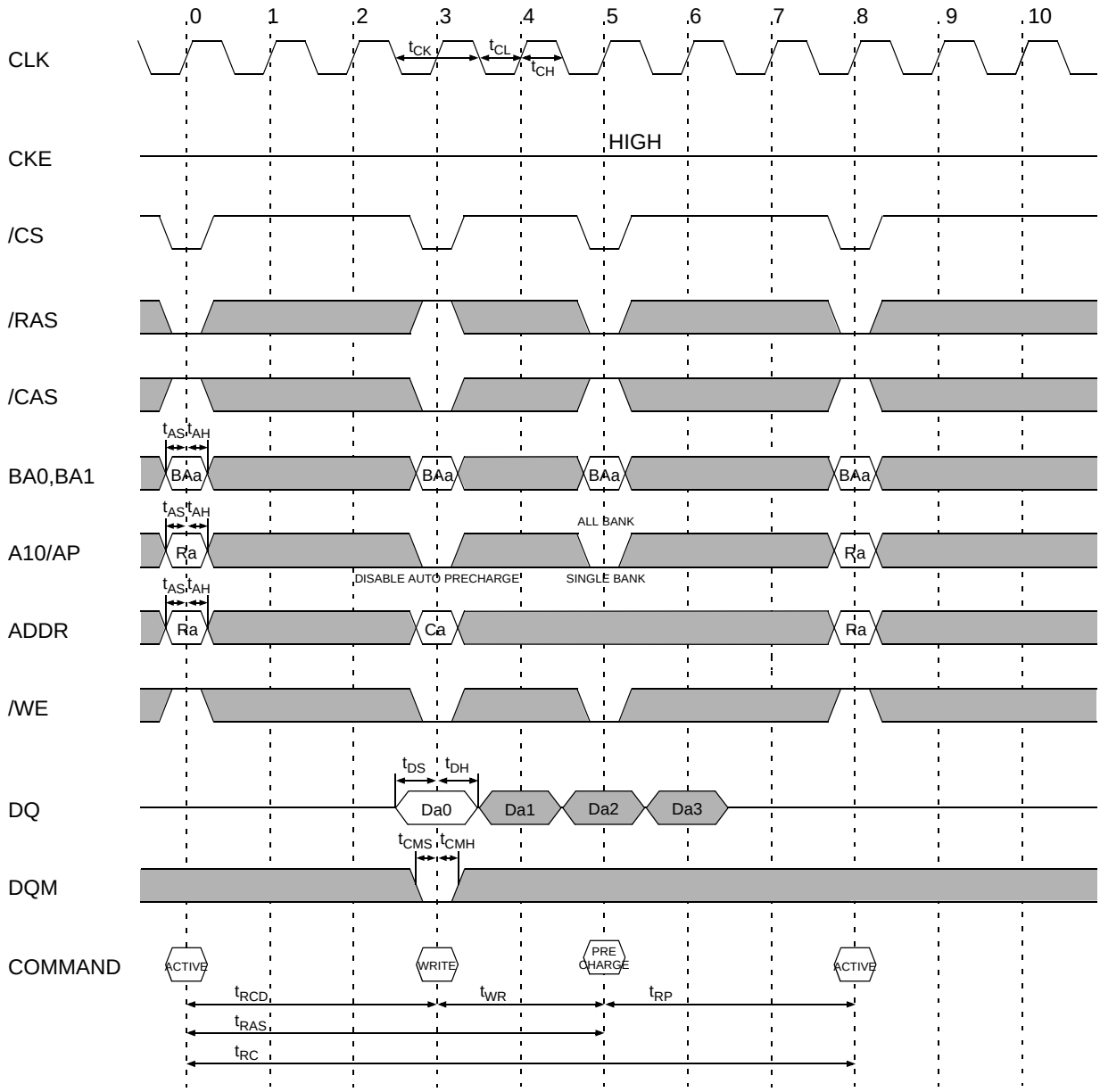
DQM Function (@BL=8) for write



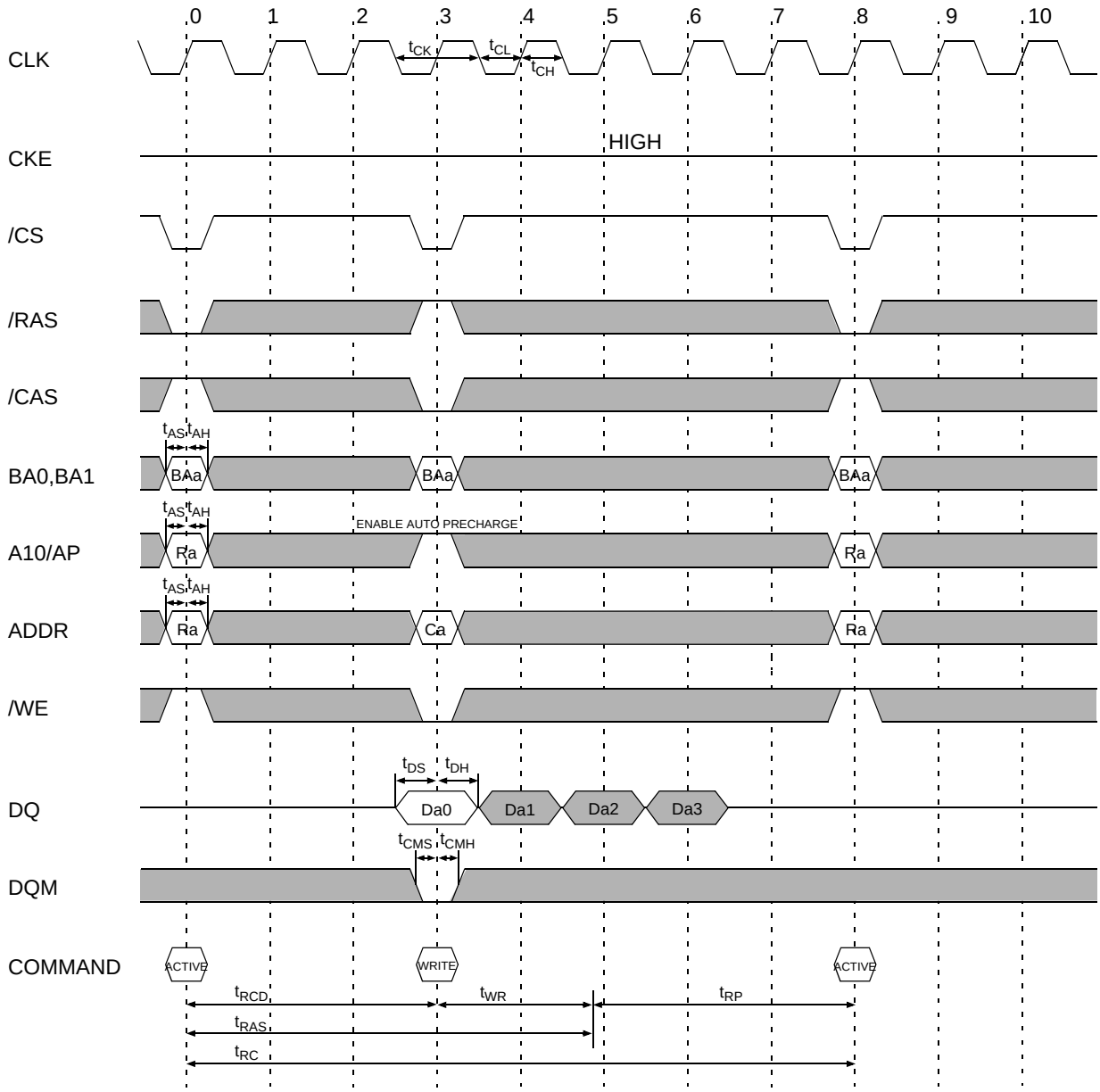
DQM Function (@BL=8, CL=2) for read



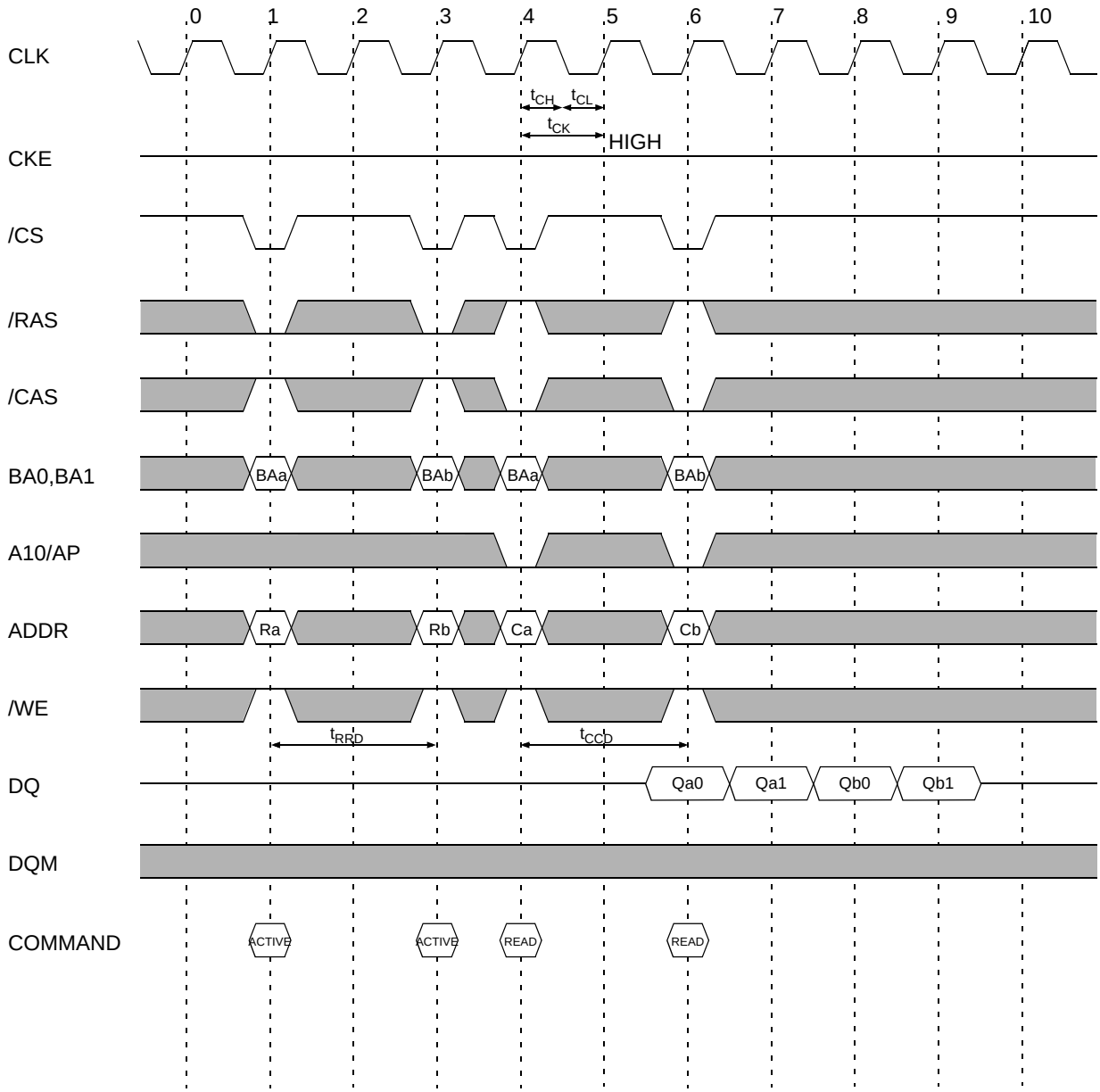
Single WRITE - Without Auto Precharge



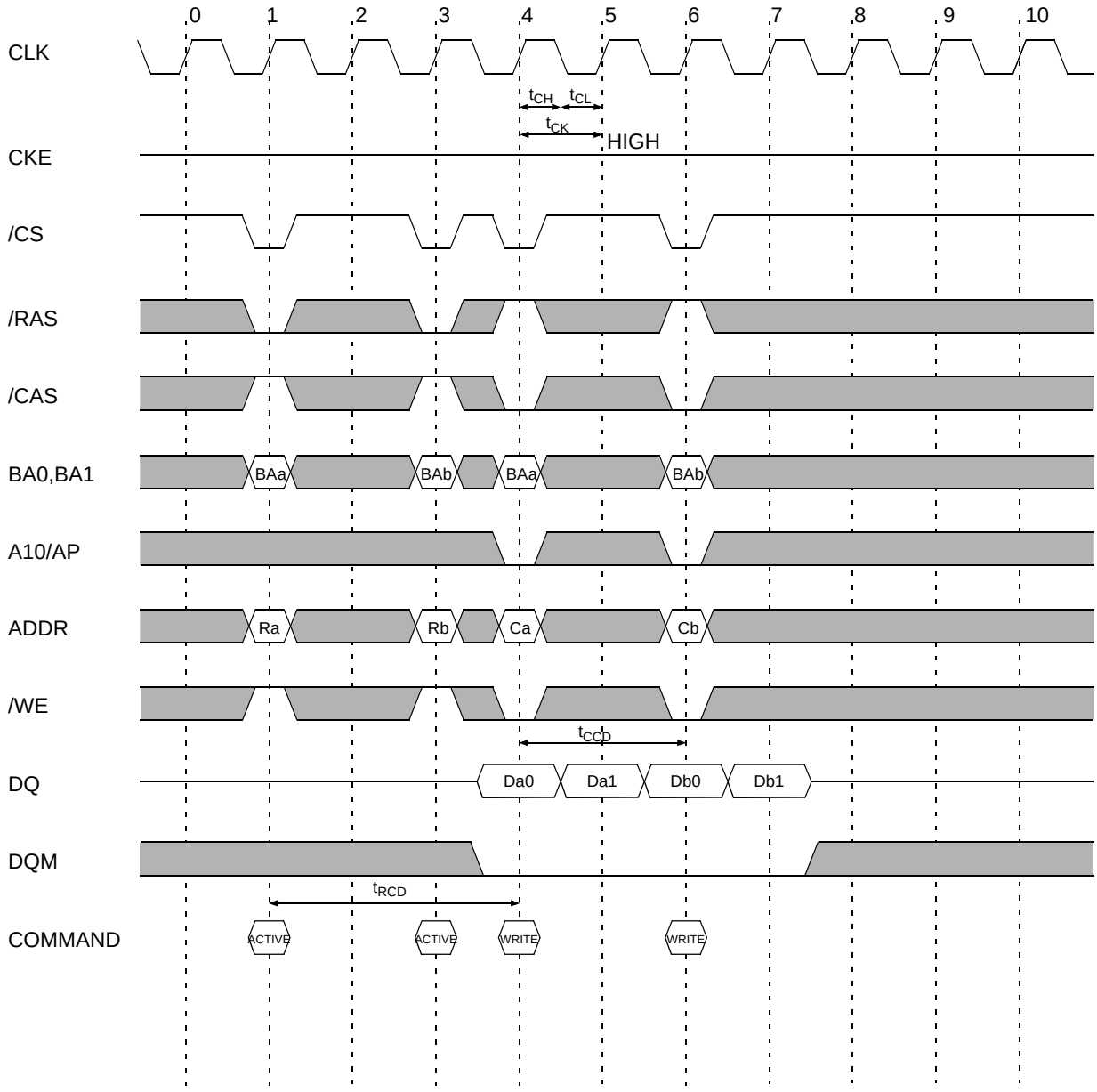
Single WRITE - With Auto Precharge



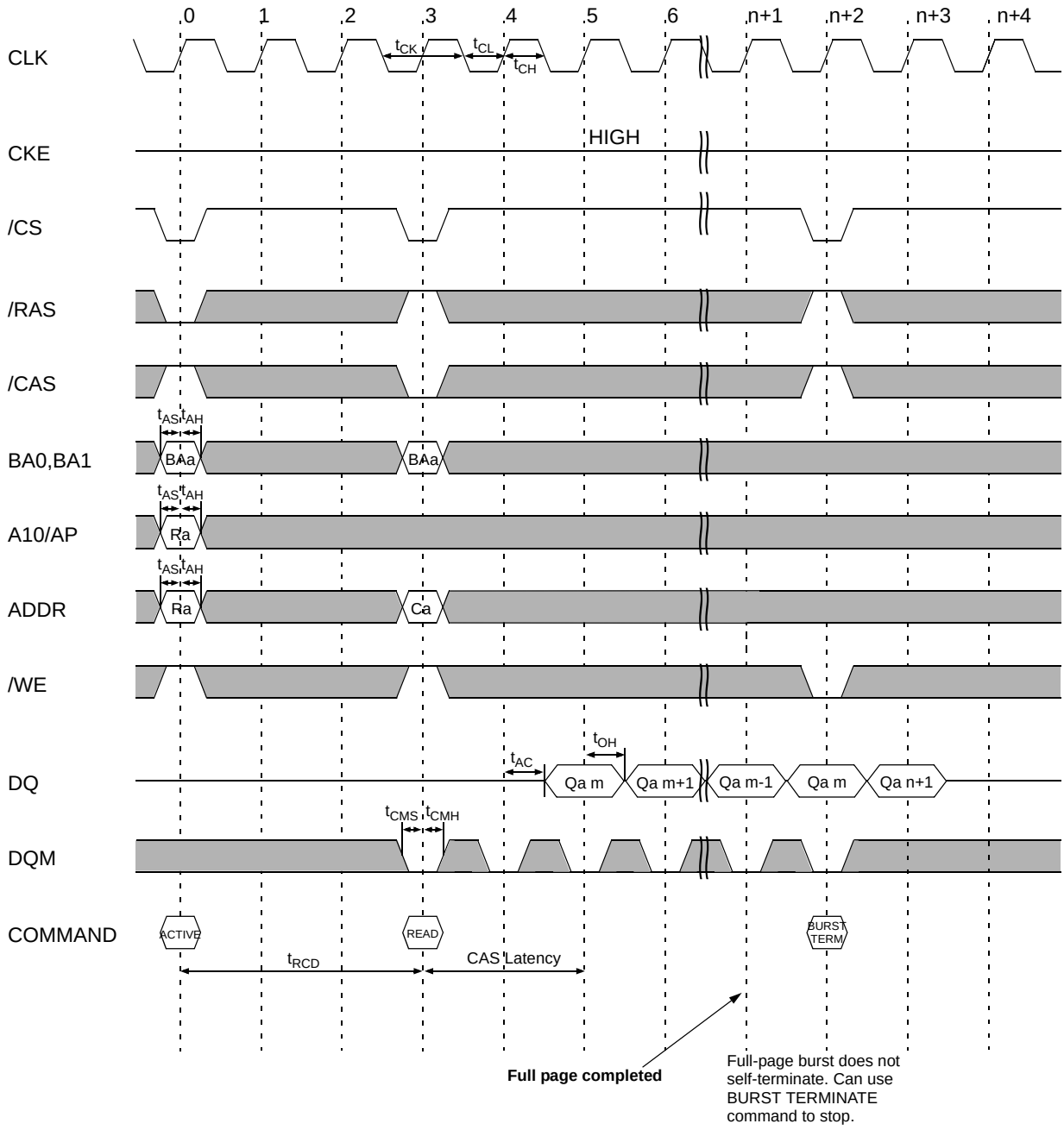
Multi Bank Interleaving READ (@ BL=2, CL=2)



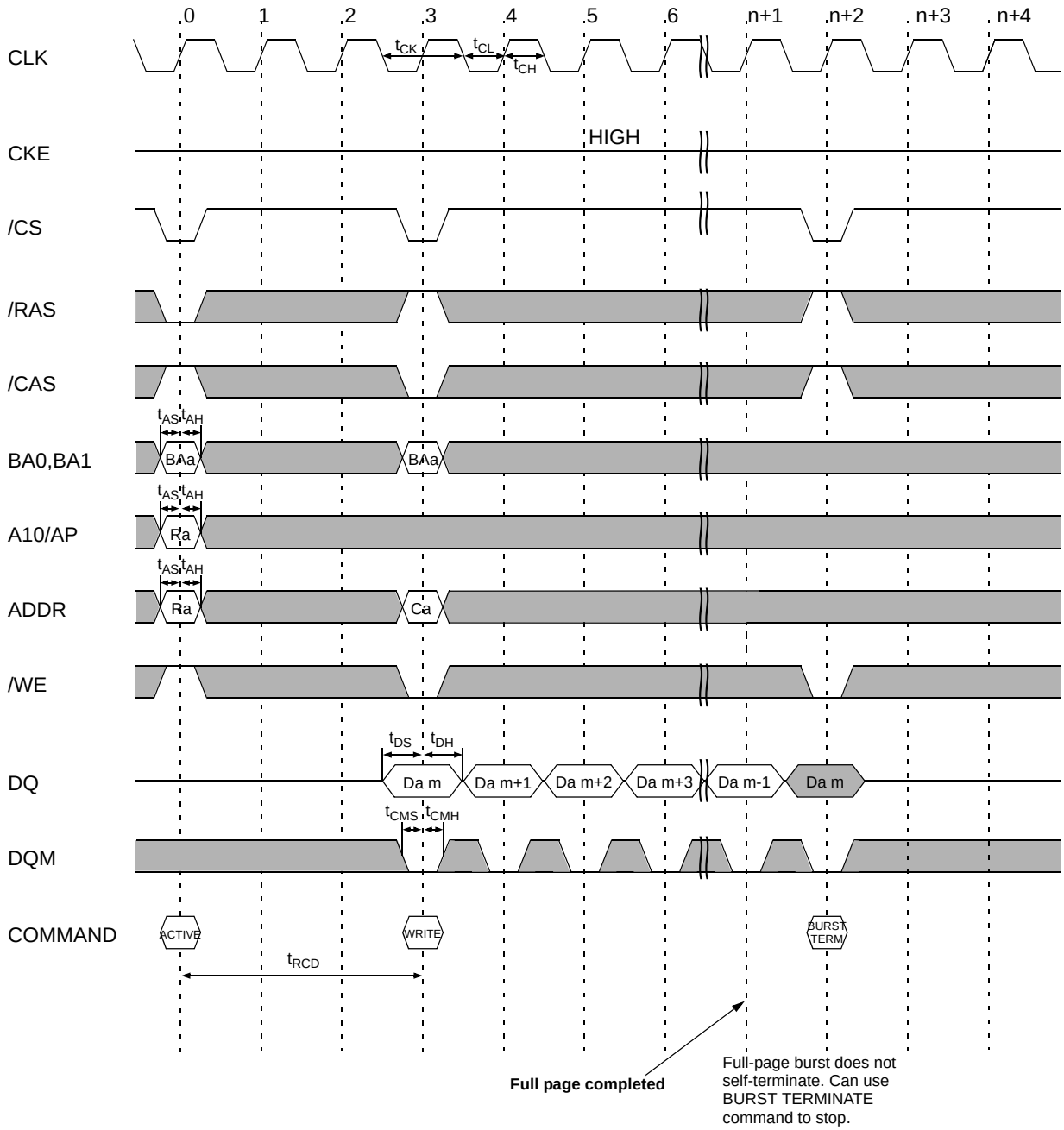
Multi Bank Interleaving WRITE (@ BL=2)



READ - Full_Page Burst



WRITE - Full_Page Burst



SDRAM FUNCTION GUIDE

EM X XX XX X X X - XX X X X

1. EMLSI Memory
2. Device Type
3. Density
4. Organization
5. Bank
6. Interface (VDD,VDDQ)
11. Temperature
10. Power
9. Speed
8. Package
7. Version

1. Memory Component

2. Device Type
- 8 ---------- Low Power SDRAM
- 9 ---------- SDRAM
- D ---------- Mobile DDR

3. Density
- 32 ---------- 32M
- 64 ---------- 64M
- 28 ---------- 128M
- 56 ---------- 256M
- 12 ---------- 512M
- 1G ---------- 1G

4. Organization
- 04 ---------- x4 bit
- 08 ---------- x8 bit
- 16 ---------- x16 bit
- 32 ---------- x32 bit

5. Bank
- 2 ---------- 2 Bank
- 4 ---------- 4 Bank

6. Interface (VDD,VDDQ)
- V ---------- LVTTL (3.3V,3.3V)
- H---------- LVTTL (3.3V,2.5V)
- K ---------- LVTTL (3.0V,3.0V)
- X ---------- LVTTL (3.0V,2.5V)
- U ---------- P-LVTTL (3.0V,1.8V)
- S ---------- LVCMOS (2.5V,2.5V)
- R ---------- LVCMOS (2.5V,1.8V)
- P ---------- LVCMOS (1.8V,1.8V)

7. Version
- Blank ---------- 1st generation
- A ----------2nd generation
- B ---------- 3rd generation
- C ---------- 4th generation
- D ---------- 5th generation

8. Package
- Blank ---------- KGD
- U ----------44 TSOP2
- P ---------- 48 FpBGA
- Z ---------- 52 FpBGA
- Y ---------- 54 FpBGA
- V ---------- 90 FpBGA

9. Speed
- 60 ---------- 6.0ns (166MHz CL=3)
- 70 ---------- 7.0ns (143MHz CL=3)
- 75 ---------- 7.5ns (133MHz CL=3)
- 7C ---------- 7.5ns (133MHz CL=2)
- 80 ---------- 8.0ns (125MHz CL=3)
- 8C ---------- 8.0ns (125MHz CL=2)
- 90 ---------- 9.0ns (111MHz CL=3)
- 10 ---------- 10.0ns (100MHz CL=3)
- 1C ---------- 10.0ns (100MHz CL=2)
- 12 ---------- 12.0ns (83MHz CL=2)
- 1L ---------- 25.0ns (40MHz CL=1)

10. Power
- U ---------- Low Low Power
- L ---------- Low Power
- S ---------- Standard Power

11. Temperature
- C ---------- Commercial (0'C ~ 70'C)
- E ---------- Extended (-25'C ~ 85'C)
- I ---------- Industrial (-40'C ~ 85'C)