

Silicon NPN Power Transistors

2SC3272

DESCRIPTION

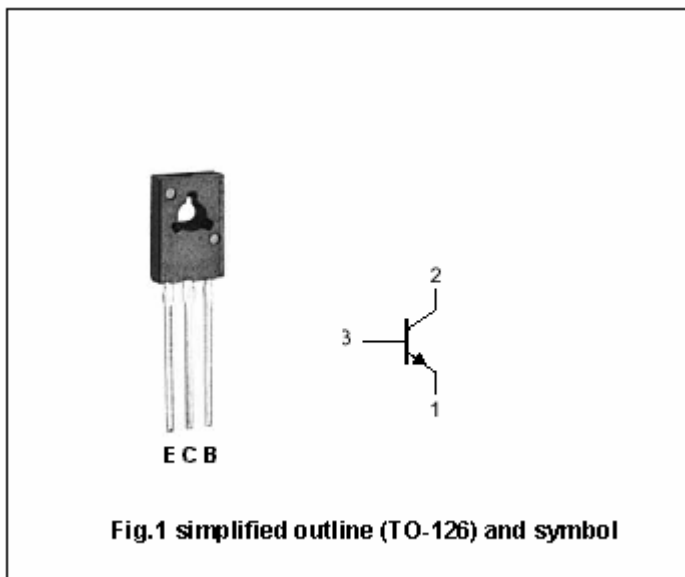
- With TO-126 package
- High breakdown voltage

APPLICATIONS

- For power amplification

PINNING □see Fig.2□

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base



Absolute maximum ratings (Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	300	V
V_{CEO}	Collector-emitter voltage	Open base	300	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		0.1	A
I_{CM}	Collector current-peak		0.2	A
P_C	Collector power dissipation	$T_C=25□$	10	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEsat}	Collector-emitter saturation voltage	I _C =50mA ; I _B =5m A			2.0	V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =10μA; I _E =0	300			V
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =1mA; I _B =0	300			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =10μA; I _C =0	5			V
h _{FE}	DC current gain	I _C =10mA ; V _{CE} =10V	39		180	
I _{CBO}	Collector cut-off current	V _{CB} =200V; I _E =0			0.5	μA
I _{EBO}	Emitter cut-off current	V _{EB} =4V; I _C =0			0.5	μA
C _{OB}	Output capacitance	I _E =0; V _{CB} =30V; f=1MHz		3		pF
f _T	Transition frequency	I _C =10mA ; V _{CB} =30V	50			MHz

PACKAGE OUTLINE

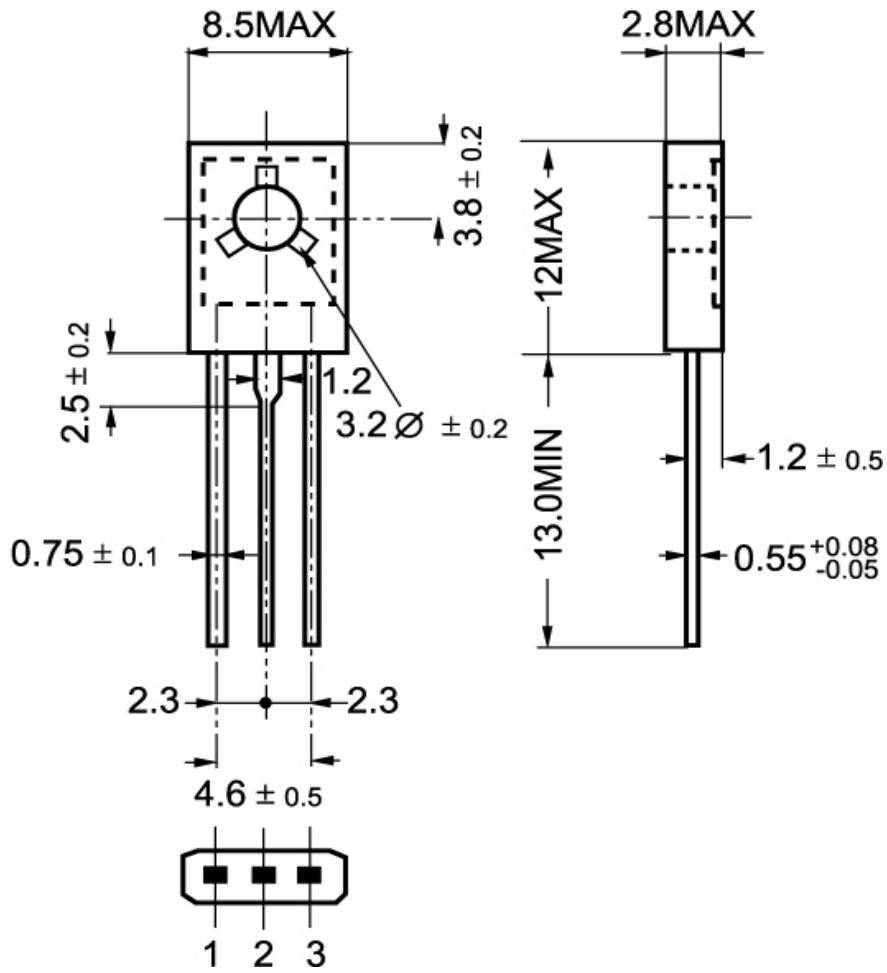


Fig.2 outline dimensions