Features

- **Single Supply for Read and Write: 2.7V to 5.5V**
- **Fast Read Access Time – 70 ns (V_{CC} = 2.7V to 3.6V); 55 ns (V_{CC} = 4.5V to 5.5V)**
- **Internal Program Control and Timer**
- **Flexible Sector Architecture**
  - **One 16K Bytes Boot Sector with Programming Lockout**
  - **Two 8K Bytes Parameter Sectors**
  - **Eight Main Memory Sectors (One 32K Bytes, Seven 64K Bytes)**
- **Fast Erase Cycle Time – 8 Seconds**
- **Byte-by-Byte Programming – 10 µs/Byte Typical**
- **Hardware Data Protection**
- **$\overline{\text{DATA}}$ Polling or Toggle Bit for End of Program Detection**
- **Low Power Dissipation**
  - **20 mA Active Current**
  - **25 µA CMOS Standby Current for V_{CC} = 2.7V to 3.6V**
  - **30 µA CMOS Standby Current for V_{CC} = 4.5V to 5.5V**
- **Minimum 100,000 Write Cycles**

4-megabit (512K x 8) Flash Memory

AT49BV040B

1. Description

The AT49BV040B is a 2.7V to 5.5V in-system reprogrammable Flash Memory. Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers an access time of 70 ns (V_{CC} = 2.7V to 3.6V) and an access time of 55 ns (V_{CC} = 4.5V to 5.5V). The power dissipation over the industrial temperature range with V_{CC} = 2.7V to 3.6V is 72 mW and is 110 mW with V_{CC} = 4.5V to 5.5V.

When the device is deselected, the CMOS standby current is less than 30 µA. To allow for simple in-system reprogrammability, the AT49BV040B does not require high input voltages for programming. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ inputs to avoid bus contention. Reprogramming the AT49BV040B is performed by erasing a sector of data and then programming on a byte by byte basis. The byte programming time is a fast 10 µs. The end of a program or erase cycle can be optionally detected by the $\overline{\text{DATA}}$ polling or toggle bit feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 100,000 cycles.

The device is erased by executing a chip erase or a sector erase command sequence; the device internally controls the erase operations. The memory array of the AT49BV040B is organized into two 8K byte parameter sectors, eight main memory sectors, and one boot sector.

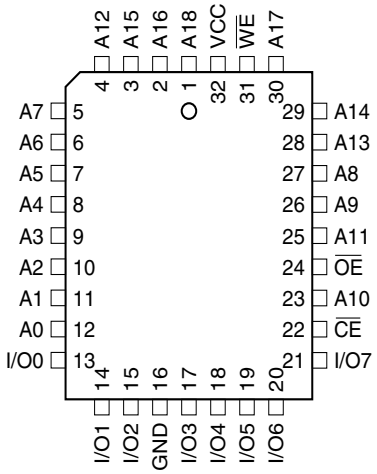
The device has the capability to protect the data in the boot sector; this feature is enabled by a command sequence. The 16K-byte boot sector includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

3499B–FLASH–4/06

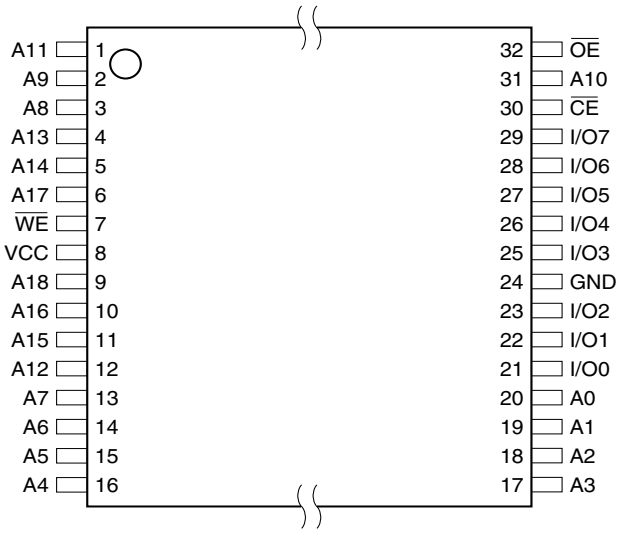
2. Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs

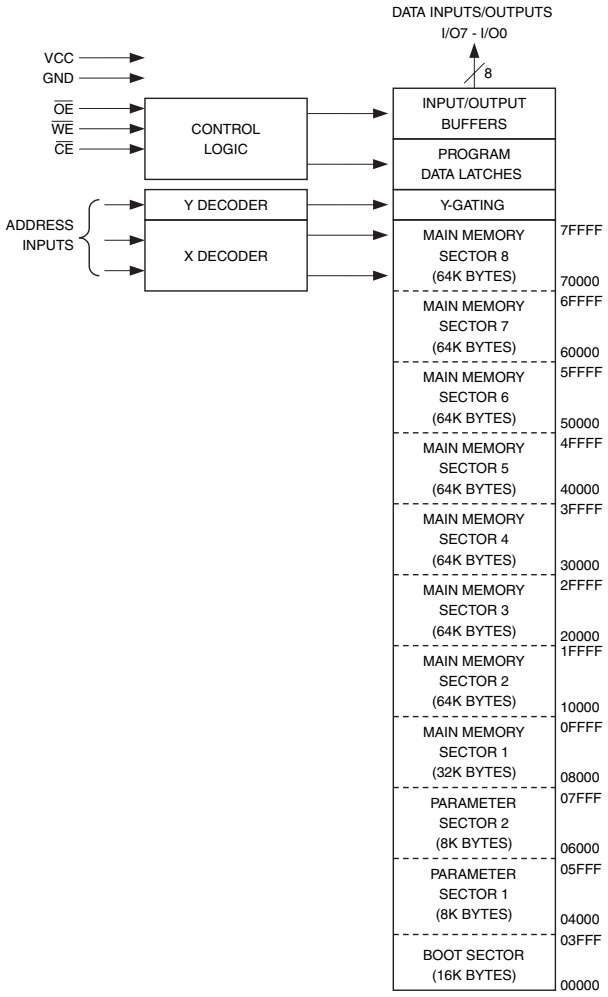
2.1 32-lead PLCC Top View



2.2 32-lead VSOP or 32-lead TSOP Top View – Type 1



3. Block Diagram



4. Device Operation

4.1 Read

The AT49BV040B is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Command Sequences

When the device is first powered on, it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table. The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

4.3 Erasure

Before a byte can be reprogrammed, it must be erased. The erased state of memory bits is a logical “1”. The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

4.3.1 Chip Erase

If the boot block lockout has been enabled, the Chip Erase function will erase Parameter Sector 1, Parameter Sector 2, Main Memory Sectors 1 - 8, but not the boot sector. If the Boot Sector Lockout has not been enabled, the Chip Erase function will erase the entire chip. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

4.3.2 Sector Erase

As an alternative to a full chip erase, the device is organized into sectors that can be individually erased. There are two 8K-byte parameter sectors and eight main memory sectors. The 8K-byte parameter sectors and the eight main memory sectors can be independently erased and reprogrammed. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion.

4.4 Byte Programming

Once the memory array is erased, the device is programmed (to a logical “0”) on a byte-by-byte basis. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is accomplished via the internal device command register and is a 4-bus cycle operation (see “Command Definition Table” on page 7). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling or toggle bit feature may also be used to indicate the end of a program cycle.

4.5 Boot Sector Programming Lockout

The device has one designated sector that has a programming lockout feature. This feature prevents programming of data in the designated sector once the feature has been enabled. The size of the sector is 16K bytes. This sector, referred to as the boot sector, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot sector’s usage as a write protected region is optional to the user. The address range of the boot sector is 00000 to 03FFF.

Once the feature is enabled, the data in the boot sector can no longer be erased or programmed. Data in the main memory and parameter sectors can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. See “Command Definition Table” on page 7.

4.5.1 Boot Sector Lockout Detection

A software method is available to determine if programming of the boot sector is locked out. When the device is in the software product identification mode (see Software Product Identification Entry/Exit on page 15) a read from address location 00002H will show if programming the boot sector is locked out. If the data on I/O0 is low, the boot sector can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the sector cannot be programmed. The software product identification code should be used to return to standard operation.

4.6 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

4.7 Data Polling

The AT49BV040B features $\overline{\text{DATA}}$ polling to indicate the end of a program or erase cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle. During a chip or sector erase operation, an attempt to read the device will give a “0” on I/O7. Once the erase operation is completed, a “1” will be read from I/O7. The Data Polling status bit must be used in conjunction with the erase/program status bit as shown in the algorithm in Figure 4-1 on page 6.

4.8 Toggle Bit

In addition to $\overline{\text{DATA}}$ polling, the AT49BV040B provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. The toggle bit status bit should be used in conjunction with the erase/program status bit shown in the algorithm in Figure 4-2 on page 6.

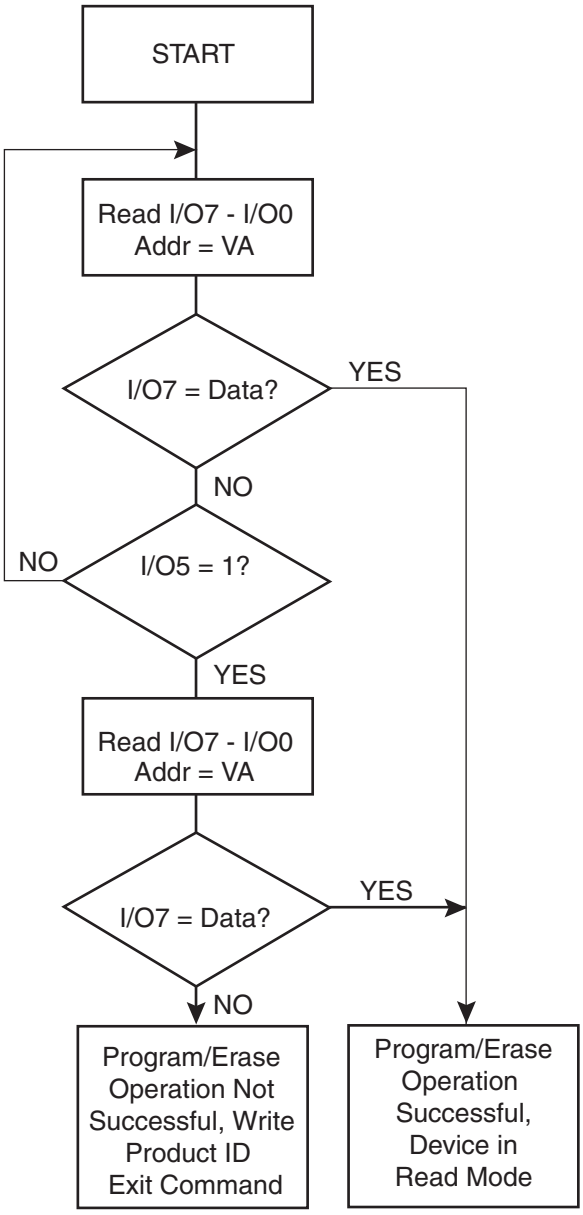
4.9 Erase/Program Status Bit

The device offers a status bit on I/O5, which indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a “1”, the device is unable to verify that an erase or a byte program operation has been successfully performed. If a program (Sector Erase) command is issued to the boot sector and the boot sector programming lockout feature is enabled, the boot sector will not be programmed (erased), and the device will go into the read mode. Once the erase/program status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. The erase/program status bit is a “0” while the erase or program operation is still in progress.

4.10 Hardware Data Protection

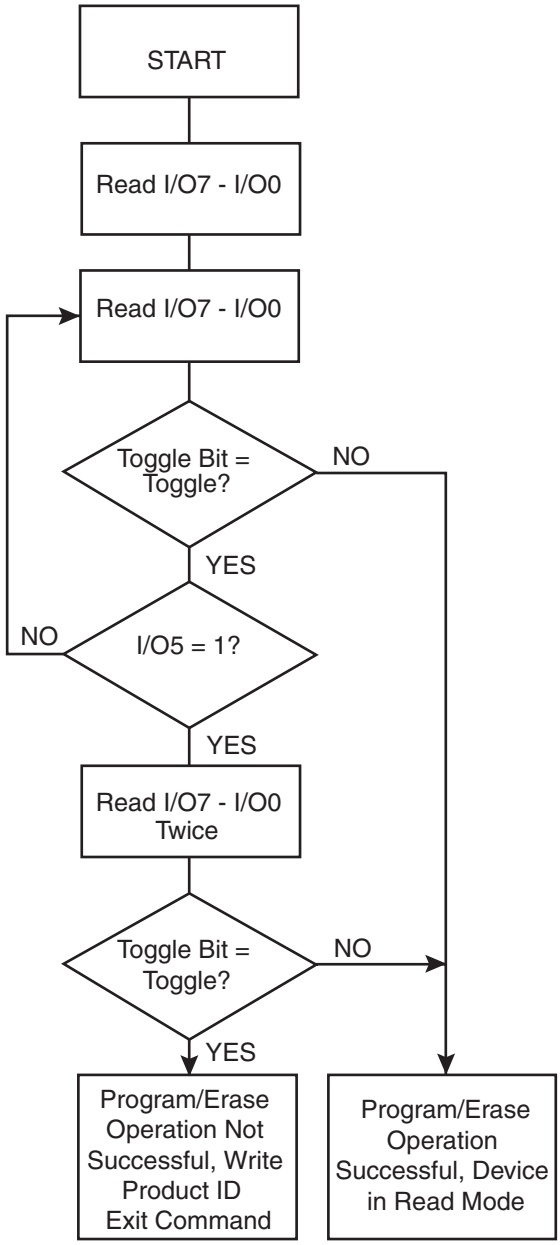
Hardware features protect against inadvertent programs to the AT49BV040B in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

Figure 4-1. $\overline{\text{Data}}$ Polling Algorithm



Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 4-2. Toggle Bit Algorithm



Note:
1. The system should recheck the toggle bit even if I/O5 = "1" because the toggle bit may stop toggling as I/O5 changes to "1".

5. Command Definition Table

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA(2)	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA(5)	30
Byte Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Boot Sector Lockout(3)	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	40
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit(4)	3	555	AA	AAA	55	555	F0						
Product ID Exit(4)	1	XXX	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O7 - I/O0 (Hex). The address format in each bus cycle is as follows: A11 - A0 (Hex); A11 - A18 (don't care).
2. Since A11 is don't care, AAA can be replaced with 2AA.
3. The 16K byte boot sector has the address range 00000H to 03FFFH.
4. Either one of the Product ID Exit commands can be used.
5. SA = sector addresses:
   SA = 00000 to 03FFF for BOOT SECTOR
   SA = 04000 to 05FFF for PARAMETER SECTOR 1
   SA = 06000 to 07FFF for PARAMETER SECTOR 2
   SA = 08000 to FFFF for MAIN MEMORY ARRAY SECTOR 1
   SA = 10000 to 1FFFF for MAIN MEMORY ARRAY SECTOR 2
   SA = 20000 to 2FFFF for MAIN MEMORY ARRAY SECTOR 3
   SA = 30000 to 3FFFF for MAIN MEMORY ARRAY SECTOR 4
   SA = 40000 to 4FFFF for MAIN MEMORY ARRAY SECTOR 5
   SA = 50000 to 5FFFF for MAIN MEMORY ARRAY SECTOR 6
   SA = 60000 to 6FFFF for MAIN MEMORY ARRAY SECTOR 7
   SA = 70000 to 7FFFF for MAIN MEMORY ARRAY SECTOR 8

6. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 with Respect to Ground	-0.6V to +10.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. Sector Address Table

Sector	Sector Size	Sector Address Range
Boot Sector	16K Bytes	00000 - 03FFF
Parameter Sector 1	8K Bytes	04000 - 05FFF
Parameter Sector 2	8K Bytes	06000 - 07FFF
Main Memory Sector 1	32K Bytes	08000 - 0FFFF
Main Memory Sector 2	64K Bytes	10000 - 1FFFF
Main Memory Sector 3	64K Bytes	20000 - 2FFFF
Main Memory Sector 4	64K Bytes	30000 - 3FFFF
Main Memory Sector 5	64K Bytes	40000 - 4FFFF
Main Memory Sector 6	64K Bytes	50000 - 5FFFF
Main Memory Sector 7	64K Bytes	60000 - 6FFFF
Main Memory Sector 8	64K Bytes	70000 - 7FFFF

8. DC and AC Operating Range

		AT49BV040B
Operating Temperature (Case)	Ind.	-40°C - 85°C
V_{CC} Power Supply		2.7V - 3.6V or 4.5V to 5.5V

9. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H,[3], A0 = V_{IL}	Manufacturer Code[4]
				A1 - A18 = V_{IL}, A9 = V_H,[3], A0 = V_{IH}	Device Code[4]
Software[5]				A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code[4]
				A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 9.5V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 13H. Additional Device Code: 10H is read from address 0003H.
5. See details under Software Product Identification Entry/Exit on page 15.

10. DC Characteristics

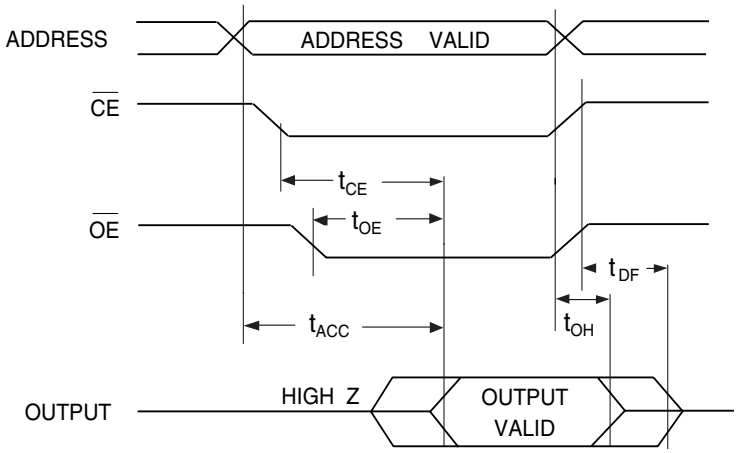
Symbol	Parameter	Condition	V_{CC} = 2.7V to 3.6V			V_{CC} = 4.5V to 5.5V			Units
			Min	Typ	Max	Min	Typ	Max	
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		15	25		25	30	µA
I_{CC}[1]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		15	20		15	20	mA
V_{IL}	Input Low Voltage				0.1 V_{CC}			0.1 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}			0.7 V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4			2.4			V

Note: 1. In the erase mode, I_{CC} is 15 mA.

11. AC Read Characteristics

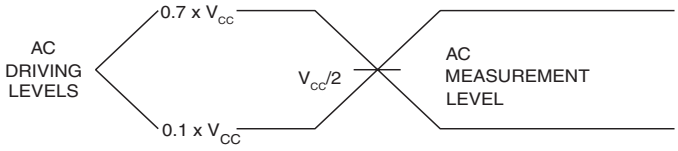
Symbol	Parameter	2.7V to 3.6V		4.5V to 5.5V		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		55	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70		55	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	35	0	15	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

12. AC Read Waveforms [1][2][3][4]



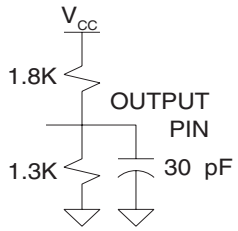
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

13. Input Test Waveform and Measurement Level



t_R, t_F < 5 ns

14. Output Load Test



15. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

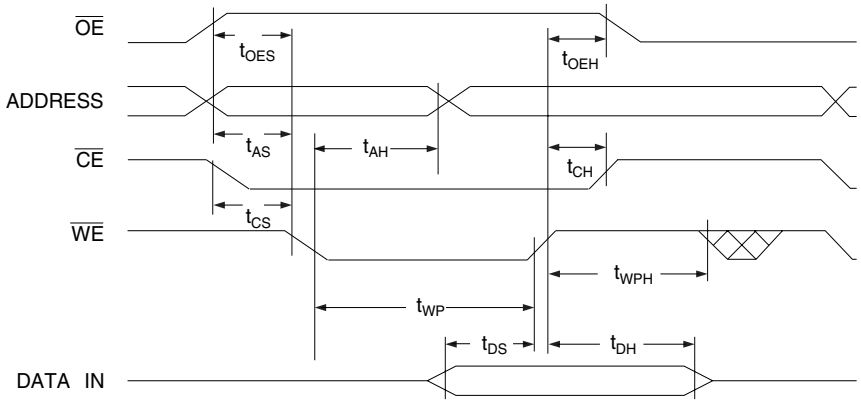
Note: 1. This parameter is characterized and is not 100% tested.

16. AC Byte Load Characteristics

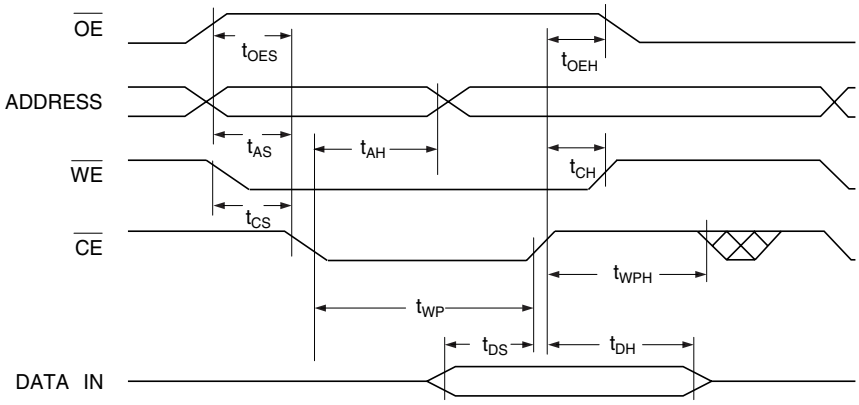
Symbol	Parameter	2.7V to 3.6V		4.5V to 5.5V		Units
		Min	Max	Min	Max	
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		0		ns
t_{AH}	Address Hold Time	20		20		ns
t_{CS}	Chip Select Set-up Time	0		0		ns
t_{CH}	Chip Select Hold Time	0		0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	30		20		ns
t_{DS}	Data Set-up Time	20		20		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		0		ns
t_{WPH}	Write Pulse Width High	20		20		ns

17. AC Byte Load Waveforms

17.1 $\overline{WE}$ Controlled



17.2 $\overline{CE}$ Controlled

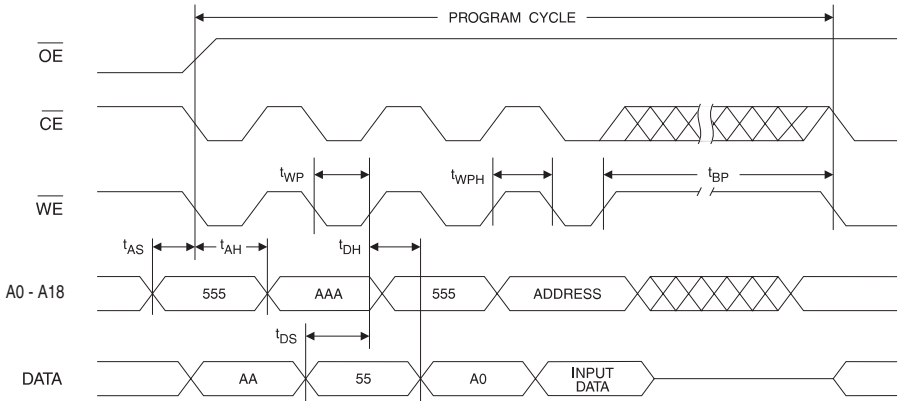


18. Program Cycle Characteristics

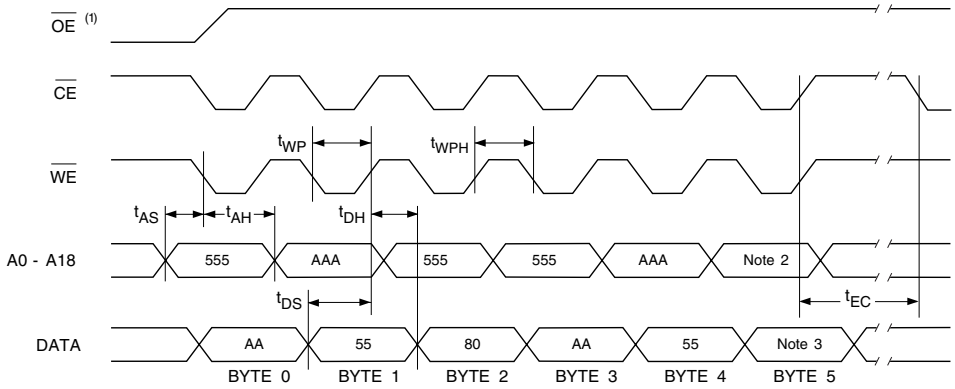
Symbol	Parameter	2.7V to 3.6V and 4.5V to 5.5V			Units
		Min	Typ	Max	
t_{BP}	Byte Programming Time		10	120	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	20			ns
t_{DS}	Data Set-up Time	20			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	30[1]			ns
t_{WPH}	Write Pulse Width High	20			ns
t_{EC}	Chip Erase Cycle Time		8		seconds
t_{SEC}	Main Sector Erase Cycle Time		900		ms

Note: 1. 20 ns for V_{CC} = 4.5V to 5.5V.

19. Program Cycle Waveforms



20. Sector or Chip Erase Cycle Waveforms



Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

2. For chip erase, the address should be 555. For sector erase the address depends on what sector is to be erased. (See note 5 under "Command Definition Table" on page 7.)

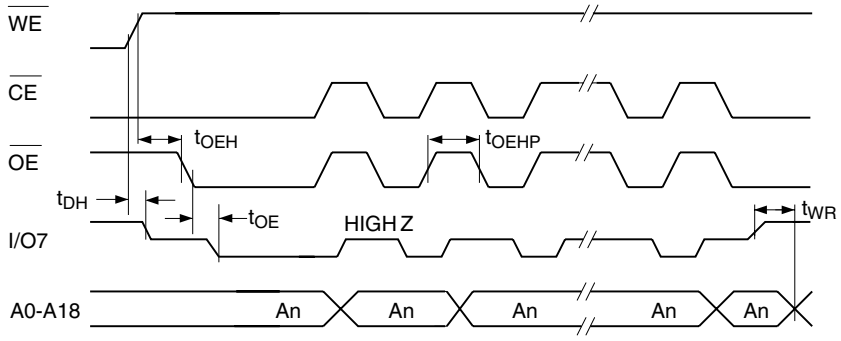
3. For chip erase, the data should be 10H. For sector erase, the data should be 30H.

21. $\overline{\text{Data}}$ Polling Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

22. $\overline{\text{Data}}$ Polling Waveforms

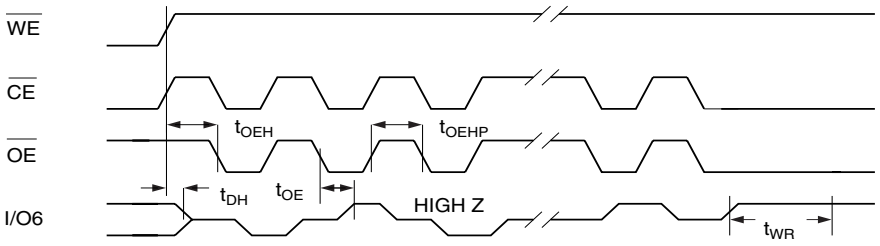


23. Toggle Bit Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

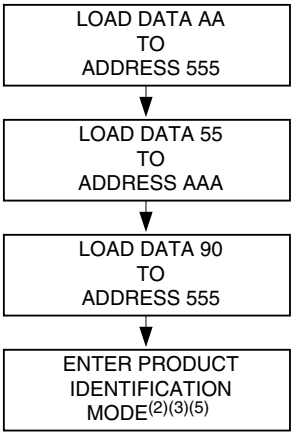
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

24. Toggle Bit Waveforms(1)(2)(3)

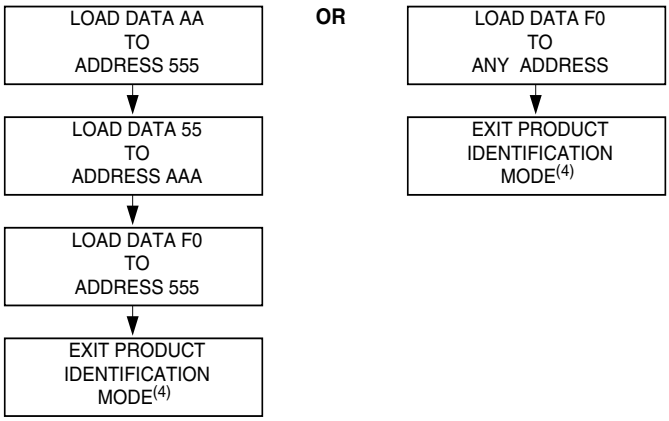


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

25. Software Product Identification Entry[1]

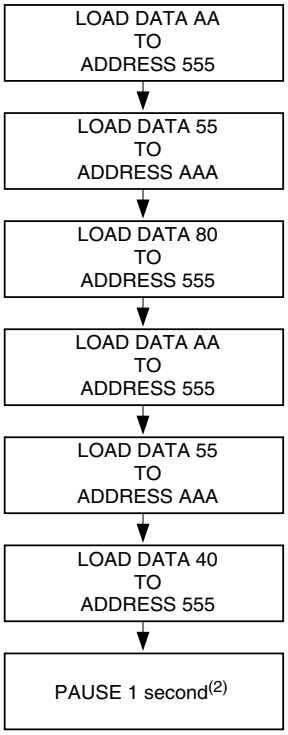


26. Software Product Identification Exit[1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A11 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
   Additional Device Code is read for address 0003H
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 13H.
   Additional Device Code: 10H.

27. Boot Block Lockout Feature Enable Algorithm[1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A11 - A0 (Hex).
2. Boot block lockout feature enabled.

28. Ordering Information

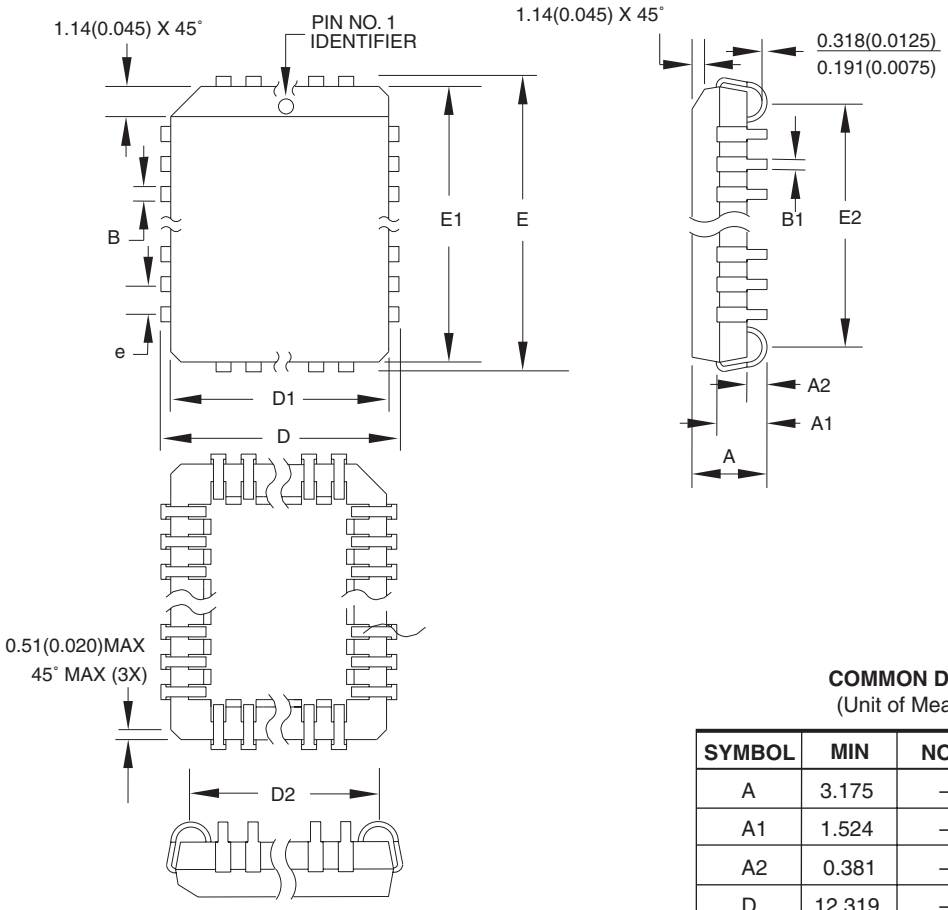
28.1 Green Package (Pb/Halide-free)

I_{CC} (mA) Active	Ordering Code	Package	Operation Range
20	AT49BV040B-JU AT49BV040B-TU AT49BV040B-VU	32J 32T 32V	Industrial (-40° to 85° C)

Package Type	
32J	32-lead, Plastic, J-leaded Chip Carrier Package (PLCC)
32T	32-lead, Thin Small Outline Package (TSOP)
32V	32-lead, Thin Small Outline Package (VSOP)

29. Packaging Information

29.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

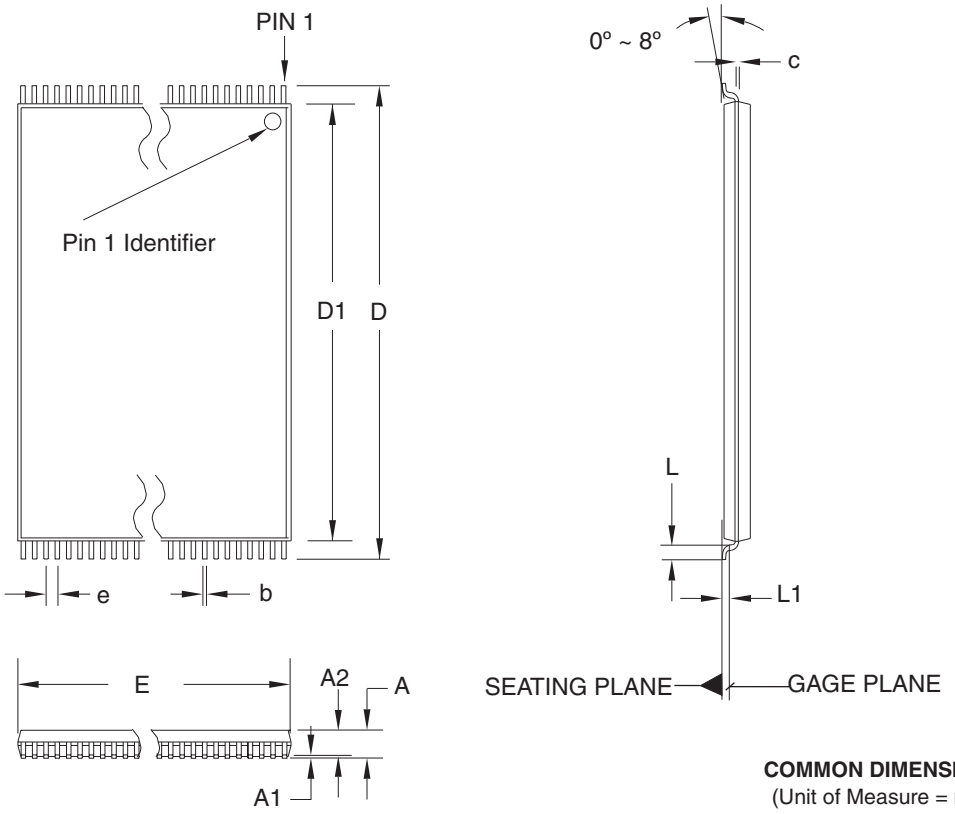
SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

29.2 32T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

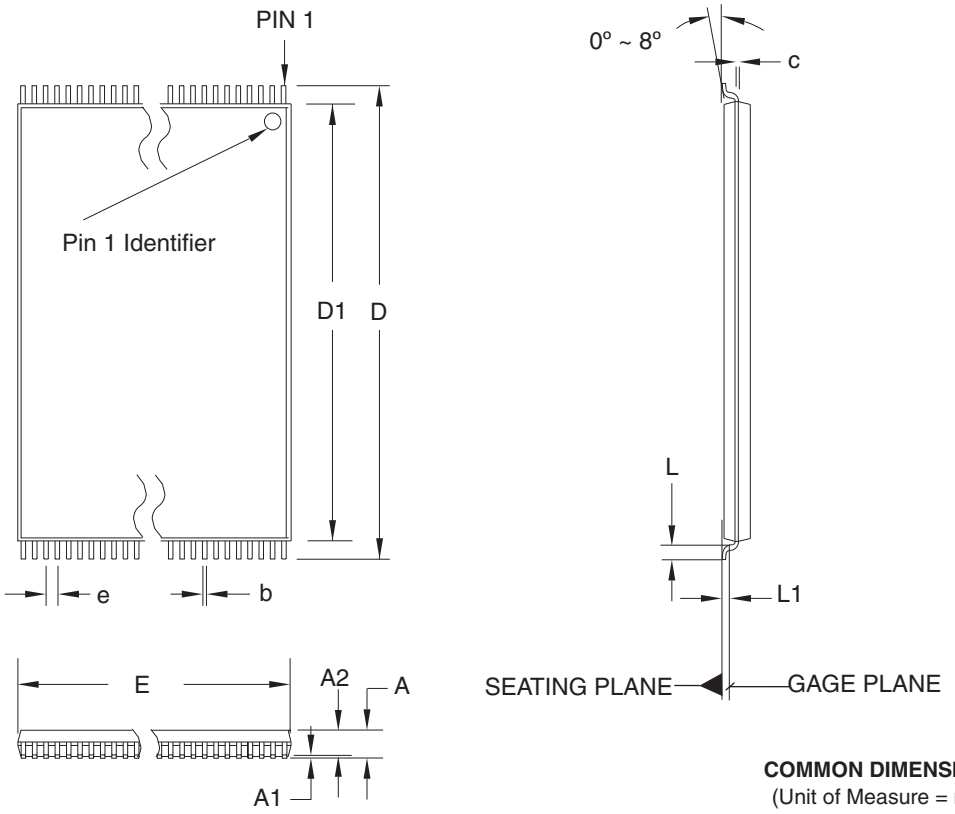
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	32T	B

29.3 32V – VSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	13.80	14.00	14.20	
D1	12.30	12.40	12.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BA.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32V**, 32-lead (8 x 14 mm Package) Plastic Thin Small Outline Package, Type I (VSOP)	32V	B

30. Revision History

Revision No.	History
Revision A – Sept. 2005	• Initial Release
Revision B – April 2006	• Combined the 3V and 5V part into one datasheet (BV). • Removed the speed of the part form the ordering information table. • Changed the address hold time to 20 ns.

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