

3-Pin μ P Voltage Supervisor

FEATURES

- Ultra Low Supply Current 1 μ A(typ.)
- Guaranteed Reset Valid to VCC=0.9V
- Available in three Output Types: Open Drain Active Low (PCS809N), Push-Pull Active Low (PCS809), Push-Pull Active High (PCS810)
- 140ms Min. Power-On Reset Pulse Width
- Internally Fixed Threshold 2.3V, 2.6V, 2.9V, 3.1V, 4.0V, 4.4V, and 4.6V
- Tight Voltage Threshold Tolerance: 1.5%
- Low profile Package: SOT-23-3

APPLICATIONS

- Notebook Computers
- Digital Still Cameras
- PDAs
- Critical Microprocessor Monitoring

| RESET THRESHOLD | |
|-----------------|------------|
| Suffix | Voltage(V) |
| L | 4.6 |
| M | 4.4 |
| J | 4.0 |
| T | 3.1 |
| S | 2.9 |
| R | 2.6 |
| P | 2.3 |

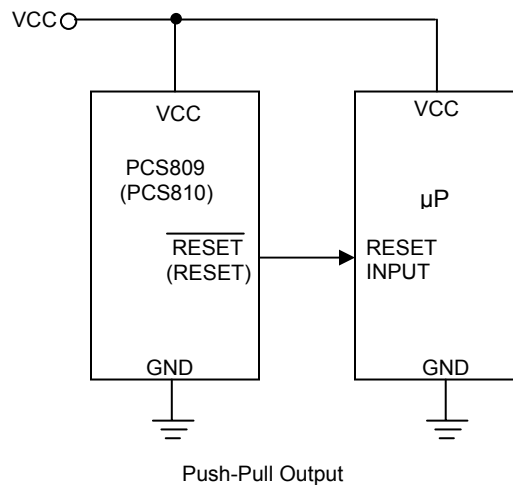
DESCRIPTION

PCS809/PCS810 are low-power microprocessor (μ P) supervisory circuits used to monitor power supplies in μ P and digital systems. They provide applications with benefits of circuit reliability and low cost by eliminating external components.

These devices perform as valid singles in applications with VCC ranging from 6.0V down to 0.9V. The reset signal lasts for a minimum period of 140ms whenever VCC supply voltage falls below preset threshold. Both PCS809 and PCS810 were designed with a reset comparator to help identify invalid signals, which last less than 140ms. The only difference between them is that they have an active-low RESET output and active-high RESET output, respectively.

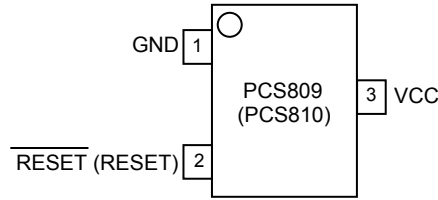
Low supply current (1 μ A) makes PCS809/PCS810 ideal for portable equipment. The devices are available in 3-SOT-23 package

Typical Operating Circuit



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Pin Diagram

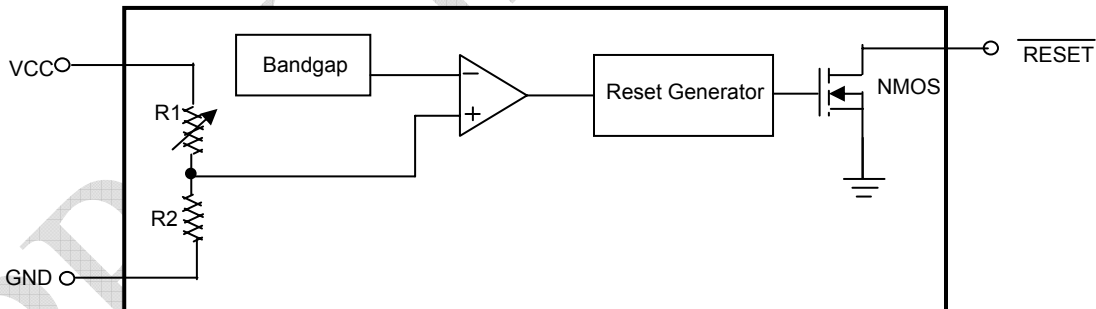


Pin Description

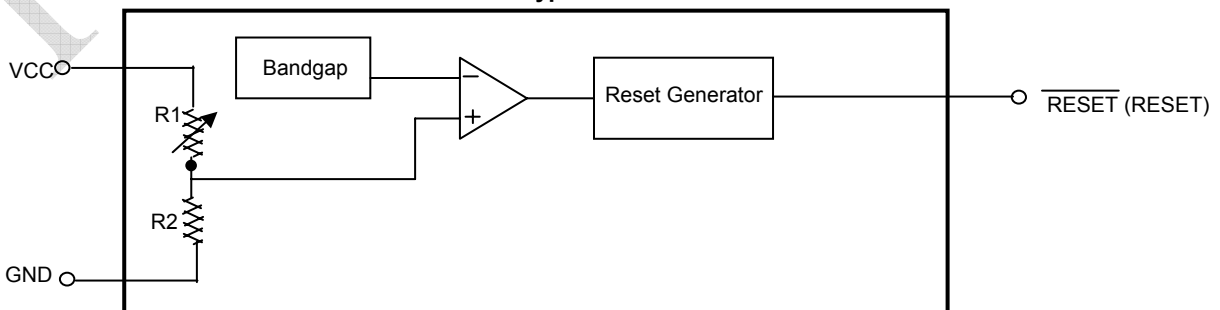
| Pin# | | Pin Name | Description |
|--------|--------|---------------------------|--|
| PCS809 | PCS810 | | |
| 1 | 1 | GND | Ground. |
| 2 | - | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ is asserted LOW if V_{CC} falls below V_{TH} . $\overline{\text{RESET}}$ remains LOW for atleast 140ms (T_{RST}) once V_{CC} exceeds the Threshold. In addition, $\overline{\text{RESET}}$ is active LOW |
| - | 2 | RESET | RESET is asserted HIGH if V_{CC} falls below V_{TH} . RESET remains HIGH for atleast 140ms (T_{RST}) once V_{CC} exceeds the threshold. In addition, RESET is active HIGH |
| 3 | 3 | VCC | Power supply input voltage (3.0V, 3.3V, 5.0V) |

Block Diagrams

N-ch Open-Drain Type



Push-Pull Type



Detailed Description

RESET OUTPUT

μ P will be activated at a valid reset state. These μ P supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

$\overline{\text{RESET}}$ is guaranteed to be a logic low for $V_{\text{TH}} > V_{\text{CC}} > 0.9\text{V}$. Once VCC exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the reset timeout period; after this interval, $\overline{\text{RESET}}$ goes high.

If a brownout condition occurs (VCC drops below the reset threshold), $\overline{\text{RESET}}$ goes low. Any time VCC goes below the reset threshold, the internal timer resets to zero, and $\overline{\text{RESET}}$ goes low. The internal timer is activated after VCC

returns above the reset threshold, and $\overline{\text{RESET}}$ remains low for the reset timeout period.

BENEFITS OF HIGHLY ACCURATE RESET THRESHOLD

PCS809/810 with specified voltage as $5\text{V} \pm 10\%$ or $3\text{V} \pm 10\%$ are ideal for systems using a $5\text{V} \pm 5\%$ or $3\text{V} \pm 5\%$ power supply. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range of the system ICs. The pre-trimmed thresholds are reducing the range over which an undesirable reset may occur.

Application Information

NEGATIVE-GOING VCC TRANSIENTS

In addition to issuing a reset to the μ P during power-up, power-down, and brownout conditions, PCS809 series are relatively resistant to short-duration negative-going VCC transient.

ENSURING A VALID RESET OUTPUT DOWN TO VCC=0

When VCC falls below 0.9V, PCS809 $\overline{\text{RESET}}$ output no longer sinks current; it becomes an open circuit. In this case, high-impedance CMOS logic inputs connecting to $\overline{\text{RESET}}$ can drift to undetermined voltages. Therefore, PCS809/810 with CMOS is perfect for most applications of

VCC below 0.9V. However in applications where $\overline{\text{RESET}}$ must be valid down to 0V, adding a pull-down resistor to $\overline{\text{RESET}}$ causes any leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low.

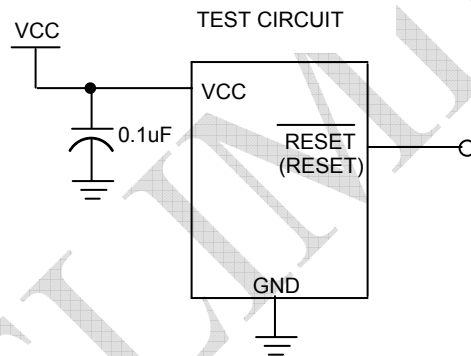
INTERFACING TO μ P WITH BIDIRECTIONAL RESET PINS

The $\overline{\text{RESET}}$ output on the PCS809 is open drain, this device interfaces easily with μ Ps that have bidirectional reset pins. Connecting the μ P supervisor's $\overline{\text{RESET}}$ output directly to the microcontroller's $\overline{\text{RESET}}$ pin with a single pull-up resistor allows either device to assert reset.

Absolute Maximum Rating

| Parameter | Min | Max | Unit |
|--|-----|----------------------|------|
| VCC | 0.3 | 6.5 | V |
| RESET, $\overline{\text{RESET}}$ | 0.3 | V _{CC} +0.3 | V |
| Input Current (VCC) | | 20 | mA |
| Output Current (RESET or $\overline{\text{RESET}}$) | | 20 | mA |
| Continuous Power Dissipation (T _A =+70°C) | | 320 | mW |
| Operating Junction Temperature Range | -40 | +85 | °C |
| Junction Temperature | | 125 | °C |
| Storage Temperature Range | -65 | 150 | °C |
| Lead Temperature (Soldering) 10 sec | | 260 | °C |

Test Circuit



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Electrical Characteristics:

(Typical values are at $T_A=+25^\circ\text{C}$ unless otherwise specified.) (Note1)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit | |
|-----------------------------|-----------------|---|--------------------------------|-------|--------|-------|----|
| Operating Voltage | VCC | | 0.9 | | 6 | V | |
| Supply Current | I _{CC} | VCC= V _{TH} +0.1V | | 1 | 3 | μA | |
| RESET threshold | V _{TH} | P device | T _A =+25°C | 2.265 | 2.3 | 2.335 | V |
| | | | T _A =-40°C to +85°C | 2.254 | | 2.346 | |
| | | R device | T _A =+25°C | 2.561 | 2.6 | 2.639 | |
| | | | T _A =-40°C to +85°C | 2.548 | | 2.652 | |
| | | S device | T _A =+25°C | 2.857 | 2.9 | 2.944 | |
| | | | T _A =-40°C to +85°C | 2.842 | | 2.958 | |
| | | T device | T _A =+25°C | 3.054 | 3.1 | 3.147 | |
| | | | T _A =-40°C to +85°C | 3.038 | | 3.162 | |
| | | J device | T _A =+25°C | 3.940 | 4.0 | 4.060 | |
| | | | T _A =-40°C to +85°C | 3.920 | | 4.080 | |
| | | M device | T _A =+25°C | 4.334 | 4.4 | 4.466 | |
| | | | T _A =-40°C to +85°C | 4.312 | | 4.488 | |
| | | L device | T _A =+25°C | 4.531 | 4.6 | 4.669 | |
| | | | T _A =-40°C to +85°C | 4.508 | | 4.692 | |
| VCC to Reset Delay | T _{RD} | VCC=V _{TH} to (V _{TH} -0.1V), V _{TH} =3.1V | | 20 | | μS | |
| Reset Active Timeout Period | T _{RP} | VCC=V _{TH} (MAX) | T _A =+25°C | 140 | 230 | 560 | mS |
| | | | T _A =-40°C to +85°C | 100 | | 1030 | |
| RESET output Voltage | V _{OH} | VCC = V _{TH} +0.1V, I _{SOURCE} =1mA | 0.8VCC | | | V | |
| | V _{OL} | VCC = V _{TH} -0.1V, I _{SINK} =1mA | | | 0.2VCC | | |
| RESET output Voltage | V _{OH} | VCC = V _{TH} +0.1V, I _{SOURCE} =1mA | 0.8VCC | | | | |
| | V _{OL} | VCC = V _{TH} -0.1V, I _{SINK} =1mA | | | 0.2VCC | | |

Note1: Specifications are production tested at $T_A=25^\circ\text{C}$. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: RESET output is for PCS809: RESET output for PCS810.

Ordering Information

| Part # | Threshold Voltage | Temperature Range | Package | Top Marking |
|---------------------------|-------------------|-------------------|----------|-------------|
| PCS809 Push-Pull type | | | | |
| PCS809LIURF | 4.6 | -40°C to +85°C | 3-SOT-23 | RA46P |
| PCS809MIURF | 4.4 | -40°C to +85°C | 3-SOT-23 | RA44P |
| PCS809JIURF | 4.0 | -40°C to +85°C | 3-SOT-23 | RA40P |
| PCS809TIURF | 3.1 | -40°C to +85°C | 3-SOT-23 | RA31P |
| PCS809SIURF | 2.9 | -40°C to +85°C | 3-SOT-23 | RA29P |
| PCS809RIURF | 2.6 | -40°C to +85°C | 3-SOT-23 | RA26P |
| PCS809PIURF | 2.3 | -40°C to +85°C | 3-SOT-23 | RA23P |
| PCS809 N Open- Drain type | | | | |
| PCS809NLIURF | 4.6 | -40°C to +85°C | 3-SOT-23 | RB46P |
| PCS809NMIURF | 4.4 | -40°C to +85°C | 3-SOT-23 | RB44P |
| PCS809NJIURF | 4.0 | -40°C to +85°C | 3-SOT-23 | RB40P |
| PCS809NTIURF | 3.1 | -40°C to +85°C | 3-SOT-23 | RB31P |
| PCS809NSIURF | 2.9 | -40°C to +85°C | 3-SOT-23 | RB29P |
| PCS809NRIURF | 2.6 | -40°C to +85°C | 3-SOT-23 | RB26P |
| PCS809NPIURF | 2.3 | -40°C to +85°C | 3-SOT-23 | RB23P |
| PCS810 ACTIVE HIGH RESET | | | | |
| PCS810LIURF | 4.6 | -40°C to +85°C | 3-SOT-23 | RD46P |
| PCS810MIURF | 4.4 | -40°C to +85°C | 3-SOT-23 | RD44P |
| PCS810JIURF | 4.0 | -40°C to +85°C | 3-SOT-23 | RD40P |
| PCS810TIURF | 3.1 | -40°C to +85°C | 3-SOT-23 | RD31P |
| PCS810SIURF | 2.9 | -40°C to +85°C | 3-SOT-23 | RD29P |
| PCS810RIURF | 2.6 | -40°C to +85°C | 3-SOT-23 | RD26P |
| PCS810PIURF | 2.3 | -40°C to +85°C | 3-SOT-23 | RD23P |

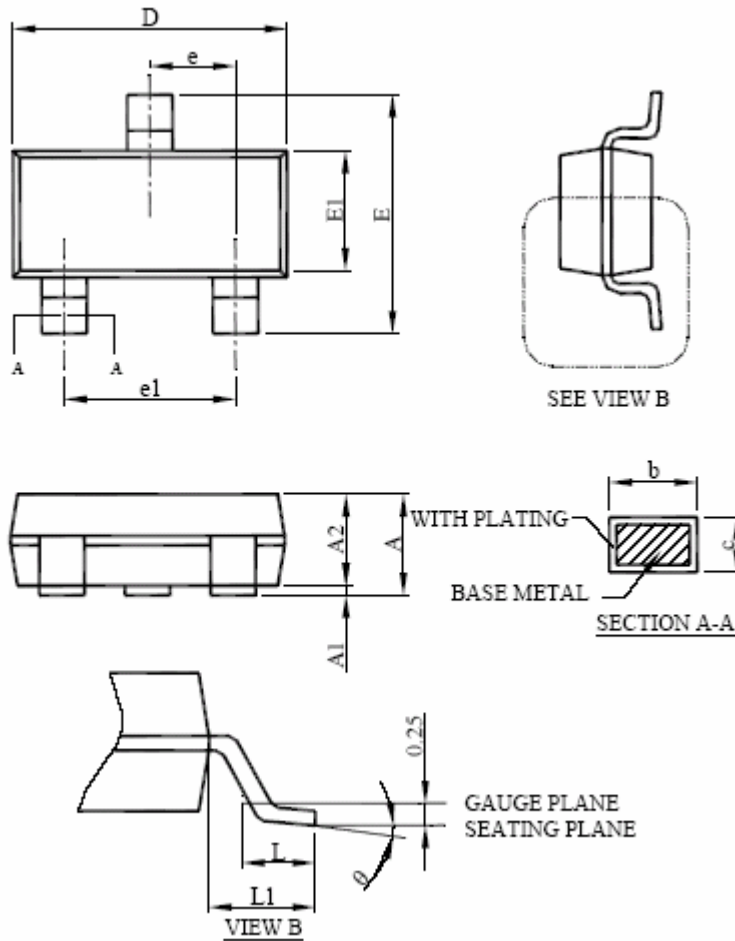
Note:

For parts to be packed in tape and reel, add "T" at the end of the part number

PulseCore Semiconductor parts are RoHS Compliant. All parts are lead free by default.

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Package Information: 3- SOT23 Package



| Symbol | Dimensions | | | |
|--------|------------|-------|-------------|------|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | 0.035 | 0.057 | 0.95 | 1.45 |
| A1 | 0.00 | 0.006 | 0.05 | 0.15 |
| A2 | 0.035 | 0.051 | 0.90 | 1.30 |
| b | 0.009 | 0.015 | 0.30 | 0.50 |
| c | 0.003 | 0.009 | 0.08 | 0.22 |
| D | 0.111 | 0.117 | 2.80 | 3.00 |
| E | 0.106 | 0.114 | 2.60 | 3.00 |
| E1 | 0.060 | 0.066 | 1.50 | 1.70 |
| L | 0.014 | 0.022 | 0.30 | 0.60 |
| L1 | 0.023 REF | | 0.60 REF | |
| e | 0.0256 BSC | | 0.95 BSC | |
| e1 | 0.0768 BSC | | 1.90 BSC | |
| theta | 0° | 8° | 0° | 8° |



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued PulseCore Semiconductor, dated 11-11-2003

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