

RoHS Compliant Product

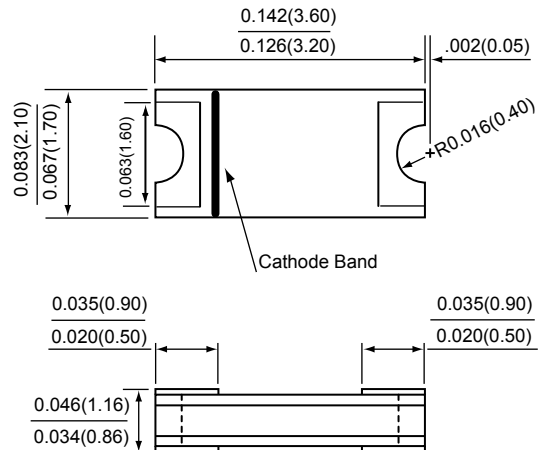
A suffix of "-C" specifies halogen & lead-free



1206

FEATURES

- * Plastic package has Underwriters Laboratory Flammability
- * Classification 94V-0
- * Low profile package
- * Built-in strain relief
- * Metal to silicon rectifier , majority carrier conduction
- * Low power loss , High efficiency
- * High current capability
- * High surge capacity
- * For using in low voltage high frequency switching power supply, inverters , free wheeling , and polarity protection applications



MECHANICAL DATA

- * Case : Packed with FRP substrate and epoxy underfilled
- * Terminals : Solder plated , solderable per MIL-STD-750, Method 2026
- * Polarity : Laser marking
- * Weight : 0.02 gram

* Dimensions in inches and (millimeters)

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Rating 25°C ambient temperature unless otherwise specified. Single phase half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.

TYPE NUMBER	SYMBOLS	SSCD204L	UNITS
Maximum DC Blocking Voltage	V_{DC}	40	V
Working Peak Reverse Voltage	V_{RMS}	40	V
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	40	V
Maximum Average Forward Rectified Current (See FIG. 1)	$I_{(AV)}$	2.0	A
Peak Forward Surge Current, 8.3 ms single half sine-wave superimposed on rated load (JEDEC method)	I_{FSM}	50	A
Maximum Instantaneous Forward Voltage at 2.0A (Note1)	V_F	0.4	V
Maximum DC Reverse Current (Note1) $T_a=25$	I_R	1.0	mA
at Rated DC Blocking Voltage $T_a=100$		10	
Typical Thermal Resistance (Note 2)	$R_{\theta JA}$	75	/ W
	$R_{\theta JL}$	17	
Operating Temperature Range	T_J	-50 ~ +125	
Storage Temperature Range	T_{STG}	-65 ~ +150	

NOTES:

1. Pulse test width PW=300 usec, 1% duty cycle.
2. Mounted on P.C. board with 0.2 x 0.2" (5.0 x 5.0mm) copper pad areas.

FIG.1 - FORWARD CURRENT DERATING CURVE

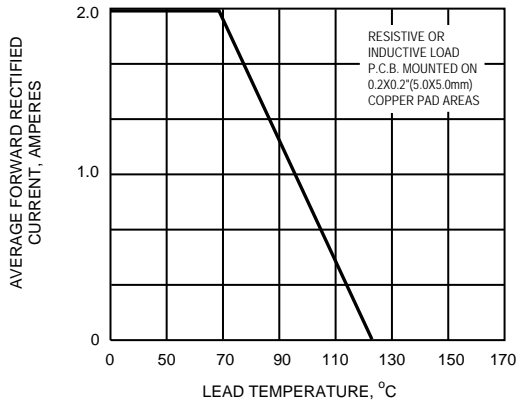


FIG.2 - MAXIMUM NON-REPETITIVE PEAK FORWARD SURGE CURRENT

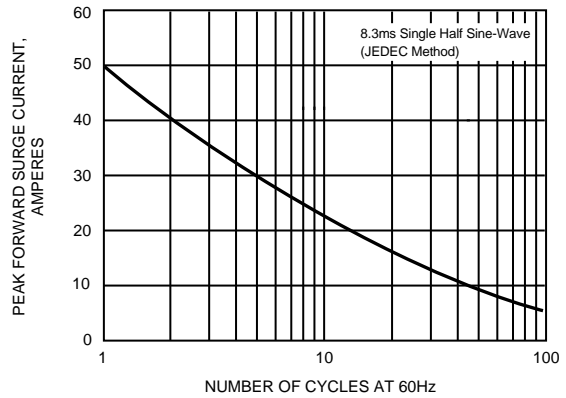


FIG.3 - TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

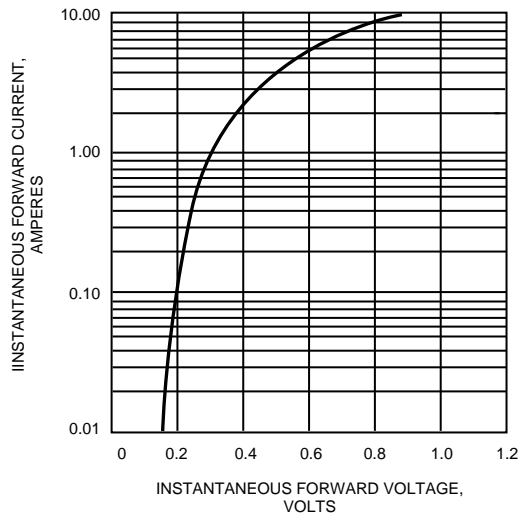


FIG.4 - TYPICAL REVERSE CHARACTERISTICS

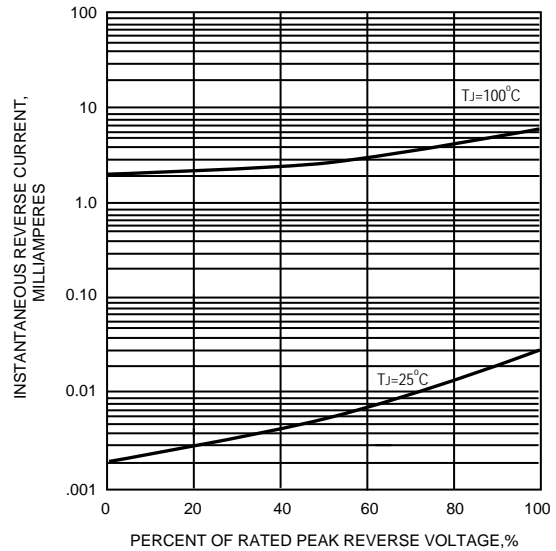


FIG.5 - TYPICAL JUNCTION CAPACITANCE

