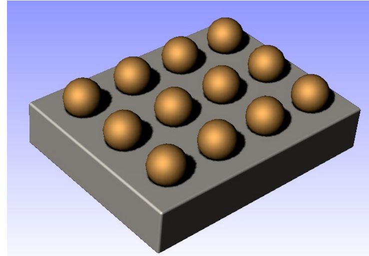
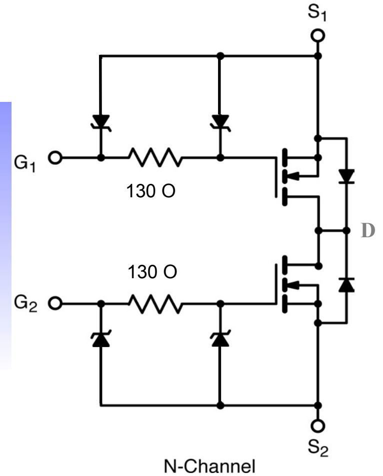
Battery Protection MicroSURF™

TS8314 – Bi-directional N-Channel 2.5V Specified MicroSURF™

General Description

Taiwan Semiconductor's new low cost, state of the art MicroSURF™ lateral MOSFET process technology in chipscale bondwireless packaging minimizes PCB space and $R_{DS(ON)}$ plus provides an ultra-low Qg X $R_{DS(ON)}$ figure of merit.



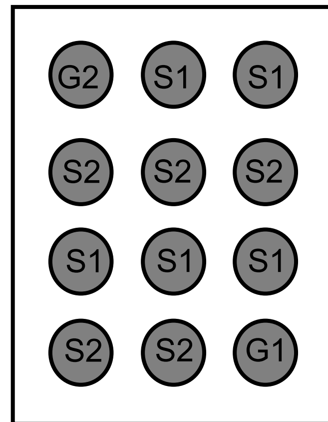


Features

- 6.5A, 20V $R_{DS1(ON)}$ equivalent = 15mΩ at 4.5 Volts
- 5.5A, 20V $R_{DS1(ON)}$ equivalent = 22mΩ at 2.5 Volts
- Low profile package: less than 0.8mm height when mounted on PCB.
- Occupies less than 1/5 the area of TSSOP-8.
- Excellent thermal characteristics.
- Integrated gate diodes provide ElectroStatic Discharge (ESD) protection of 4000V Human Body Model (HBM).
- Lead free solder bumps available.

MicroSURF™ for Battery Protection

Patent Pending



Bottom: Bump Side

Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{S1S2}	Source1-Source2 Voltage	20	V
V_{GS}	Gate-Source Voltage	+12 / -0.5	V
I_{S1S2}	Source1-Source2 Current – Continuous	6.5	A
	– Pulsed	13	
P_D	Power Dissipation (Steady State)	1.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	ºC

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	82	°C/W
$R_{\theta JR}$	Thermal Resistance, Junction-to-Balls	7	

Electrical Characteristics

Electrical Characteristics

T_A=25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{(BD)S\,IS2S}$	Source-to-Source Breakdown Voltage	V_{GS}=0V, I_S=250µA	20			V
$I_{S\,IS2S}$	Zero Gate Voltage Source Current	$V_{S\,IS2}$=20V, V_{GS}=0V, T=150°C			50	µA
I_{GSS}	Gate-Body Leakage	V_{GS}=7V, $V_{S\,IS2}$=0V			100	nA
I_{GSS}	Gate-Body Leakage	V_{GS}=12V, $V_{S\,IS2}$=0V			10	mA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{S\,IS2}$=V_{GS}, I_S=250µA		0.8	1.2	V
$r_{S\,IS2(on)}$	Source-to-Source On-State Resistance	V_{GS}=4.5V, I_S=6.5A		26	30	mΩ
	Source-to-Source On-State Resistance	V_{GS}=2.5V, I_S=5.5A		38	44	mΩ
$r_{DS\,I(on)}$ equivalent	Source-to-Source On-State Resistance	V_{GS}=4.5V, I_S=6.5A		13	15	mΩ
	Drain-to-Source On-State Resistance	V_{GS}=2.5V, I_S=5.5A		19	22	mΩ
C_{iss}	Input Capacitance	$V_{S\,IS2}$=20V, V_G=0V, F=1MHZ		1100		pF
C_{oss}	Output Capacitance	$V_{S\,IS2}$=20V, V_G=0V, F=1MHZ		400		pF
C_{rss}	Reverse Transfer Capacitance	$V_{S\,IS2}$=20V, V_G=0V, F=1MHZ		300		pF
Q_g	Total Gate Charge	V_{GS}=5V, I_S=8A, $V_{S\,IS2}$=10V		15		nC
t_{rr}	Source-Drain Reverse Recovery Time	I_S=1A, V_{GS}=0V, di/dt=100A/µs		40		ns
V_{SS}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.71		V

OUTPUT CHARACTERISTICS

V_{GS} = 4.5V

V_{GS} = 3.5V

I_D (A)

30
25
20
15
10
5
0

0 1 2 3 4 5 6 7 8 9 10

V_{DS} (VOLTS)

TRANSFER CHARACTERISTICS

V_{DS} = 5V

I_D (A)

30
20
10
0

125ºC
25ºC

0 0.4 0.8 1.2 1.6 2.0

V_{GS} - (VOLTS)

ON - RESISTANCE vs. DRAIN CURRENT

$R_{DS(ON)}$ (MΩ)

30
25
20
15
10
5
0

V_{GS} = 2.5v

V_{GS} = 4.5v

V_{GS} = 10v

0 5 10 15 20 25

V_D (A)

ON - RESISTANCE vs. GATE-SOURCE VOLTAGE

I_D = 5A

125ºC

25ºC

$R_{DS(ON)}$ (mΩ)

40
30
25
20
15
10
5
0

0
2
4
6
8
10

V_{GS} (VOLTS)

ON - RESISTANCE vs. JUNCTION TEMPERATURE

NORMALIZED ON- RESISTANCE

1.6
1.4
1.2
1.0
0.8
0.6

V_{GS} = 5.0v
I_D = 5A

0 25 50 75 100 125 150 175

TEMPERATURE (°C)

CAPACITANCE CHARACTERISTICS

CAPACITANCE (pF)

3000

2500

2000

1500

1000

500

0

Ciss

Coss

Crss

0 5 10 15 20

CAPACITANCE CHARACTERISTICS

GATE - CHARGE CHARACTERISTICS

GATE - CHARGE CHARACTERISTICS

BODY CIODE CHARACTERISTIC
SOURCE-TO-DRAIN VOLTAGE DIODE FORWARD BIAS

I_S SOURCE CURRENT (AMPS)

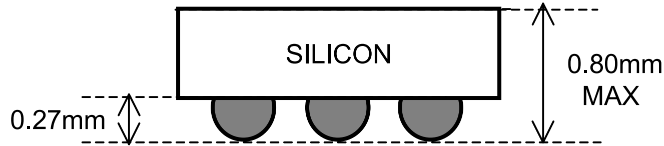
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0

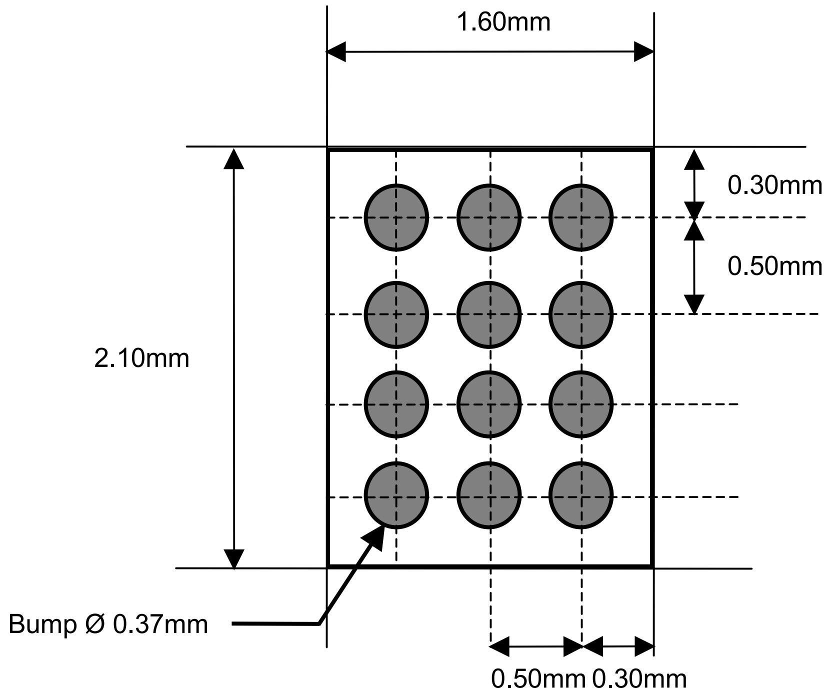
Tj = 150ºC
Tj = 25ºC

0 0.2 0.4 0.6 0.8 1.0 1.2

V_{SD}

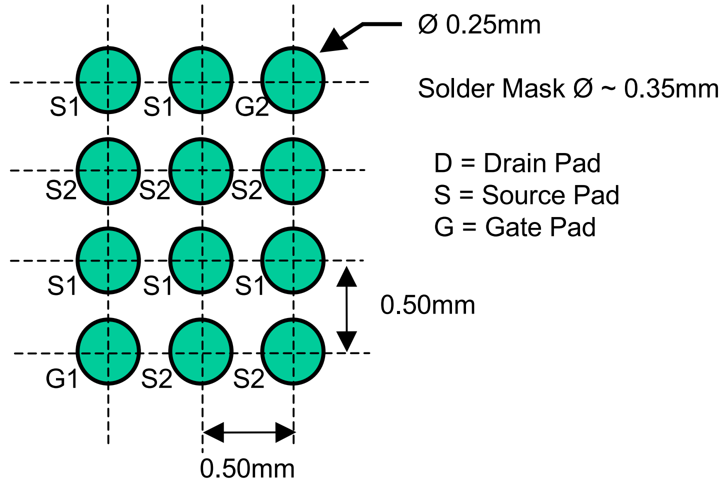
Dimensional Outline and Pad Layout



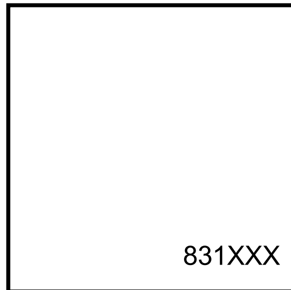


Bumps are Eutectic solder 63/37 Sn/Pb

Dimensional Outline and Pad Layout



LAND PATTERN
RECOMMENDATION

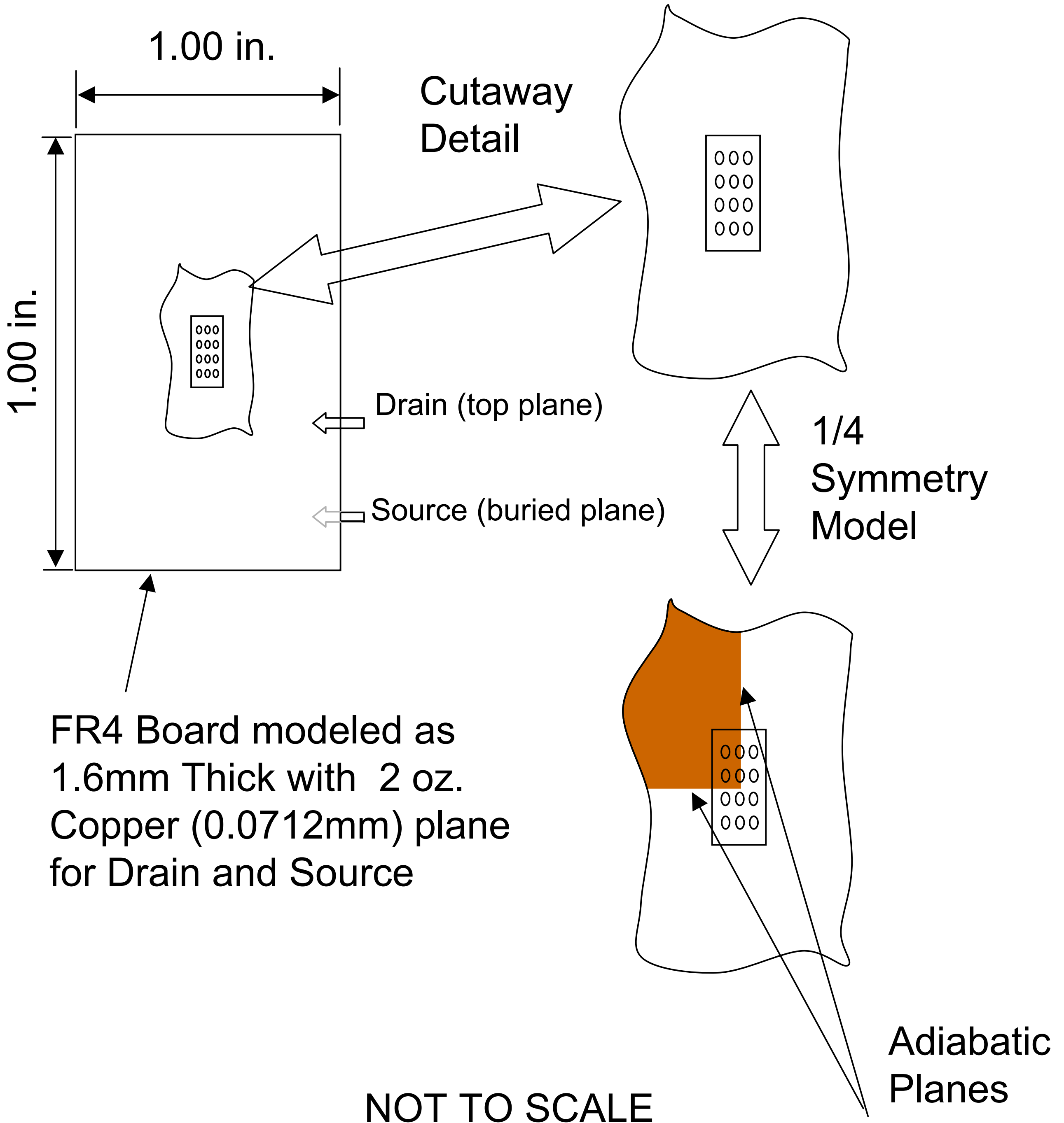


MARK ON BACKSIDE OF DIE

XXX = Date/Lot Traceability Code

TS8314 Thermal Resistance Analysis

TS8314 Die Top View -transparent view for clarity.



Finite Element Model:

- Linear Thermal elements. Combination of tetrahedrals, 6 noded prisms and 8 noded bricks

- Heat Transfer conditions:
  - Bottom of FR4 board constrained to 25 degrees C
  - Power dissipation = 0.4 W per quarter model, in the form of a uniform heat flux at the die junction surface.

- Linear Thermal conduction analysis. *No convection or radiation* included in model.

- ~9800K elements.

Material Properties Used for Analysis

Material	Thickness (mm)	K (W/m°C)
FR4	1.60000	2.5
Copper Layers (2 oz.)	0.07120	390
Solder (96.8Sn/2.6Ag/.6Cu)	0.27000	50
Silicon	0.64000	150
Via (Composite of Cu and Epoxy)	See model	210

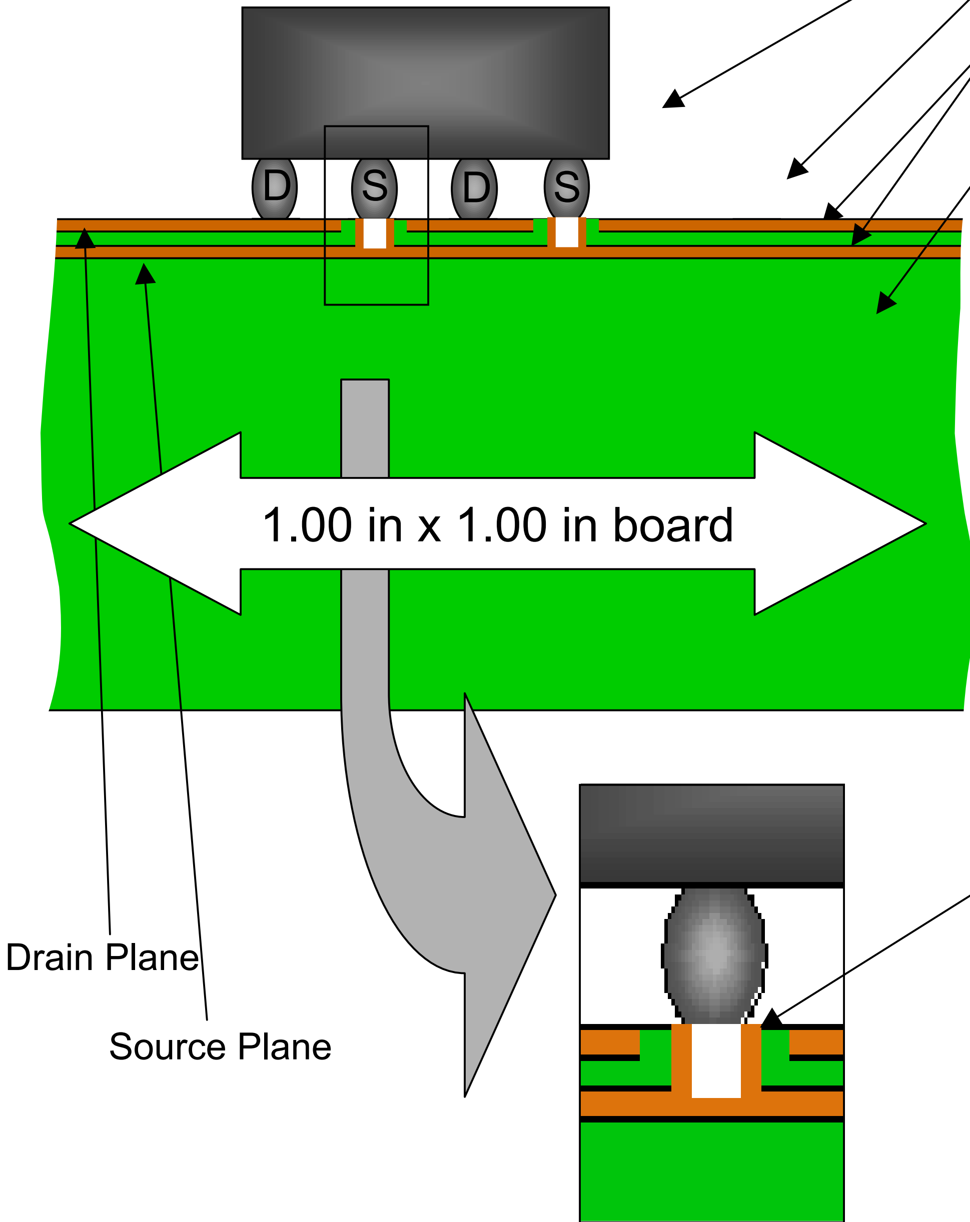
NOTE: 1. Values obtained from http://www.boulder.nist.gov/div853/lead%20free/part2.htm

2. Solder thermal conductivity is best conservative estimate based on composition

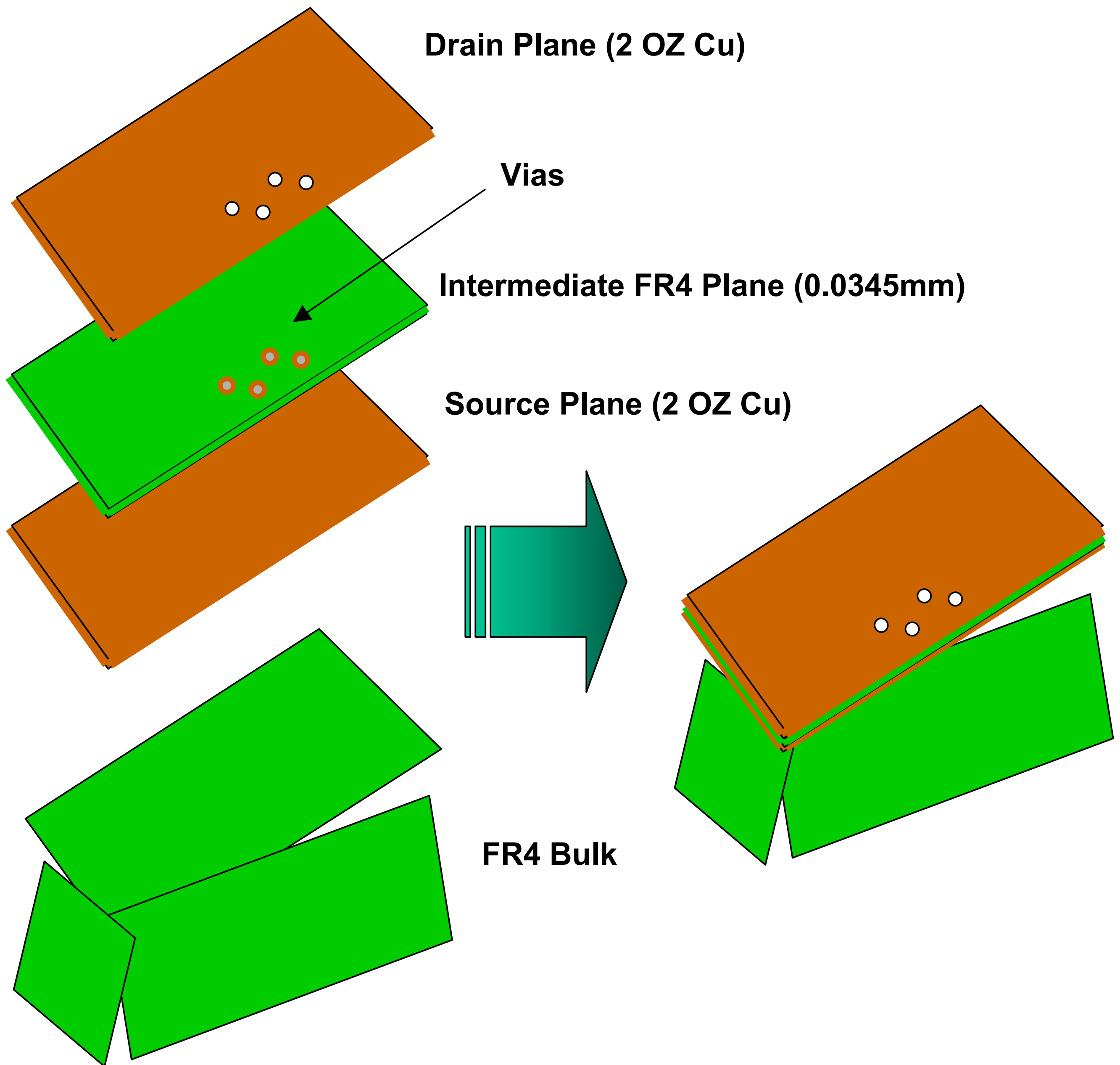
Model: Taiwan Semiconductor TS8314 Part

Cross Section of FEA Model

Thicknesses
Si Die (0.64 mm)
Solder Bump (0.27 mm)
Copper (0.0712 mm)
= 2 0Z. (2.8 mils)
FR4 (1.60 mm total)

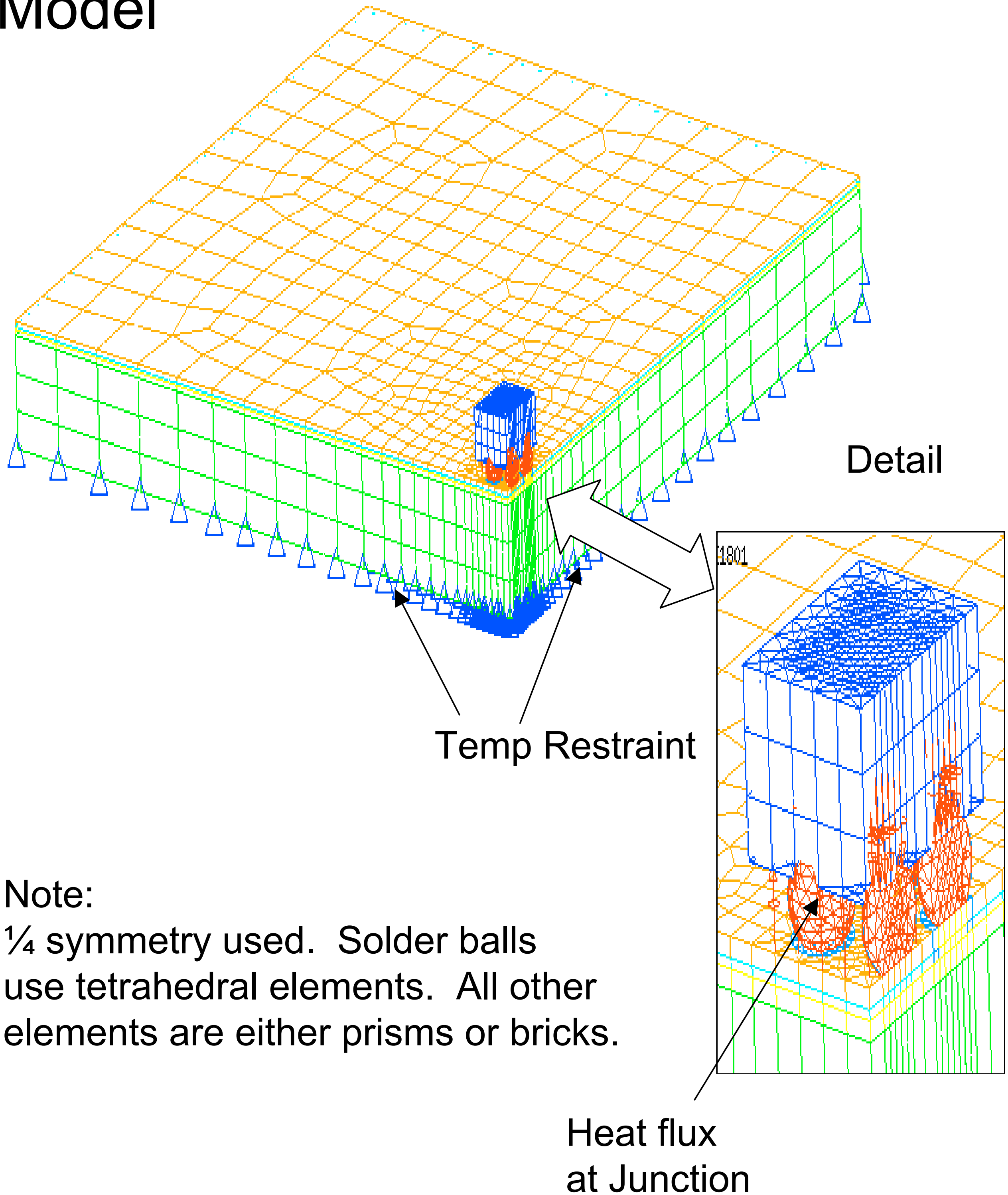


Via: 0.25 mm Dia. with 2 OZ copper plated hole, filled with conductive epoxy.



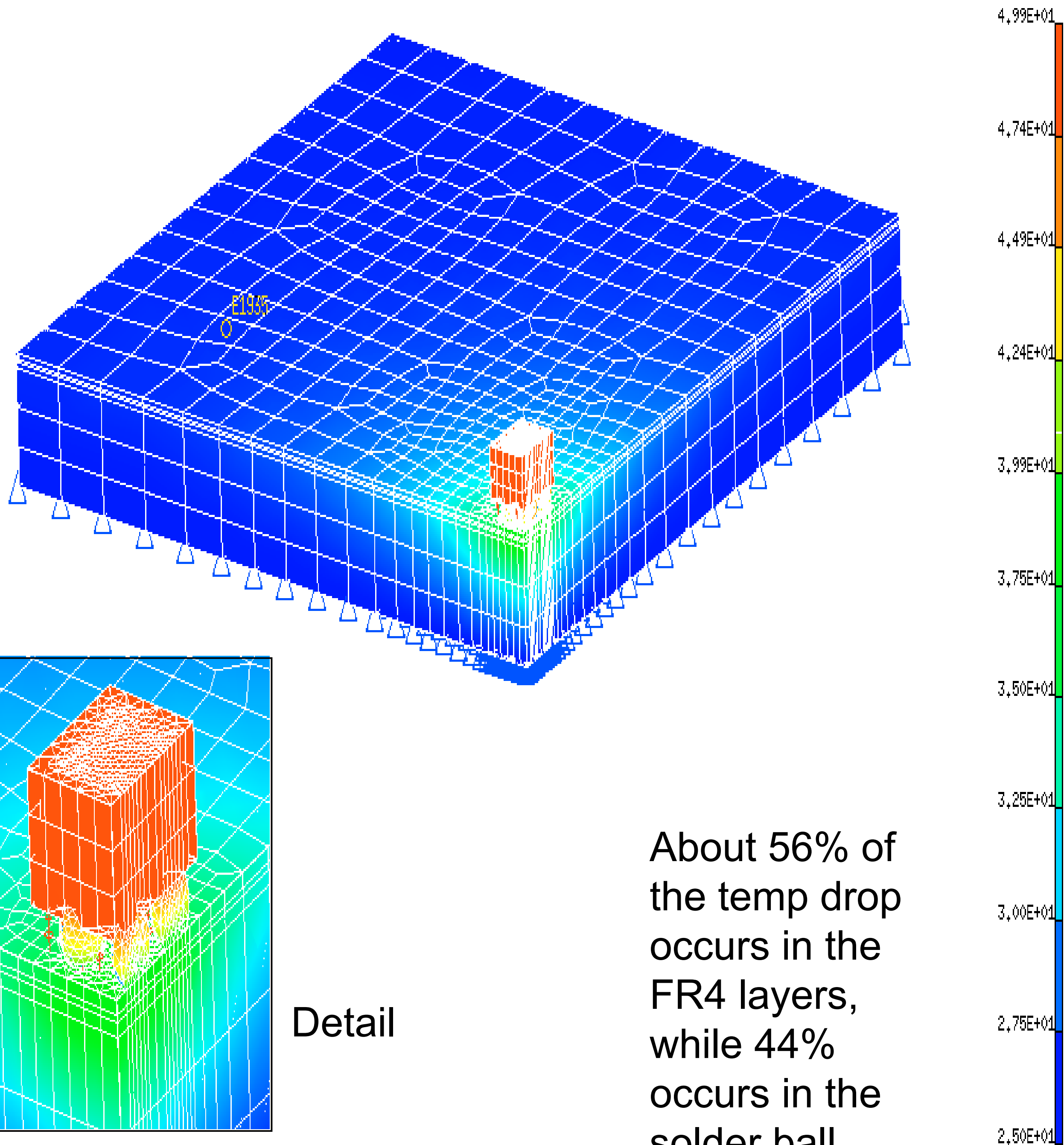
BREAKDOWN OF FR4 LAYERS USED
IN THE FE MODEL. Total Thickness 1.6 mm)
This illustration shows the ½ symmetry model.
The actual FE model uses ¼ symmetry for efficiency.

FEA Model



Note:
¼ symmetry used. Solder balls use tetrahedral elements. All other elements are either prisms or bricks.

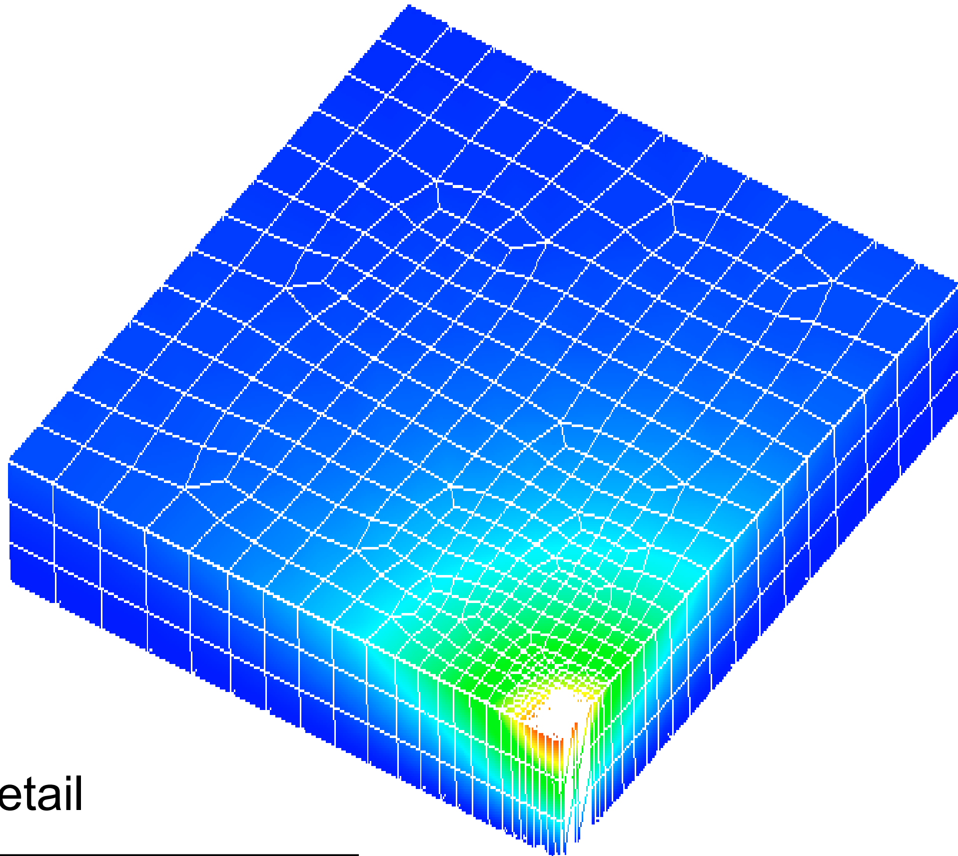
General Result:

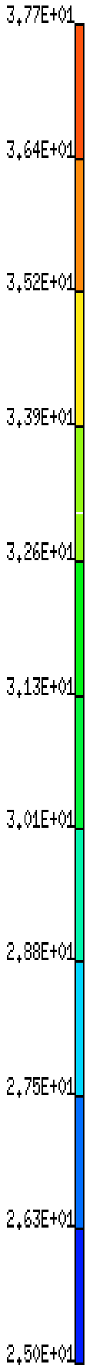


About 56% of the temp drop occurs in the FR4 layers, while 44% occurs in the solder ball.

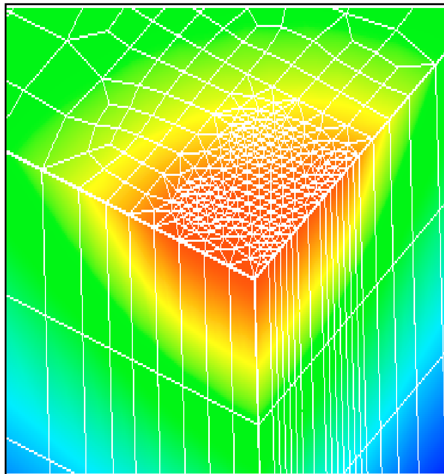
RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 2.50E+01 MAX: 3.77E+01

VALUE OPTION:ACTUAL





Detail

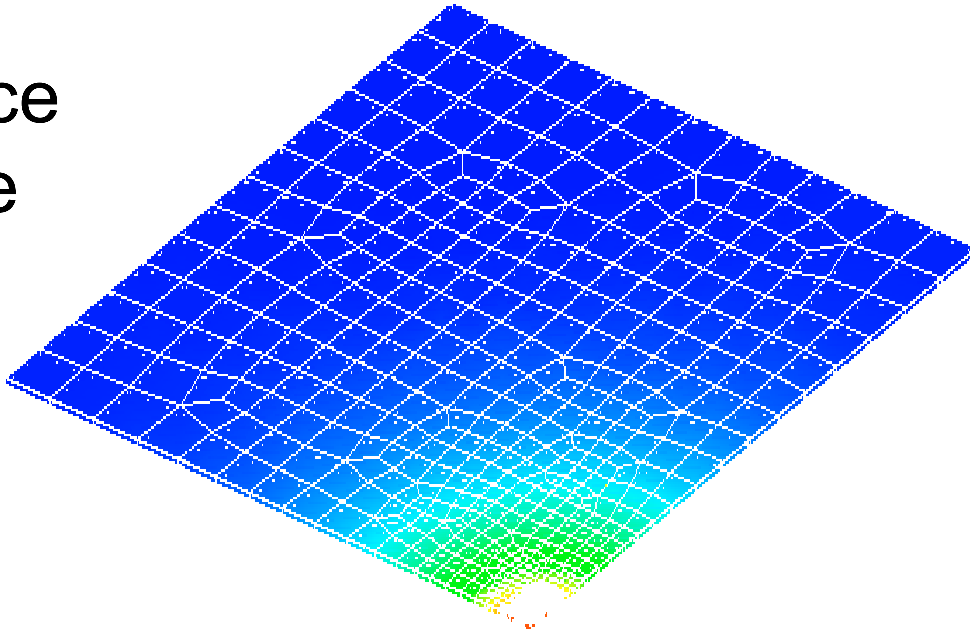


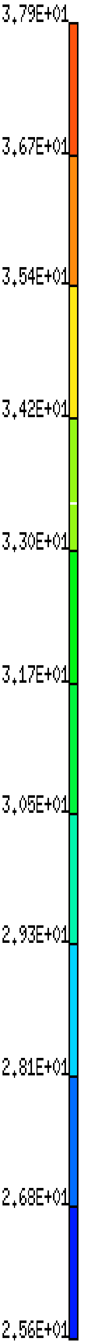
FR4: Not including Copper Planes

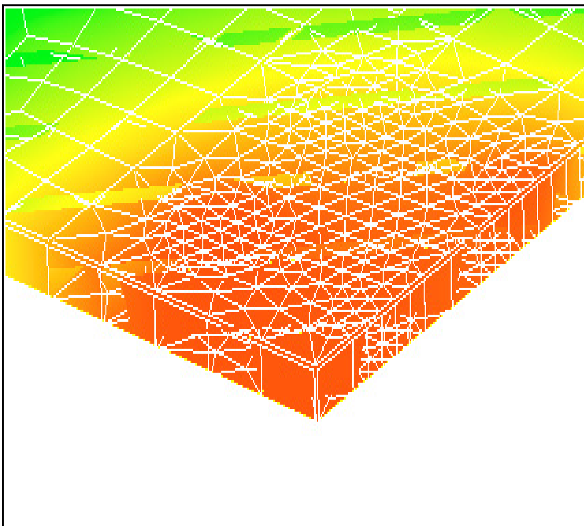
RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 2.56E+01 MAX: 3.79E+01

VALUE OPTION:ACTUAL

FR4: source plane



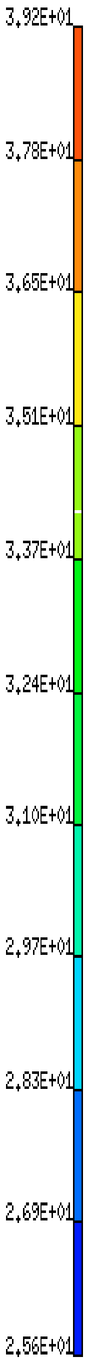


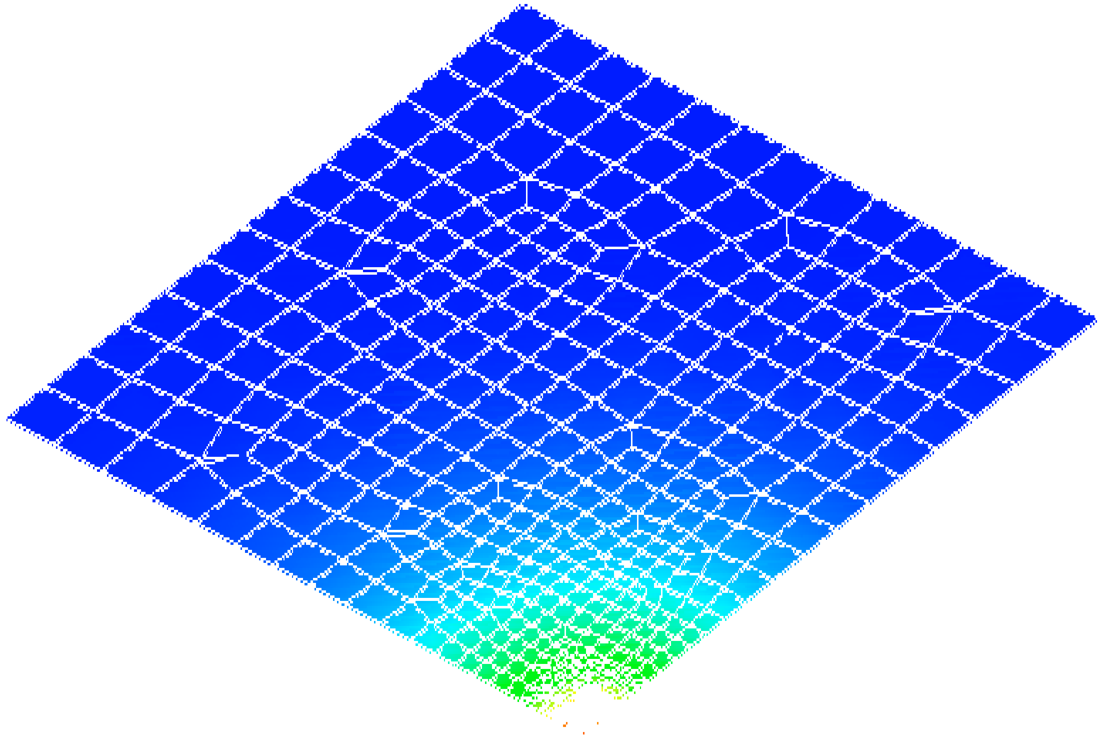


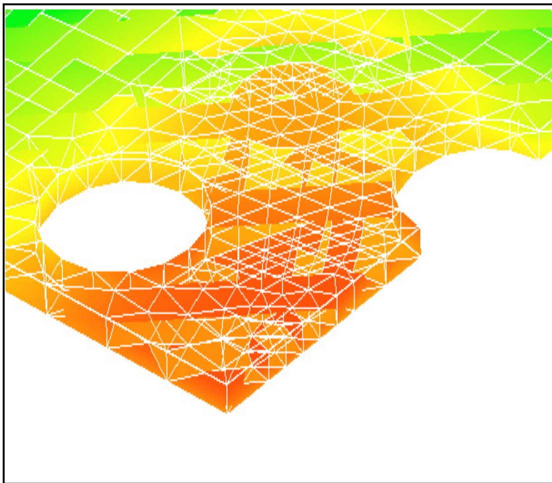
Detail

RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 2.56E+01 MAX: 3.92E+01

VALUE OPTION:ACTUAL







Intermediate FR4 plane

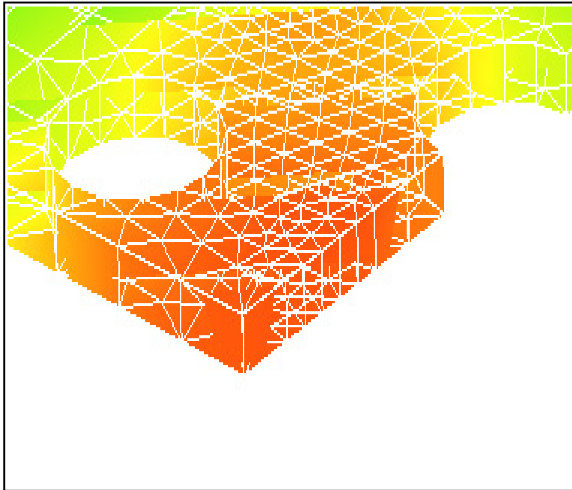
Detail

RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 2.56E+01 MAX: 3.93E+01

VALUE OPTION:ACTUAL

3.93E+01
3.80E+01
3.66E+01
3.52E+01
3.39E+01
3.25E+01
3.11E+01
2.97E+01
2.84E+01
2.70E+01
2.56E+01

Drain FR4 plane



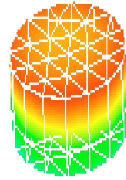
Detail

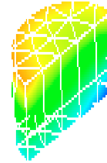
RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 3.66E+01 MAX: 3.94E+01

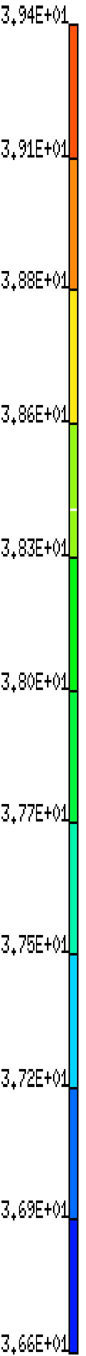
VALUE OPTION:ACTUAL

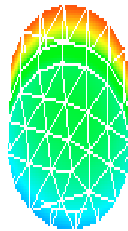
Top Side

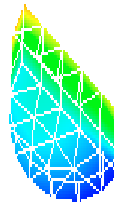
Vias from solder balls to source plane









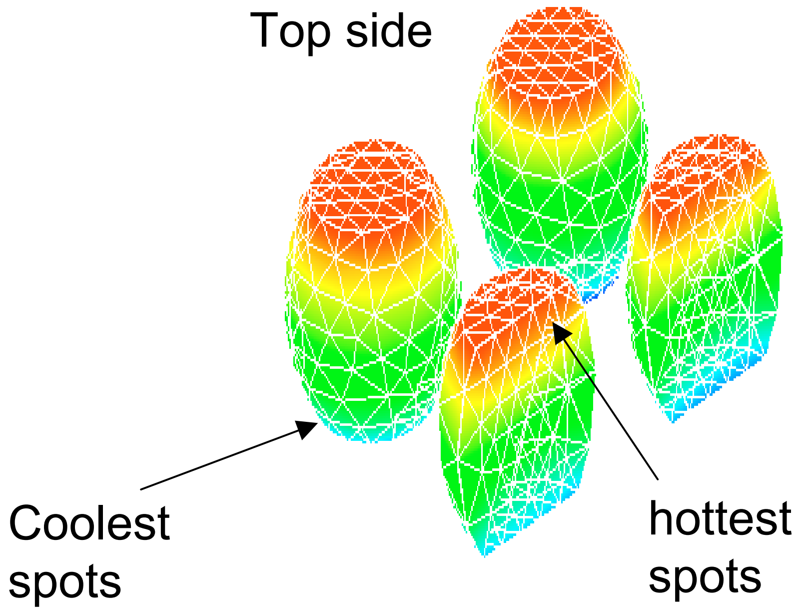


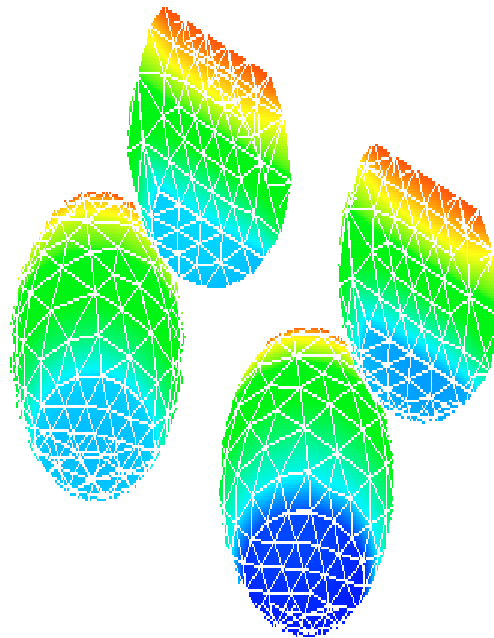
Bottom Side

RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 3.65E+01 MAX: 4.92E+01

VALUE OPTION:ACTUAL

Solder Balls:





Bottom Side

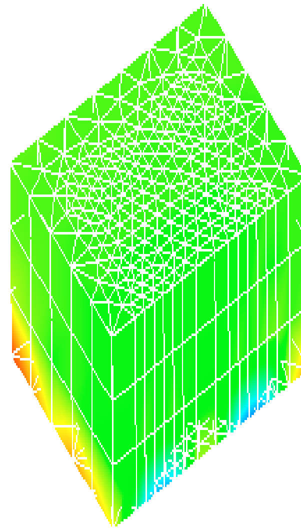
4.92E+01
4.79E+01
4.67E+01
4.54E+01
4.41E+01
4.28E+01
4.16E+01
4.03E+01
3.90E+01
3.78E+01
3.65E+01

RESULTS: 1- B.C. 1,TEMPERATURE_1,LOAD SET 1
TEMPERATURE - MAG MIN: 4.87E+01 MAX: 5.00E+01

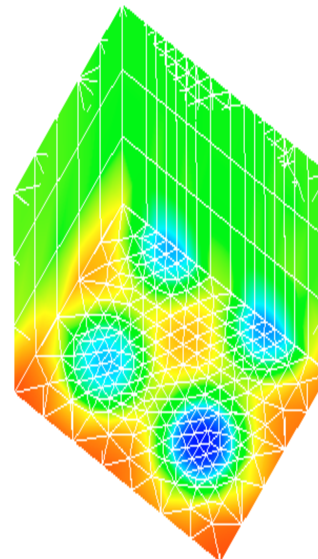
VALUE OPTION:ACTUA

Top Side

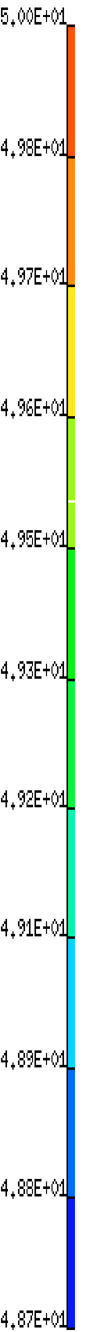
Silicon:



NOTE: The difference between min and max temperatures is only 1.3°C.



Bottom Side



Summary of Results

Thermal Resistance calculations:

$$\theta = \frac{\Delta T}{Power}$$

Layer *	ΔT (°C)	Resistance (°C/W)
Junction to bottom of Ball (Average)	10.5000	6.56250
Ball to bottom of Drain Plane	0.0037	0.00231
Drain Plane to bottom of Intermediate FR4	1.3800	0.86250
Intermediate FR4 to bottom of Source Plane	0.0120	0.00750
Souce Plane to bottom of FR4	12.5500	7.84375
Total Junction to bottom of FR4	**24.4457**	**15.27856**

* temperatures are taken on the hottest spot in each layer and the node directly underneath it on the opposite side