

1-Mbit (64K x 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2V–3.6V and 4.5V–5.5V
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 4 μ A
- Ultra low active power
 - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} , and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 44-Pin TSOP II package

Functional Description

The CY62126ESL is a high performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power

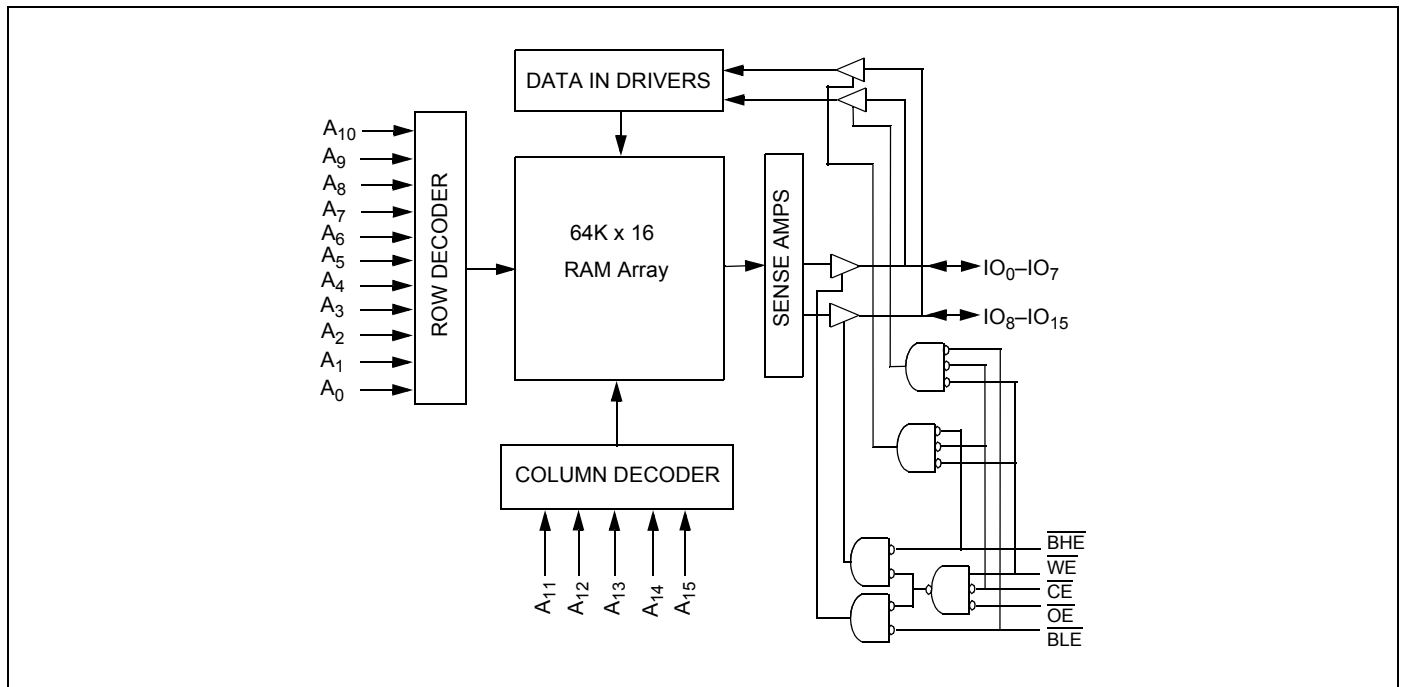
consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE} HIGH). The input and output pins (IO₀ through IO₁₅) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , BLE HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins (IO₀ through IO₇) is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (\overline{BHE}) is LOW, then data from IO pins (IO₈ through IO₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on IO₀ to IO₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on IO₈ to IO₁₅. See the Truth Table on page 10 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

Logic Block Diagram



Pin Configuration

44-Pin TSOP II (Top View) [1]

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
CE	6	39	BLE
IO ₀	7	38	IO ₁₅
IO ₁	8	37	IO ₁₄
IO ₂	9	36	IO ₁₃
IO ₃	10	35	IO ₁₂
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
IO ₄	13	32	IO ₁₁
IO ₅	14	31	IO ₁₀
IO ₆	15	30	IO ₉
IO ₇	16	29	IO ₈
WE	17	28	NC
A ₁₅	18	27	A ₈
A ₁₄	19	26	A ₉
A ₁₃	20	25	A ₁₀
A ₁₂	21	24	A ₁₁
NC	22	23	NC

Product Portfolio

Product	Range	V _{CC} Range (V) [2]	Speed (ns)	Power Dissipation					
				Operating I _{CC} , (mA)				Standby, I _{SB2} (μA)	
				f = 1MHz		f = f _{max}			
				Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62126ESL	Industrial	2.2V–3.6V and 4.5V–5.5V	45	1.3	2	11	16	1	4

Notes

1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6V to 4.5V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied 55°C to +125°C

Supply Voltage to Ground Potential -0.5V to 6.0V

DC Voltage Applied to Outputs in High-Z State^[4, 5] -0.5V to 6.0V

DC Input Voltage^[4, 5] -0.5V to 6.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch up Current..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62126ESL	Industrial	-40°C to +85°C	2.2V–3.6V, and 4.5V–5.5V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit	
			Min	Typ ^[3]	Max		
V _{OH}	Output HIGH Voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OH} = -0.1 mA	2.0		V	
		2.7 ≤ V _{CC} ≤ 3.6	I _{OH} = -1.0 mA	2.4			
		4.5 ≤ V _{CC} ≤ 5.5	I _{OH} = -1.0 mA	2.4			
V _{OL}	Output LOW Voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OL} = 0.1 mA		0.4	V	
		2.7 ≤ V _{CC} ≤ 3.6	I _{OL} = 2.1mA		0.4		
		4.5 ≤ V _{CC} ≤ 5.5	I _{OL} = 2.1mA		0.4		
V _{IH}	Input HIGH Voltage	2.2 ≤ V _{CC} ≤ 2.7		1.8	V _{CC} + 0.3	V	
		2.7 ≤ V _{CC} ≤ 3.6		2.2	V _{CC} + 0.3		
		4.5 ≤ V _{CC} ≤ 5.5		2.2	V _{CC} + 0.5		
V _{IL}	Input LOW Voltage	2.2 ≤ V _{CC} ≤ 2.7		-0.3	0.6	V	
		2.7 ≤ V _{CC} ≤ 3.6		-0.3	0.8		
		4.5 ≤ V _{CC} ≤ 5.5		-0.5	0.8		
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		-1	+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1	+1	μA	
I _{CC}	V _{CC} Operating Supply Current	f = f _{max} = 1/t _{RC}	V _{CC} = V _{CCmax}		11	16	mA
		f = 1 MHz	I _{OUT} = 0 mA, CMOS levels		1.3	2.0	
I _{SB1}	Automatic CE Power down Current — CMOS Inputs	CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (OE and WE), V _{CC} = V _{CC(max)}			1	4	μA
I _{SB2}	Automatic CE Power down Current — CMOS Inputs	CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = V _{CC(max)}			1	4	μA

Notes

4. V_{IL}(min) = -2.0V for pulse durations less than 20 ns.

5. V_{IH}(max) = V_{CC} + 0.75V for pulse durations less than 20 ns.

6. Full Device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

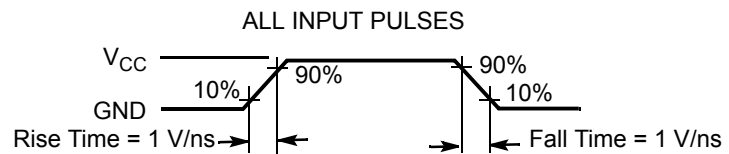
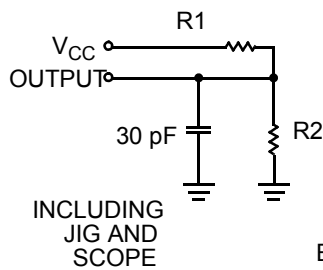
Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output Capacitance		10	pF

Thermal Resistance

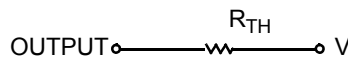
Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	28.2	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		3.4	°C/W

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT



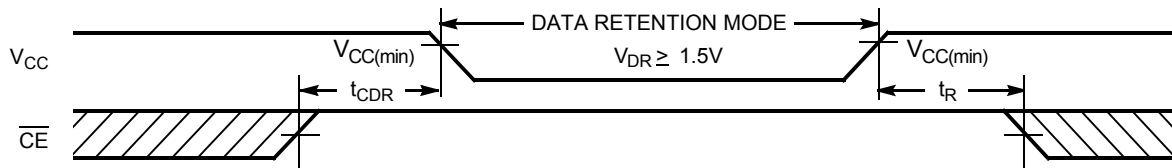
Parameters	2.50V	3.0V	5.0V	Unit
R1	16600	1103	1800	Ω
R2	15400	1554	990	Ω
R _{TH}	8000	645	639	Ω
V _{TH}	1.2	1.75	1.77	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[3]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			3	μA
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu s$ or stable at $V_{CC(min)} \geq 100 \mu s$.

Switching Characteristics

 Over the Operating Range ^[9]

Parameter	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	\overline{CE} LOW to Data Valid		45	ns
t_{DOE}	\overline{OE} LOW to Data Valid		22	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[10]	5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[10, 11]		18	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[10]	10		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[10, 11]		18	ns
t_{PU}	\overline{CE} LOW to Power Up	0		ns
t_{PD}	\overline{CE} HIGH to Power Up		45	ns
t_{DBE}	\overline{BHE} / \overline{BLE} LOW to Data Valid		22	ns
t_{LZBE}	\overline{BHE} / \overline{BLE} LOW to Low Z ^[10]	5		ns
t_{HZBE}	\overline{BHE} / \overline{BLE} HIGH to High Z ^[10, 11]		18	ns
Write Cycle ^[12]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	\overline{CE} LOW to Write End	35		ns
t_{AW}	Address Setup to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	35		ns
t_{BW}	\overline{BHE} / \overline{BLE} Pulse Width	35		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[10, 11]		18	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[10]	10		ns

Notes

9. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" on page 4.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the output enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 1. Read Cycle No. 1 (Address Transition Controlled) [13, 14]

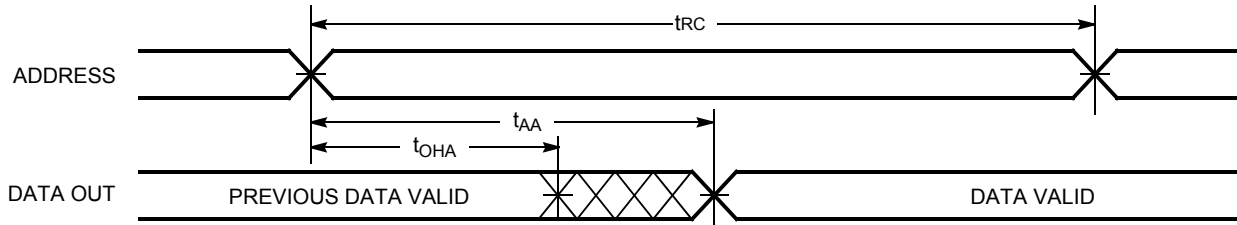
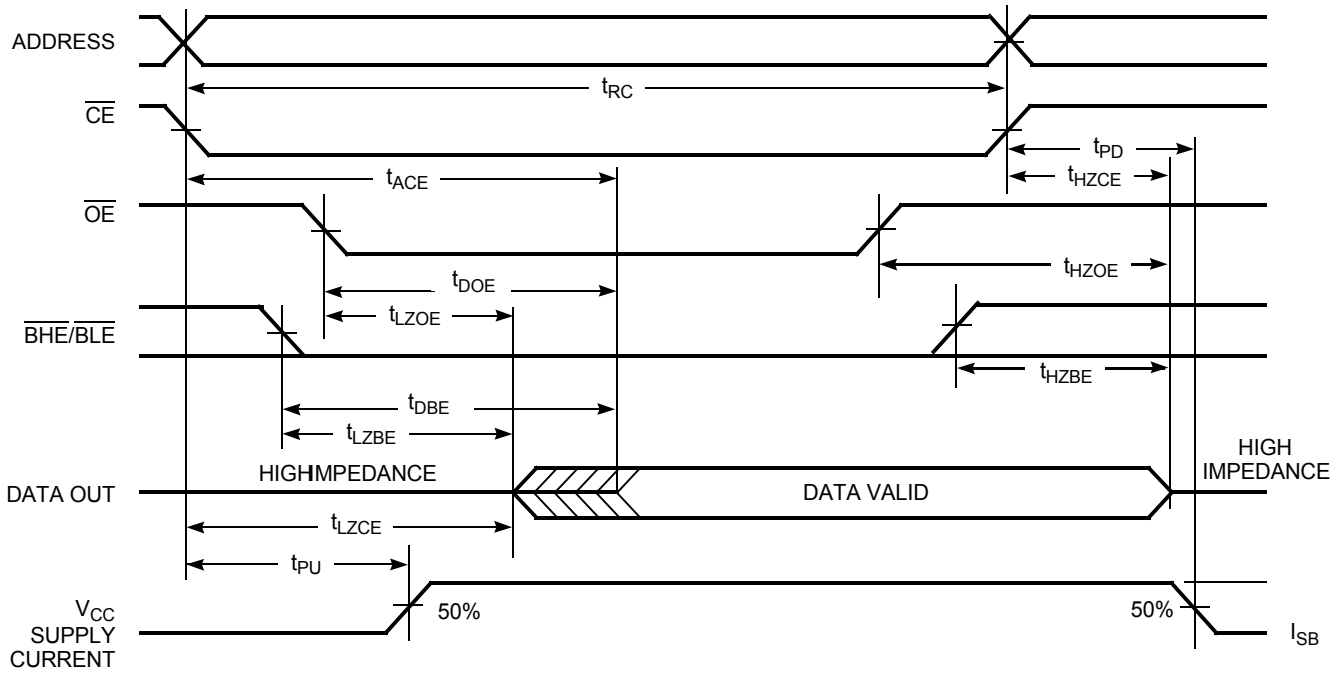


Figure 2. Read Cycle No. 2 (\overline{OE} Controlled) [14, 15]



Notes

13. Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} .
14. \overline{WE} is HIGH for read cycles.
15. Address valid before or similar to \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 3. Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [16, 17]

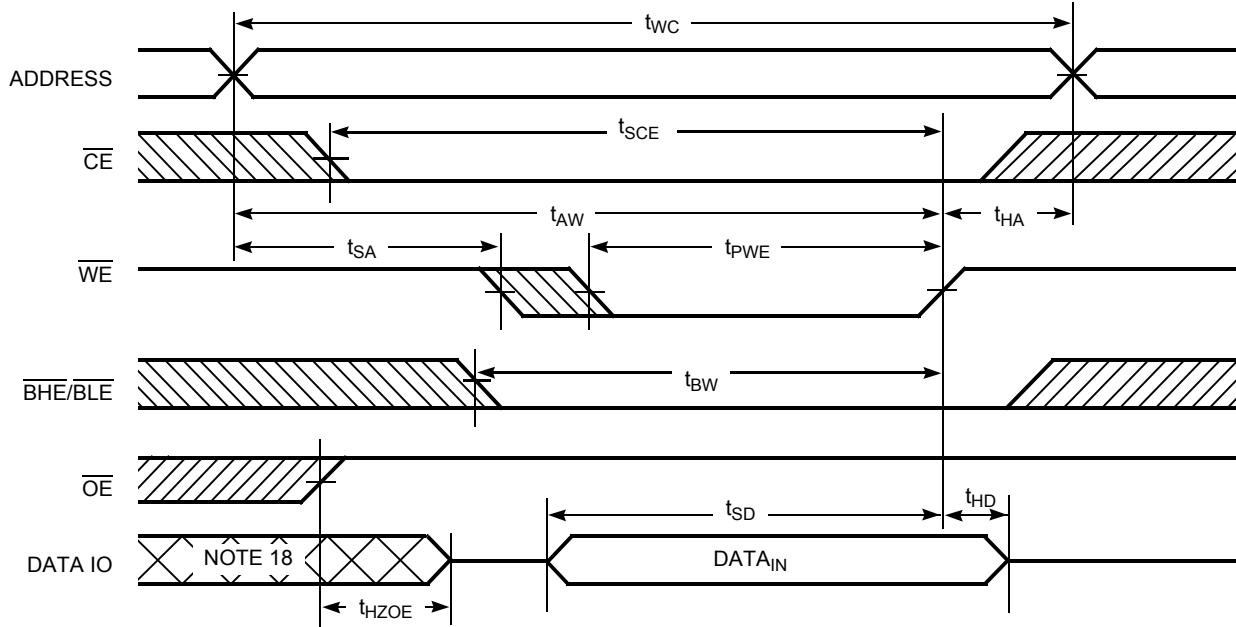
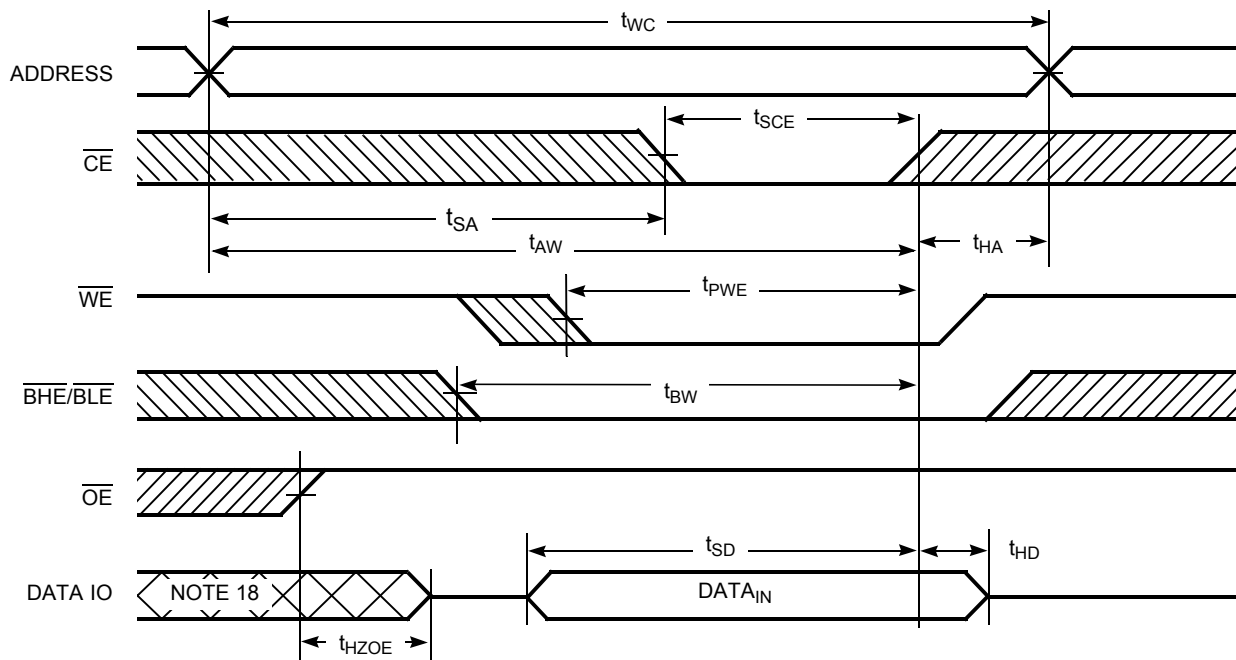


Figure 4. Write Cycle No. 2 (\overline{CE} Controlled) [16, 17]



Notes

- 16. Data IO is high impedance if $\overline{OE} = V_{IH}$.
- 17. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
- 18. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [17]

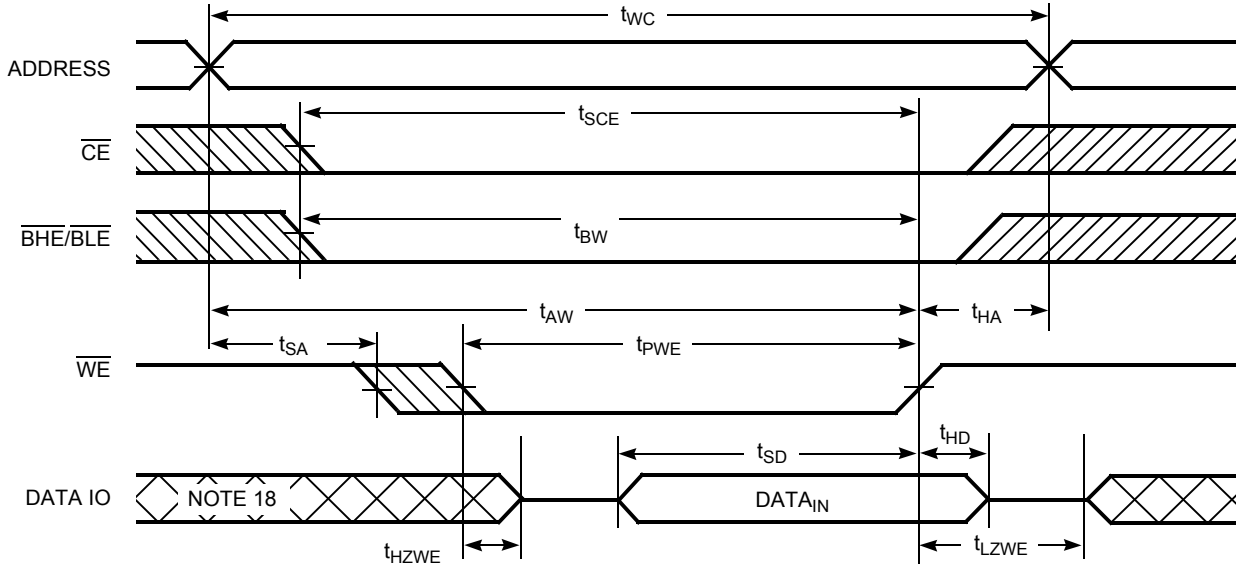
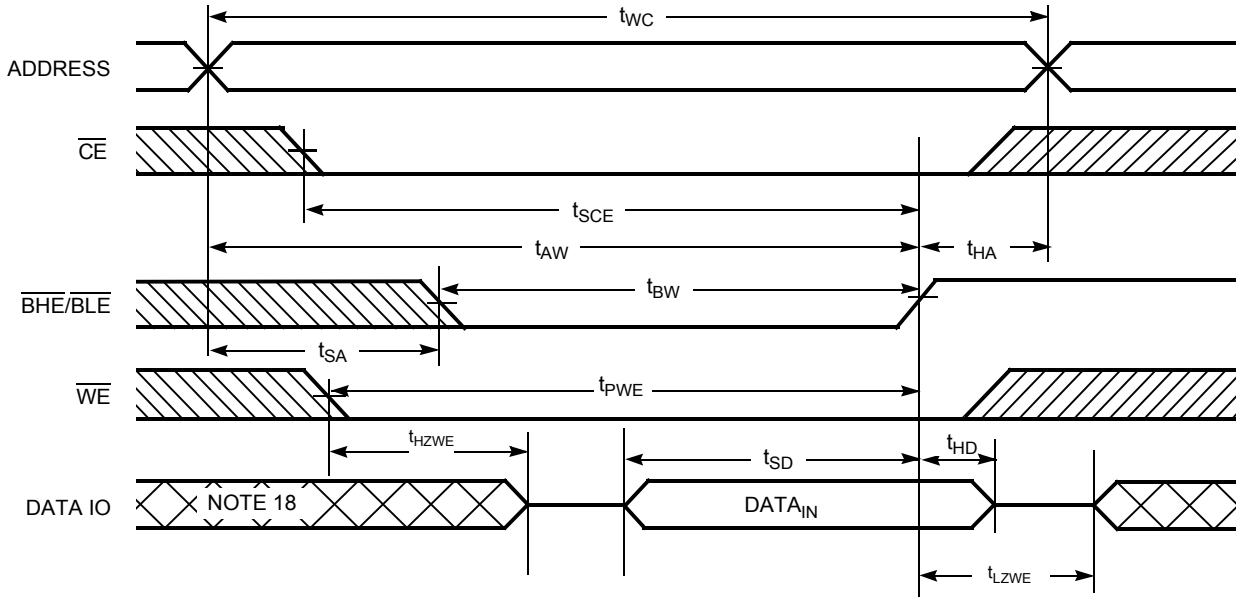


Figure 6. Write Cycle No. 4 ($\overline{BHE/BLE}$ Controlled, \overline{OE} LOW) [17]



Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect or Power Down	Standby (I_{SB})
X	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (IO_0 - IO_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (IO_0 - IO_7); IO_8 - IO_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (IO_8 - IO_{15}); IO_0 - IO_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (IO_0 - IO_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (IO_0 - IO_7); IO_8 - IO_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (IO_8 - IO_{15}); IO_0 - IO_7 in High Z	Write	Active (I_{CC})

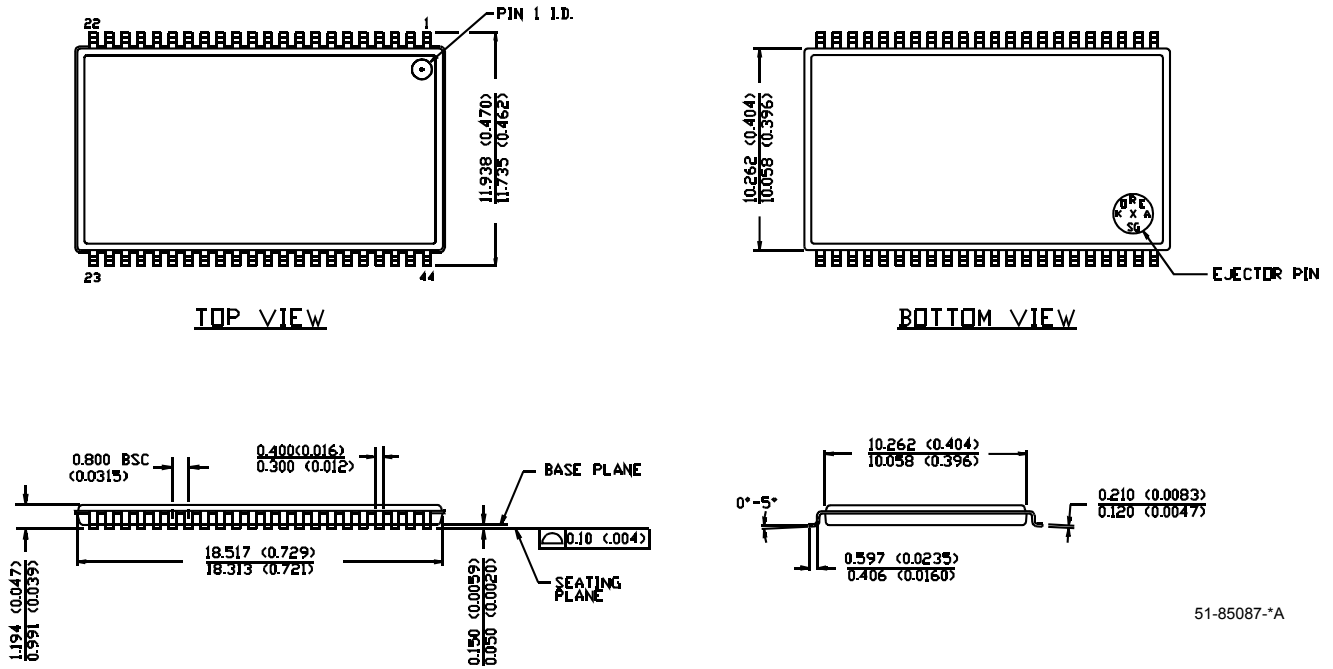
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62126ESL-45ZSXI	51-85087	44-Pin TSOP II (Pb-free)	Industrial

Package Diagrams

Figure 7. 44-Pin Thin Small Outline Package Type II, 51-85087

DIMENSION IN MM (INCH)
MAX
MIN



51-85087-A

Document History Page

Document Title: CY62126ESL MoBL® 1-Mbit (64K x 16) Static RAM				
Document Number: 001-45076				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	2610988	11/21/08	VKN/PYRS	New data sheet
*A	2718906	06/15/2009	VKN	Post to external web

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

© Cypress Semiconductor Corporation, 2008-2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress’ product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.