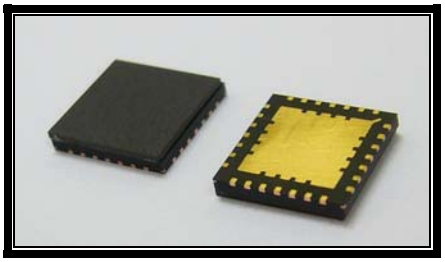
RFMA7090-1W-Q7

UPDATED: 04/24/2008

7.0 – 9.0 GHz High Gain Surface-Mounted PA

FEATURES

- **7.0 – 9.0GHz Operating Frequency Range**
- **30.0dBm Output Power @1dB Compression**
- **34.0dB Typical Power Gain @1dB Compression**
- **-41dBc OIMD3 @Pout 20dBm/tone**
- **7X7mm QFN Package**



APPLICATIONS

- **Point-to-point and point-to-multipoint radio**
- **Military Radar Systems**

ELECTRICAL CHARACTERISTICS (T_B=25 °C)

SYMBOL	PARAMETER/TEST CONDITIONS	MIN	TYP	MAX	UNITS
F	Operating Frequency Range	7.0		9.0	GHz
P_{1dB}	Output Power @1dB Gain Compression	29.0	30.0		dBm
G_{1dB}	Gain @1dB Gain Compression	29.0	34.0		dB
OIMD3	Output 3rd Order Intermodulation Distortion @Δf=10MHz, Pout = 20dBm/tone		-41	-38	dBc
Input RL	Input Return Loss		-10	-8	dB
Output RL	Output Return Loss		-5		dB
I_{D1}	Drain Current[1]		180	220	mA
I_{D2}	Drain Current[1]		800	940	mA
V_{D1}, V_{D2}	Drain Voltage		7	8	V
V_{G1}, V_{G2}	Gate Voltage	-2.5		-0.25	V
Rth	Thermal Resistance[2]		9		°C/W
Tb	Operating Base Plate Temperature	-30		+80	°C

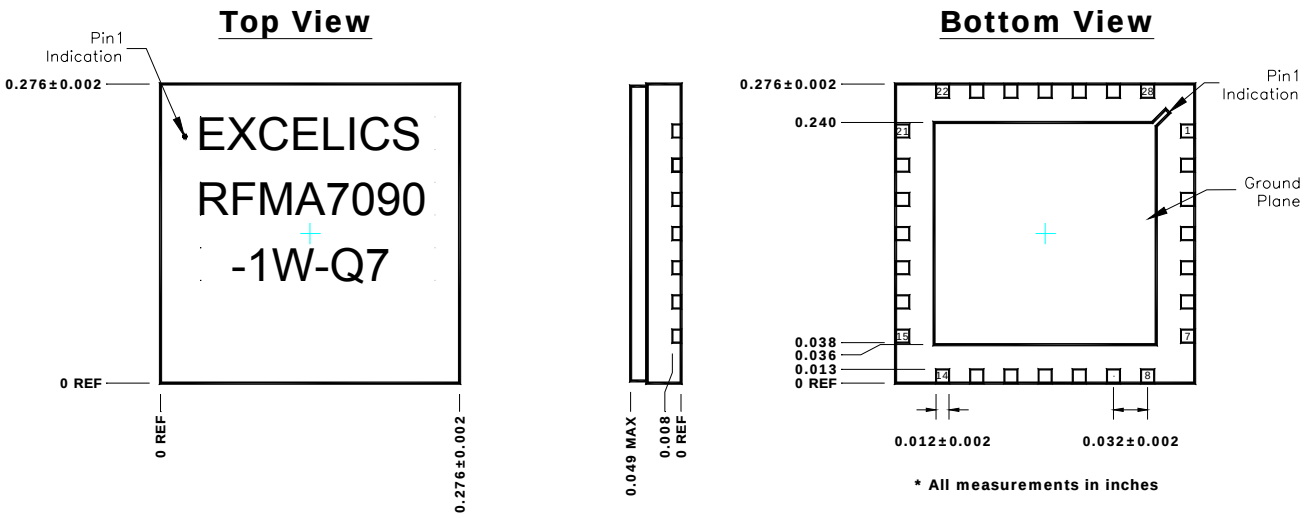
1. Recommended to bias each amplifier stage separately using a gate voltage range, starting from -2.5 to -0.3V to achieve typical current levels.
2. Rth is mounting dependent. Measured result when used with Excelics recommended evaluation board.

MAXIMUM RATINGS AT 25°C[3,4]

SYMBOL	CHARACTERISTIC	ABSOLUTE	CONTINOUS
V_{D1}, V_{D2}	Drain to Source Voltage	12V	8 V
V_{G1}, V_{G2}	Gate to Source Voltage	-5V	-2.5 V
I_{D1}, I_{D2}	Drain Current	Idss	220, 940mA
P_{IN}	Input Power	20dBm	@ 3dB compression
T_{CH}	Channel Temperature	175°C	150°C
T_{STG}	Storage Temperature	-65/175°C	-65/150°C
P_T	Total Power Dissipation	15.0W	12.6W

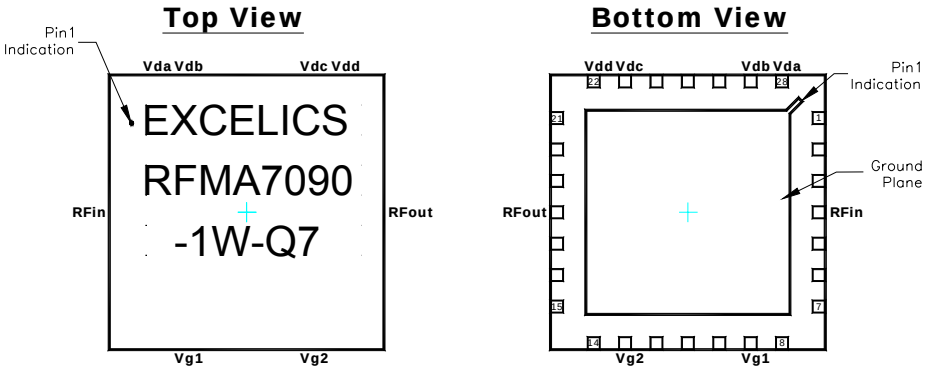
3. Operation beyond *absolute* or *continuous* ratings may result in permanent damage or reduction of MTTF respectively.
4. Bias conditions must also satisfy the following equation V_{DS}*I_{DS} < (T_{CH} –T_B)/R_{TH}; where T_B = Temperature of Base Plate

Package Dimension and Pin Assignment



Additional Notes:

1) Ground Plane must be soldered to PCB RF ground
2) All dimensions are in inches
3) Refer to Excelics application notes on QFNs for further guidelines
4) Pin Assignment:



Pin	Assignment
1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 14	NC
4	RF_{in}
9	V_{g1}
13	V_{g2}
15, 16, 17, 19, 20, 21, 22, 24, 25, 26, 28	NC
18	RF_{out}
22, 23	V_{dd}, V_{dc}
27, 28	V_{db}, V_{da}

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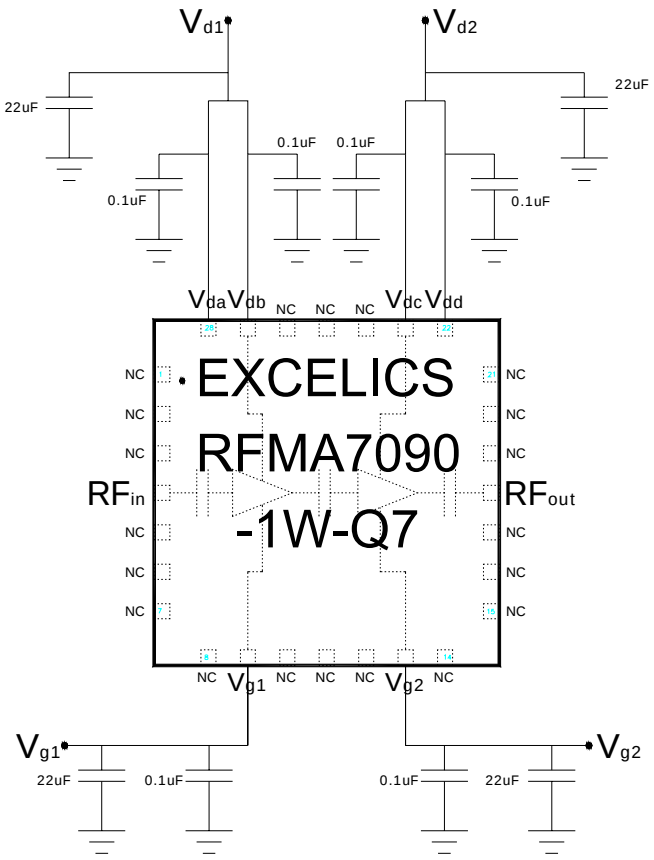
Recommended Circuit Schematic:



Notes:

1) External bypass capacitors should be placed as close to the package as possible.
2) Dual biasing sequence required:
   a. Turn-on Sequence: Apply V_{g1} = -2.5V, V_{g2} = -2.5V, followed by V_{d1} = V_{d2} = 7V, lastly increase V_{g1} & V_{g2} in sequence until required I_{d1} and I_{d2} is obtained.
   b. Turn-off Sequence: Turn off V_{d1} & V_{d2}, followed by V_{g1} & V_{g2}
3) Demonstration board available upon request.