M/A-COM Technology Solutions

Silicon PIN Limiter Diodes

V13

Features

- Low Insertion Loss and Noise Figure
- High Peak and Average Operating Power
- Various P1dB Compression Powers
- Low Flat Leakage Power
- Proven Reliable, Silicon Nitride Passivation
- RoHS Compliant

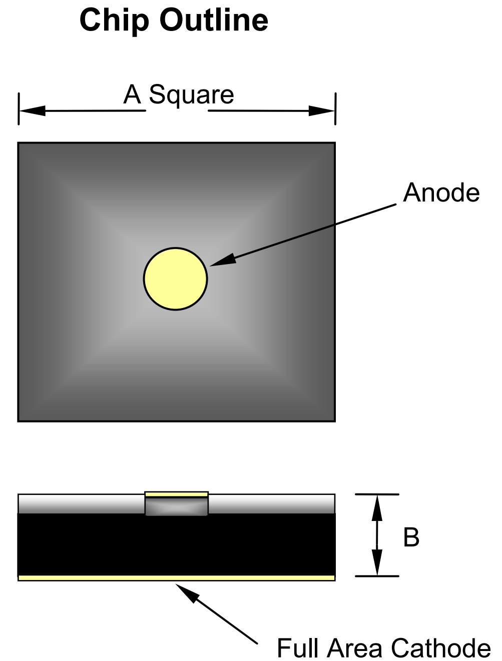
Description

M/A-COM Technology Solutions produces a series of silicon PIN limiter diodes with small and medium I-region lengths which are specifically designed for high signal applications. The devices are designed to provide low insertion loss, at zero bias, as well as low flat leakage power with fast signal response/recovery times. Parts are available as discrete die or assembled into a variety of surface mount or ceramic pill packages. See the *Available Case Style* table on page 6 for the specific ceramic package styles and their availability for individual part numbers.

Applications

The MA4Lseries of PIN limiter diodes are designed for use in passive limiter control circuits to protect sensitive receiver components such as low noise amplifiers (LNA), detectors, and mixers covering the 10 MHz to 18 GHz frequency range.

Chip Outline



ODS	Dimension	mils	µm
134	A	15 ± 2	381 ± 51
	B	7 ±1*	178 ± 25.4

Note:
The MADL-000301-01340W and MA4L401-134 "B" dimension, is 10 ±1 mils

Absolute Maximum Ratings[1] T_{AMB} = 25°C *(Unless otherwise specified)*

Parameter	Absolute Maximum
Forward Current	100mA
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +150°C
Junction Temperature	+175°C
RF Peak & C.W. Incident Power	Per Performance Table
Mounting Temperature	+320°C for 10 sec.

Note:
1. Exceeding any of the above ratings may cause permanent damage.

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Un-Packaged Die Electrical Specifications at T_{AMB} = 25°C

Part Number	Minimum Reverse Voltage V_R	Maximum Reverse Voltage V_R	Minimum C_{j0V} pF	Maximum C_{j0V} pF	Maximum $R_{S\ 10mA}$ Ohms[1]	Nominal Characteristics: Carrier Lifetime I_{FOR}=10mA I_{REV}= -6mA nS[1]	Nominal Characteristics: I-Region Thickness µM	Nominal Characteristics: Contact Diameter mils	Nominal Characteristics: Thermal Resistance °C/W[1]
MA4L011-134	15	35	0.08	0.18	2.10	10	2	1.2	175
MA4L021-134	20	35	0.10	0.20	2.10	10	2	1.2	175
MA4L022-134	20	35	0.09	0.19	2.00	10	2	1.2	175
MA4L031-134	30	50	0.14	0.21	2.00	20	3	1.4	150
MA4L032-134	30	50	0.13	0.20	2.50	15	3	1.5	150
MA4L062-134	50	75	0.07	0.15	2.50	70	4	1.5	150
MA4L101-134	100			0.15	2.00	90	13	3.5	30
MADL-000301-01340W	200			0.20	1.50	200	20	3.0	30
MA4L401-134	250			0.30	1.20	800	25	4.5	25

Note:
1. Test performed with the chip mounted in an ODS-30 package.

*Nominal High Signal Performance at T_{AMB} = 25°C

Part Number	Incident Peak Power for 1dB Limiting @ 9.4GHz dBm	Incident Peak Power for 10dB Limiting @ 9.4GHz dBm	Incident Peak Power for 15dB Limiting @ 9.4GHz dBm	Recovery Time (3 dB) @ 50W Peak Power nS	Maximum Incident Peak Power Watts	Maximum CW Input Power Watts
MA4L011-134	7	30	40	10	80	2
MA4L021-134	8	31	41	15	90	3
MA4L022-134	8	31	41	15	90	3
MA4L031-134	10	33	43	25	125	4
MA4L032-134	11	34	44	25	125	4
MA4L062-134	15	38	50	75	200	5
MA4L101-134	20	45	53	100	250	6
MADL-000301-01340W	23	46	59	50	500	7
MA4L401-134	30	52	60	250	1000	10

***See page 3 for high signal performance parameter notes.**

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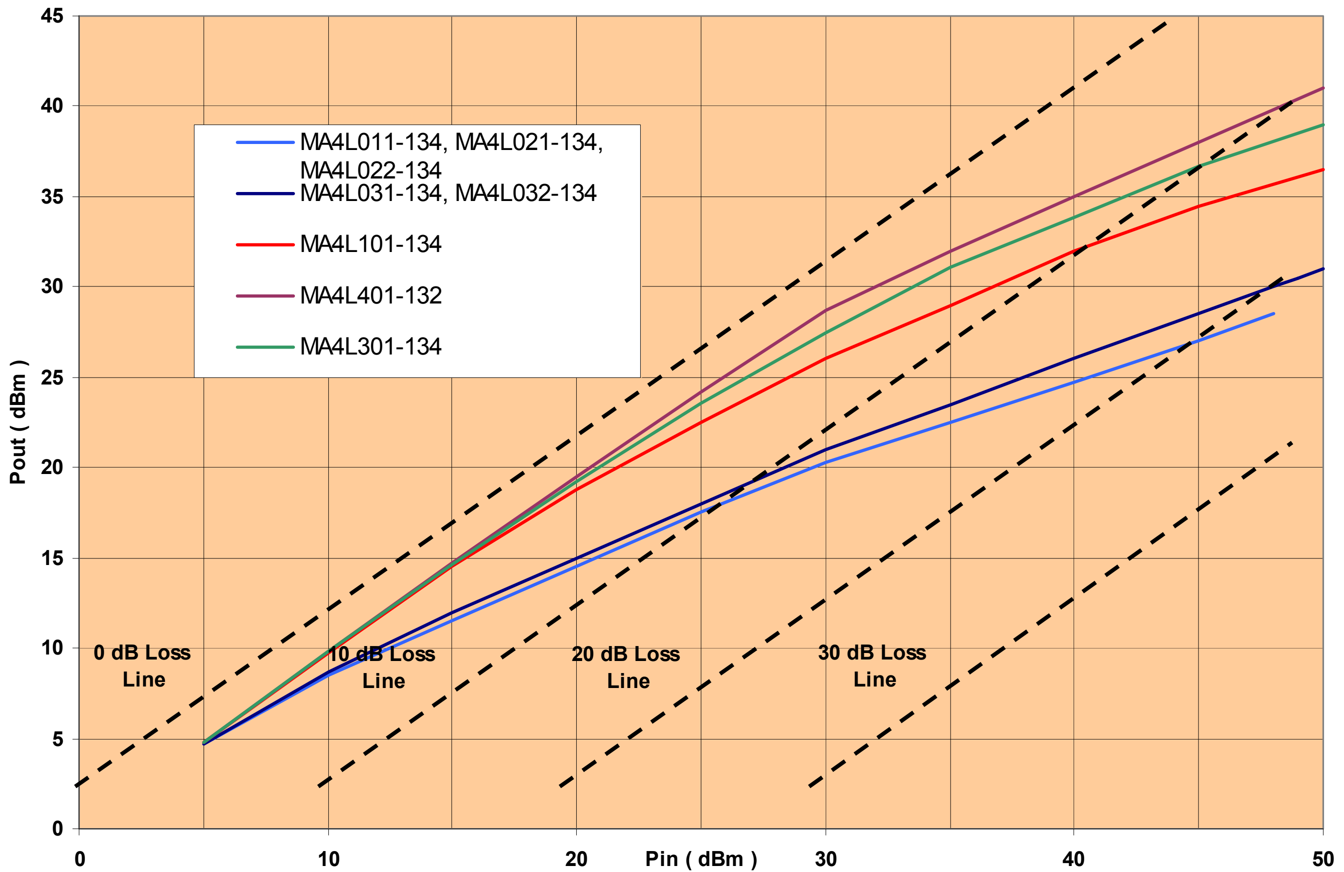
Typical High Signal Peak Power Performance for the Single Shunt Limiter Diode in a 50 Ω Test Fixture



High Signal Performance: Measured using a single shunt diode (die) attached directly to the gold plated RF housing ground with 2 mil thick conductive silver epoxy in a 50Ω, SMA, connectorized test fixture. Chip anode contact is thermo-compression wire bonded using a 1 mil. dia. gold wire onto a 7.2 mil thick Rogers 5880 Duroid microstrip trace. A shunt coil provides the D.C. return. Test frequency = 9.4 GHz, For peak power measurements RF pulse width = 1.0 µS, 0.001% duty cycle.

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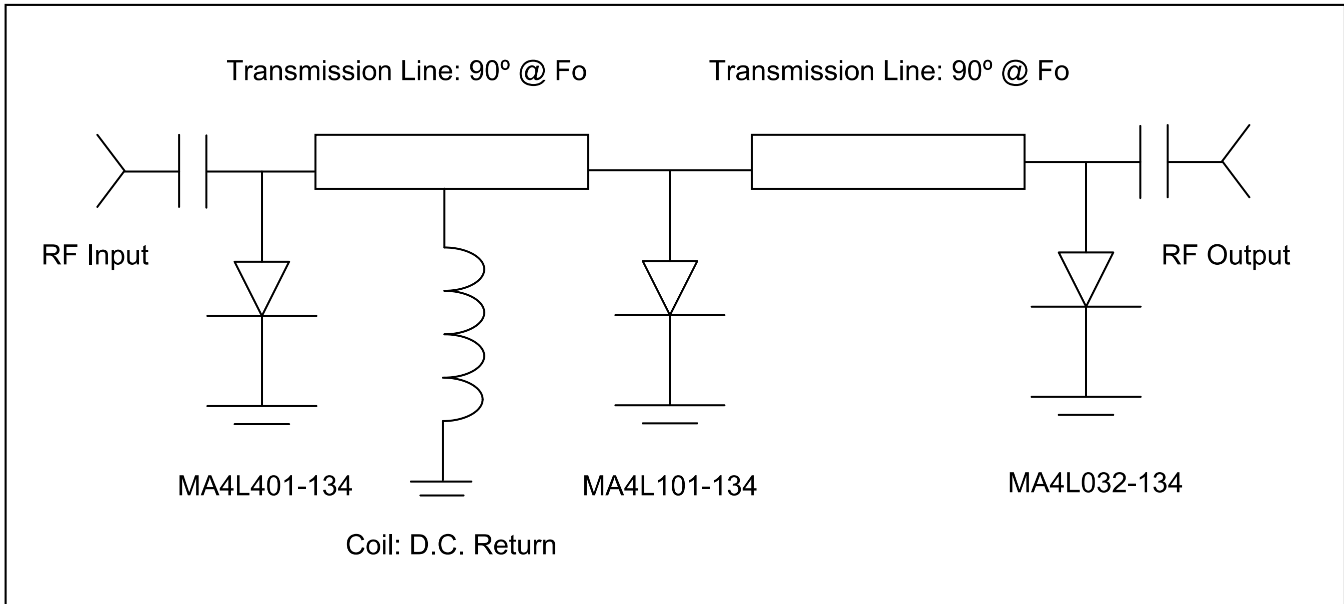
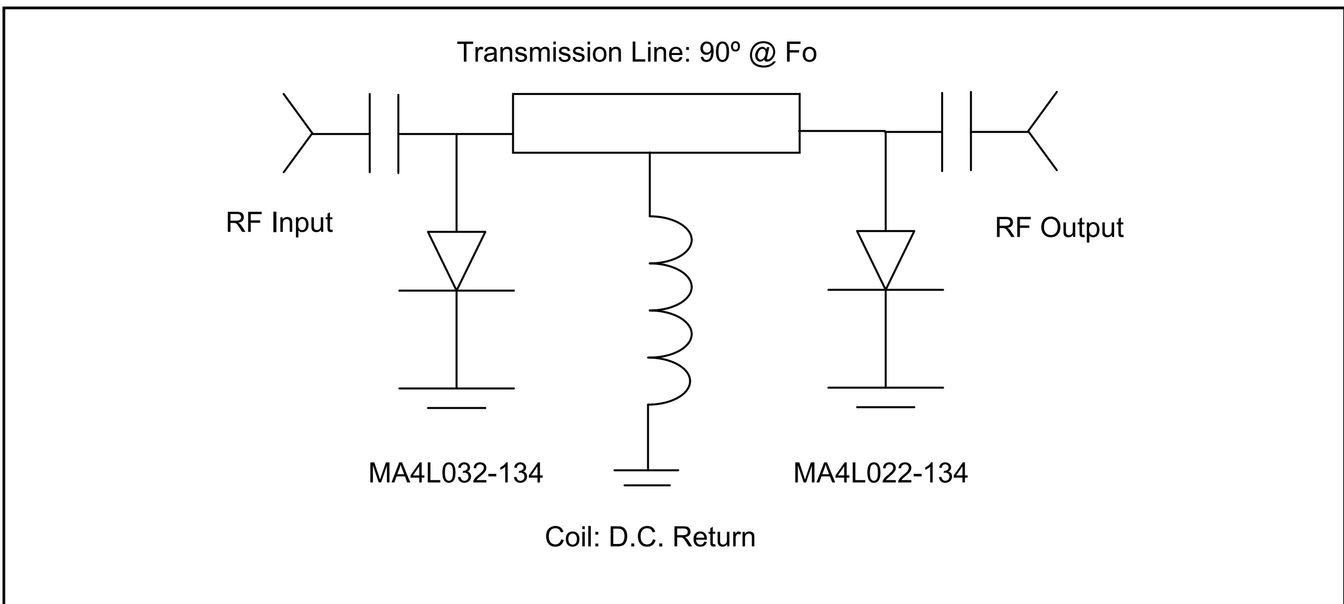
Application Circuits

Typical +60dBm Peak Power, 1µS P.W., 0.001% Duty Cycle, +20dBm Flat Leakage Limiter Circuit



Typical +50dBm Peak Power, 1µS P.W., 0.001% Duty Cycle, +20dBm Flat Leakage Limiter Circuit



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Notes for Specification and Nominal High Signal Performance Tables:

1) ***Maximum Series Resistance***: R_S, is measured at 500 MHz in the ODS-30 package and is equivalent to the total diode resistance: R_S = Rj (Junction Resistance) + R_O (Ohmic Resistance)
2) ***Nominal C.W. Thermal Resistance***: Θ_{TH} is measured in a ceramic pill package, ODS-30, mounted to a metal (infinite) heatsink. Chip only thermal resistance values are approximately 2°C/W lower than the ODS-30 listed package values in the specifications table.
3) ***Maximum High Signal Performance***: Measured using a single shunt diode (die) attached directly to the gold plated RF housing ground with 2 mil thick conductive silver epoxy in a 50Ω, SMA, connectorized test fixture. Chip anode contact is thermo-compression wire bonded using a 1 mil. diameter gold wire onto a 7.2 mil thick Rogers 5880 Duroid microstrip trace. A shunt coil provides the D.C. return. Test frequency = 9.4 GHz, RF pulse width = 1.0 μS, Duty Cycle = 0.001%.
4) ***Maximum C.W. Incident Power***: Measured in a 50Ω, SMA, connectorized housing @ 4GHz utilizing a TWT amplifier and the same single diode assembly configuration as stated in Note 3 above.

Die Handling and Mounting Information

Handling: All semiconductor chips should be handled with care in order to avoid damage or contamination from perspiration, salts, and skin oils. For individual die, the use of plastic tipped tweezers or vacuum pick up tools is strongly recommended. Bulk handling should ensure that abrasion and mechanical shock are minimized.

Die Attach: The die have Ti-Pt-Au back and anode metal, with a final gold thickness of 1.0μM. Die can be mounted with a gold-tin, eutectic solder perform or conductive silver epoxy. The metal RF and D.C. ground plane mounting surface must be free of contamination and should have a surface flatness or < ± 0.002".

- ***Eutectic Die Attachment Using Hot Gas Die Bonder:*** An 80/20, gold / tin eutectic solder perform is recommended with a work surface temperature of 255°C and a tool tip temperature of 220°C. When the hot gas is applied, the temperature at the tool tip should be approximately 290°C. The chip should not be exposed to a temperatures in excess of 320°C for more than 10 seconds.

- ***Eutectic Die Attachment Using Reflow Oven:*** Refer to Application Note M538, "Surface Mounting Instructions".

- ***Epoxy Die Attachment:*** A thin, controlled amount of electrically conductive silver epoxy should be applied, approximately 1-2 mils thick to minimize ohmic and thermal resistances. A small epoxy fillet should be visible around the outer perimeter of the chip after placement to ensure full area coverage. Cure the conductive silver epoxy per the manufacturer's schedule, typically 150˚C for 1 hour.

Wire Bonding: The chip's anode metallization stack is comprised of Ti/Pt/Au with a final gold thickness of 1.0μM. Thermo-compression wedge bonding using a .7 to 1 mil diameter gold wire is recommended, depending on the contact diameter. The heat stage temperature should be set to approximately 200°C with a bonding tip temperature of 125˚C and a force of 18 to 40 grams. Use of ultrasonic energy is not advised but if necessary it should be adjusted to the minimum required to achieve a good bond. Excessive energy or force applied to the top contact will cause the metallization to dislodge and lift off. Automatic ball bonding may also be used.

See Application Note M541, "Bonding and Handling Procedures for Chip Diode Devices" for more detailed handling and assembly information.

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Part Numbering and Ordering Information

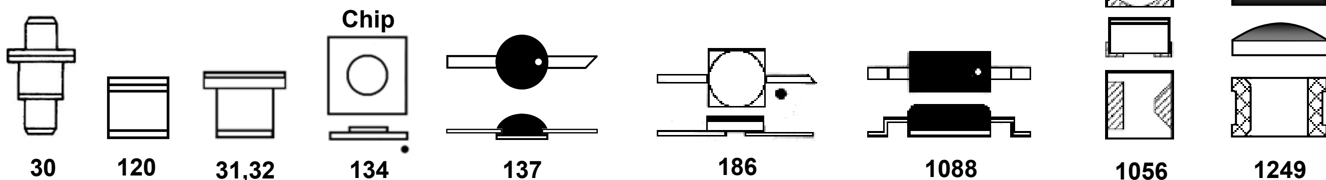
When ordering the die only, use the base part number followed by a dash and the number 134.
For example: *The chip version of base part number MA4L021 is MA4L021-134.*

When ordering packaged parts, use the base part number followed by a dash plus the associated suffix as defined in Table I "Available Case Styles" below, except where the complete part number with dash number is given.
For example: *The MA4L011-134 die in the 186 style package becomes MA4L011-186.*

The capacitance values in the specification table on page 2 lists the junction capacitance for the chip. The capacitance for the same chip in an alternative package will be different and is computed by adding the junction capacitance of the chip plus the parasitic capacitance of the alternative package as defined in Table II "Associated Package Parasitics" below.

Table I Available Case Styles

Base Part	Available Package Styles
MA4L011	30, 31, 32, 54, 134, 137,186, 1056, 1088
MA4L021	31, 120, 134, 1056
MA4L022	30, 32, 120, 134, 137, 186, 1056
MA4L031	31, 36, 134, 186, 1056
MA4L032	31, 32, 134, 186, 1056
MA4L062	134
MADL-000062-105600	1056 (uses MA4L062 chip)
MA4L101	30, 134, 186
MA4L301	31,1249, 1056
MADL-000301-01340W	134 (chip used in MA4L301 series)
MA4L401	30, 31, 120,134, 1056



Package dimensions can be found on the M/A-COM Technology Solutions website under Outline Drawings

Table II Associated Package Parasitics

Package Style	Package Description	Nominal	
		C_{PKG} pF	L_S nH
30	Ceramic Pill	0.18	0.60
31	Ceramic Pill	0.18	0.60
32	Ceramic Pill	0.30	0.40
120	Ceramic Pill	0.13	0.40
134	Chip	N/A	N/A
137	Epoxy Encapsulated Ceramic Surface Mount with Leads	0.14	0.70
186	Ceramic Surface Mount with Leads	0.15	0.70
1056	Ceramic Surface Mount with Wrap Around Contacts	0.20	0.70
1088	Epoxy Encapsulated Ceramic Surface Mount with Leads	0.12	0.70
1249	Epoxy Encapsulated Ceramic Surface Mount with Wrap Around Contacts	0.12	0.70

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