

M3776AM8A/MCA/MFA-XXXGP

SINGLE-CHIP 16-BIT MICROCOMPUTER

REJ03B0085-0100Z Rev.1.00 2004.02.17

1. DESCRIPTION

This microcomputer is a single-chip microcomputer that adopts a high-performance silicon gate CMOS process, and is contained in a 100-pin plastic mold QFP. This single-chip microcomputer is provided with an instruction queue buffer and a data buffer for executing instructions at high speed. The central processing unit runs in a 16-bit parallel processing mode but can be converted into an 8-bit parallel processing mode when necessary. This product has been designed exclusively for video equipment system controls, incorporating a time measuring circuit for VCR servo control, a real-time pattern generating circuit, analog amplifiers, an OSD display circuit, and a data slicer, among its many other peripheral capabilities.

1.1 FEATURE	S
Number of basic	instructions 103
Memory size	RAM M3776AM8A-XXXGP:2048bytes
	M3776AMCA-XXXGP:2560bytes
	M3776AMFA-XXXGP:3072bytes
	ROM M3776AM8A-XXXGP:64kbytes
	M3776AMCA-XXXGP:96kbytes
	M3776AMFA-XXXGP:120kbytes
●Instruction execu	ution time
(fastest instruction	on, 16 MHz high-speed mode) 250 ns
(fastest instruction	on, 12 MHz double-speed mode)
	167 ns
●Single power sou	ırce
In 16 MHz high-s	speed mode
(OSD/data slicer	off) 4.0 V to 5.5 V
(OSD/data slicer	on) 4.75 V to 5.25 V
In 12 MHz doubl	e-speed mode
(OSD/data slicer	off) 4.0 V to 5.5 V
(OSD/data slicer	on) 4.75 V to 5.25 V
In 32 kHz low-sp	eed mode
(OSD/data slicer	off) 2.6 V to 5.5 V
●OSD power sour	ce 4.75 V to 5.25 V
●Interrupt	23 factors, 6 levels
●16-bit timer	3
●8-bit timer	3
●Clock-synchrono	us serial I/O2
(one of which ca	n perform automatic 64-byte transfers)
●I ² C-Bus interface	e (single master) 1
●8-bit A-D convert	er1 unit (11 channel inputs)
●8-bit D-A convert	er2
●12/14-bit PWM	2
●14-bit PWM	
●Time measureme	ent circuit (TMT)
One counter fo	r measuring time to generate input signals
DRFG, CPFG, C	PPG, VSYNG, and GEN
One counter for	measuring time to generate input signals RLS

- Amplification circuits
 - CTL head control circuit, CTL amplifier, CTL schmidt circuit, drum PG circuit, drum FG circuit, capstan FG circuit, capstan FG amplifier circuit
- Pulse duty detection circuit (VISS and VASS signal detection features embedded) Measures PBCTL signal duty ratio.
- Synchronous signal separation circuit
- ●EOR output feature (HASW, CROT)2-bit output
- Watchdog timer

- 4 Embedded clock-generating circuits
 Built-in feed-back resistor between XIN–XOUT
 Built-in feed-back resistor between XCIN–XCOUT
- ●CPU double-speed enable (f(XIN) max. 12.0 MHz)
- ●ROM correction function included
- ●OSD function

Display characters	32 characters	X 16 lines
Kinds of characters	Composite Output	254 kinds
	RGB Output	285 kinds
Kinds of character size	es	8 kinds
Output method C	Composite video signal, RGB ou	utput (PAL,
N	MPAL, NTSC, NPAL)	
Special function	Display with backgrour	nd shadow
	(button display)	
^	(4 =0)	

On-chip sync correct circuit (AFC)

Data slicerOn-chip slicer for XDS

1.2 APPLICATION

VCR, TVCR

starting OSD vertical display

Remote-control noise filter (majority of 4 samplings)

Outputs real-time pattern to exterior, RECCTL signal to CTL head control circuit, trigger for start the A-D converter, trigger for

●Real-time pattern (RTP) generation circuit

and RIT

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