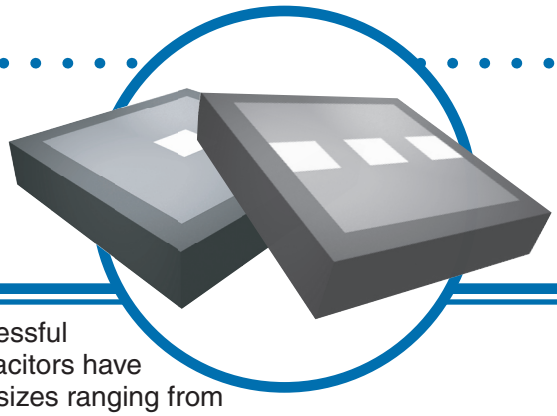
Wire Bondable Chip Capacitor

WBC Capacitor Series

- Silicon Dioxide/Silicon Nitride dielectric
- Capacitance range from 10pF to 1000pF
- Silicon substrate with gold or aluminum backing

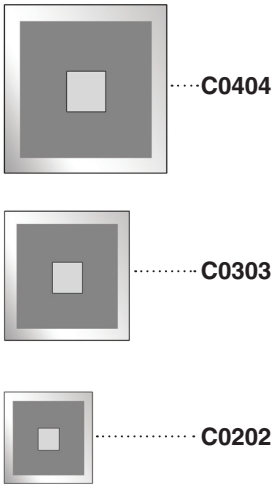


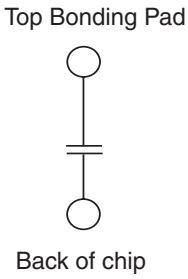
IRC's wire-bondable chip capacitors are based on the successful TaNCAP® line of RC networks on silicon. The new chip capacitors have the advantage of excellent performance in extremely small sizes ranging from 20 to 60 mils square.

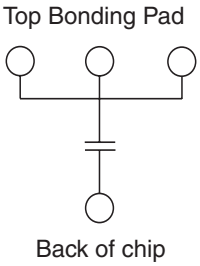
Capacitors are 100% electrically tested with mil screening to MIL-STD-883 also available.

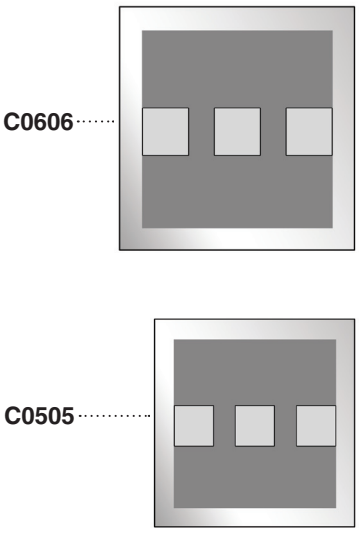
For demanding hybrid circuit and/or chip and wire applications, specify IRC's WBC capacitor series.

Physical Data









Manufacturing Capabilities Data

Style	Size	Capacitance Range	Voltage
C0202	0.020″± 0.001 sq. (0.508mm ±0.025)	10pF to 51pF	40
C0303	0.030″± 0.001 sq. (0.762mm ±0.025)	33pF to 100pF	55
C0404	0.040″± 0.001 sq. (1.016mm ±0.025)	56pF to 220pF	50
C0505	0.055″± 0.001 sq. (1.397mm ±0.025)	160pF to 360pF	20
C0606	0.060″± 0.001 sq. (1.524mm ±0.025)	160pF to 1000pF	20

General Note
IRC reserves the right to make changes in product specification without notice or liability.
All information is subject to IRC's own data and is considered accurate at time of going to print.

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Wire Bondable Chip Capacitor

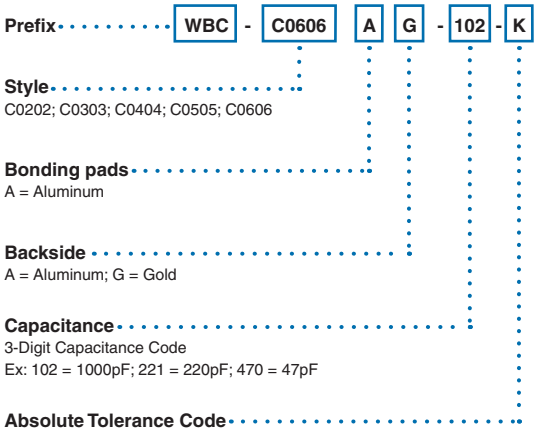
Electrical Data

Capacitance Range	10pF to 1000pF
Dissipation Factor 1Khz, +25°C, 1V$_{RMS}$	0.5% min
Absolute Tolerance	to ±5%
Operating Temperature	-55°C to +125°C
Noise	<-30dB
Substrate Material	Semiconductor Silicon (10KÅ SiO_2 minimum)
Substrate Thickness	0.010˝ ±0.001 (0.254mm ±0.025)
Bond Pad Metallization	Aluminum: 10KÅ minimum
Backside	Aluminum: 10KÅ minimum Gold: 3KÅ minimum
Dielectric	Silicon Dioxide and/or Silicon Nitride
Passivation	Silicon Dioxide or Silicon Nitride

Environmental Data

Test	Method	Max ΔC
Thermal Shock	MIL-STD-202 Method 107 Test condition F	±0.25% + 0.25pF max
Moisture Resistance	MIL-STD-202 Method 106	±1.0% + 0.25pF max
Short Time Overload	+25°C, 5 seconds 1.5 X rated voltage	±0.25% + 0.25pF mx
Life at Elevated Temperature	MIL-STD-202 Method 108 125°C, 1000 hours	±0.25% + 0.25pF max
High Temperature Exposure	100 hours @ 150°C ambient	±0.25% + 0.25pF max

Ordering Data



Packaging
Standard packaging is 2˝ x 2˝ chip tray. For additional information or to discuss your specific requirements, please contact our Applications Team using the contact details below.