

Single P-channel MOSFET

ELM17415GA-S

■ General description

ELM17415GA-S uses advanced trench technology to provide excellent $R_{ds(on)}$, low gate charge and operation with gate voltages as low as 2.5V and internal ESD protection.

■ Features

- $V_{ds} = -20V$
- $I_d = -2A$ ($V_{gs} = -10V$)
- $R_{ds(on)} < 100m\Omega$ ($V_{gs} = -10V$)
- $R_{ds(on)} < 125m\Omega$ ($V_{gs} = -4.5V$)
- $R_{ds(on)} < 170m\Omega$ ($V_{gs} = -2.5V$)
- ESD Rating : 2000V HBM

■ Maximum absolute ratings

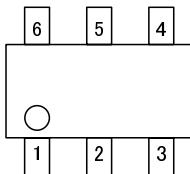
Parameter	Symbol	Limit	Unit	Note
Drain-source voltage	V_{ds}	-20	V	
Gate-source voltage	V_{gs}	± 12	V	
Continuous drain current	I_d	-2.0	A	1
Ta=70°C		-1.6		
Pulsed drain current	I_{dm}	-8	A	2
Power dissipation	P_d	0.625	W	1
Ta=25°C		0.400		
Junction and storage temperature range	T_j, T_{stg}	-55 to 150	°C	

■ Thermal characteristics

Parameter		Symbol	Typ.	Max.	Unit	Note
Maximum junction-to-ambient	t≤10s	$R_{\theta ja}$	160	200	°C/W	1
Maximum junction-to-ambient	Steady-state		180	220	°C/W	
Maximum junction-to-lead	Steady-state	$R_{\theta jl}$	130	160	°C/W	3

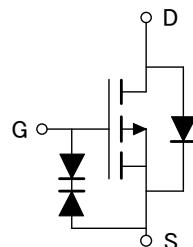
■ Pin configuration

SC-70-6 (TOP VIEW)



Pin No.	Pin name
1	DRAIN
2	DRAIN
3	GATE
4	SOURCE
5	DRAIN
6	DRAIN

■ Circuit



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■ Electrical characteristics

T_a=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	BVdss	Id=-250 μA, Vgs=0V	-20			V
Zero gate voltage drain current	Idss	Vds=-16V Vgs=0V			-0.5 -2.5	μA
Gate-body leakage current	Igss	Vds=0V, Vgs=±10V Vds=0V, Vgs=±12V			±1 ±10	μA
Gate threshold voltage	Vgs(th)	Vds=Vgs, Id=-250 μA	-0.7	-0.9	-1.4	V
On state drain current	Id(on)	Vgs=-4.5V, Vds=-5V	-15			A
Static drain-source on-resistance	Rds(on)	Vgs=-10V Id=-2A	80	100		m Ω
		Tj=125°C	115			
		Vgs=-4.5V, Id=-1.3A	98	125		m Ω
		Vgs=-2.5V, Id=-1A	130	170		m Ω
Forward transconductance	Gfs	Vds=-5V, Id=-2A	5			S
Diode forward voltage	Vsd	Is=-1A, Vgs=0V		-0.84	-0.95	V
Max. body-diode continuous current	Is				-0.6	A
DYNAMIC PARAMETERS						
Input capacitance	Ciss	Vgs=0V, Vds=-10V, f=1MHz		512	620	pF
Output capacitance	Coss			77		pF
Reverse transfer capacitance	Crss			62		pF
Gate resistance	Rg	Vgs=0V, Vds=0V, f=1MHz		9.2	13.0	Ω
SWITCHING PARAMETERS						
Total gate charge	Qg	Vgs=-4.5V, Vds=-10V Id=-2A		4.9	6.0	nC
Gate-source charge	Qgs			3.5		nC
Gate-drain charge	Qgd			3.7		nC
Turn-on delay time	td(on)	Vgs=-4.5V, Vds=-10V Rl=5 Ω, Rgen=3 Ω		11	13	ns
Turn-on rise time	tr			8	10	ns
Turn-off delay time	td(off)			34	41	ns
Turn-off fall time	tf			12	15	ns
Body diode reverse recovery time	trr	If=-2A, dl/dt=100A/μs		13	17	ns
Body diode reverse recovery charge	Qrr	If=-2A, dl/dt=100A/μs		4	6	nC

NOTE :

1. The value of R_{θja} is measured with the device mounted on 1in² FR-4 board of 2oz. Copper, in still air environment with T_a=25°C. The value in any given applications depends on the user's specific board design, The current rating is based on the t ≤ 10s thermal resistance rating.
2. Repetitive rating, pulse width limited by junction temperature.
3. The R_{θja} is the sum of the thermal impedance from junction to lead R_{θjl} and lead to ambient.
4. The static characteristics in Figures 1 to 6 are obtained using 80μs pulses, duty cycle 0.5%max.
5. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_a=25°C. The SOA curve provides a single pulse rating.

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■ Typical electrical and thermal characteristics

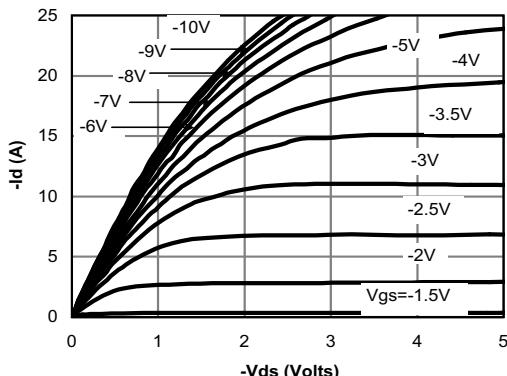


Fig 1: On-Region Characteristics

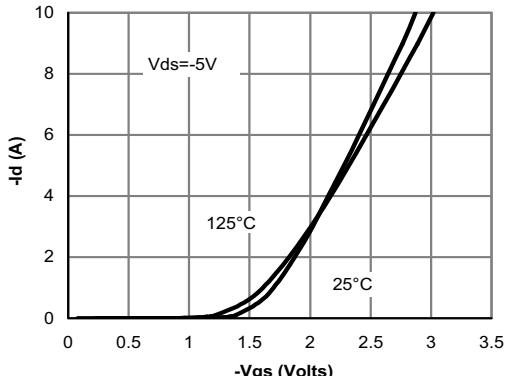


Figure 2: Transfer Characteristics

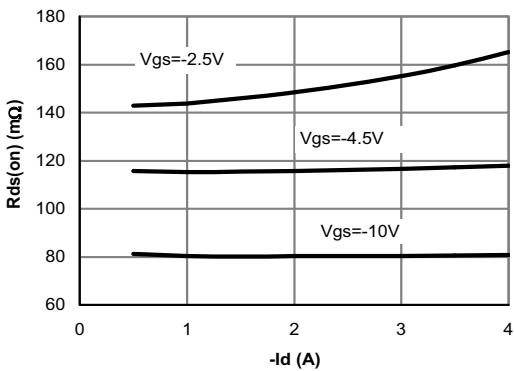


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

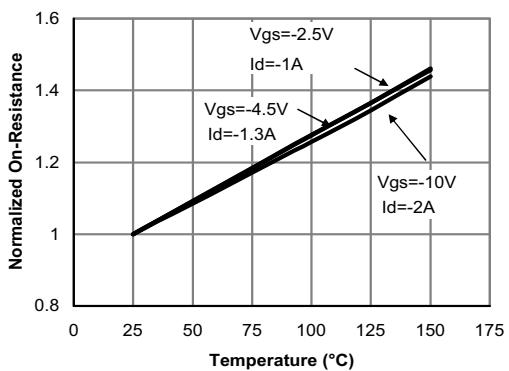


Figure 4: On-Resistance vs. Junction Temperature

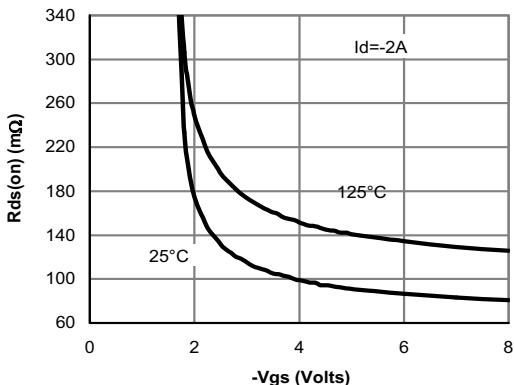


Figure 5: On-Resistance vs. Gate-Source Voltage

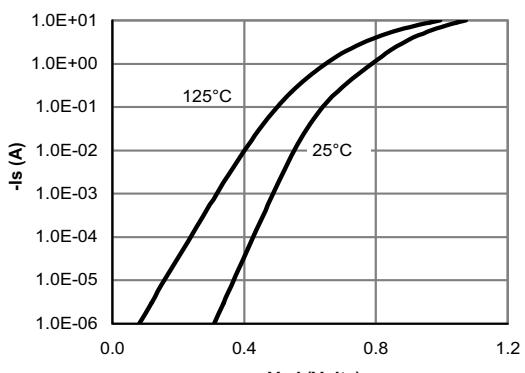


Figure 6: Body-Diode Characteristics

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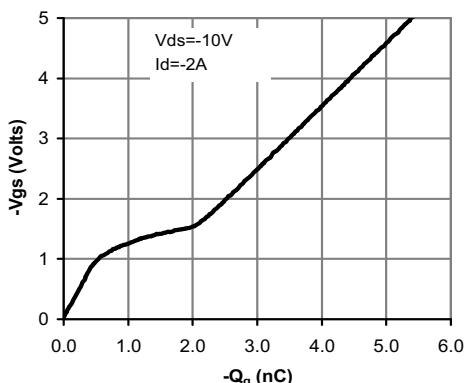


Figure 7: Gate-Charge Characteristics

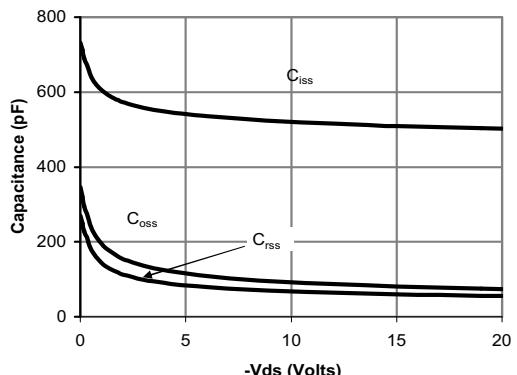


Figure 8: Capacitance Characteristics

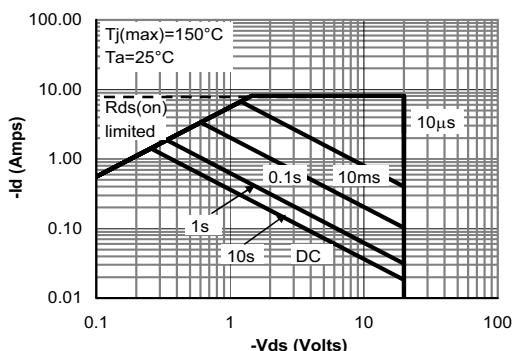


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

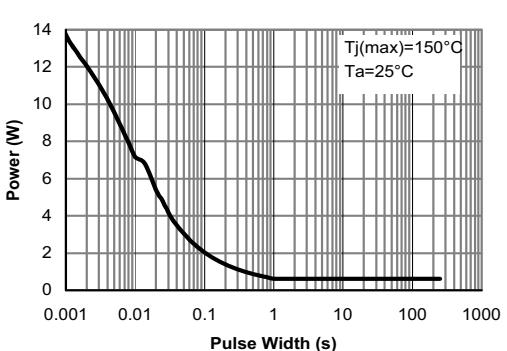


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

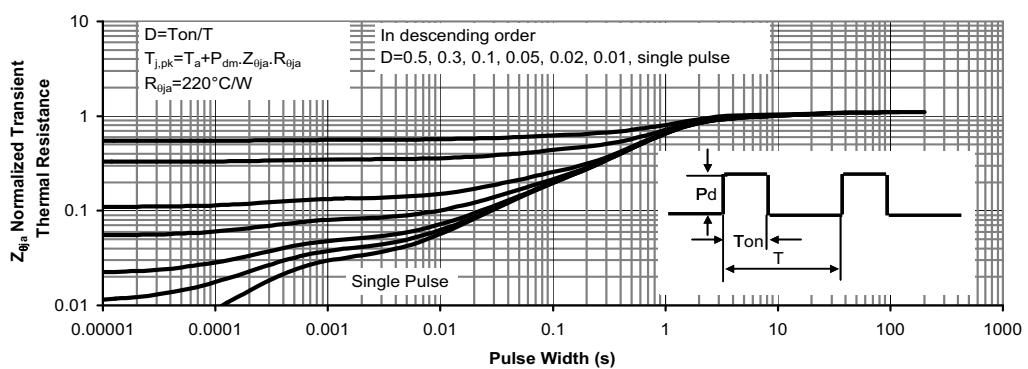


Figure 11: Normalized Maximum Transient Thermal Impedance