Wideband/Video “T” Switches

FEATURES

- Wide Bandwidth: 500 MHz
- Low Crosstalk: –85 dB
- High Off-Isolation: –80 dB @ 5 MHz
- “T” Switch Configuration
- TTL and CMOS Logic Compatible
- Fast Switching—t_{ON}: 45 ns
- Low $r_{DS(on)}$: 30 Ω

BENEFITS

- Flat Frequency Response
- High Color Fidelity
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Reduced Power Consumption
- Improved Data Throughput

APPLICATIONS

- RF and Video Switching
- RGB Switching
- Local and Wide Area Networks
- Video Routing
- Fast Data Acquisition
- ATE
- Radar/FLR Systems
- Video Multiplexing

DESCRIPTION

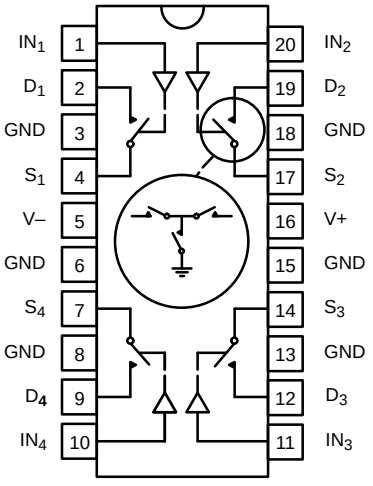
The DG540/541/542 are high performance monolithic wideband/video switches designed for switching RF, video and digital signals. By utilizing a “T” switch configuration on each channel, these devices achieve exceptionally low crosstalk and high off-isolation. The crosstalk and off-isolation of the DG540 are further improved by the introduction of extra GND pins between signal pins.

To achieve TTL compatibility, low channel capacitances and fast switching times, the DG540 family is built on the Vishay Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when on.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG540

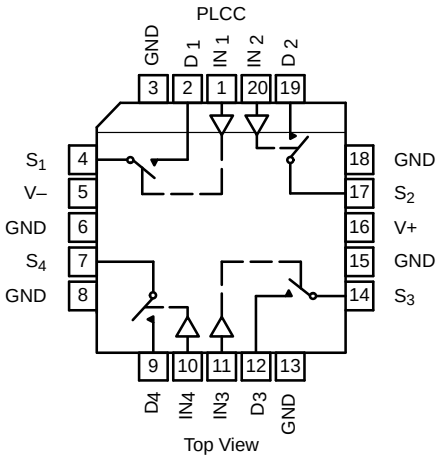
Dual-In-Line



Top View

DG540

PLCC



Top View

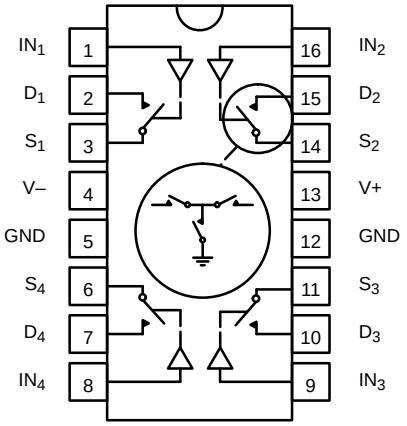
TRUTH TABLE	
Logic	**Switch**
0	OFF
1	ON

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2 V

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG541

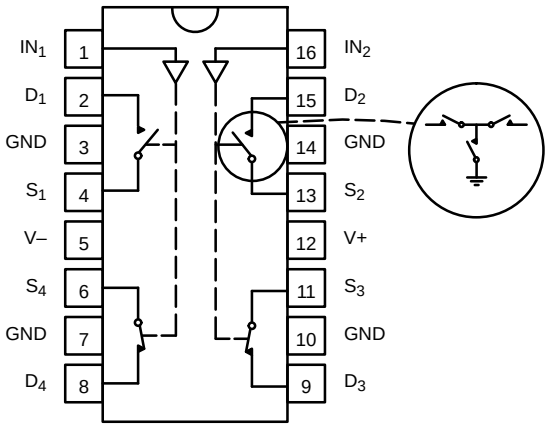
Dual-In-Line and SOIC



Top View

DG542

Dual-In-Line and SOIC



Top View

TRUTH TABLE - DG541	
Logic	**Switch**
0	OFF
1	ON

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2 V

TRUTH TABLE - DG542		
Logic	**SW_1, SW_2**	**SW_3, SW_4**
0	OFF	ON
1	ON	OFF

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
DG540		
–40 to 85°C	20-Pin Plastic DIP	DG540DJ
	20-Pin PLCC	DG540DN
–55 to 125°C	20-Pin Sidebraze	DG540AP
		DG540AP/883
DG541		
–40 to 85°C	16-Pin Plastic DIP	DG541DJ
	16-Pin Narrow SOIC	DG541DY
–55 to 125°C	16-Pin Sidebraze	DG541AP
		DG541AP/883, 5962-9076401MEA
DG542		
–40 to 85°C	16-Pin Plastic DIP	DG542DJ
	16-Pin Narrow SOIC	DG542DY
–55 to 125°C	16-Pin Sidebraze	DG542AP
		DG542AP/883, 5962-91555201MEA

ABSOLUTE MAXIMUM RATINGS

V+ to V– ..... –0.3 V to 21 V
V+ to GND ..... –0.3 V to 21 V
V– to GND ..... –19 V to +0.3 V
Digital Inputs ..... (V–) –0.3 V to (V+) +0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V–) –0.3 V to (V–) +14 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 20 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max) ..... 40 mA
Storage Temperature (AP Suffix) ..... –65 to 150°C
(DJ, DN, DY Suffixes) ..... –65 to 125°C

Power Dissipation (Package)a
16-Pin Plastic DIP[b] ..... 470 mW
20-Pin Plastic DIP[c] ..... 800 mW
16-Pin Narrow Body SOIC[d] ..... 640 mW
20-Pin PLCC[d] ..... 800 mW
16-, 20-Pin Sidebraze DIP[e] ..... 900 mW

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 6.5 mW/°C above 25°C
c. Derate 7 mW/°C above 25°C
d. Derate 10 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

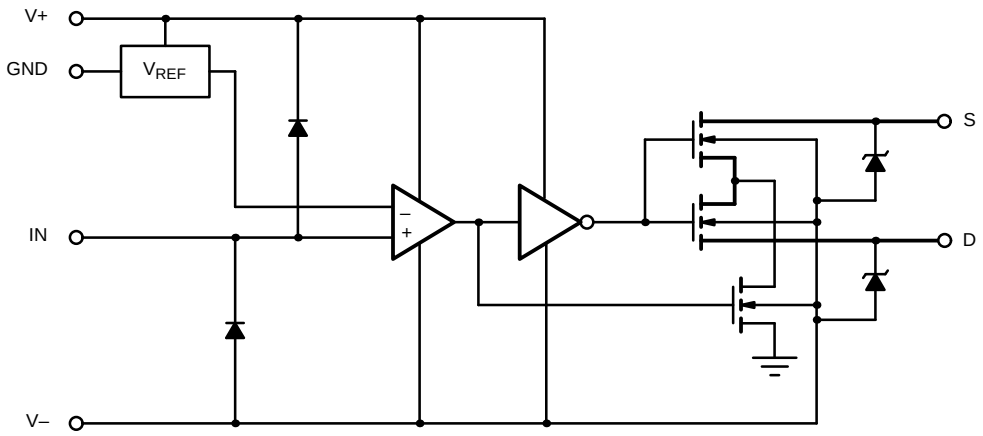


FIGURE 1.

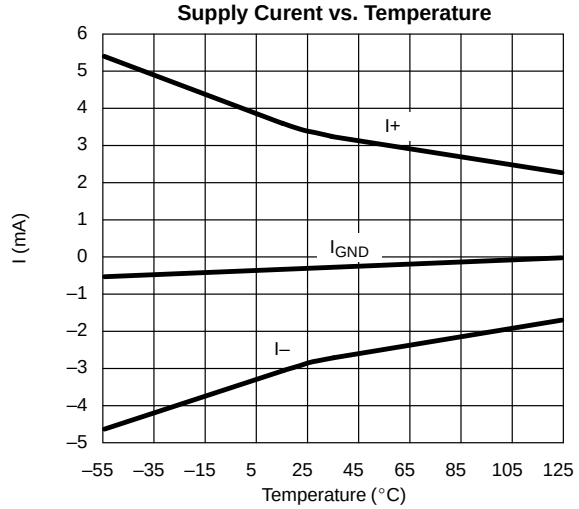
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V– = –3 V V_{INH} = 2 V, V_{INL} = 0.8 V[f]		Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffixes –40 to 85°C Min[d]	D Suffixes –40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range	V_{ANALOG}	V– = –5 V, V+ = 12 V		Full		–5	5	–5	5	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = 0 V		Room Full	30		60 100		60 75	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$			Room	2		6		6	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V		Room Full	–0.05	–10 –500	10 500	–10 –100	10 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0 V		Room Full	–0.05	–10 –500	10 500	–10 –100	10 100	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V		Room Full	–0.05	–10 –1000	10 1000	–10 –100	10 100	
Digital Control										
Input Voltage High	V_{INH}			Full		2		2		V
Input Voltage Low	V_{INL}			Full			0.8		0.8	
Input Current	I_{IN}	V_{IN} = GND or V+		Room Full	0.05	–1 –20	1 20	–1 –20	1 20	µA
Dynamic Characteristics										
On State Input Capacitance[e]	$C_{S(on)}$	V_S = V_D = 0 V		Room	14		20		20	pF
Off State Input Capacitance[e]	$C_{S(off)}$	V_S = 0 V		Room	2		4		4	
Off State Output Capacitance[e]	$C_{D(off)}$	V_D = 0 V		Room	2		4		4	
Bandwidth	BW	R_L = 50 Ω, See Figure 5		Room	500					MHz
Turn On Time	t_{ON}	R_L = 1 kΩ C_L = 35 pF 50% to 90% See Figure 2	DG540 DG541	Room Full	45		70 130		70 130	ns
			DG542	Room Full	55		100 160		100 160	
Turn Off Time	t_{OFF}		DG540 DG541	Room Full	20		50 85		50 85	
			DG542	Room Full	25		60 85		60 85	
Charge Injection	Q	C_L = 1000 pF, V_S = 0 V See Figure 3		Room	–25					pC
Off Isolation	OIRR	R_{IN} = 75 Ω R_L = 75 Ω f = 5 MHz See Figure 4	DG540	Room	–80					dB
			DG541	Room	–60					
			DG542	Room	–75					
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω f = 5 MHz, See Figure 6		Room	–85					
Power Supplies										
Positive Supply Current	I+	All Channels On or Off		Room Full	3.5		6 9		6 9	mA
Negative Supply Current	I–			Room Full	–3.2	–6 –9		–6 –9		

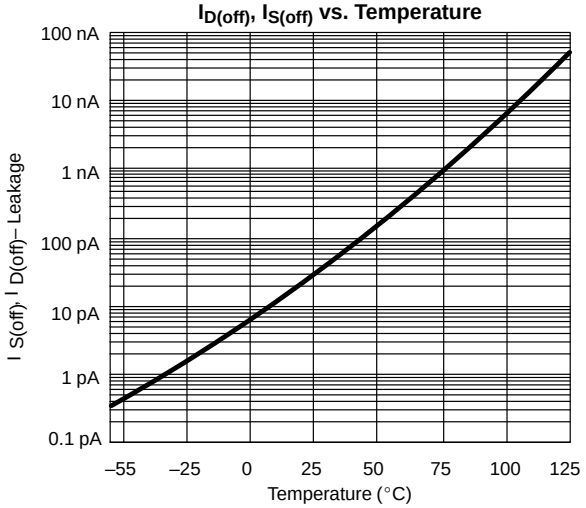
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

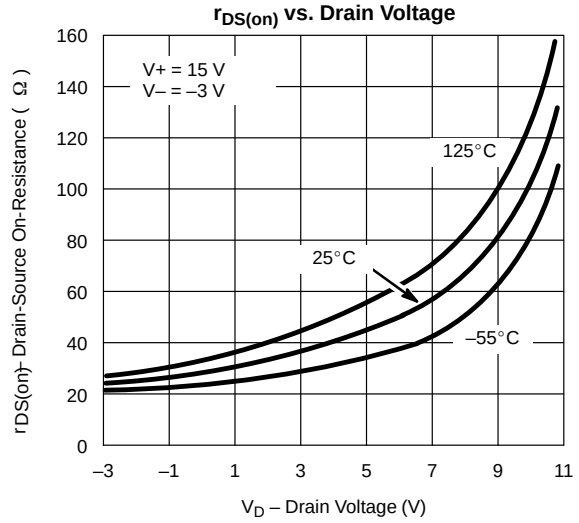
Supply Curent vs. Temperature



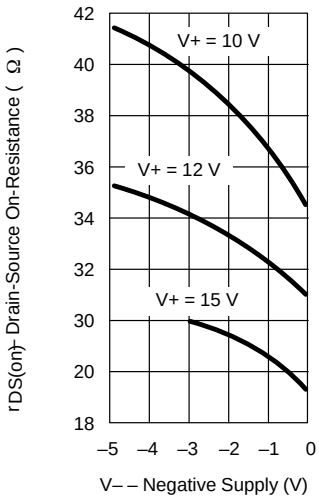
$I_{D(off)}$, $I_{S(off)}$ vs. Temperature



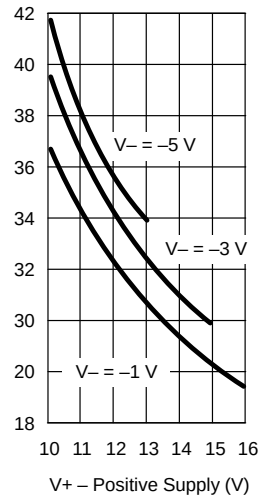
$r_{DS(on)}$ vs. Drain Voltage



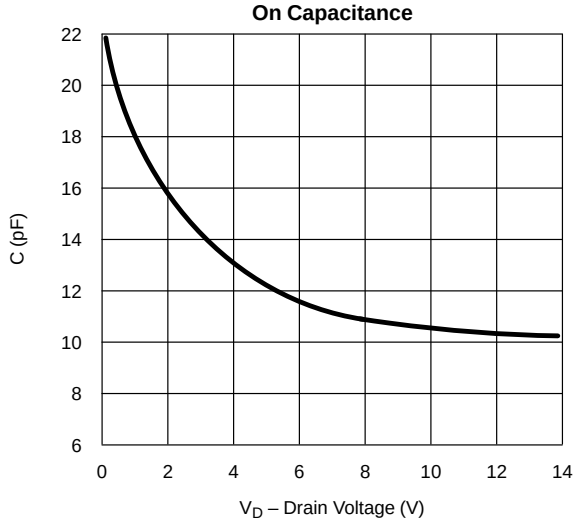
V+ Constant



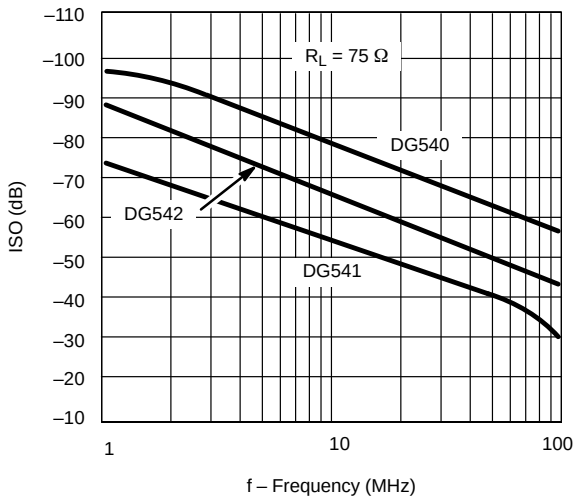
V– Constant



On Capacitance

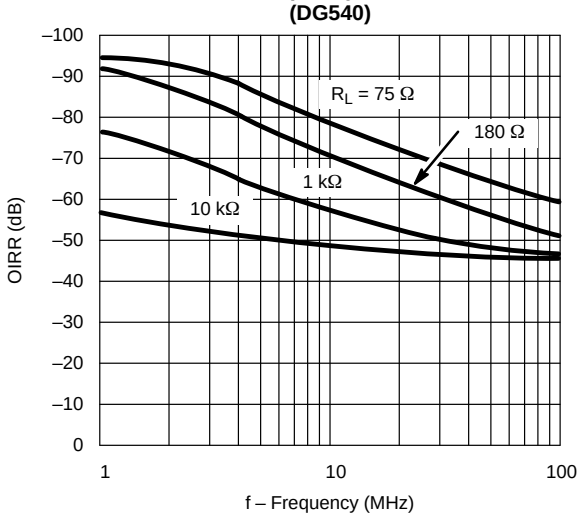


Off Isolation

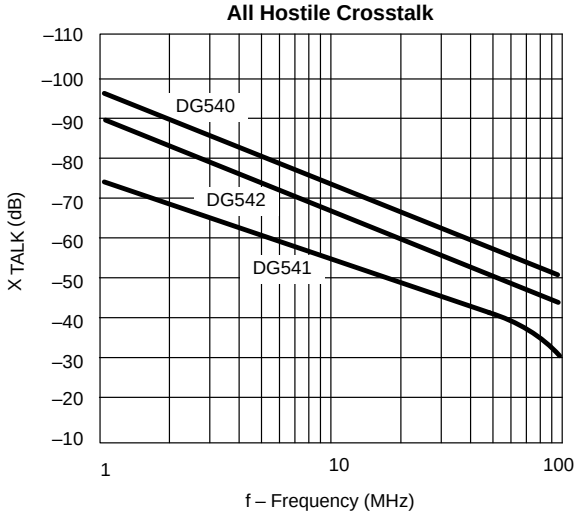


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

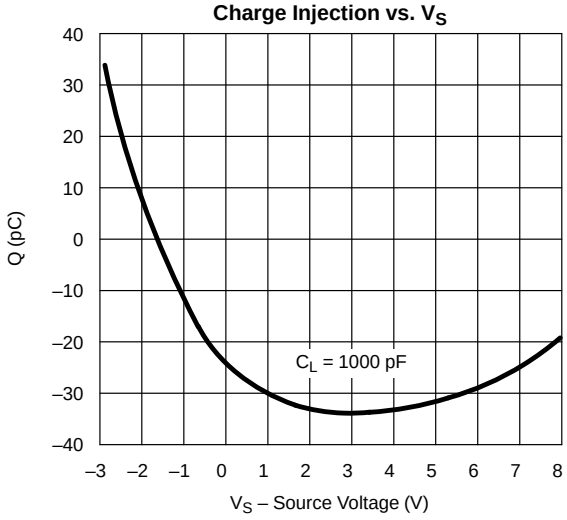
Off Isolation vs. Frequency and Load Resistance (DG540)



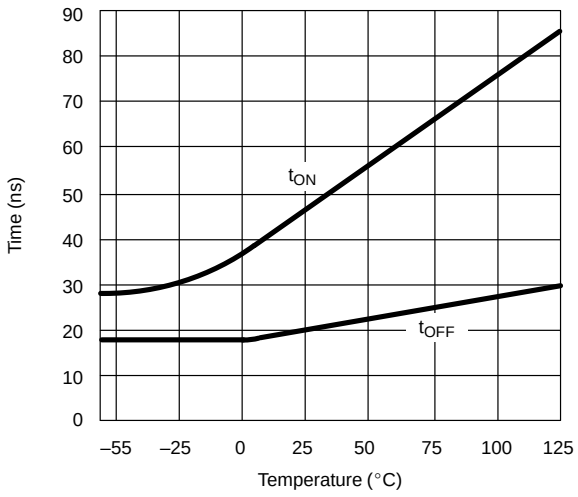
All Hostile Crosstalk



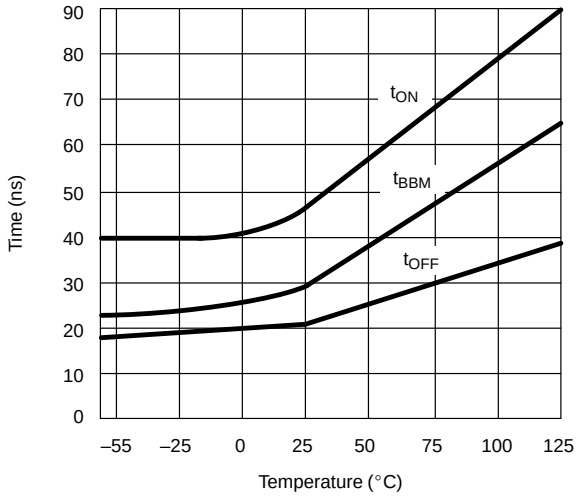
Charge Injection vs. V_S



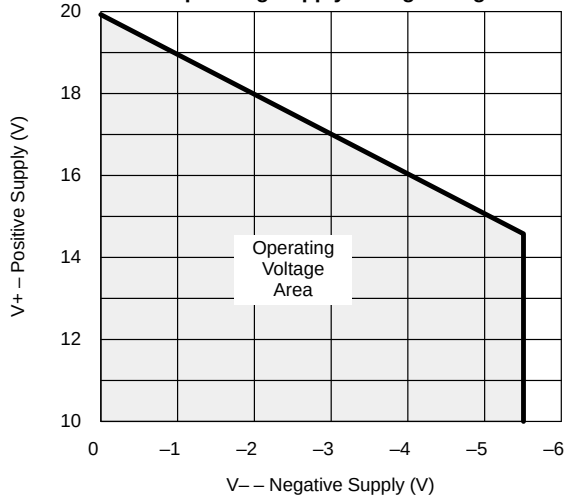
Switching Times vs. Temperature (DG540/541)



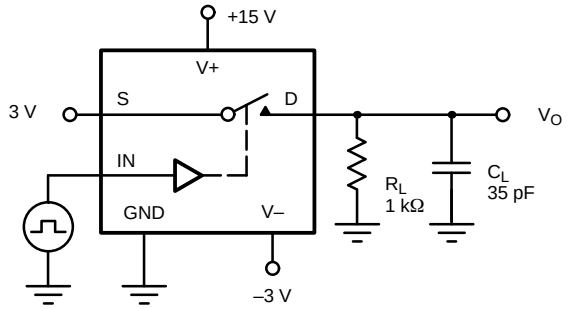
Switching and Break-Before-Make Time vs. Temperature (DG542)



Operating Supply Voltage Range



TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

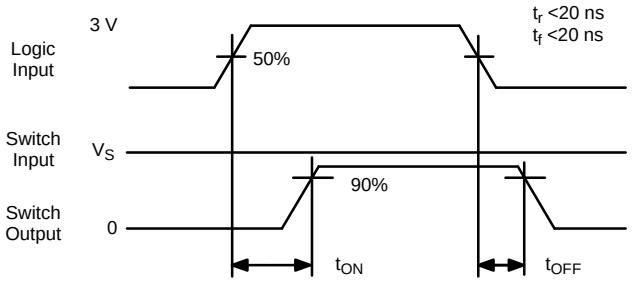
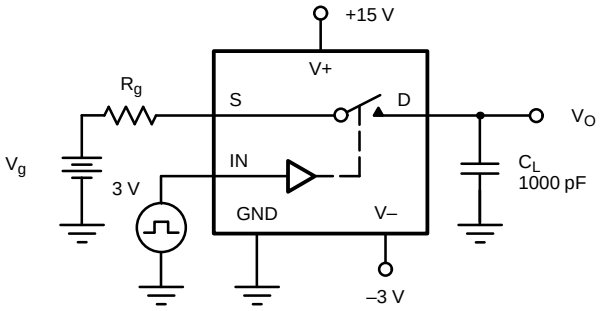
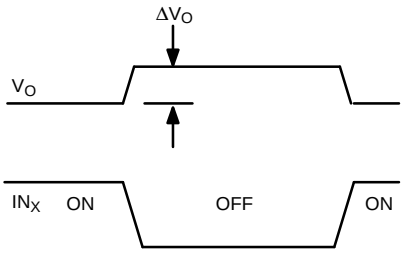


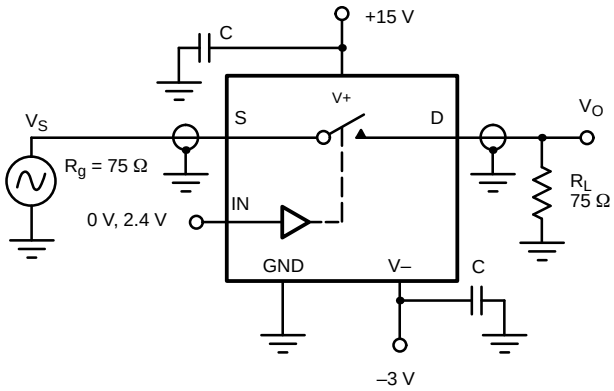
FIGURE 2. Switching Time





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $\Delta Q = C_L \times DV_O$

FIGURE 3. Charge Injection



Off Isolation = 20 log $\left| \frac{V_S}{V_O} \right|$

C = RF Bypass

FIGURE 4. Off Isolation

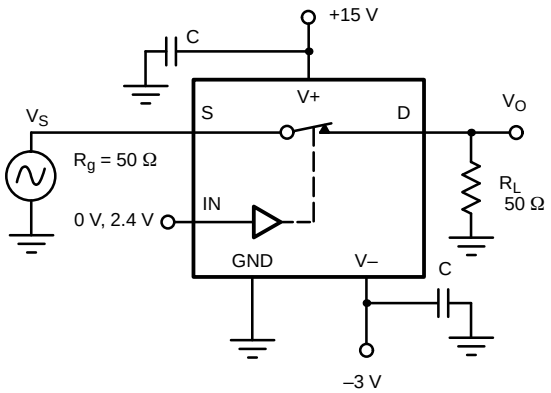


FIGURE 5. Bandwidth

TEST CIRCUITS

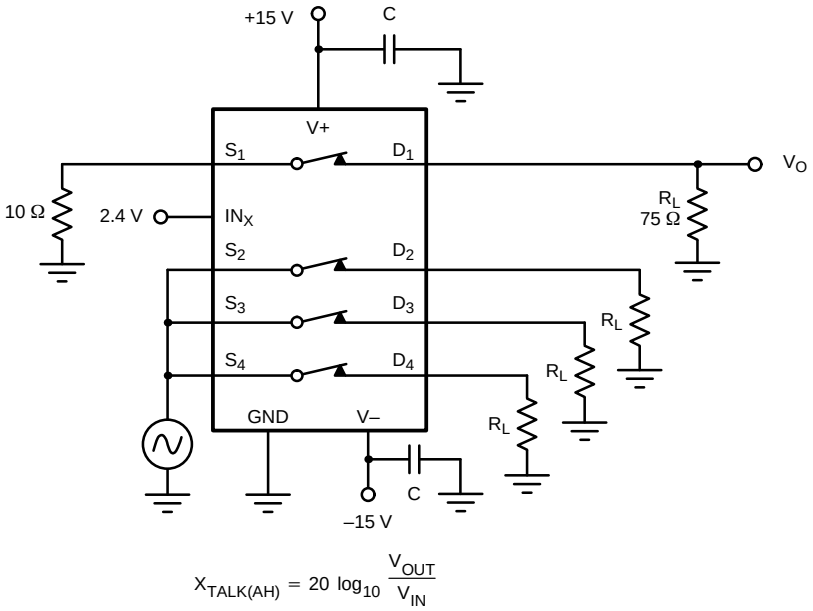


FIGURE 6. All Hostile Crosstalk

APPLICATIONS

Device Description

The DG540/541/542 family of wideband switches offers true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay.

Built on the Siliconix D/CMOS process, these "T" switches provide excellent off-isolation with a bandwidth of around 500 MHz (350 MHz for DG541). Silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

Frequency Response

A single switch on-channel exhibits both resistance [$r_{DS(on)}$] and capacitance [$C_{S(on)}$]. This RC combination has an attenuation effect on the analog signal – which is frequency dependent (like an RC low-pass filter). The –3-dB bandwidth of the DG540 is typically 500 MHz (into 50 Ω). This measured figure of 500 MHz illustrates that the switch channel can not be represented by a two stage RC combination. The on capacitance of the channel is distributed along the on-resistance, and hence becomes a more complex multi stage network of R's and C's making up the total $r_{DS(on)}$ and $C_{S(on)}$. See Application Note AN502 for more details.

Off-Isolation and Crosstalk

Off-isolation and crosstalk are affected by the load resistance and parasitic inter-electrode capacitances. Higher off-isolation is achieved with lower values of R_L. However, low values of R_L increase insertion loss requiring gain adjustments down the line. Stray capacitances, even a fraction of 1 pF, can cause a large crosstalk increase. Good layout and ground shielding techniques can considerably improve your ac circuit performance.

APPLICATIONS

Power Supplies

A useful feature of the DG54X family is its power supply flexibility. It can be operated from a single positive supply (V+) if required (V– connected to ground).

Note that the analog signal must not exceed V– by more than –0.3 V to prevent forward biasing the substrate p-n junction. The use of a V– supply has a number of advantages:

1. It allows flexibility in analog signal handling, i.e., with V– = –5 V and V+ = 12 V; up to ±5-V ac signals can be controlled.
2. The value of on capacitance [$C_{S(on)}$] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in $C_{S(on)}$ for an increasing V body–source. Note, however, that to increase V– normally requires V+ to be reduced (since V+ to V– = 21 V max.). Reduction in V+ causes an increase in $r_{DS(on)}$, hence a compromise has to be achieved. It is also useful to note that optimum video linearity performance (e.g., differential phase and gain) occurs when V– is around –3 V.
3. V– eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

Decoupling

It is an established RF design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG54X is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential.

Rules:

1. Decoupling capacitors should be incorporated on all power supply pins (V+, V–). (See Figure 7.)
2. They should be mounted as close as possible to the device pins.
3. Capacitors should have good high frequency characteristics – tantalum bead and/or monolithic ceramic types are adequate.

Suitable decoupling capacitors are 1- to 10-μF tantalum bead, plus 10- to 100-nF ceramic.

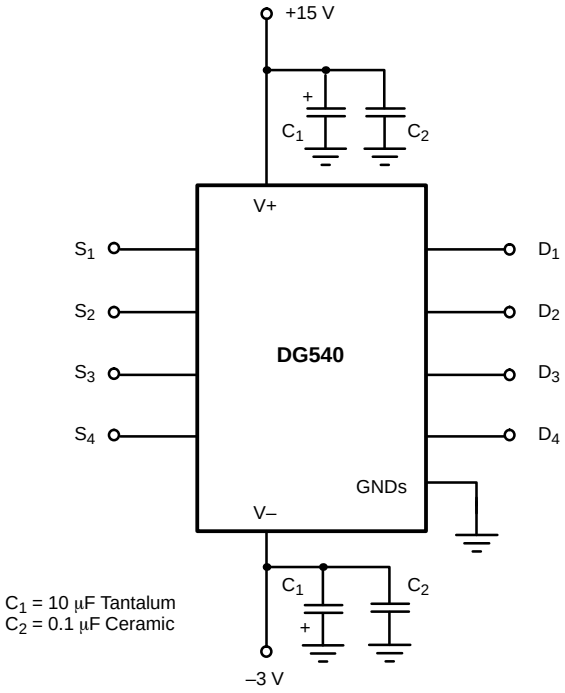


FIGURE 7. Supply Decoupling

Board Layout

PCB layout rules for good high frequency performance must be observed to achieve the performance boasted by the DG540. Some tips for minimizing stray effects are:

1. Use extensive ground planes on double sided PCB, separating adjacent signal paths. Multilayer PCB is even better.
2. Keep signal paths as short as practically possible, with all channel paths of near equal length.
3. Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current flowing through ground path parasitic resistance from coupling between channels.

APPLICATIONS

Figure 8 shows a 4-channel video multiplexer using a DG540.

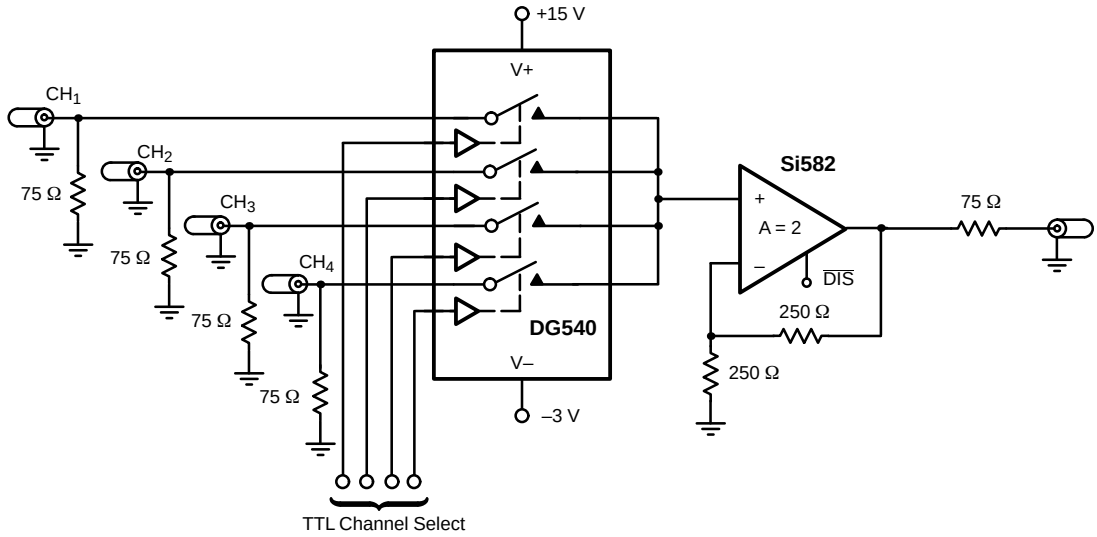


FIGURE 8. 4 by 1 Video Multiplexing Using the DG540

Figure 9 shows an RGB selector switch using two DG542s.

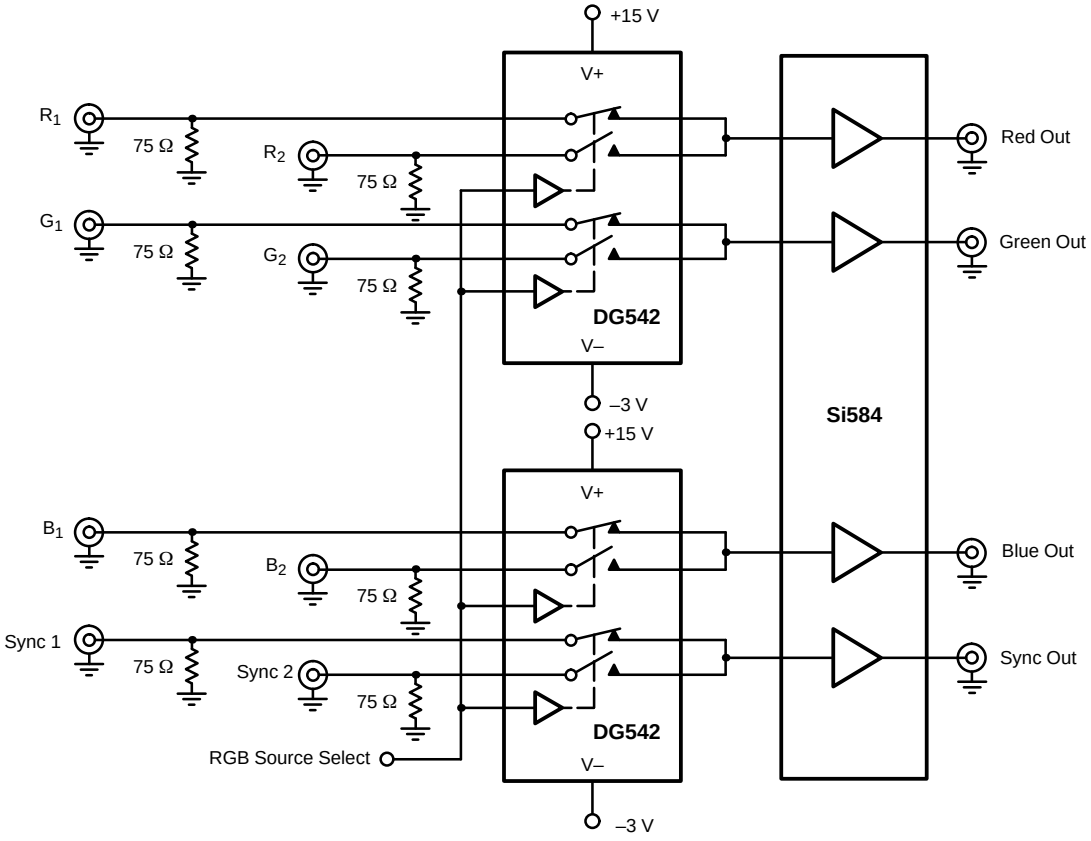


FIGURE 9. RGB Selector Using Two DG542s

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