AKD4620B-B
AK4620B Evaluation board Rev.1

GENERAL DESCRIPTION

The AKD4620B-B is an evaluation board for the AK4620B, the 24Bit A/D & D/A converter. The AKD4620B-B can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D→D/A). The AKD4620B-B also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4620B-B --- Evaluation board for AK4620B
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

☐ Digital interface
- **DIT (AK4114): optical or BNC**
- **DIR (AK4114): optical or BNC**

☐ 10pin header for serial control interface

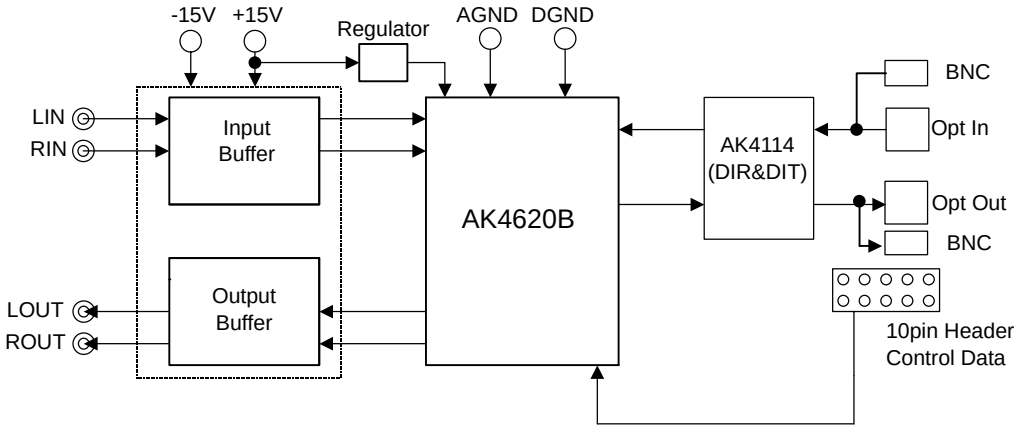


Figure 1. AKD4620B-B Block Diagram

* Circuit diagram are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply line

[+15V]	(green)	= +15V
[-15V]	(blue)	= -15V
[GND]	(black)	= 0V

Note: Each supply line should be distributed from the power supply unit.

2) Set up the evaluation modes, jumper pins and DIP switch. (See the followings.)

3) Power on

The AK4620B should be reset once bringing SW2 (PDN) “L” upon power-up.

■ Evaluation modes

Applicable evaluation modes

(1) Loopback mode (Default)
(2) Evaluation of DAC
(3) Evaluation of ADC

1) Loopback mode (Default)

1-1) Analog input mode

Jumper	JP3 (LIN)	JP4 (AINL)	JP5 (RIN)	JP6 (AINR)	SW1-2 (ADMODE)	
Single-ended	SINGLE	SINGLE	SINGLE	SINGLE	OFF	
Differential	DIFF	DIFF	DIFF	DIFF	ON	(Default)

Table 1. Analog Input Mode

* As for analog input circuit, please see the following item "Analog Input Buffer Circuit".

1-2) Sampling speed & MCLK frequency

a) parallel mode

SW1-1 (P/S)	SW1-4 (DFS0)	SW1-6 (CKS1)	SW1-7 (CKS0)	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4620B	MCLK Frequency of AK4620B	
ON	OFF	OFF	ON	ON	OFF	Normal Speed	512fs	(Default)
ON	ON	OFF	ON	OFF	OFF	Double Speed	256fs	

Table 2. Sampling Speed & Master clock Frequency in parallel mode

* Parallel mode does not support quad speed mode.

b) serial mode

SW1 (P/S)	DFS1 bit	DFS0 bit	CMODE bit	CKS1 bit	CKS0 bit	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4620B	MCLK Frequency of AK4620B
OFF	0	0	0	0	1	ON	OFF	Normal Speed	512fs
OFF	0	1	0	0	1	OFF	OFF	Double Speed	256fs
OFF	1	0	0	0	1	ON	ON	Quad Speed	128fs

Table 3. Sampling Speed & Master clock Frequency in serial mode

* In serial mode, SW1-4(DFS0), SW1-6(CKS1) and SW1-7(CSK0) should be always "OFF", and DFS1, DFS0, CKS1, CKS0 and CMODE bits in the AK4620B should be set via the printer port (PORT3).

1-3) AK4114's master clock mode & reference X'tal frequency

Mode	SW3-6 (CM1)	SW3-7 (CM0)	PLL	X'tal	Clock source	SDTO	
1	OFF	ON	OFF	ON	X'tal	DAUX	(Default)

Table 4. AK4114'S Clock Operation Mode

SW3-1 (XTL1)	SW3-2 (XTL0)	X'tal Frequency	
ON	OFF	24.576MHz	(Default)

Table 5. Reference X'tal frequency

2) Evaluation of D/A using DIR. (Optical link)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT1). PORT1 is also used for the evaluation using such as CD test disk.

BNC connector is recommended for an evaluation of the Sound quality.

2-1) DIR input interface (Default: JP2="OPT")

Jumper	JP2 (RX3)
Normal & Double Speed	OPT or BNC
Quard Speed	BNC

Table 6. DIR Input Interface

2-2) Sampling speed & MCLK frequency

a) parallel mode

SW1-1 (P/S)	SW1-4 (DFS0)	SW1-6 (CKS1)	SW1-7 (CKS0)	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4620B	MCLK Frequency of AK4620B
ON	OFF	OFF	OFF	OFF	OFF	Normal Speed	256fs
ON	OFF	OFF	ON	ON	OFF	Normal Speed	512fs
ON	ON	OFF	ON	OFF	OFF	Double Speed	256fs

Table 7. Sampling Speed & Master clock Frequency in parallel mode

* Parallel mode does not support quad speed mode.

b) serial mode

SW1-1 (P/S)	DFS1 bit	DFS0 bit	CMODE bit	CKS1 bit	CKS0 bit	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4620B	MCLK Frequency of AK4620B
OFF	0	0	0	0	0	OFF	OFF	Normal Speed	256fs
OFF	0	0	0	0	1	ON	OFF	Normal Speed	512fs
OFF	0	1	0	0	1	OFF	OFF	Double Speed	256fs
OFF	1	0	0	0	1	ON	ON	Quad Speed	128fs

Table 8. Sampling Speed & Master clock Frequency in serial mode

* In serial mode, SW1-4(DFS0), SW1-6(CKS1) and SW1-7(CSK0) should be always “OFF”, and DFS1, DFS0, CKS1, CKS0 and CMODE bits in the AK4620B should be set via the printer port (PORT3).

2-3) AK4114’s master clock mode & reference X’tal frequency

Mode	SW3-6 (CM1)	SW3-7 (CM0)	PLL	X'tal	Clock source	SDTO
0	OFF	OFF	ON	OFF	PLL	RX

Table 9. Clock Operation Mode

SW3-1 (XTL1)	SW3-2 (XTL0)	X’tal Frequency
ON	ON	OFF

Table 10. Reference X’tal frequency

3) Evaluation of A/D using DIT. (Optical link)

DIT generates audio bi-phase signal from received data and which is output through optical connector (PORT2). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input.

3-1) Analog input mode

Jumper	JP3 (LIN)	JP4 (AINL)	JP5 (RIN)	JP6 (AINR)	SW1-2 (ADMODE)
Single-ended	SINGLE	SINGLE	SINGLE	SINGLE	OFF
Differential	DIFF	DIFF	DIFF	DIFF	ON

Table 11. Analog Input Mode

* As for analog input circuit, please see the following item "Analog Input Buffer Circuit".

3-2) DIT output interface (Default: JP7="OPT")

Jumper	JP7 (TX)
Normal & Double Speed	OPT or BNC
Quard Speed	BNC

Table 12. DIT Output Interface

3-3) Sampling speed & MCLK frequency

a) parallel mode

SW1-1 (P/S)	SW1-4 (DFS0)	SW1-6 (CKS1)	SW1-7 (CKS0)	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4620B	MCLK Frequency of AK4620B
ON	OFF	OFF	OFF	OFF	OFF	Normal Speed	256fs
ON	OFF	OFF	ON	ON	OFF	Normal Speed	512fs
ON	ON	OFF	ON	OFF	OFF	Double Speed	256fs

Table 13. Sampling Speed & Master clock Frequency in parallel mode

* Parallel mode does not support quad speed mode.

b) serial mode

SW1-1 (P/S)	DFS1 bit	DFS0 bit	CMODE bit	CKS1 bit	CKS0 bit	SW3-4 (OCKS1)	SW3-5 (OCKS0)	Sampling Speed of AK4620B	MCLK Frequency of AK4620B
L	0	0	0	0	0	OFF	OFF	Normal Speed	256fs
L	0	0	0	0	1	ON	OFF	Normal Speed	512fs
L	0	1	0	0	1	OFF	OFF	Double Speed	256fs
L	1	0	0	0	1	ON	ON	Quad Speed	128fs

Table 14. Sampling Speed & Master clock Frequency in serial mode

* In serial mode, SW1-4(DFS0), SW1-6(CKS1) and S1-7(CSK0) should be always “OFF”, and DFS1, DFS0, CKS1, CKS0 and CMODE bits in the AK4620B should be set via the printer port (PORT3).

3-4) AK4114’s master clock mode & reference X’tal frequency

3-4-1) PLL is used as clock source

Synchronized signal should be set via PORT1(optical) or J6(BNC).

Mode	SW3-6 (CM1)	SW3-7 (CM0)	PLL	X'tal	Clock source	SDTO
0	OFF	OFF	ON	OFF	PLL	RX

Table 15. Clock Operation Mode (PLL)

SW3-1 (XTL1)	SW3-2 (XTL0)	X’tal Frequency
1	1	OFF

Table 16. Reference X’tal frequency(PLL)

3-4-2) X’tal is used as clock source

Mode	SW3-6 (CM1)	SW3-7 (CM0)	PLL	X'tal	Clock source	SDTO
1	OFF	ON	OFF	ON	X’tal	DAUX

Table 17. Clock Operation Mode (X’tal)

SW3-1 (XTL1)	SW3-2 (XTL0)	X’tal Frequency
1	0	24.576MHz

Table 18. Reference X’tal frequency (X’tal)

■ Set-up of SW1 and SW3

1) Set-up of SW1(AK4620B's mode set-up)

1-1) Audio data format in parallel mode

Mode	DIF (SW1-5)	SDTO	SDTI	LRCK	BICK	
2	OFF	24bit MSB Justified	24bit MSB Justified	H/L	≥48fs	(Default)
3	ON	I^2S Compatible	I^2S Compatible	L/H	≥48fs	

Table 19. Audio data format (parallel Mode)

1-2) De-emphasis control in parallel mode

DEM0 pin (SW1-3)	MODE	
OFF	ON(44.1KHz)	
ON	OFF	(Default)

Table 20. De-emphasis control (parallel mode)

1-3) parallel mode/ serial mode

P/S pin (SW1-1)	MODE	
OFF	Serial	
ON	Parallel	(Default)

Table 21. Set up P/S pin

2) Set-up of SW3(AK4114's mode set-up)

2-1) Audio data format

Mode	DIF0 (SW3-5)	SDTO	SDTI	LRCK	BICK	
4	L	24bit MSB Justified	24bit MSB Justified	H/L	≥48fs	(Default)
5	H	I^2S Compatible	I^2S Compatible	L/H	≥48fs	

Table22. Audio data format

* DIF1=L and DIF2=H are fixed in AKD4620B-B evaluation board.

■ The function of the toggle SW.

[SW2] : Resets the AK4620B. Keep "H" during normal operation.

■ Serial control mode

The AK4620B can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3(CR-I/F) with PC by 10-wire flat cable packed with the AKD4620B-B.

Take care of the direction of connector. There is a mark at pin#1.

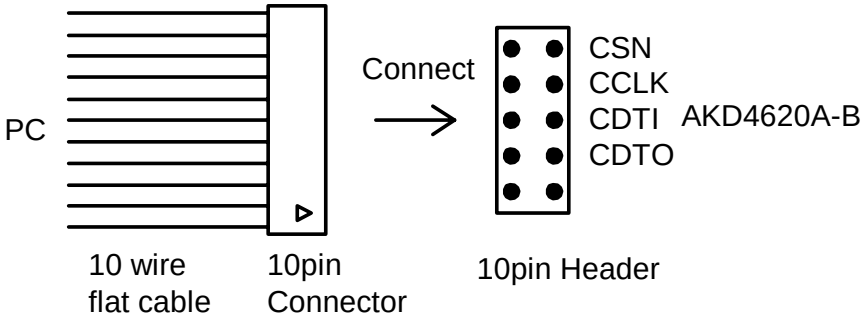


Figure 2. Connect of 10 wire flat cable

■ Analog Input Buffer Circuit

1. Differential Input Mode

The AK4620B can accept input voltages from AGND to VA. The input signal range scales with the VREF voltage and is nominally 2.82Vpp (VREF = 5V). Figure 3 shows an input buffer circuit example. This is a fully differential input buffer circuit with an inverted amplifier (fc=370KHz,gain: –10dB).
The capacitor of 10nF between AINL+/– (AINR+/–) decreases the clock feedthrough noise of the modulator, and composes a 1st order LPF (fc=360kHz) with a 22Ω resistor before the capacitor.

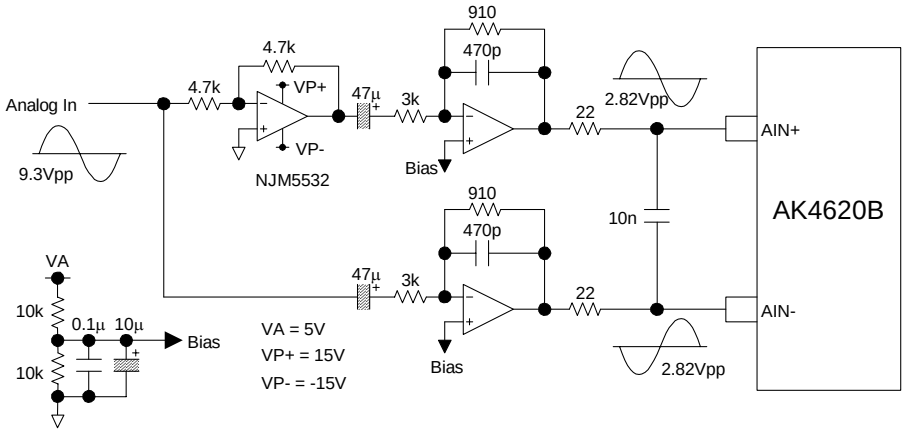


Figure 3. Input buffer circuit in differential mode

2. Single-ended Input Mode

When the AK4620B is evaluated by single-ended mode, C49 and C90 should be removed.

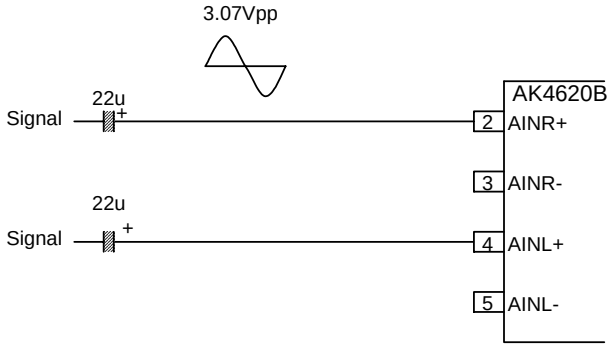


Figure 4. Input buffer circuit in Single-ended mode

■ Analog Output Buffer Circuit

The differential output circuit(2nd order LPF,fc=182KHz,Q=0.637,G=+3.9dB) and LPF(1st order LPF, fc=284KHz, G=-0.84dB) is implemented on board. The differential outputs of AK4620B is buffered by non-inverted circuit and output via Cannon connector (differential output). LPF adds differential outputs. NJM5534D is used for op-amp on this board that has low noise and high voltage torelance characteristics. Analog signal is output via BNC connectors on the board. The output level is about 2.8Vrms (typ@VREF=5.0V) by BNC.

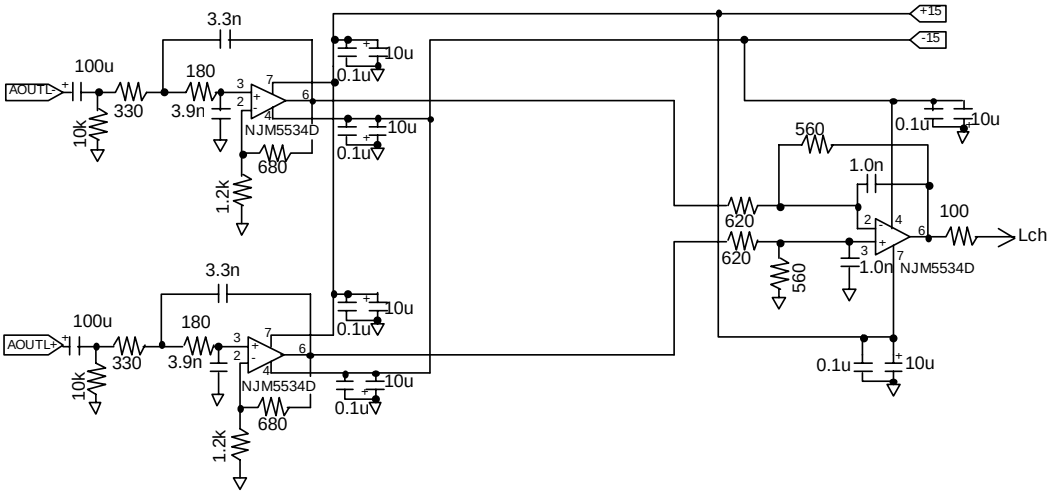


Figure 5. Output buffer circuit

* AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4620B-B according to previous term.

2. Connect IBM-AT compatible PC with AKD4620B-B by 10-line type flat cable (packed with AKD4620B-B). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4620B-B Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4620b-b.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button

■ Explanation of each buttons

[Port Reset] :	Set up the USB interface board (AKDUSBIF-A) .
[Write default] :	Initialize the register of AK4620B.
[All Write] :	Write all registers that is currently displayed.
[Function1] :	Dialog to write data by keyboard operation.
[Function2] :	Dialog to write data by keyboard operation.
[Function3] :	The sequence of register setting can be set and executed.
[Function4] :	The sequence that is created on [Function3] can be assigned to buttons and executed.
[Function5]:	The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
[SAVE] :	Save the current register setting.
[OPEN] :	Write the saved values to all register.
[Write] :	Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to the AK4620B, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to the AK4620B, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate volume

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to the AK4620B by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to the AK4620B, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is "akr".

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is "akr".

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4620B. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is "aks".

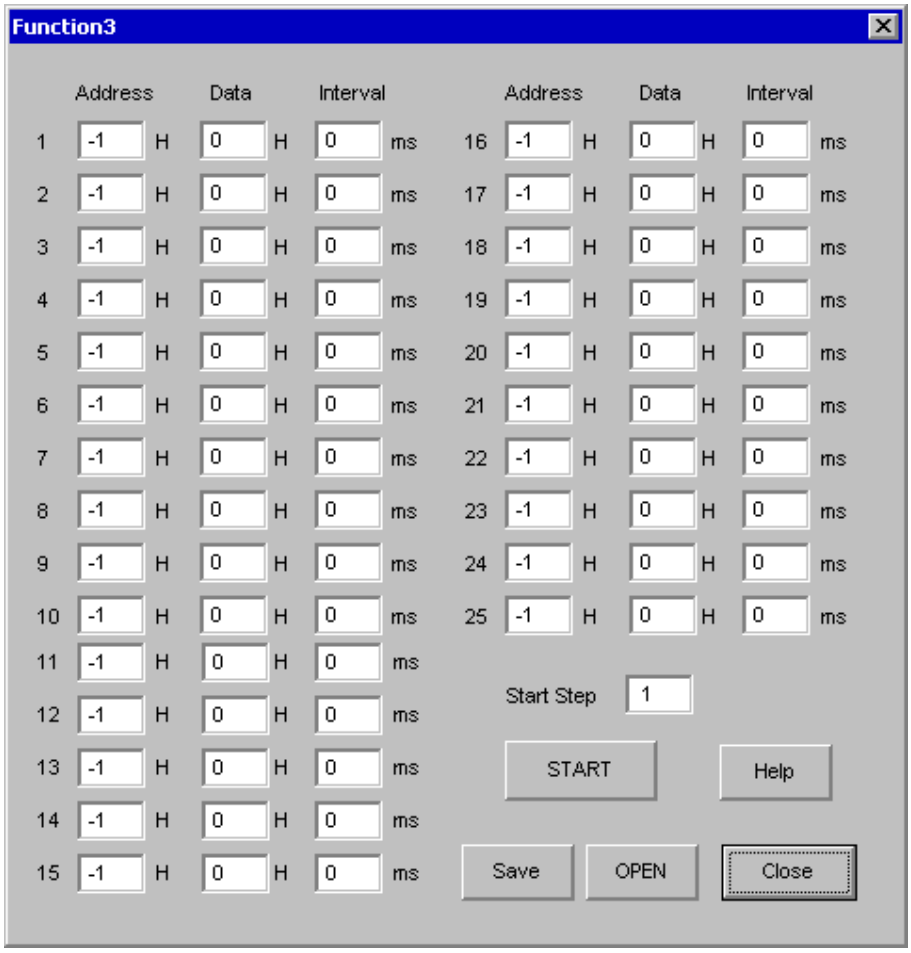


Figure 6. Window of [F3]

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 10 opens.

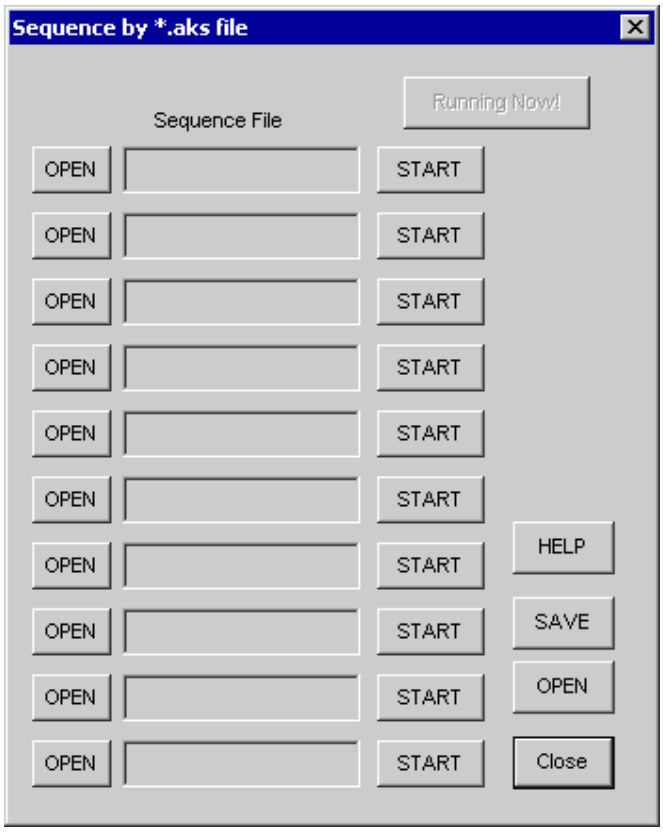


Figure 7. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 11. (In case that the selected sequence file name is "DAC_Stereo_ON.aks")

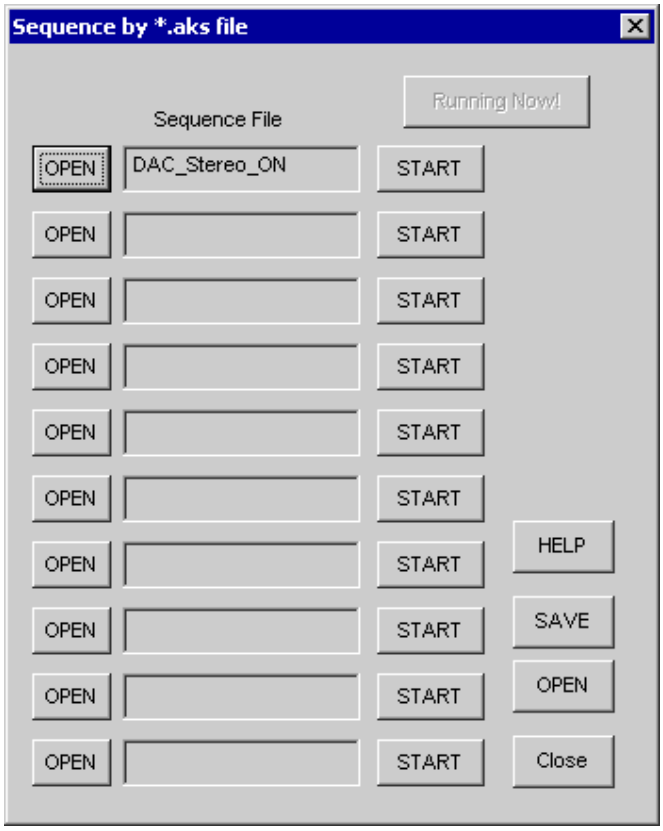


Figure 8. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is "*.ak4".

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 12 opens.

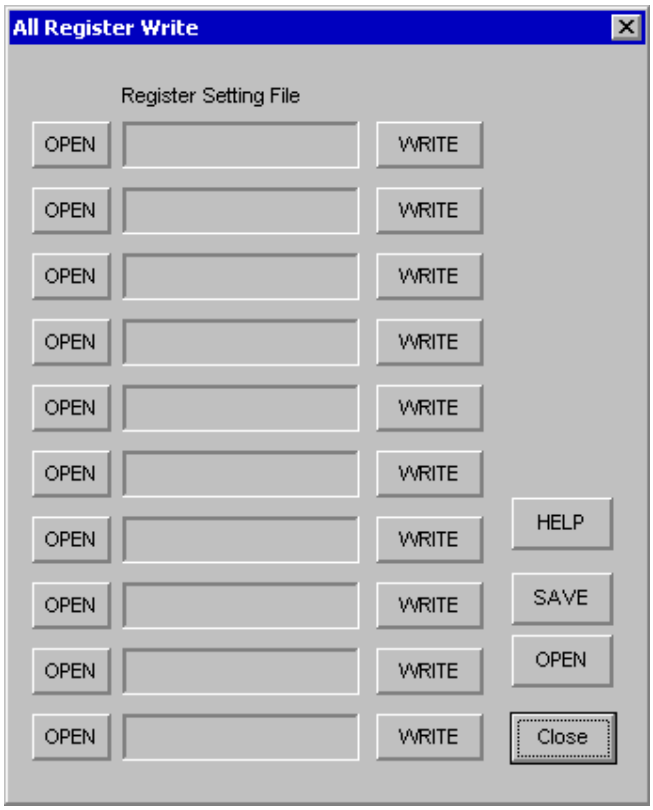


Figure 9. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 13. (In case that the selected file name is "DAC_Output.akr")

(2) Click [WRITE] button, then the register setting is executed.

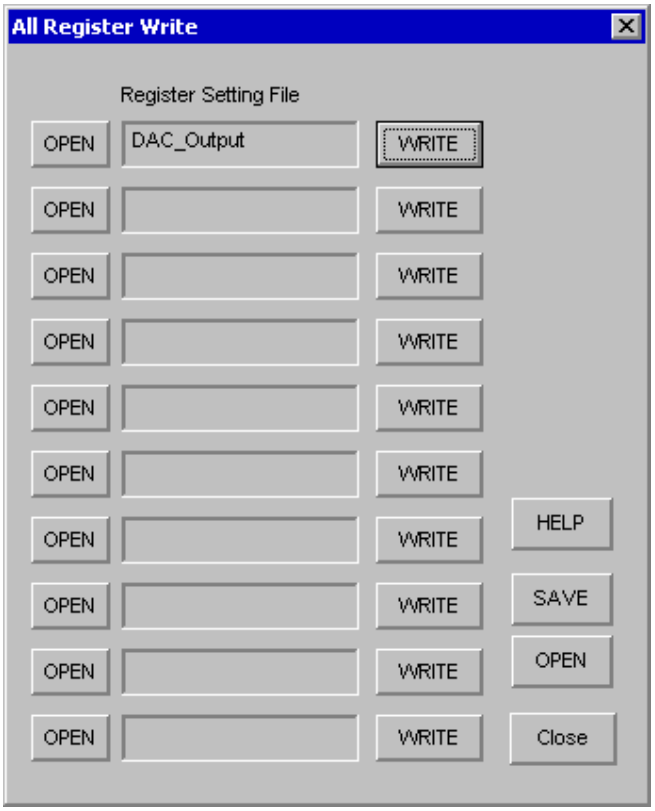


Figure 10. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

MEASUREMENT RESULTS

[Measurement condition]
Measurement unit: Audio Precision System Two Cascade
MCLK: 512fs (44.1kHz), 256fs (96kHz), 128fs (192kHz)
BICK: 64fs
Power supply Voltage: VA=VT=5.0V, VD=3.3V
Interface: Internal DIT or DIR (44.1kHz, 96kHz, 192KHz)
Temperature: Room Temp.

1. ADC (Single-ended)

fs=44.1kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	20kLPF	89.7dB	90.0dB
DR	1kHz, -60dB	20kLPF	108.2dB	108.2dB
DR	1kHz, -60dB	20kLPF, A-weighted	110.9dB	110.9dB
S/N	No input	20kLPF, A-weighted	110.9dB	110.9dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	40kLPF	89.2dB	89.5dB
DR	1kHz, -60dB	40kLPF	104.8dB	104.7dB
DR	1kHz, -60dB	40kLPF, A-weighted	110.7dB	110.7dB
S/N	No input	40kLPF, A-weighted	110.7dB	110.7dB

fs=192kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	40kLPF	89.0dB	89.3dB
DR	1kHz, -60dB	40kLPF	104.8dB	104.8dB
DR	1kHz, -60dB	40kLPF, A-weighted	110.6dB	110.6dB
S/N	No input	40kLPF, A-weighted	110.5dB	110.5dB

2. ADC (Differential)

fs=44.1kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	20kLPF	100.7dB	101.5dB
DR	1kHz, -60dB	20kLPF	111.8dB	111.8dB
DR	1kHz, -60dB	20kLPF, A-weighted	114.5dB	114.4dB
S/N	No input	20kLPF, A-weighted	114.5dB	114.4dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	40kLPF	101.0dB	101.5dB
DR	1kHz, -60dB	40kLPF	107.6dB	107.6dB
DR	1kHz, -60dB	40kLPF, A-weighted	114.3dB	114.2dB
S/N	No input	40kLPF, A-weighted	114.3dB	114.2dB

fs=192kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, -1dB	40kLPF	100.8dB	101.4dB
DR	1kHz, -60dB	40kLPF	107.5dB	107.4dB
DR	1kHz, -60dB	40kLPF, A-weighted	113.8dB	114.0dB
S/N	No input	40kLPF, A-weighted	113.8dB	114.0dB

3. DAC

fs=44.1kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, 0dB	20kLPF	99.8dB	96.7dB
DR	1kHz, -60dB	20kLPF	113.0dB	113.0dB
DR	1kHz, -60dB	22kLPF, A-weighted	115.2dB	115.2dB
S/N	“0” data	22kLPF, A-weighted	115.3dB	115.3dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, 0dB	40kLPF	99.3dB	96.8dB
DR	1kHz, -60dB	40kLPF	110.3dB	110.4dB
DR	1kHz, -60dB	40kLPF, A-weighted	115.3dB	115 .3dB
S/N	“0” data	40kLPF, A-weighted	115.3dB	115.4dB

fs=192kHz

Parameter	Input signal	Measurement filter	Results	
			L ch	R ch
S/(N+D)	1kHz, 0dB	40kLPF	98.6dB	96.3dB
DR	1kHz, -60dB	40kLPF	110.0dB	110.0dB
DR	1kHz, -60dB	40kLPF, A-weighted	114.9dB	114.9dB
S/N	“0” data	40kLPF, A-weighted	115.3dB	115.3dB

[Plots]

ADC (Single-ended)

(fs=44.1kHz)

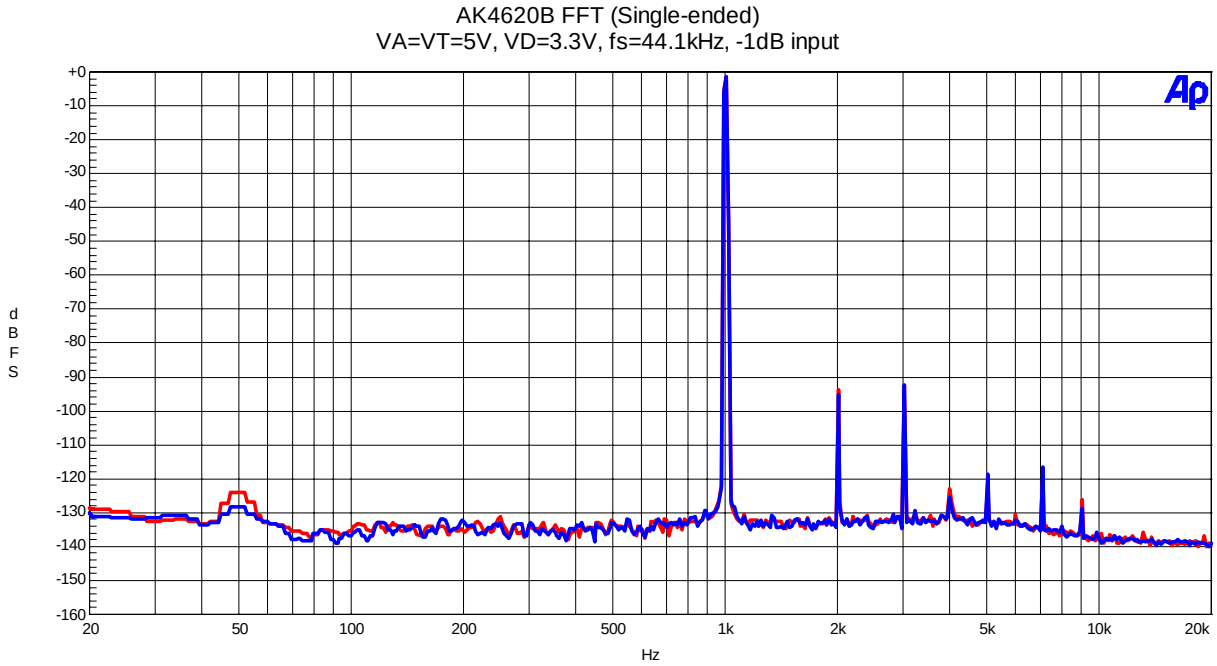


Figure 11. FFT (fin=1kHz, Input Level=-1dBFS)

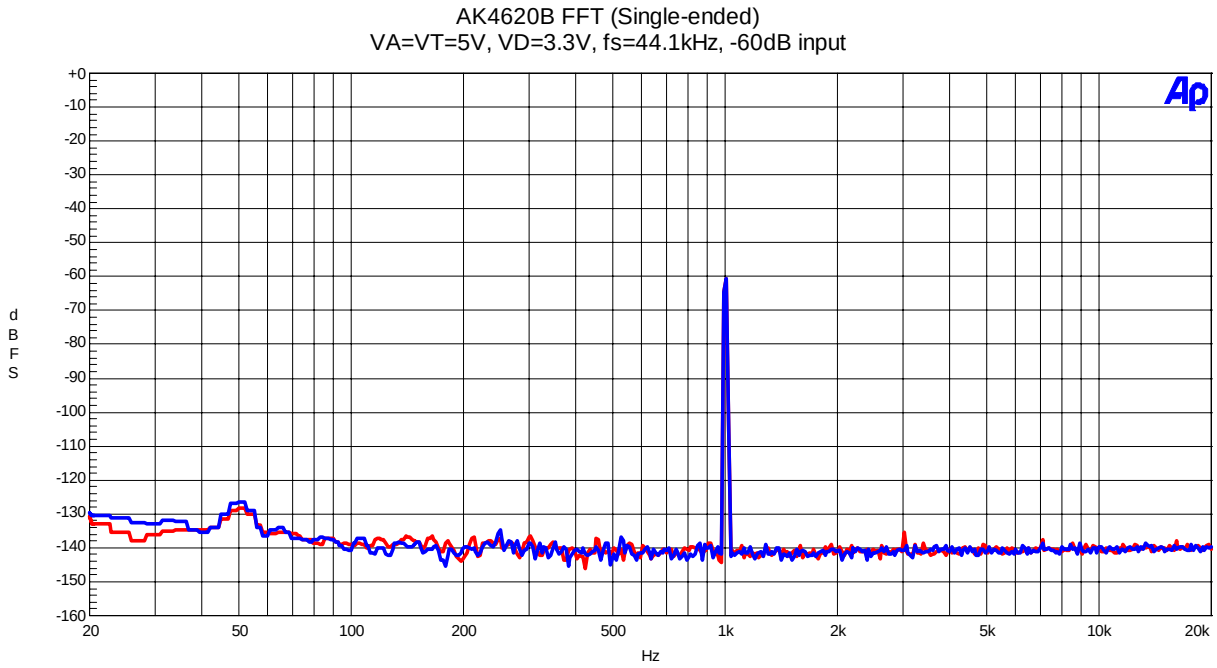


Figure 12. FFT (fin=1kHz, Input Level=-60dBFS)

(fs=44.1kHz)

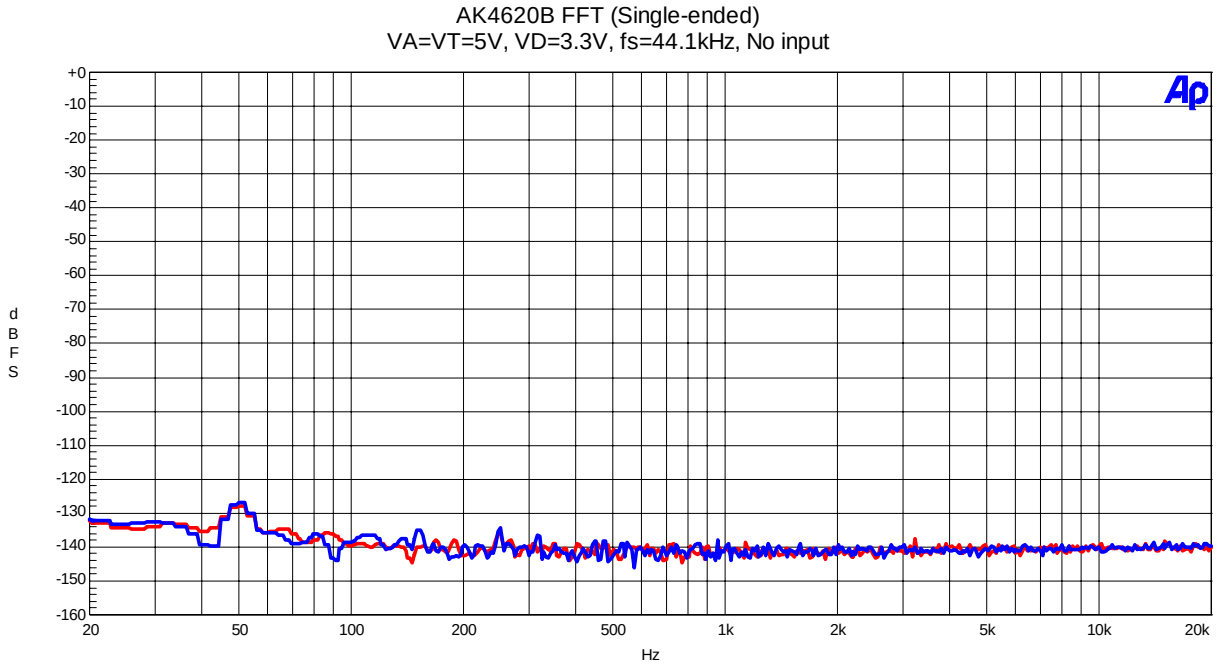


Figure 13. FFT (Noise Floor)

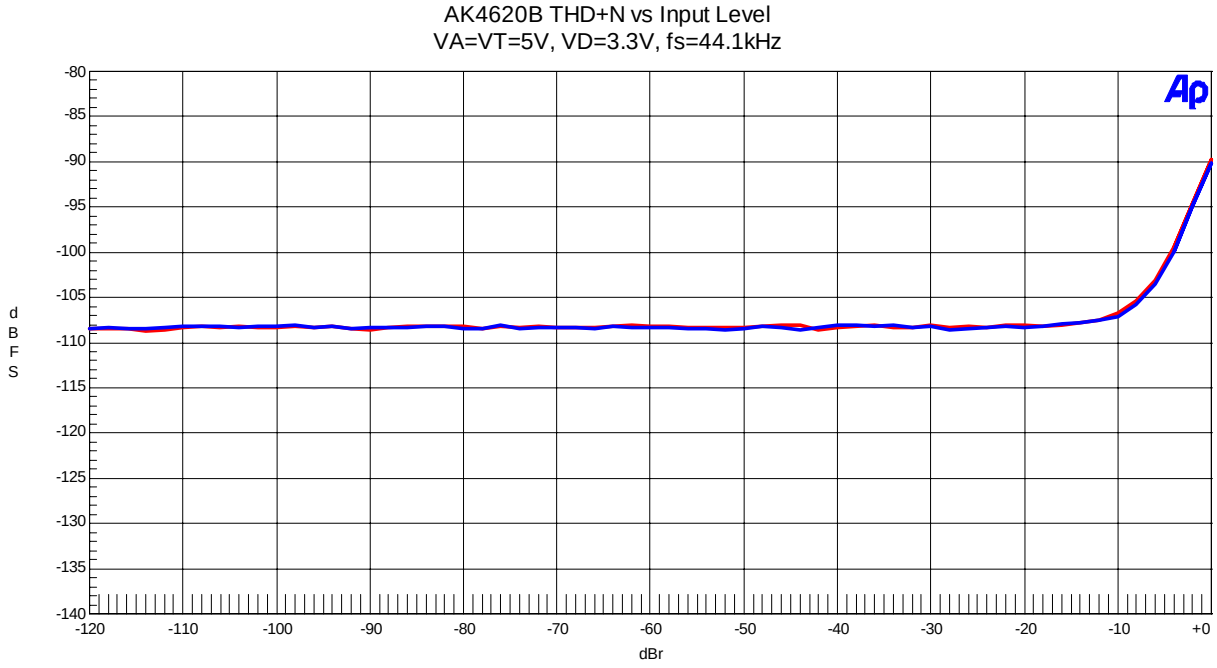


Figure 14. THD+N vs. Input level (fin=1kHz)

(fs=44.1kHz)

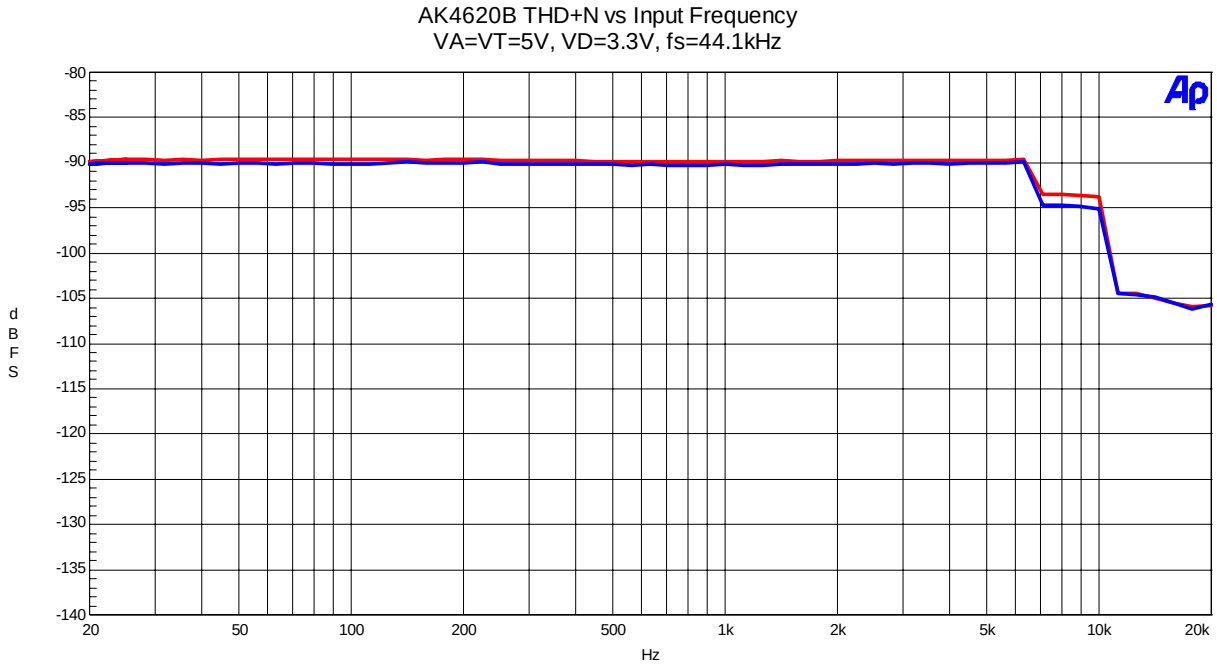


Figure 15. THD +N vs. Input Frequency (Input level=-1dBFS)

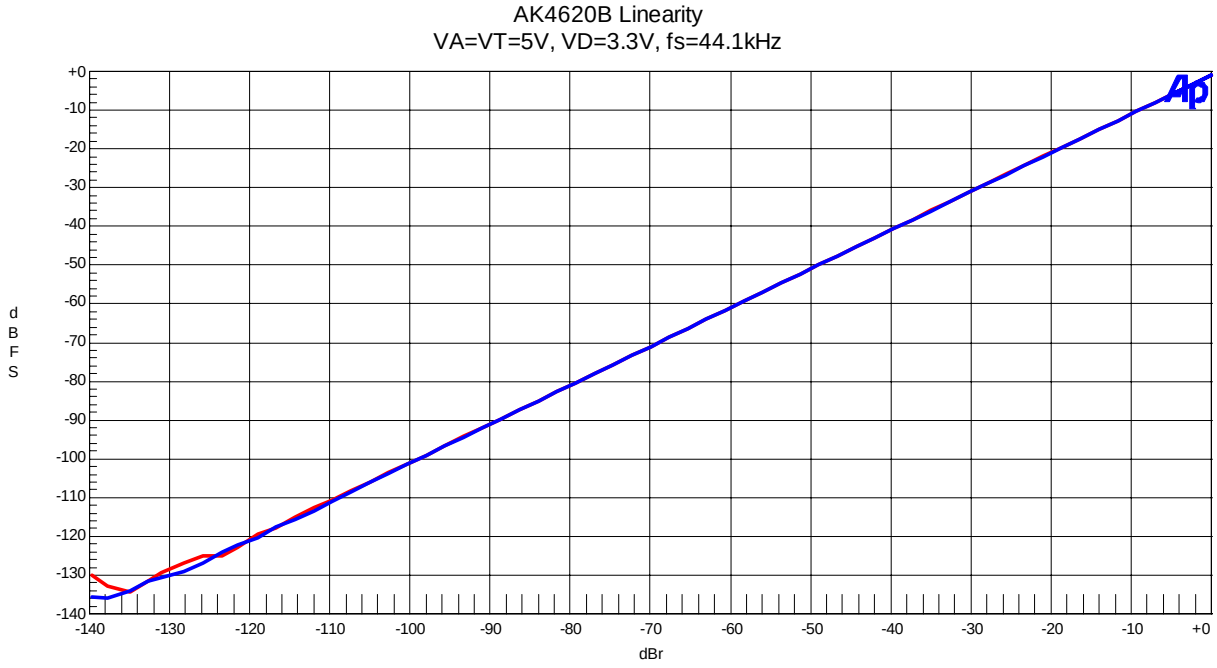


Figure 16. Linearity (fin=1kHz)

(fs=44.1kHz)

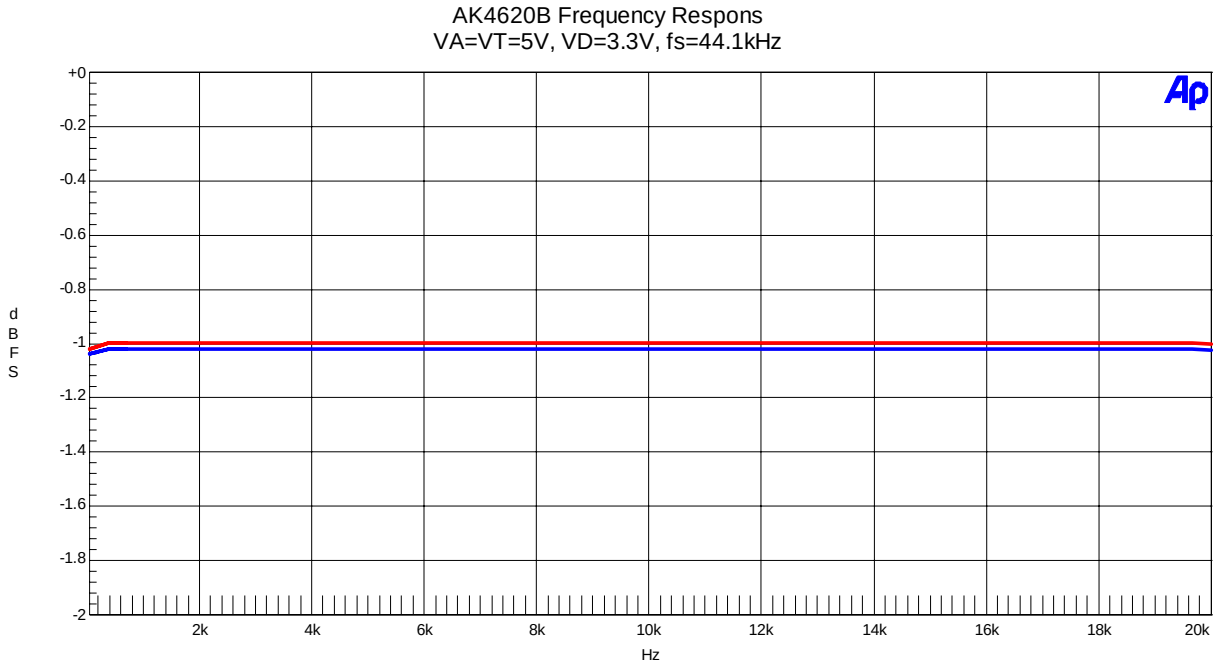


Figure 17. Frequency Response

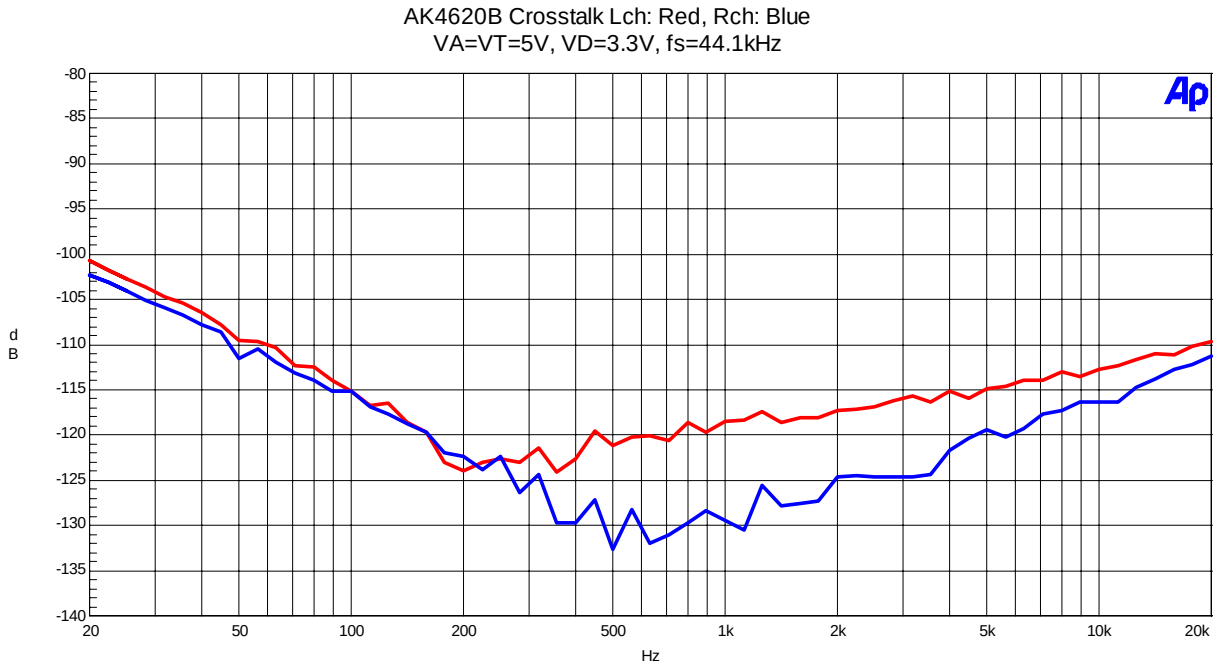


Figure 18. Crosstalk

(fs=96kHz)

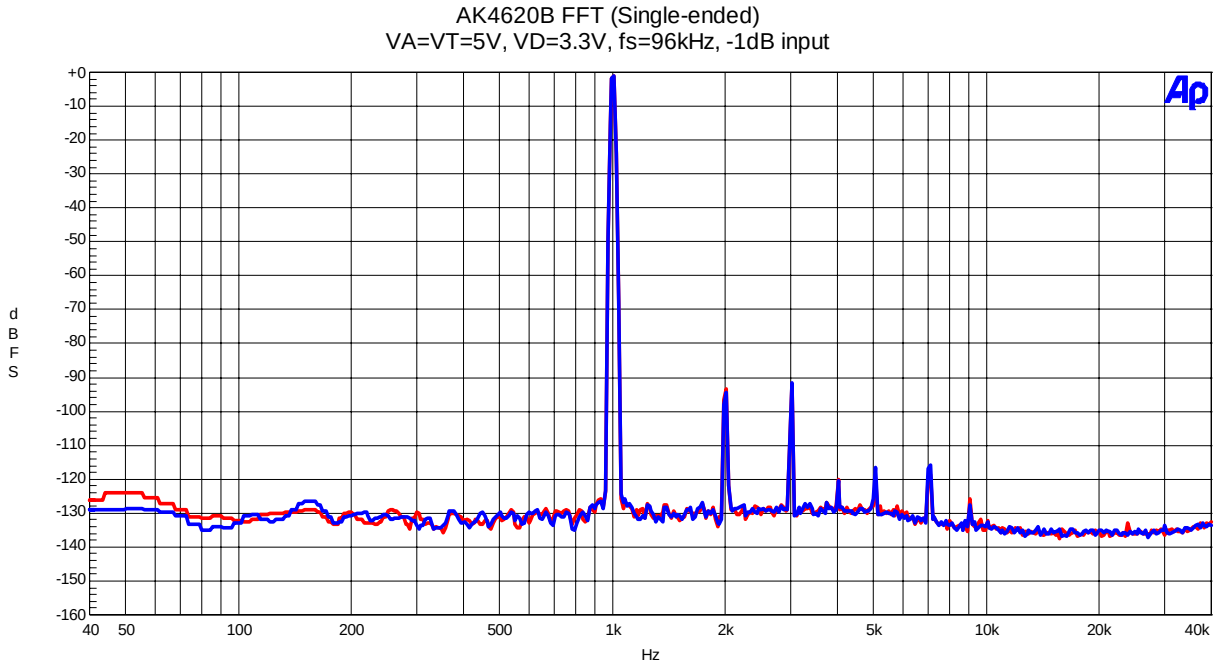


Figure 19. FFT (fin=1kHz, Input Level=-1dBFS)

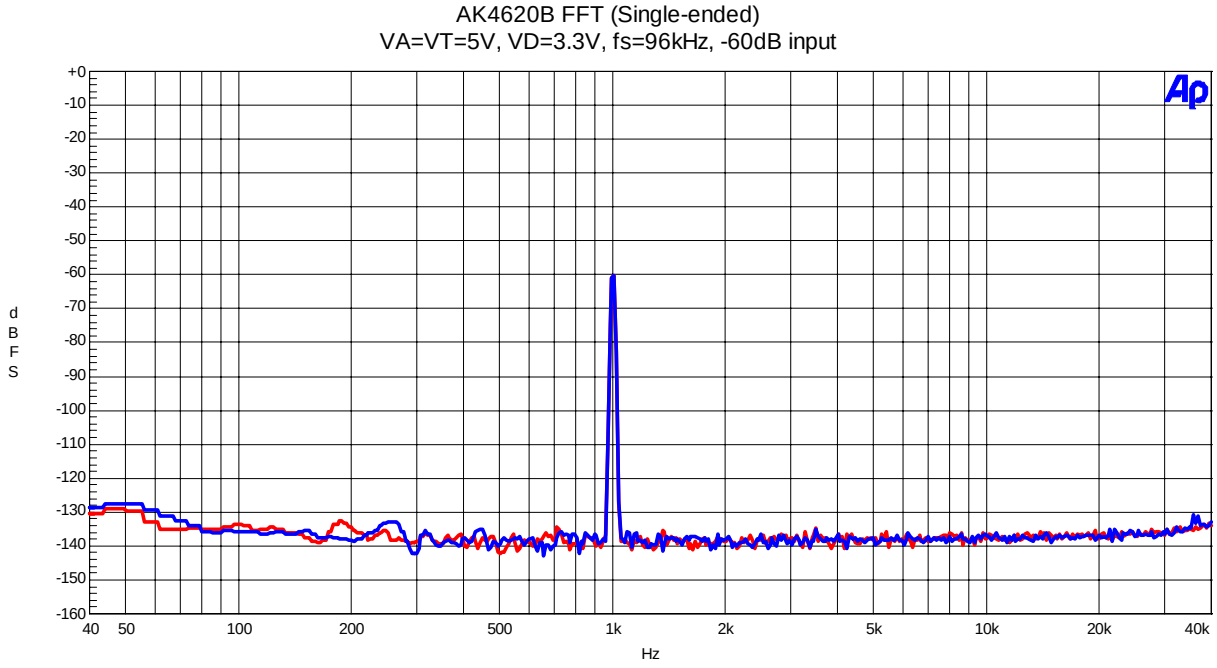


Figure 20. FFT (fin=1kHz, Input Level=-60dBFS)

(fs=96kHz)

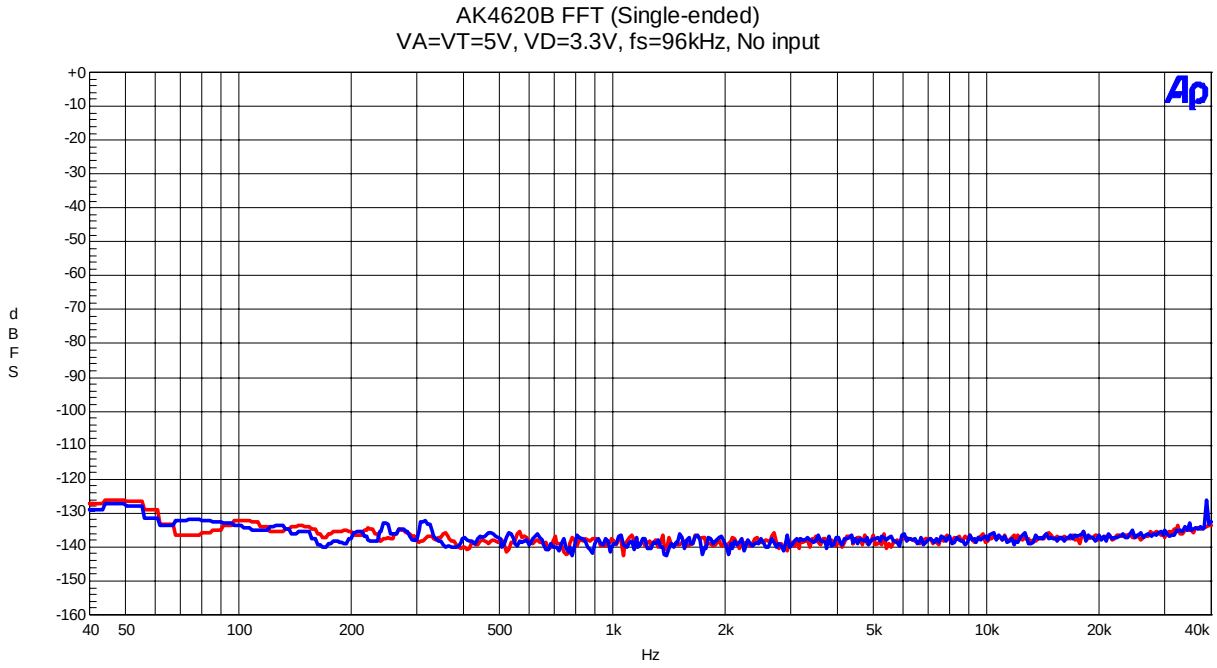


Figure 21. FFT (Noise Floor)

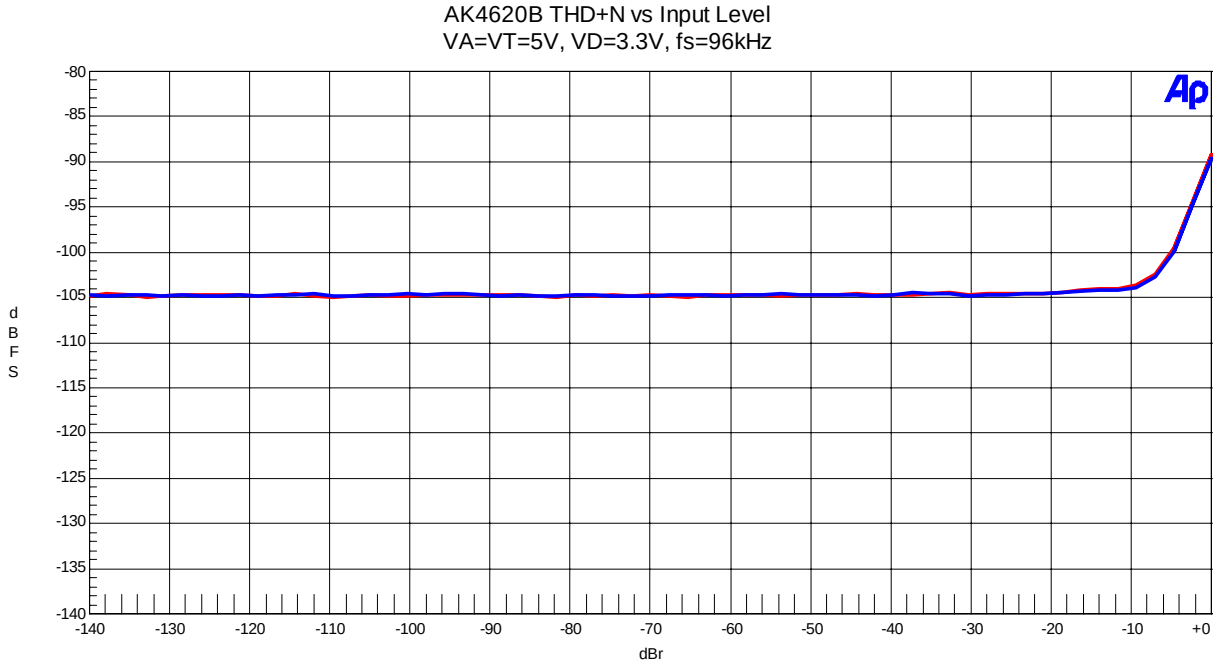


Figure 22. THD +N vs. Input level (fin=1kHz)

(fs=96kHz)

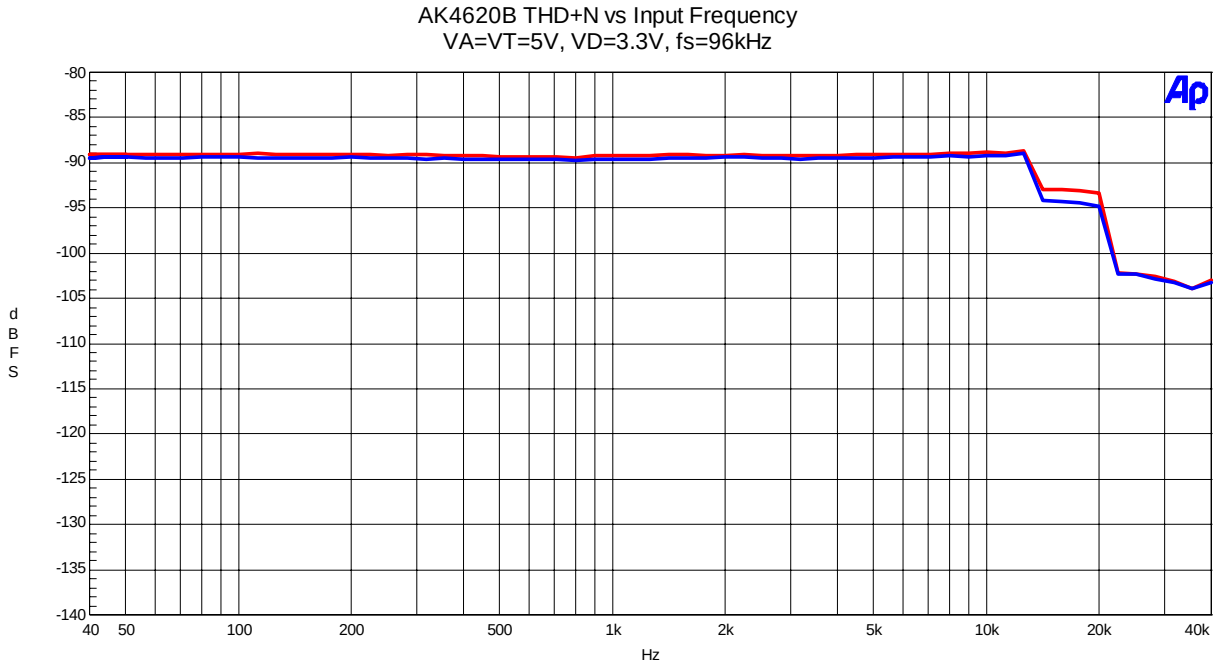


Figure 23. THD +N vs. Input Frequency (Input level=-1dBFS)

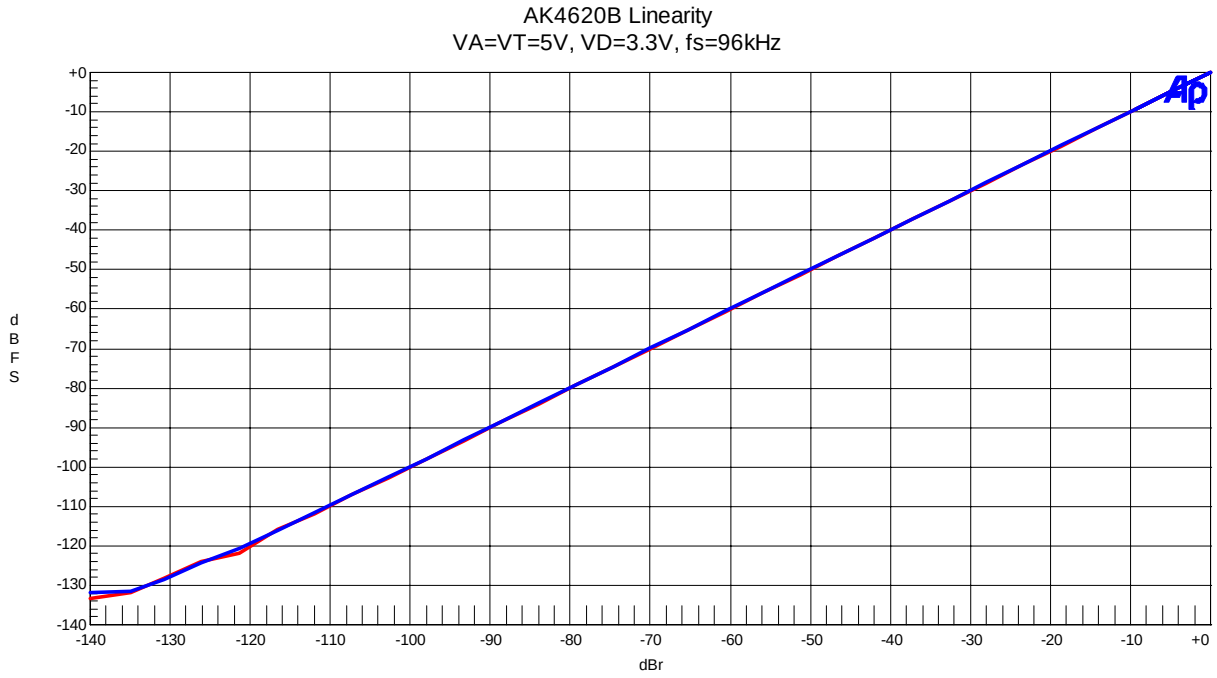


Figure 24. Linearity (fin=1kHz)

(fs=96kHz)

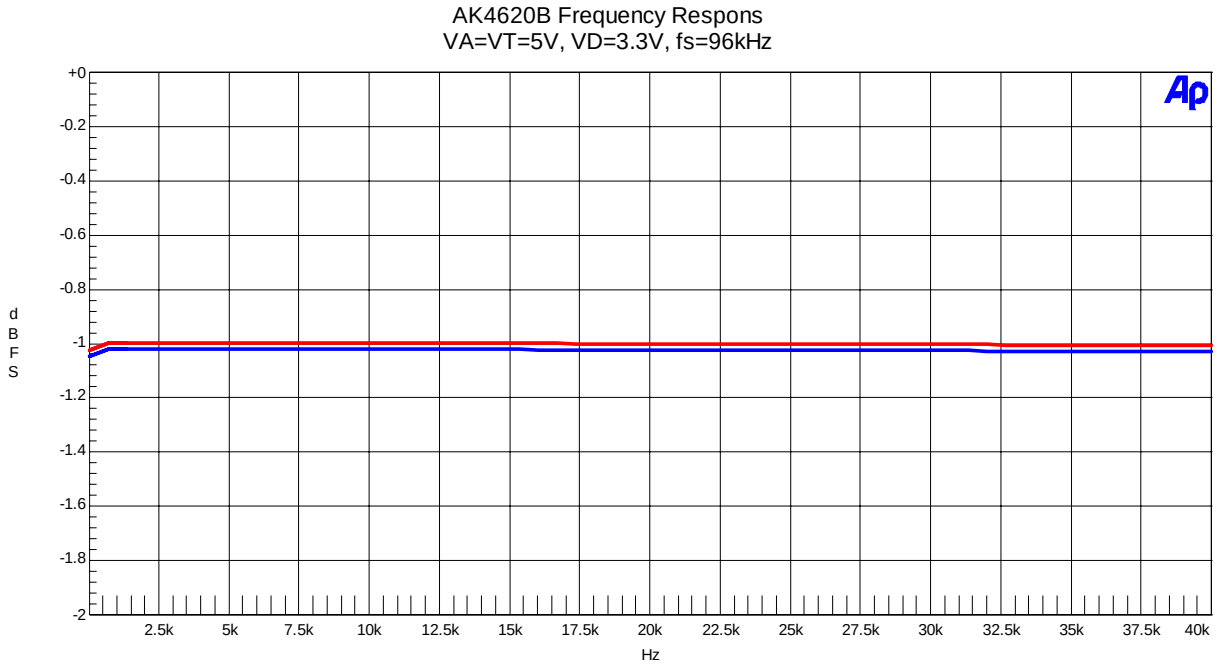


Figure 25. Frequency Response

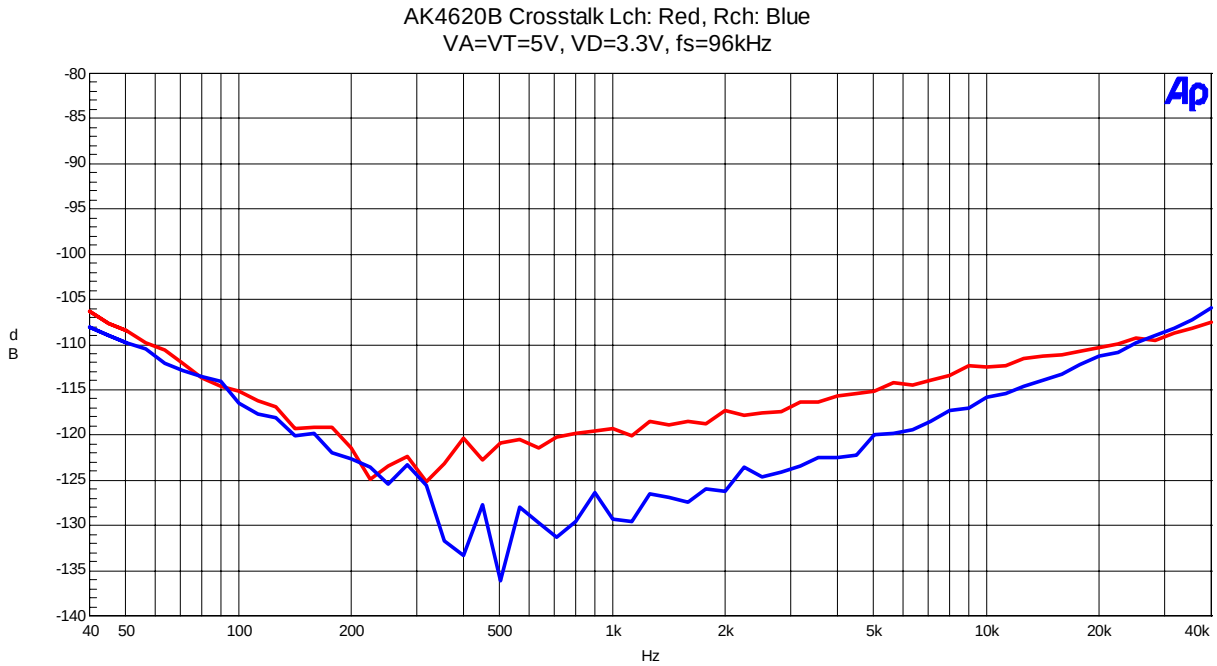


Figure 26. Crosstalk

(fs=192kHz)

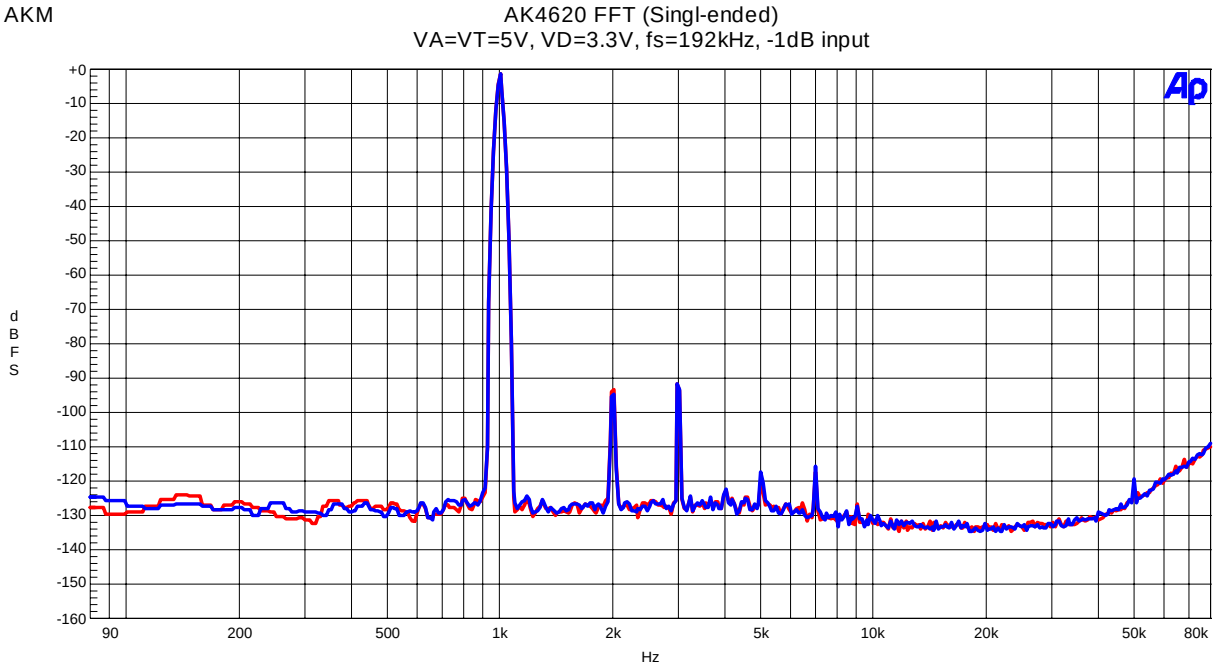


Figure 27. FFT (fin=1kHz, Input Level=-1dBFS)

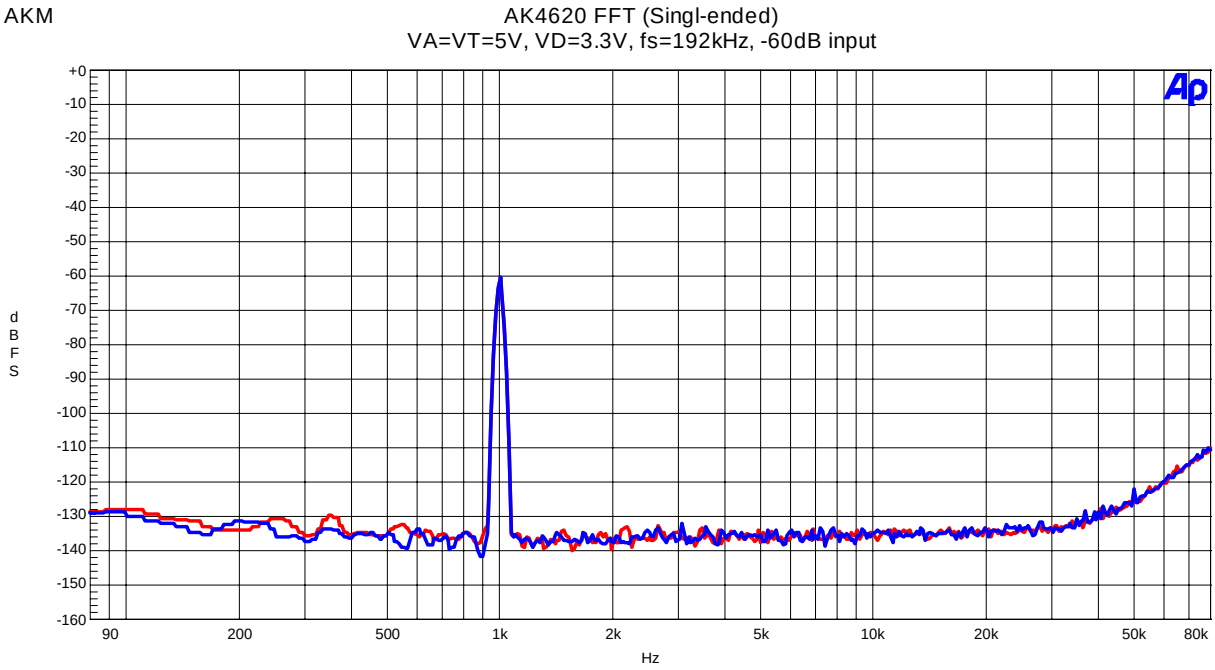


Figure 28. FFT (fin=1kHz, Input Level=-60dBFS)

(fs=192kHz)

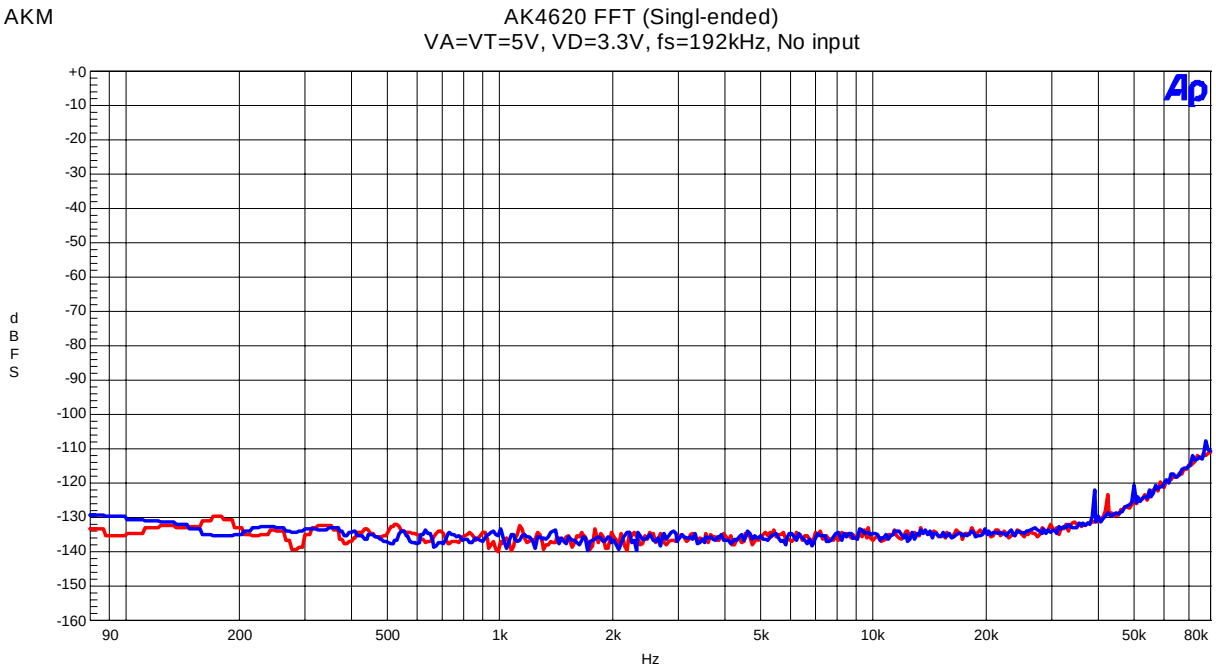


Figure 29. FFT (Noise Floor)

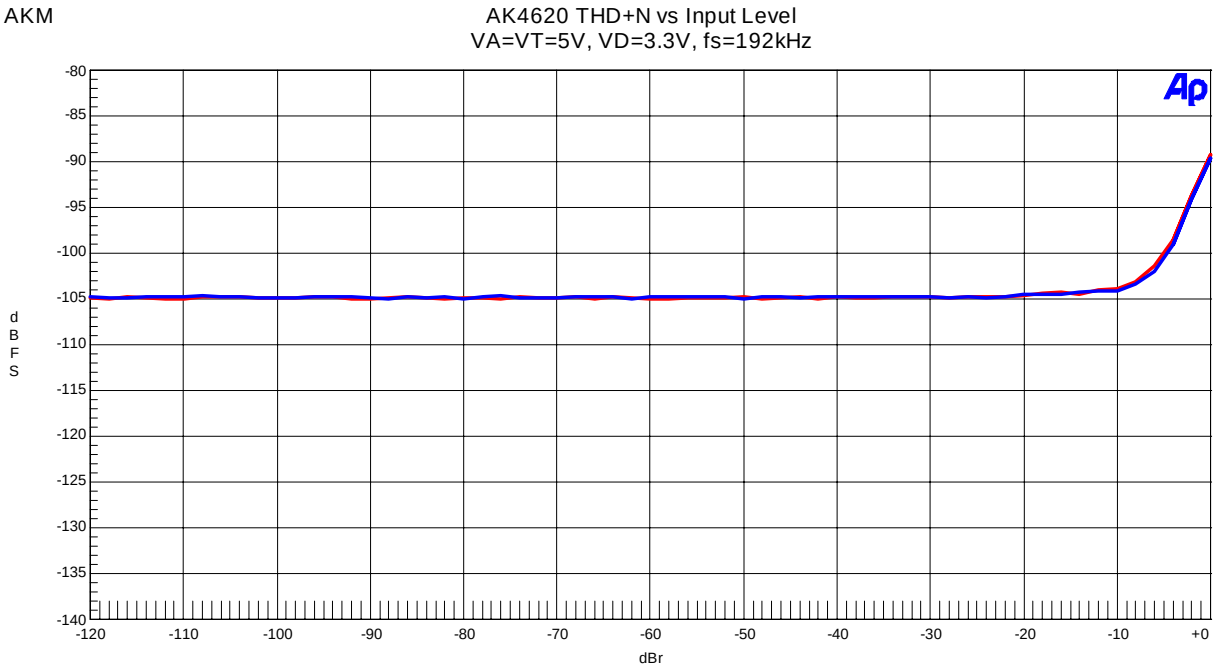


Figure 30. THD+N vs. Input level (fin=1kHz)

(fs=192kHz)

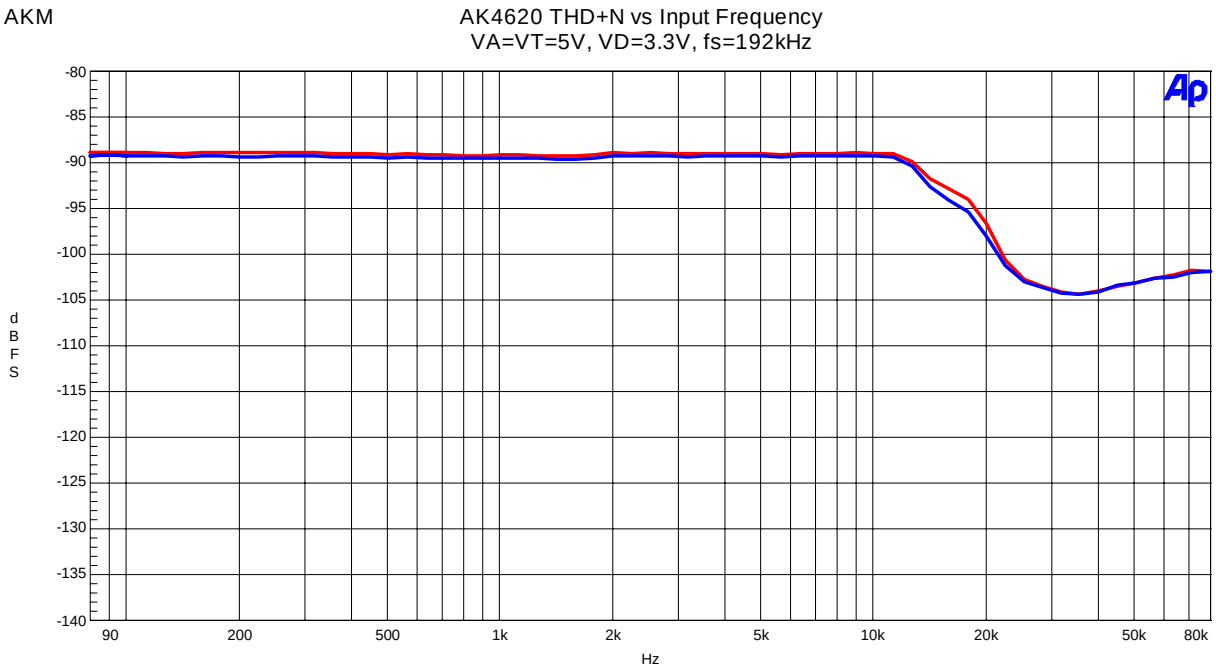


Figure 31. THD+N vs. Input Frequency (Input level=-1dBFS)

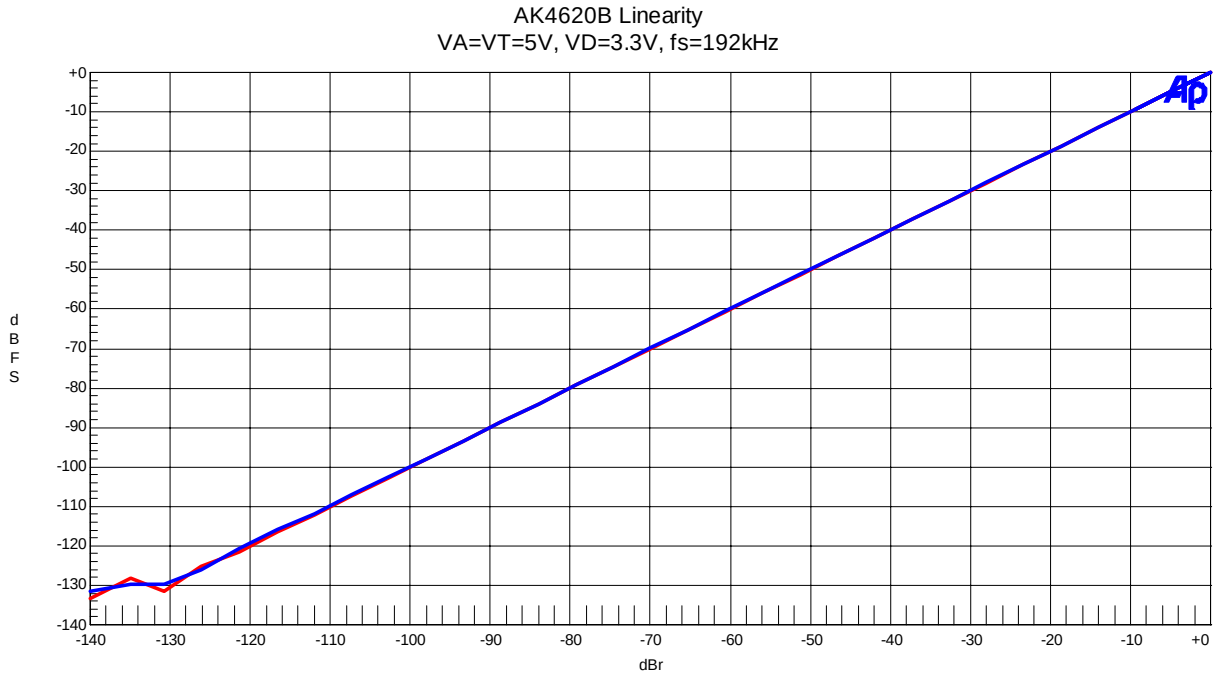


Figure 32. Linearity (fin=1kHz)

(fs=192kHz)

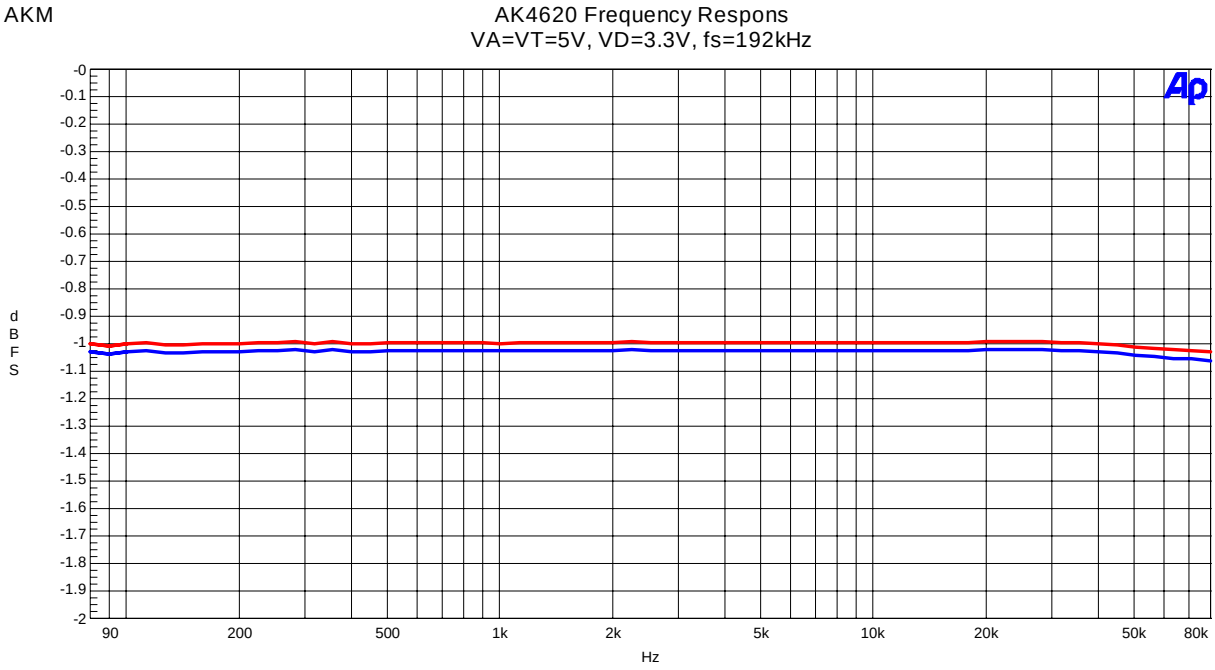


Figure 33. Frequency Response

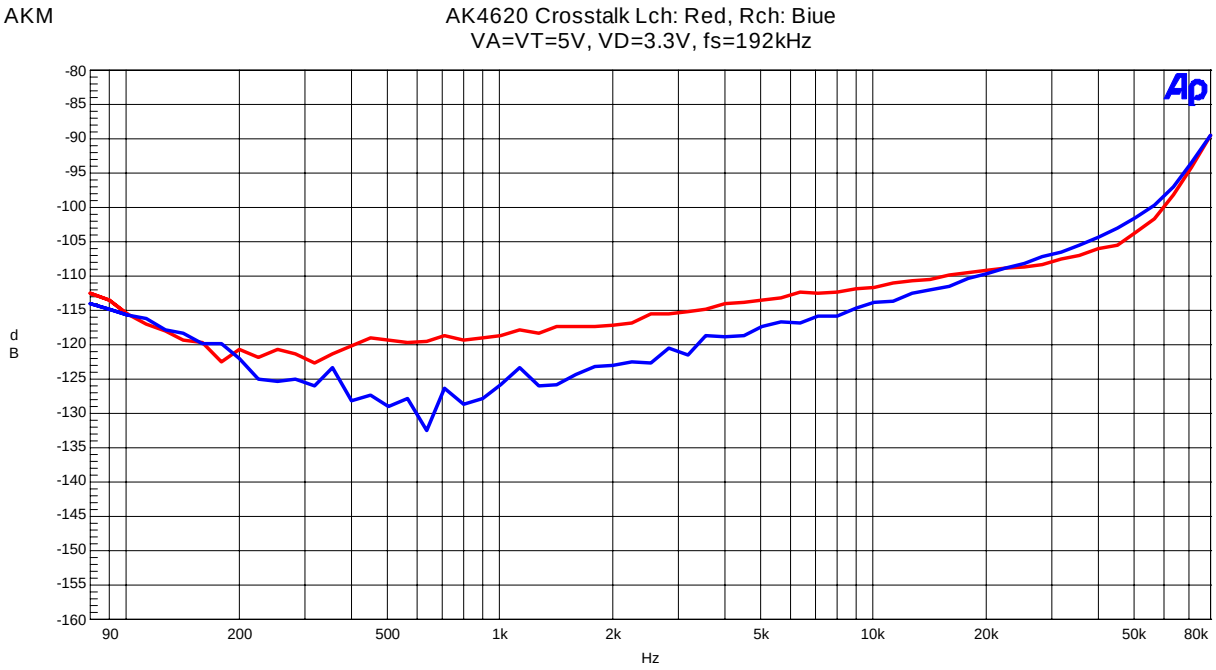


Figure 34. Crosstalk

ADC (Differential)

(fs=44.1kHz)

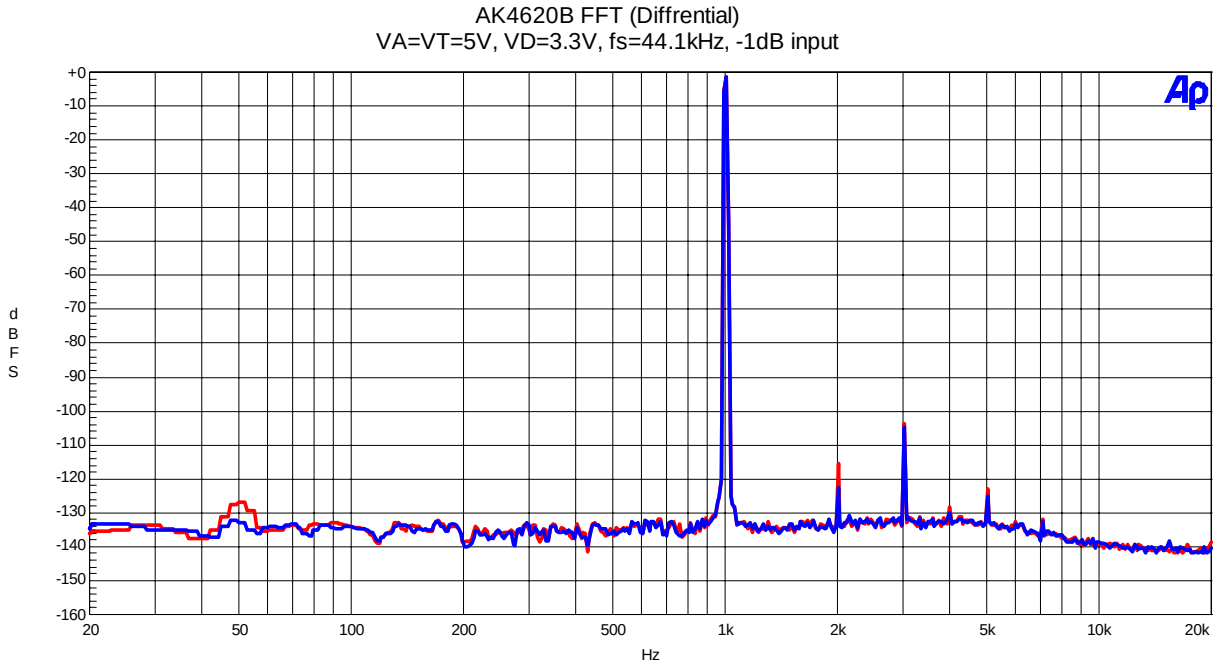


Figure 35. FFT (fin=1kHz, Input Level=-1dBFS)

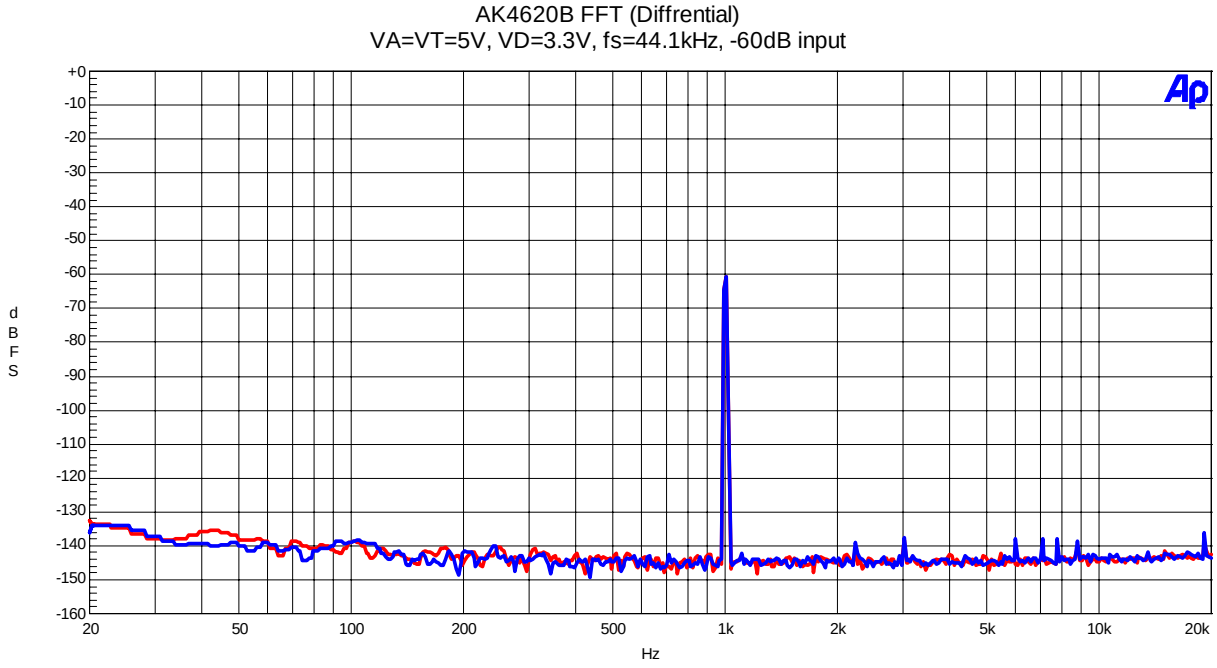


Figure 36. FFT (fin=1kHz, Input Level=-60dBFS)

(fs=44.1kHz)

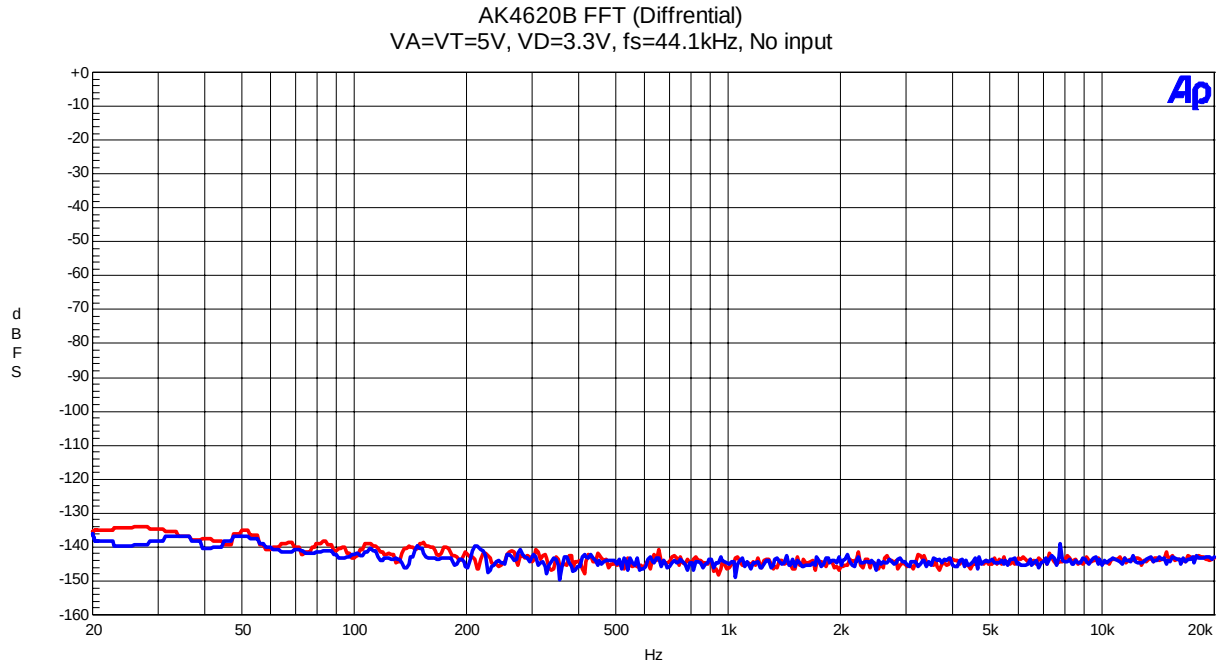


Figure 37. FFT (Noise Floor)

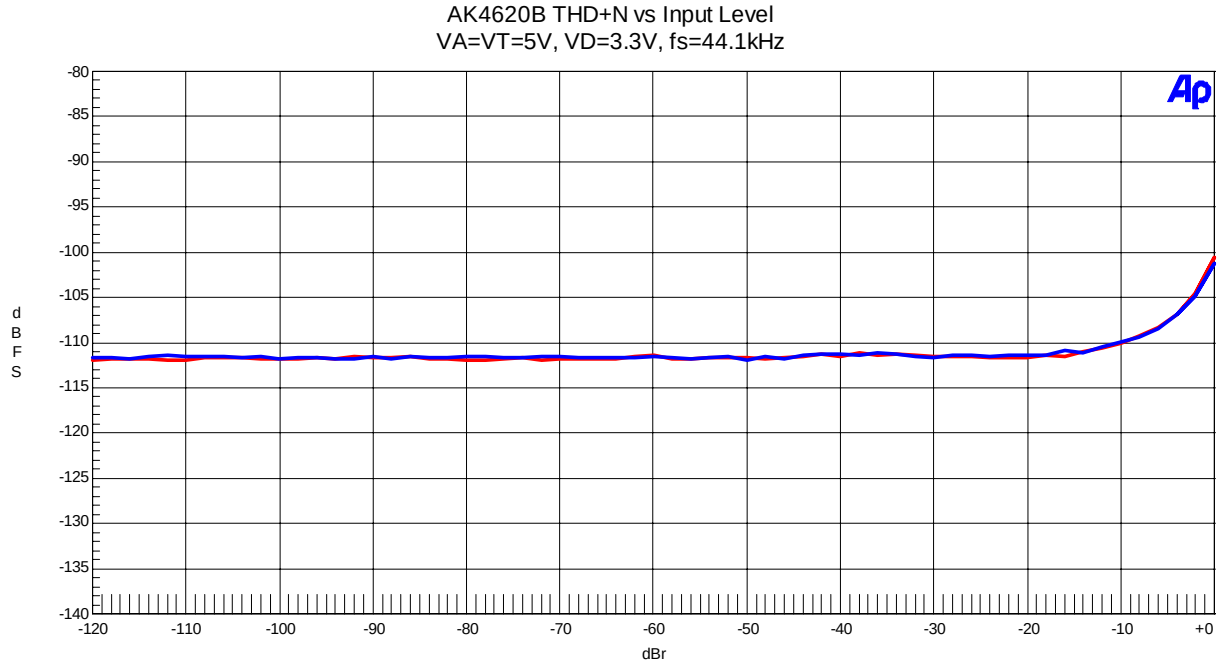


Figure 38**. THD+N vs. Input level (fin=1kHz)**

(fs=44.1kHz)

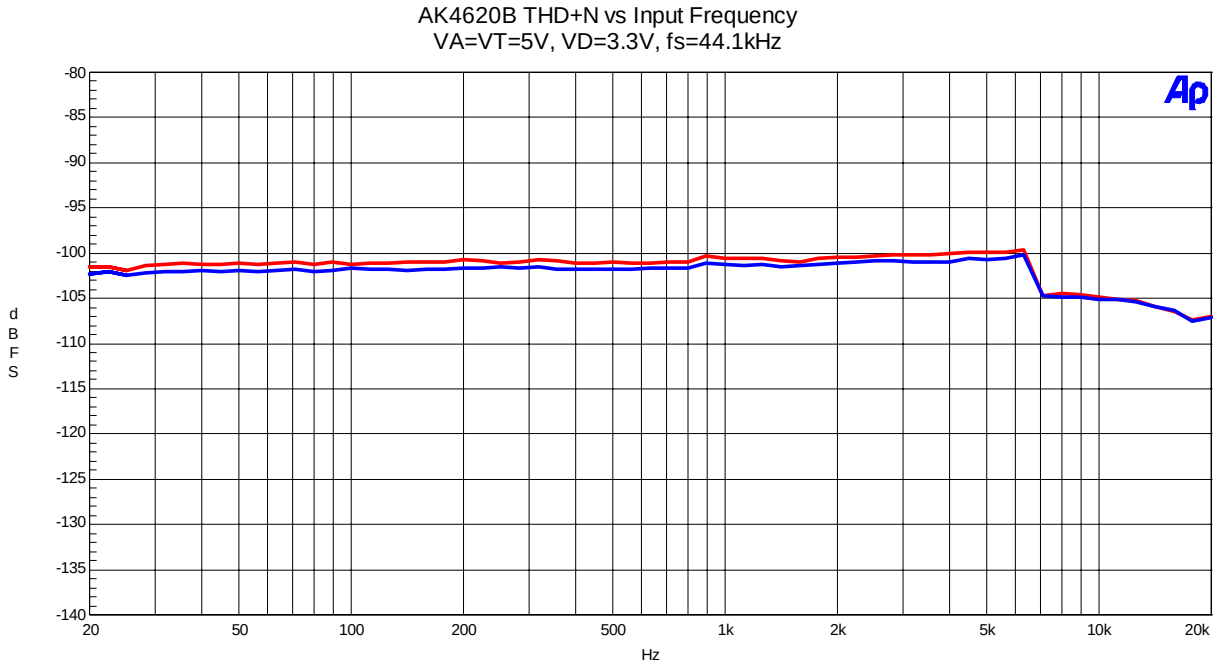


Figure 39. THD +N vs. Input Frequency (Input level=-1dBFS)

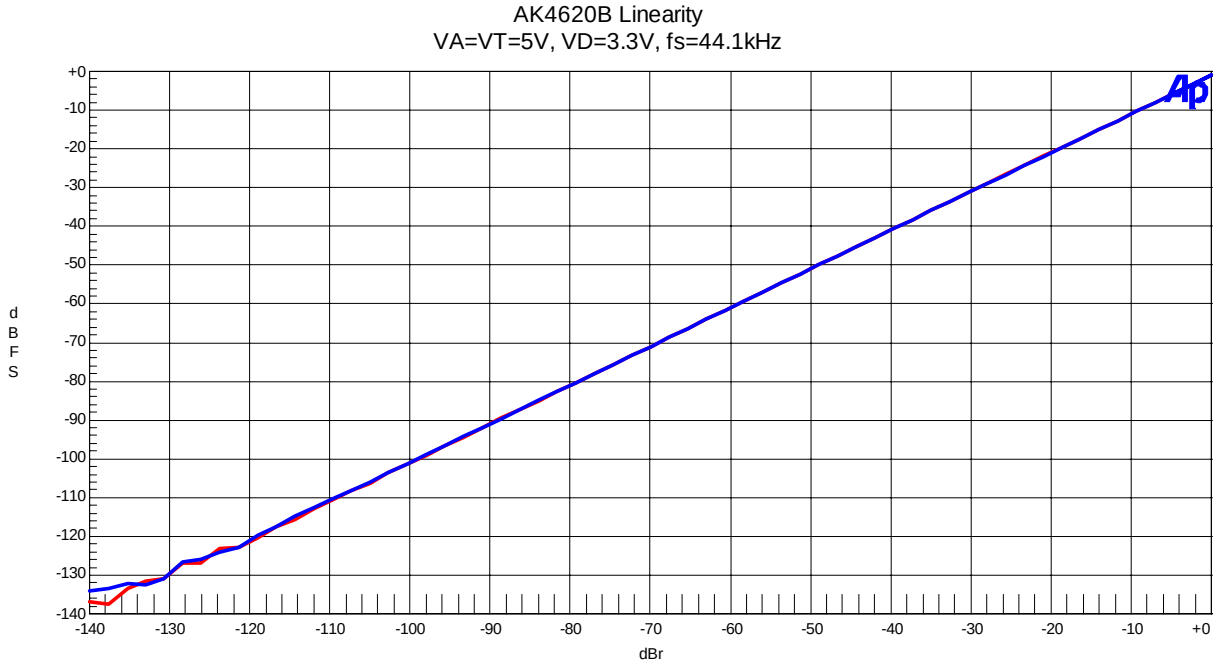


Figure 40. Linearity (fin=1kHz)

(fs=44.1kHz)

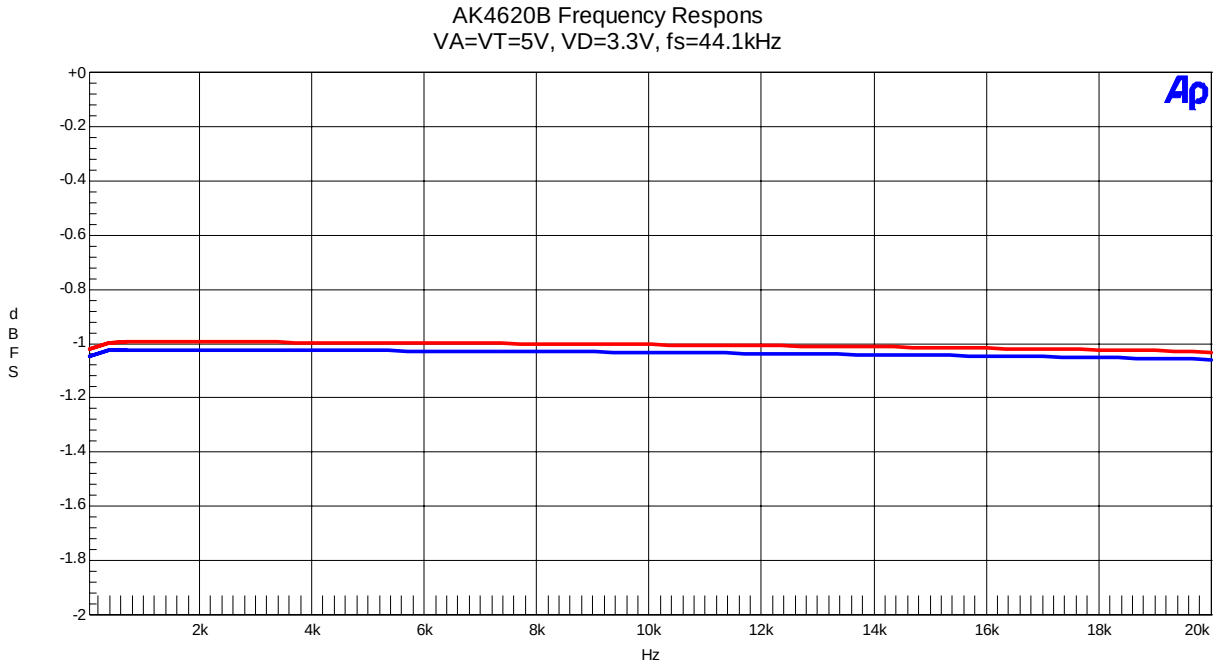


Figure 41. Frequency Response

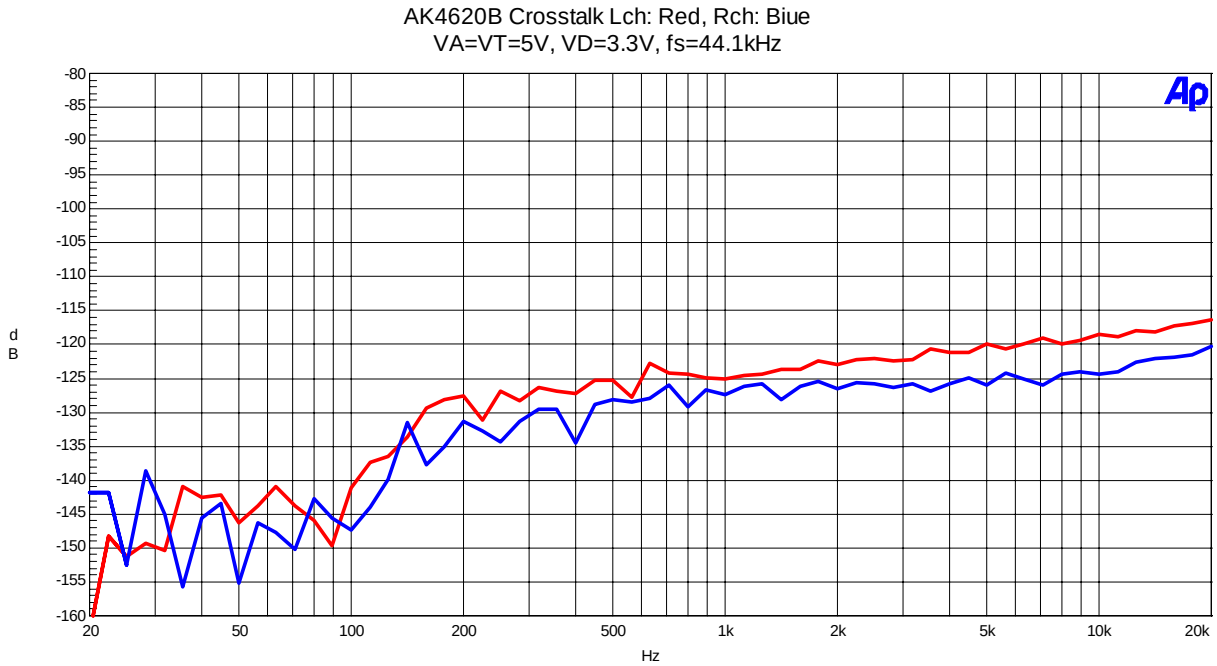


Figure 42. Crosstalk

(fs=96kHz)

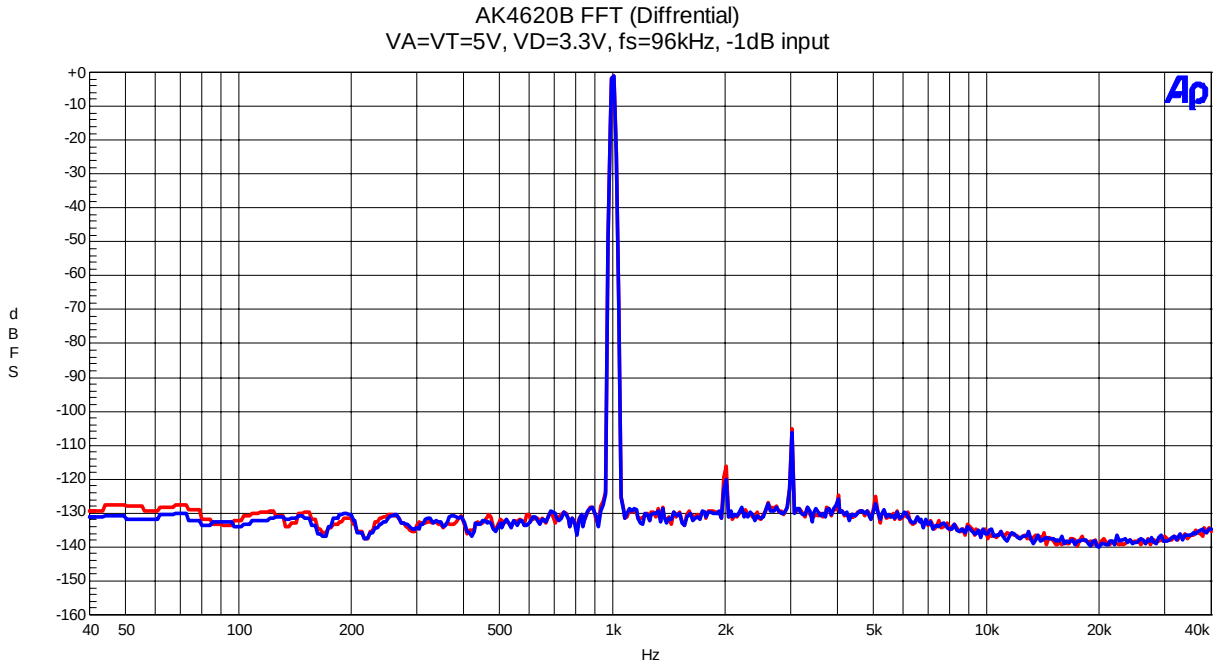


Figure 43. FFT (fin=1kHz, Input Level=-1dBFS)

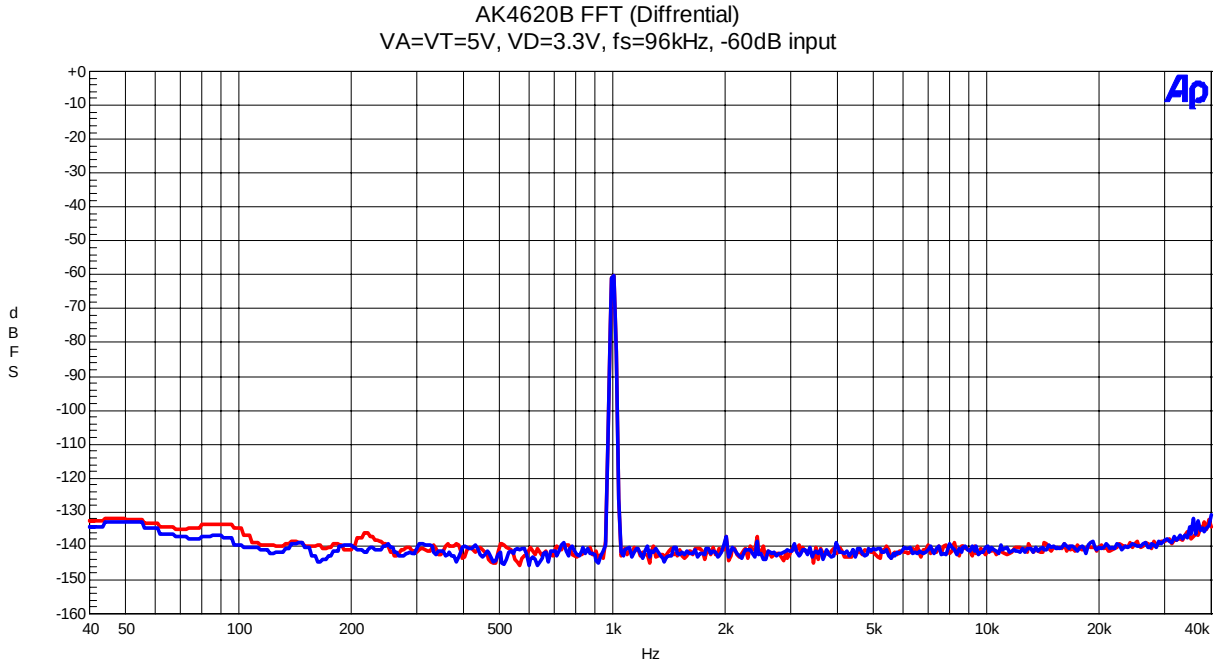


Figure 44. FFT (fin=1kHz, Input Level=-60dBFS)

(fs=96kHz)

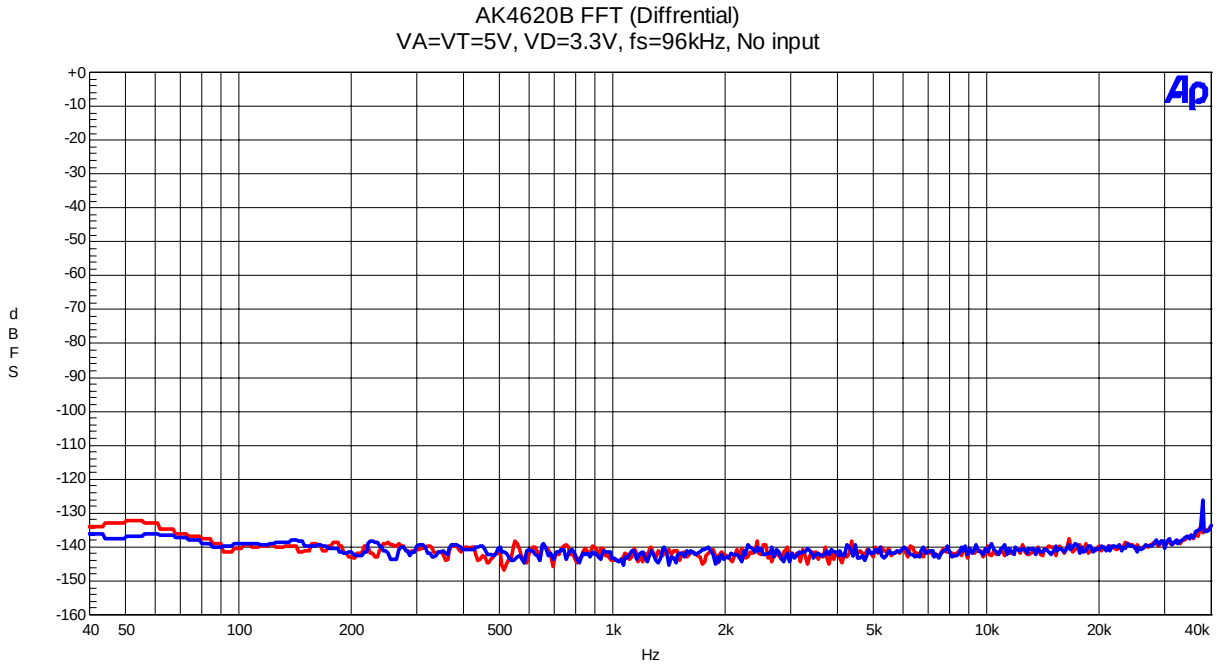


Figure 45. FFT (Noise Floor)

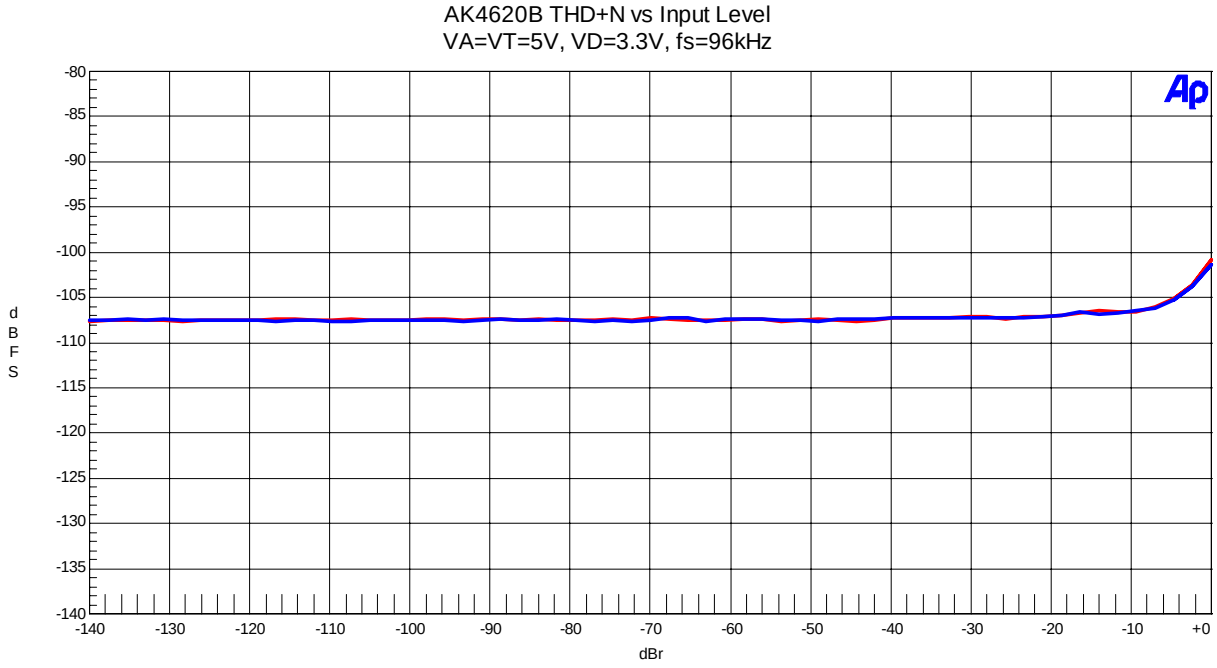


Figure 46. THD +N vs. Input level (fin=1kHz)

(fs=96kHz)

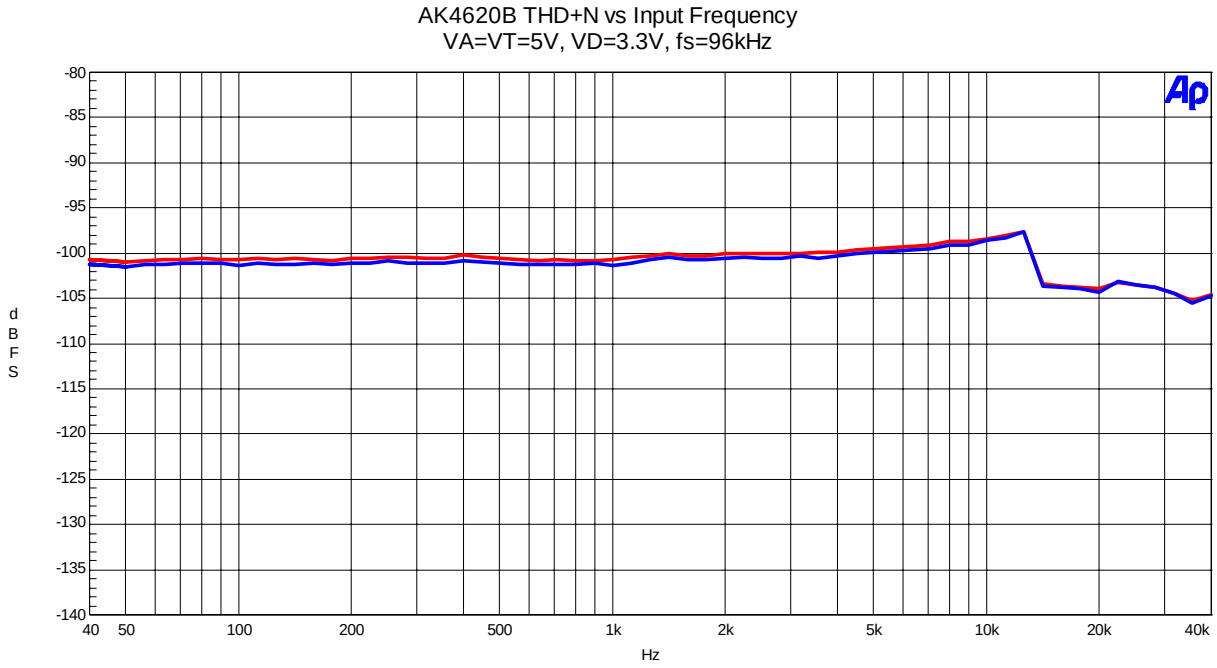


Figure 47. THD +N vs. Input Frequency (Input level=-1dBFS)

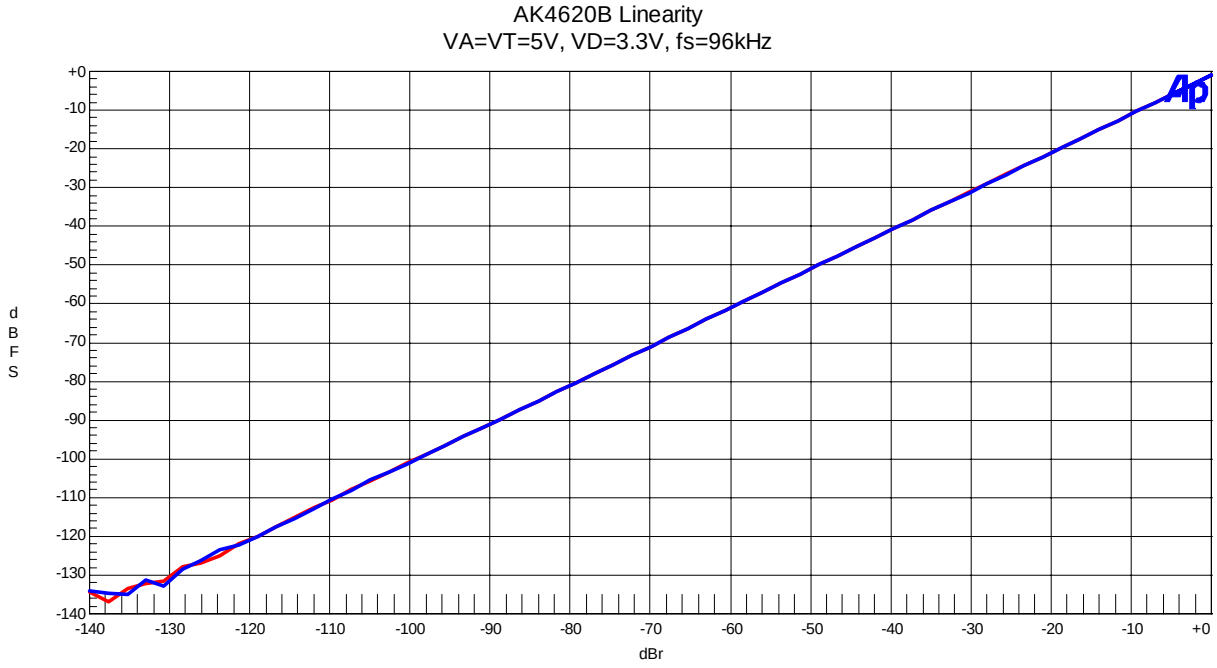


Figure 48. Linearity (fin=1kHz)

(fs=96kHz)

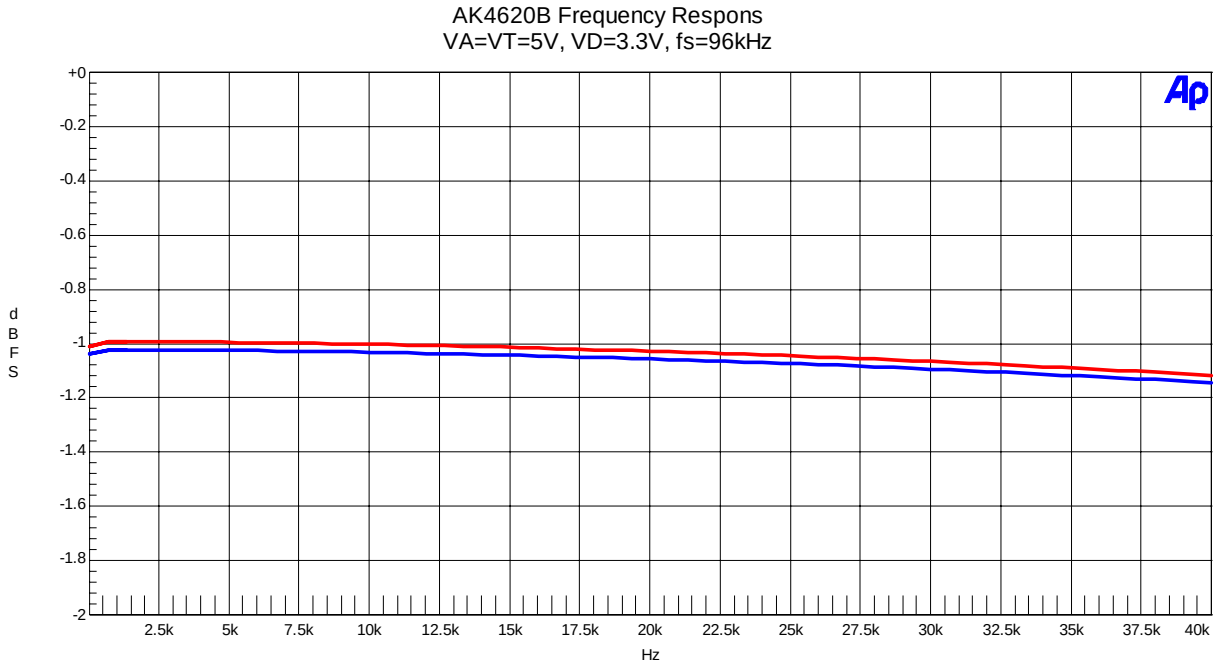


Figure 49. Frequency Response

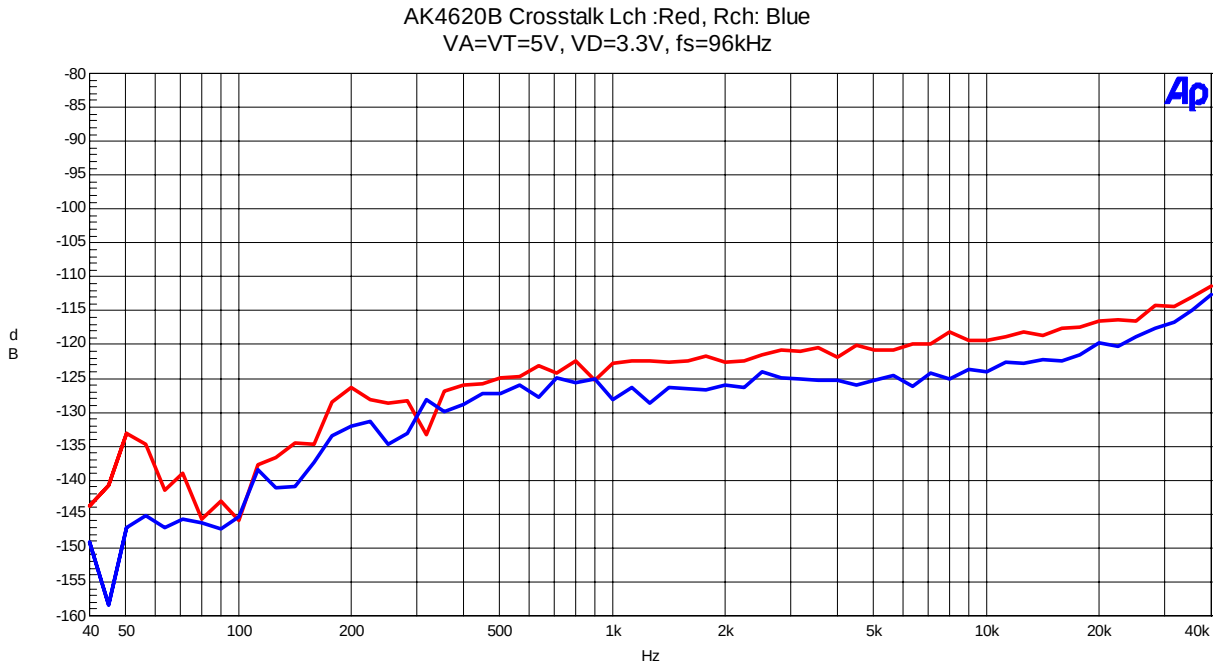


Figure 50. Crosstalk

(fs=192kHz)

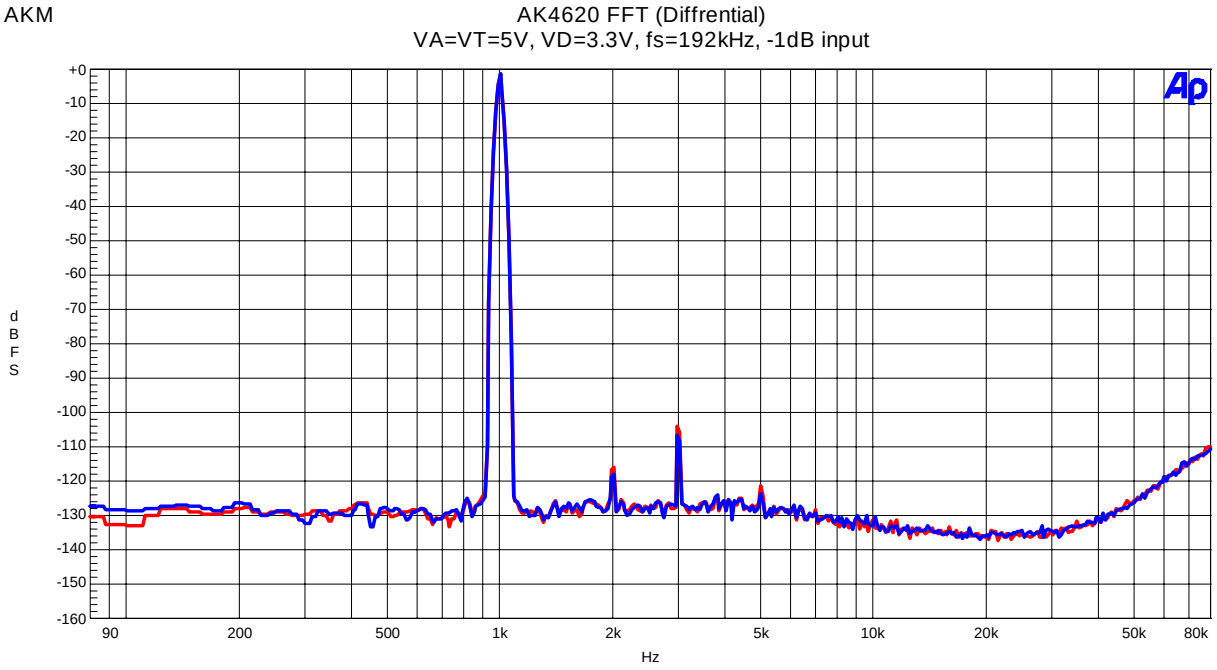


Figure 51. FFT (fin=1kHz, Input Level=-1dBFS)

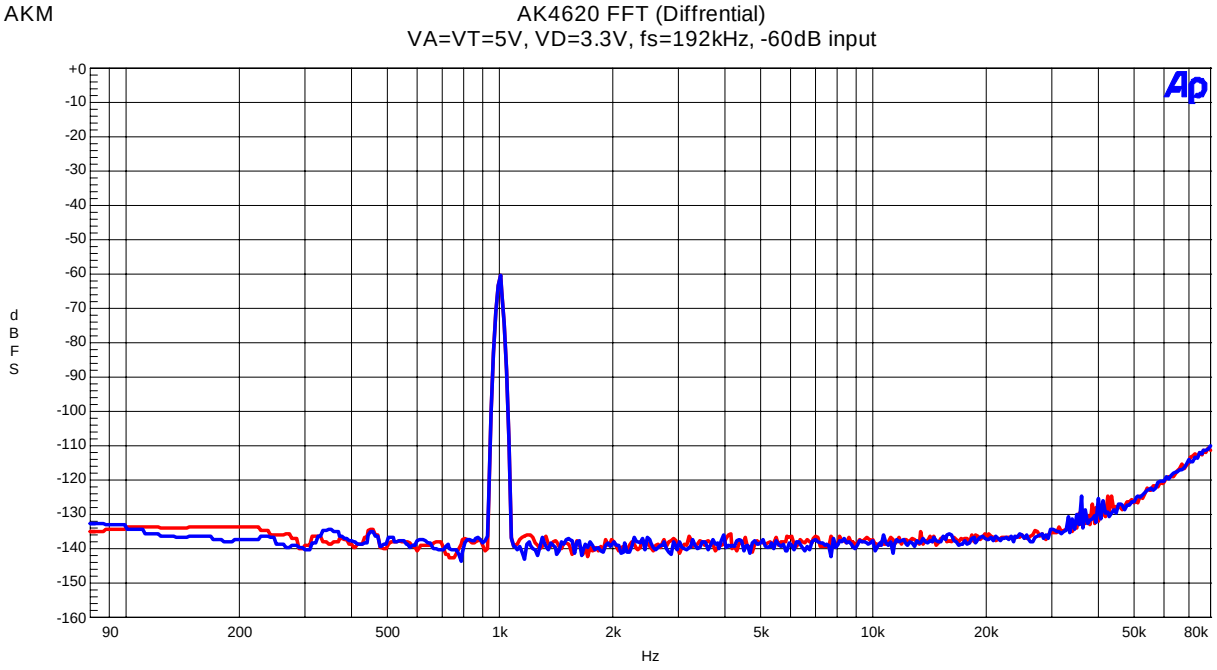


Figure 52. FFT (fin=1kHz, Input Level=-60dBFS)

(fs=192kHz)

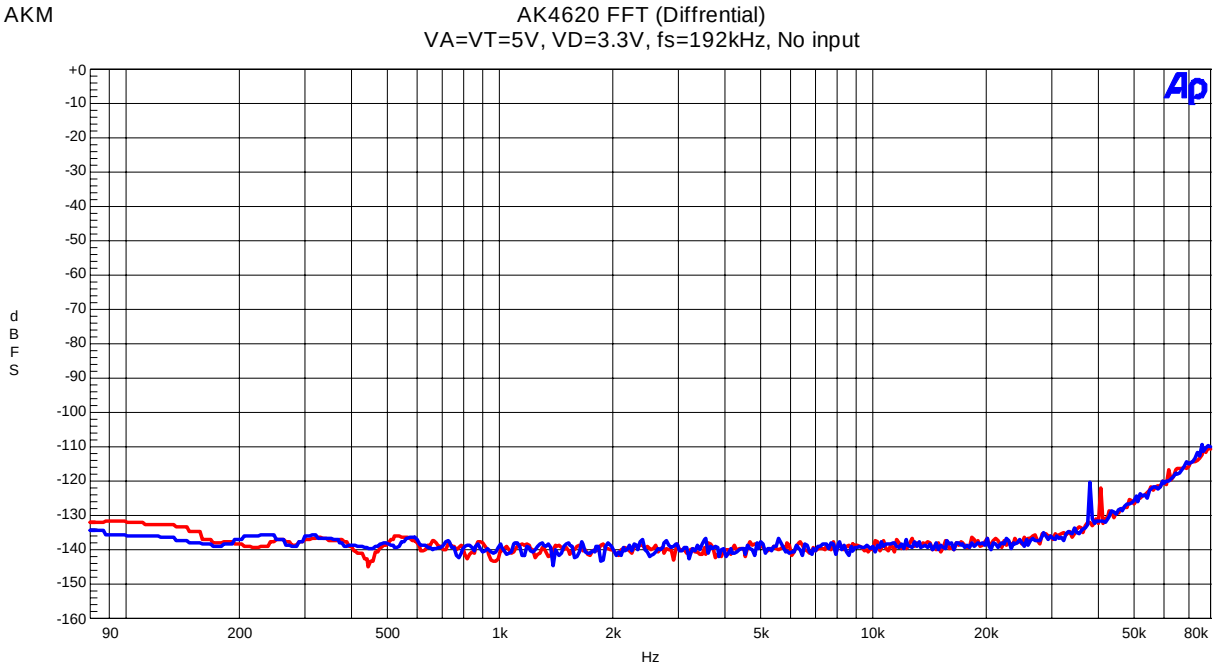


Figure 53. FFT (Noise Floor)

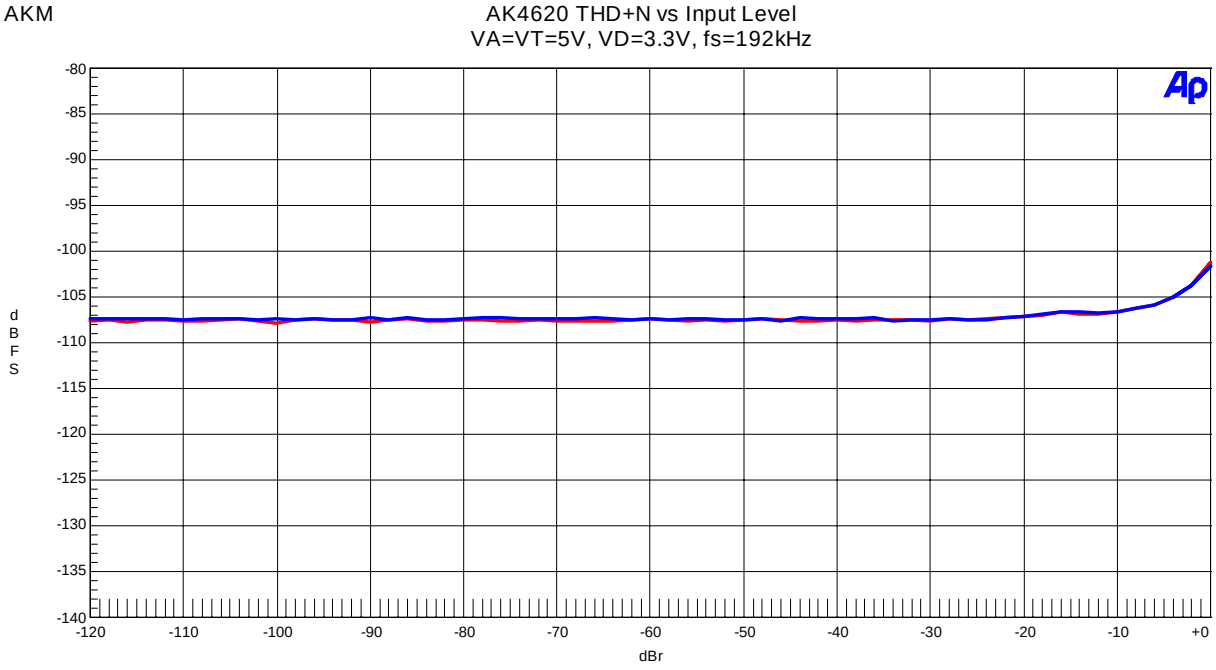


Figure 54. THD+N vs. Input level (fin=1kHz)

(fs=192kHz)

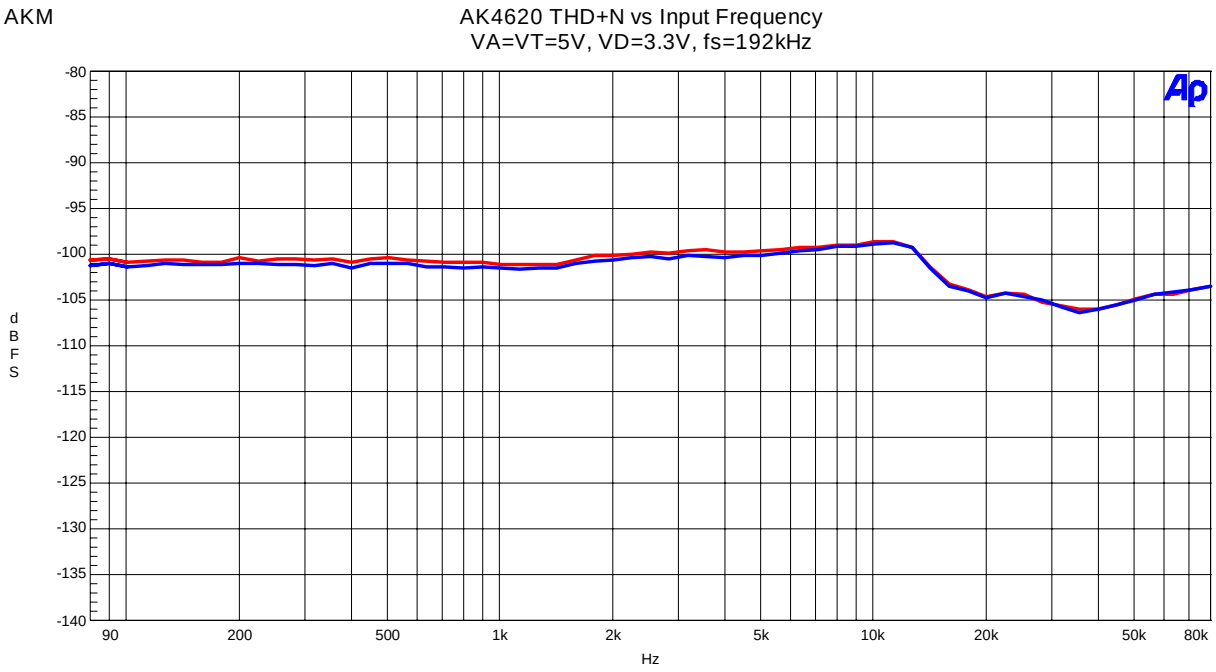


Figure 55. THD+N vs. Input Frequency (Input level=-1dBFS)

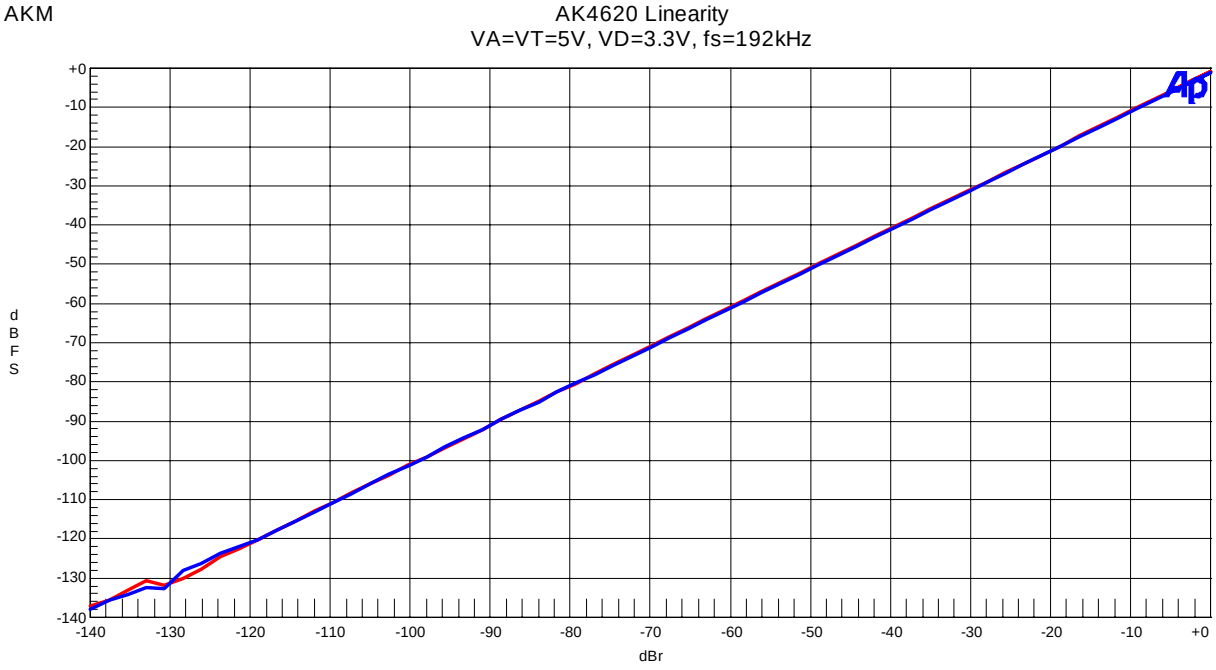


Figure 56. Linearity (fin=1kHz)

(fs=192kHz)

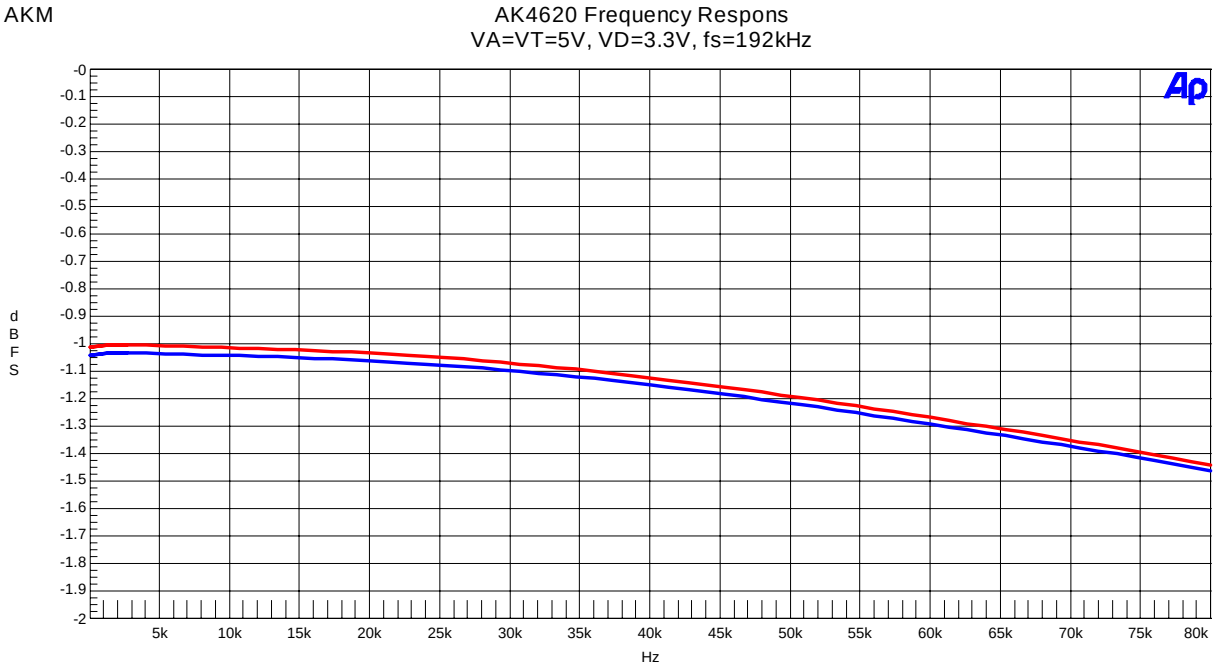


Figure 57. Frequency Response

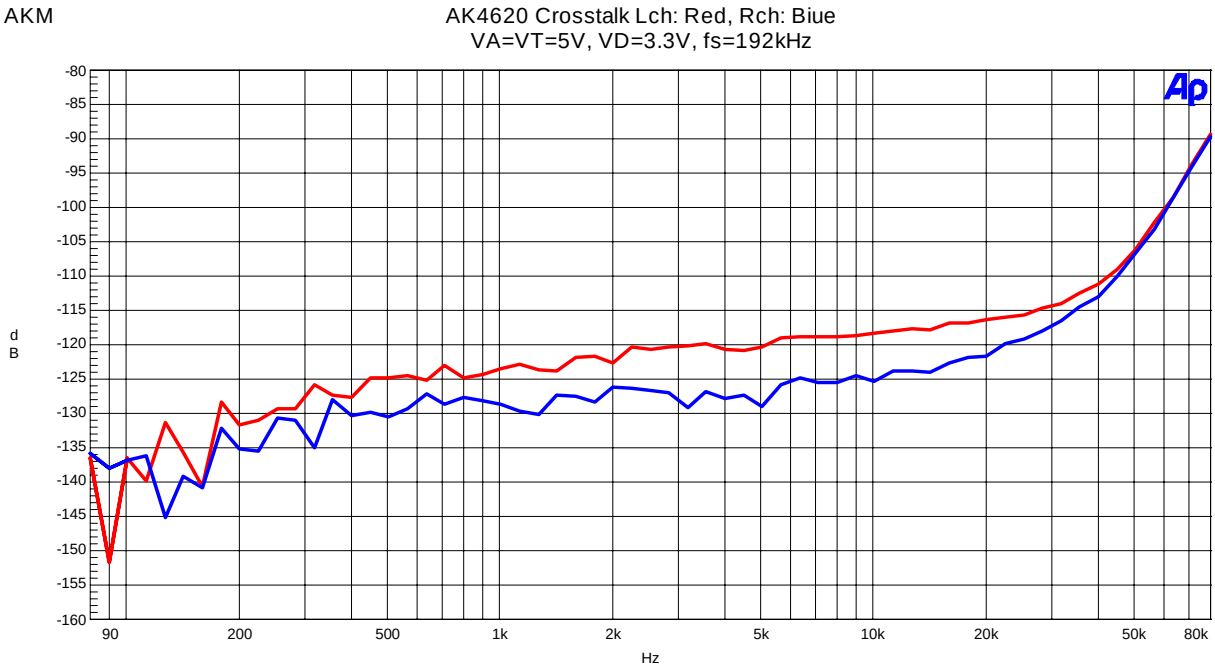


Figure 58. Crosstalk

DAC

(fs=44.1kHz)

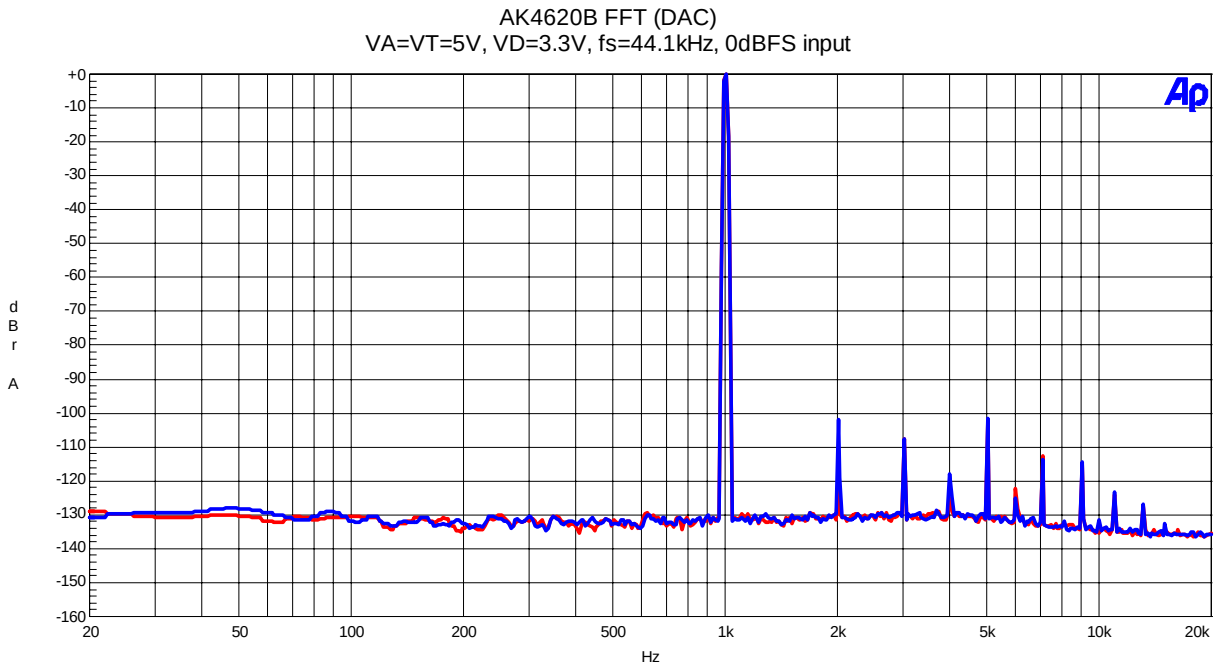


Figure 59. FFT (fin=1kHz, Input Level=0BFS)

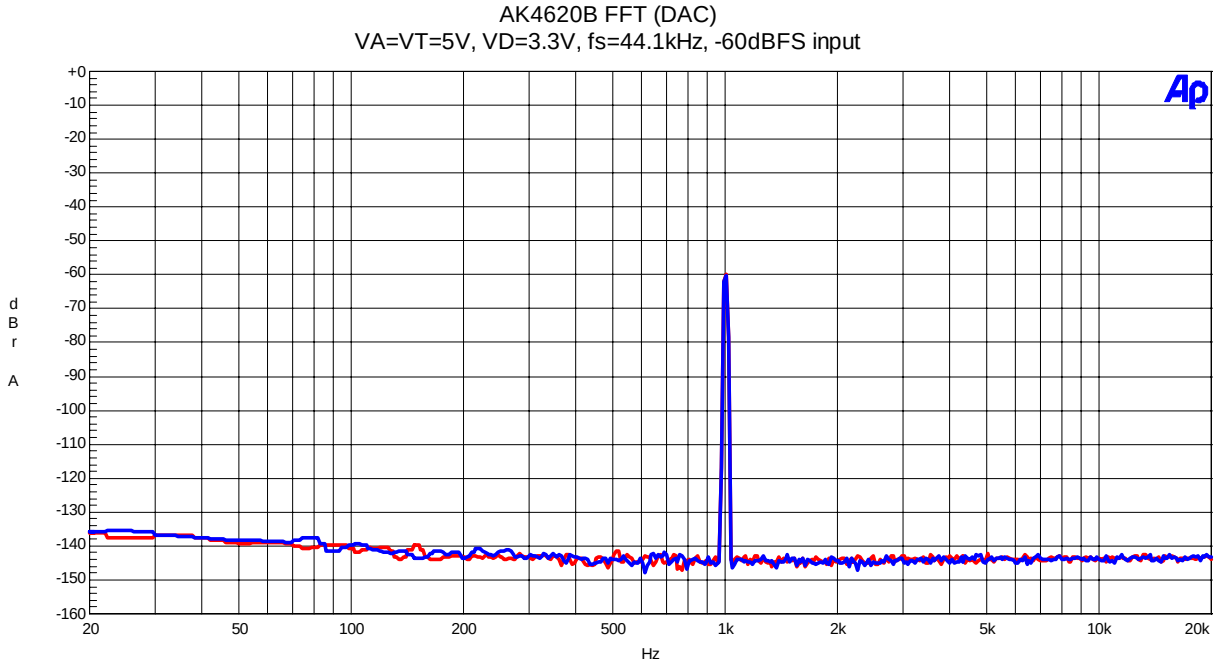


Figure 60. FFT (fin=1kHz, Input Level=-60dBFS)

(fs=44.1kHz)

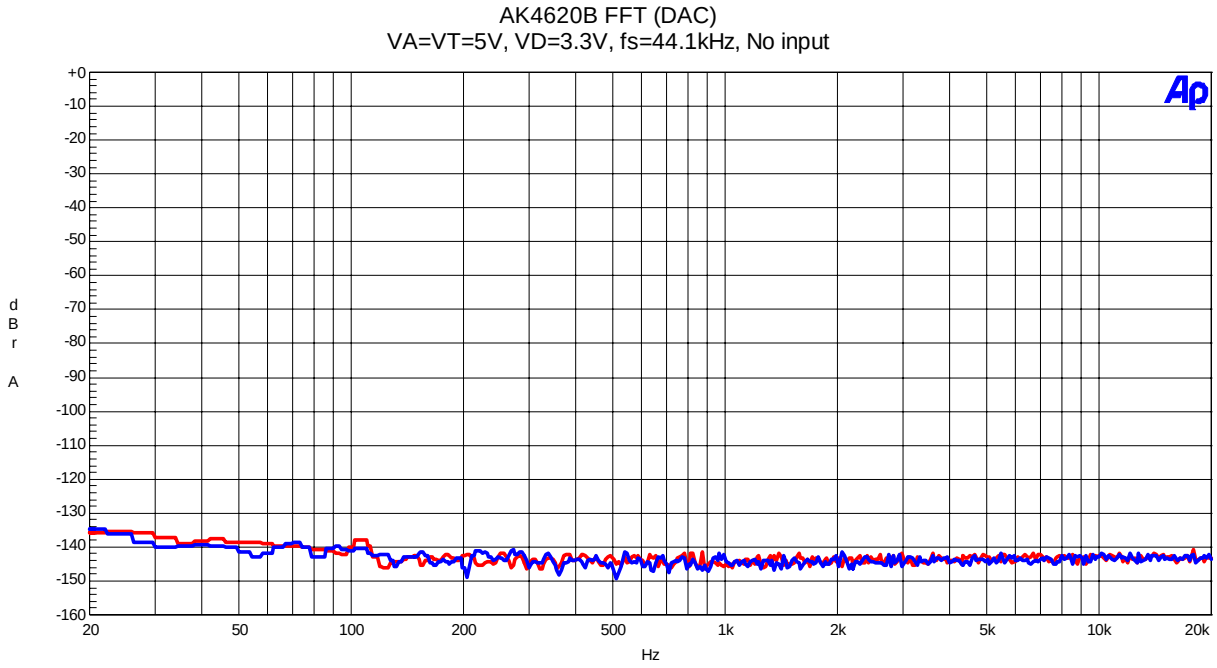


Figure 61. FFT (Noise Floor)

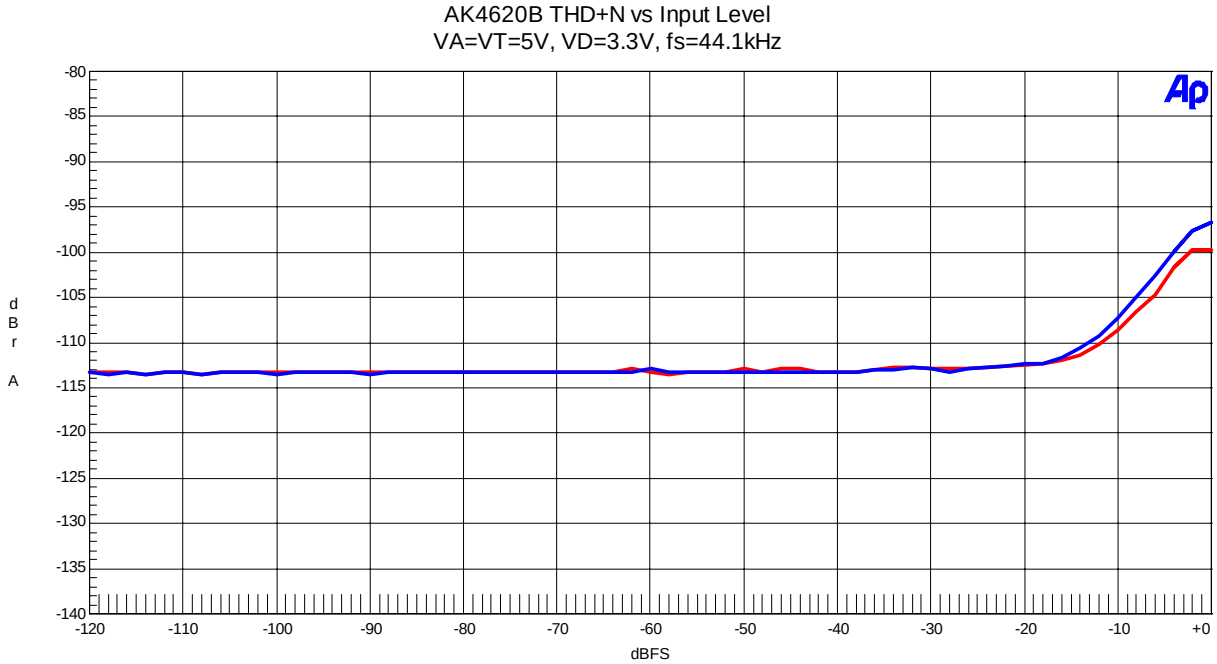


Figure 62. THD+N vs. Input level (fin=1kHz)

(fs=44.1kHz)

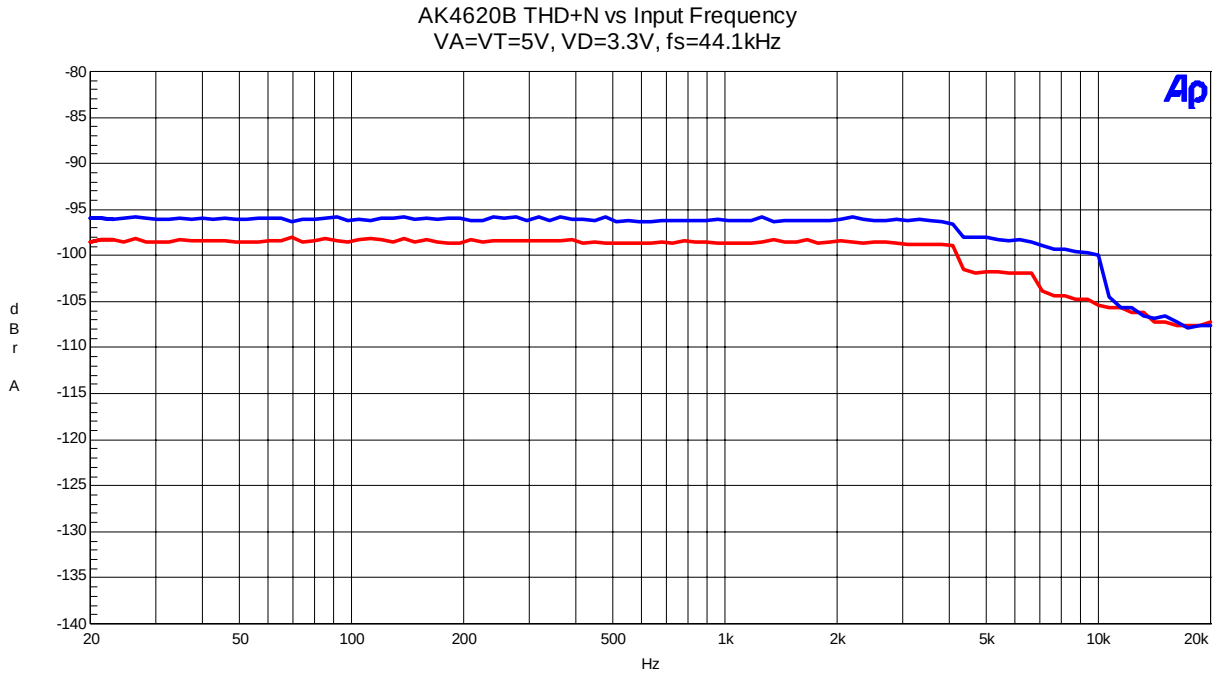


Figure 63. THD +N vs. Input Frequency (Input level=0dBFS)

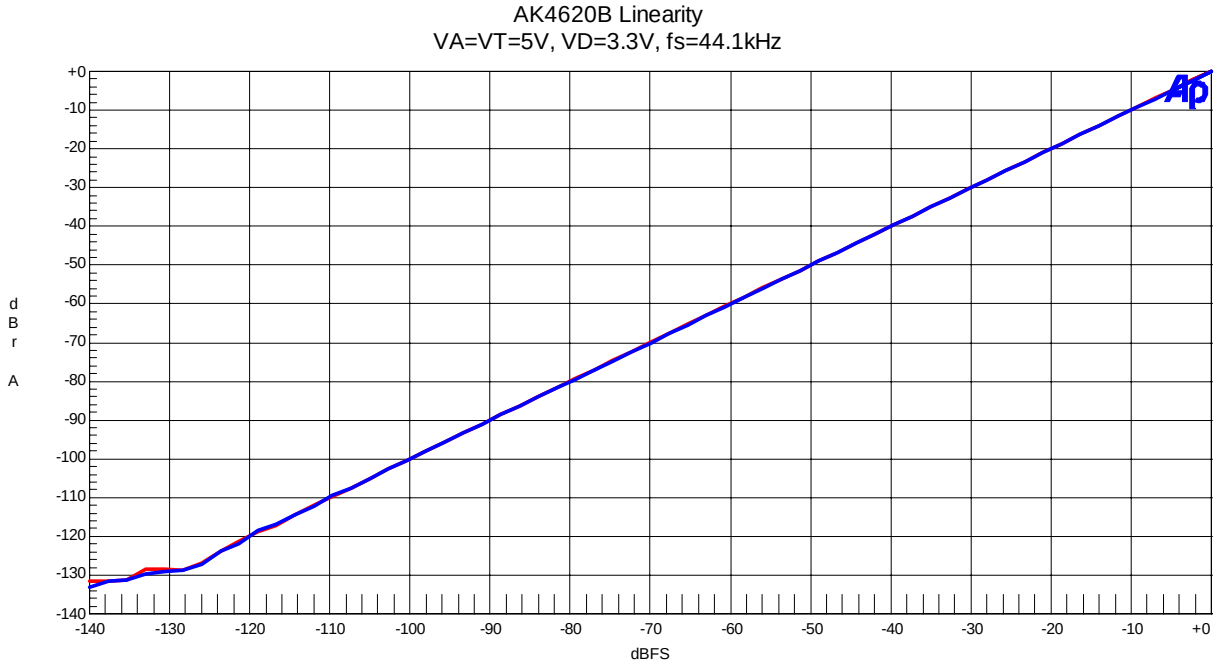


Figure 64. Linearity (fin=1kHz)

(fs=44.1kHz)

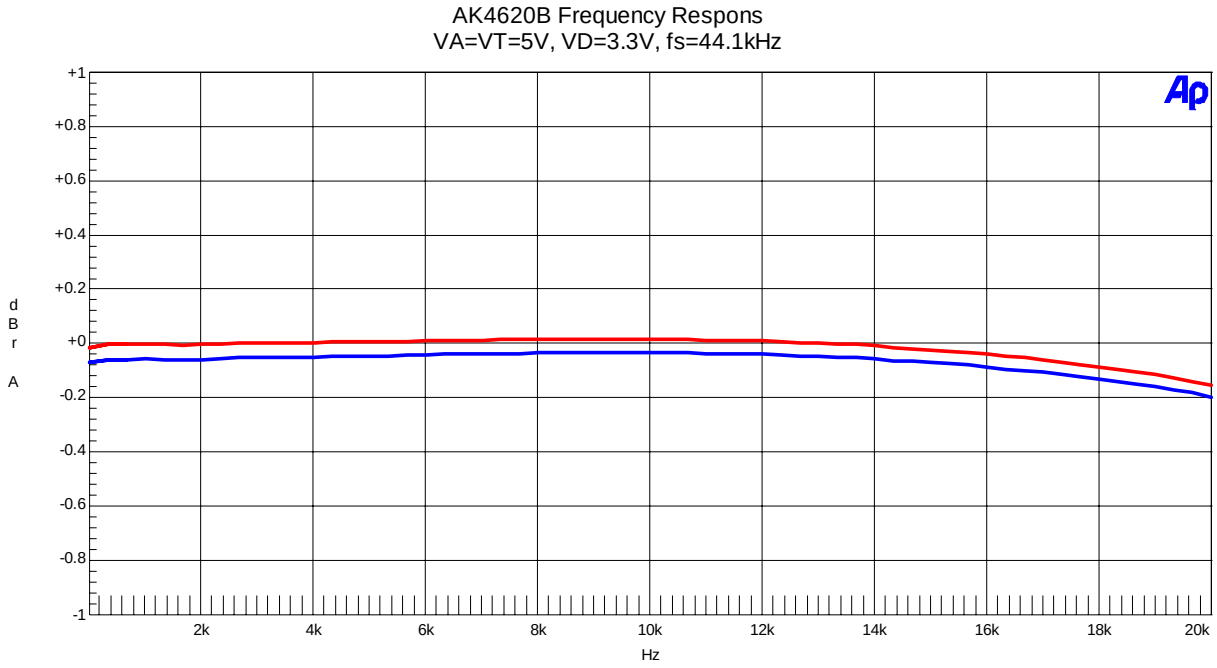


Figure 65. Frequency Response (Input level=0dBFS)

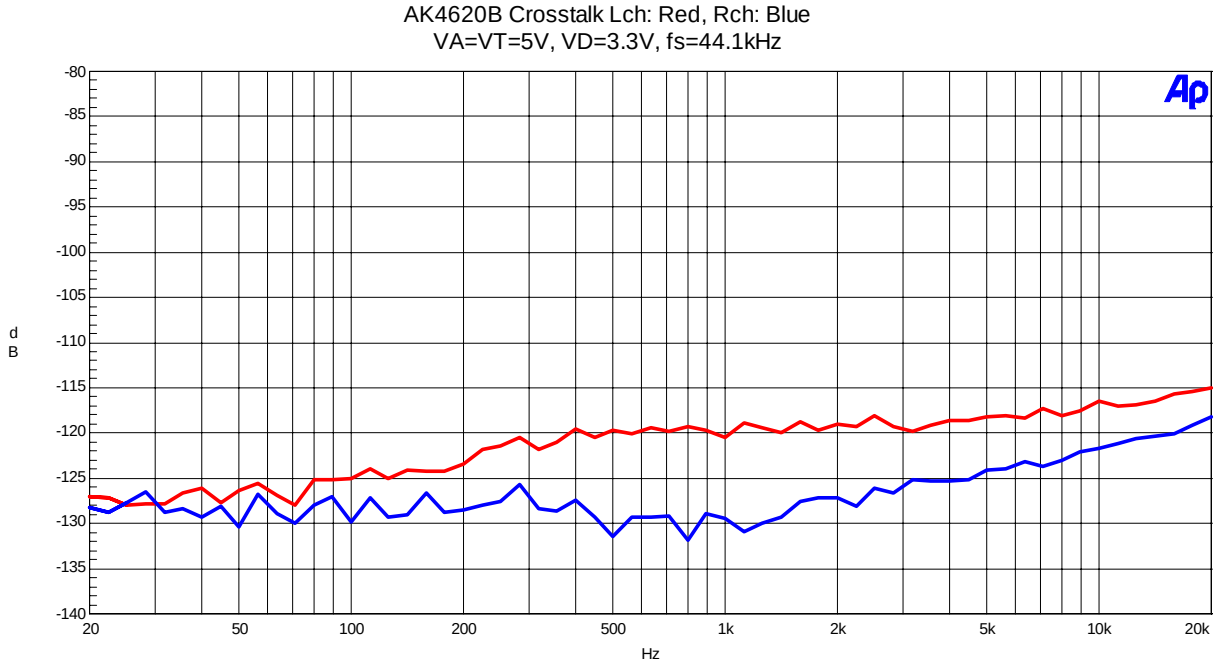


Figure 66. Crosstalk

(fs=44.1kHz)

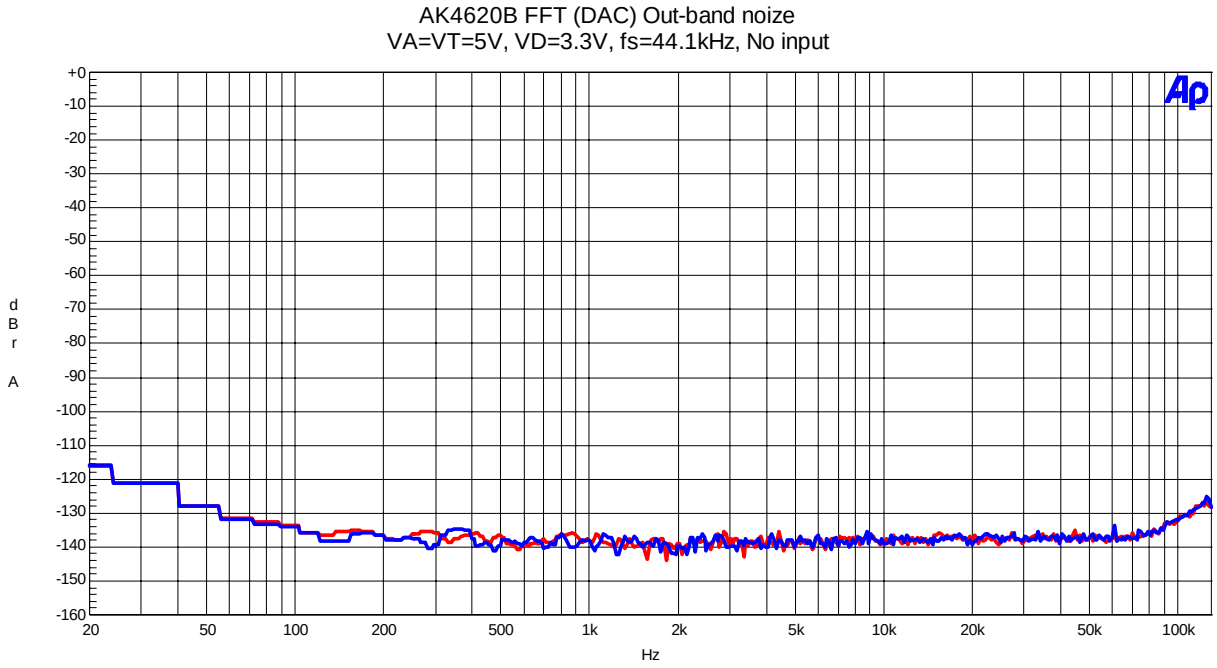


Figure 67. Out-of-band Noise

(fs=96kHz)

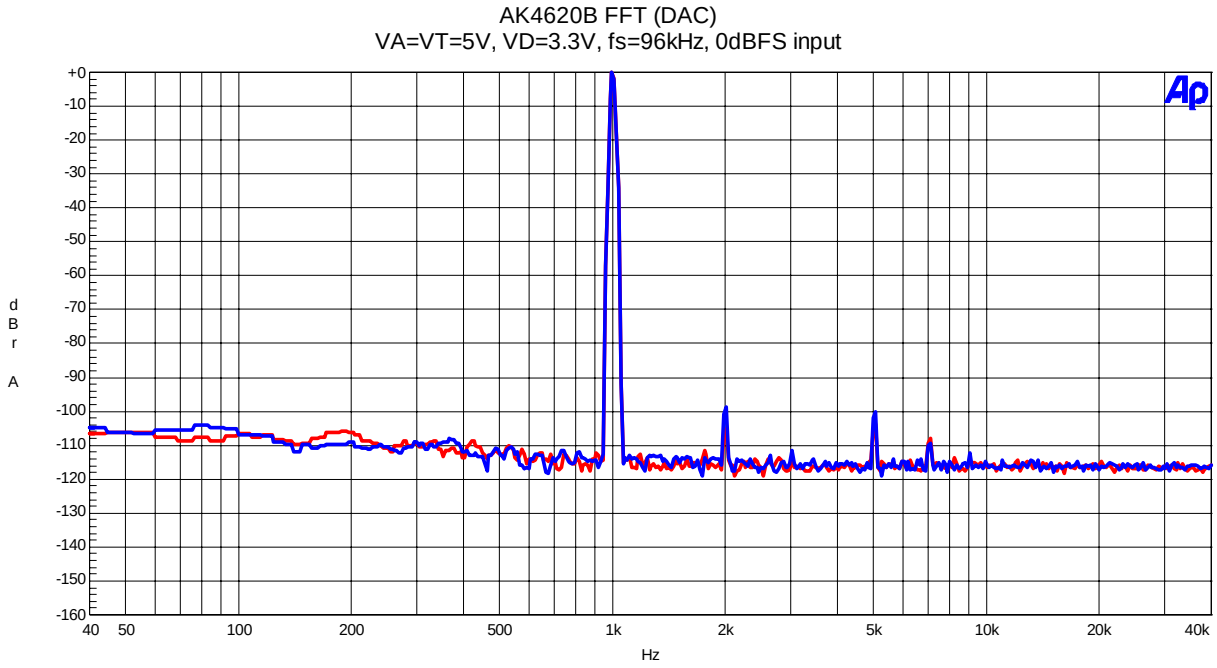


Figure 68. FFT (fin=1kHz, Input Level=0dBFS)

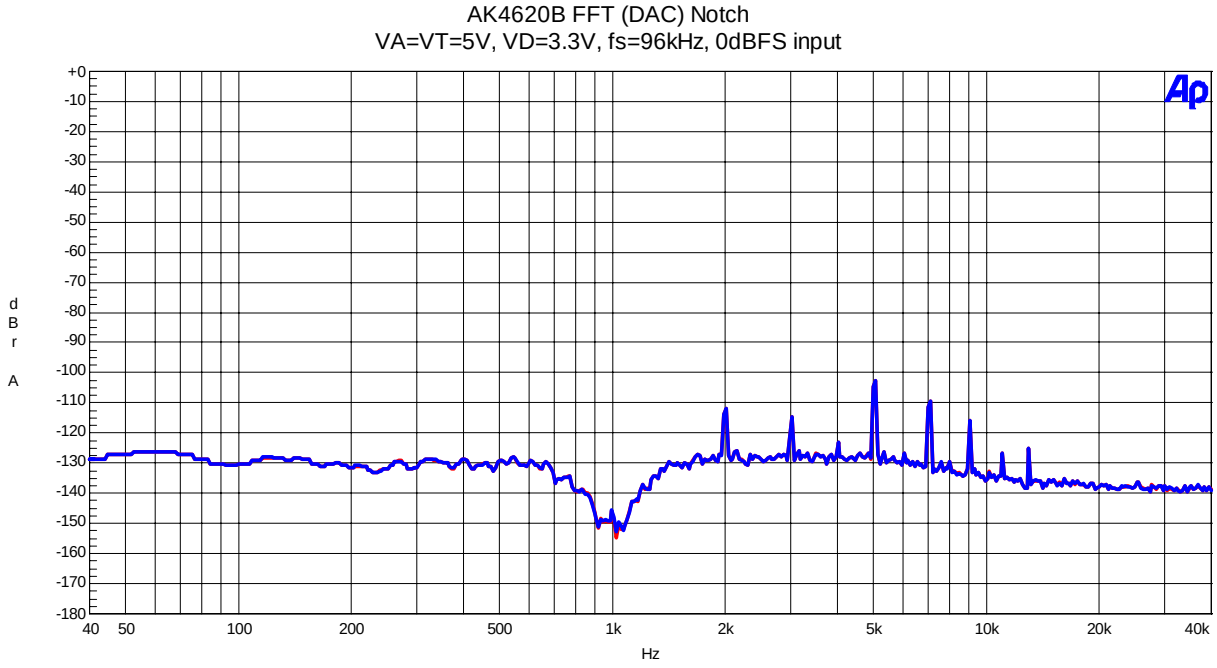


Figure 69. FFT (fin=1kHz, Input Level=0dBFS, Notch Filter)

(fs=96kHz)

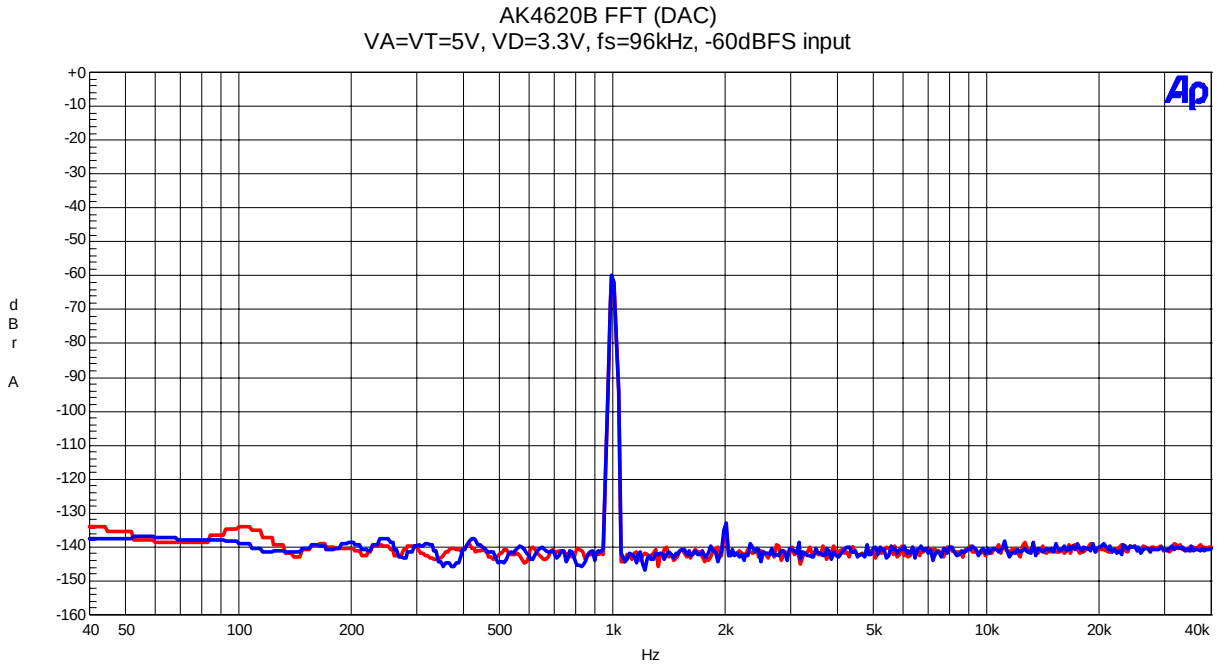


Figure 70. FFT (fin=1kHz, Input Level=-60dBFS)

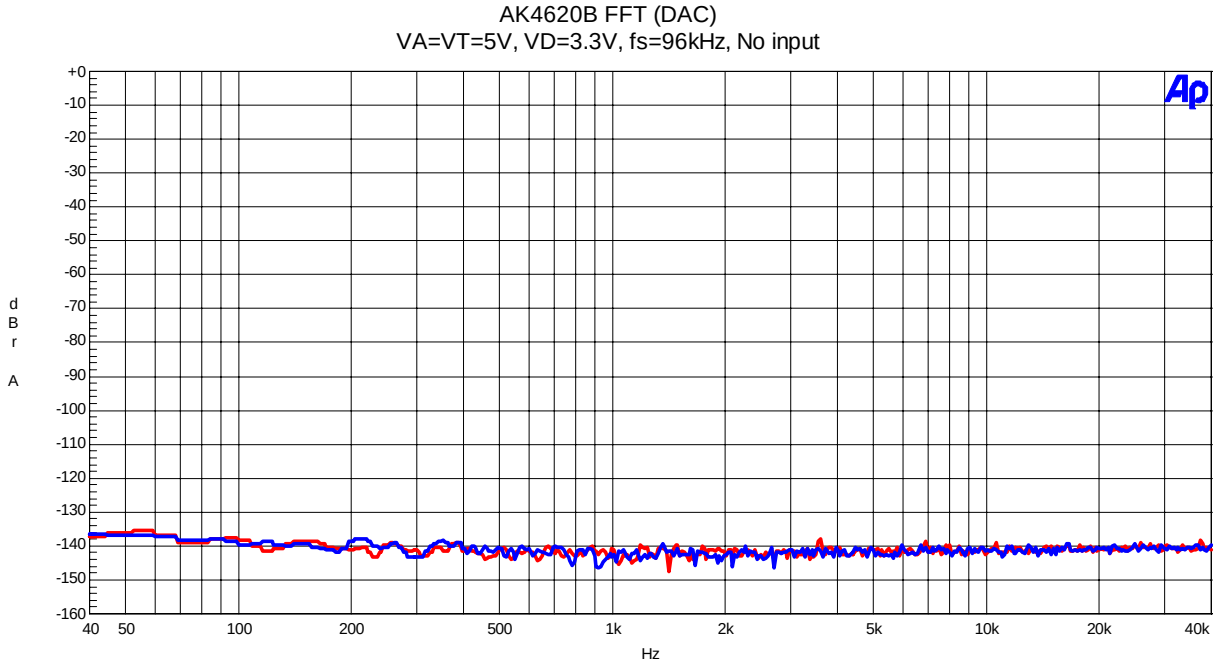


Figure 71. FFT (Noise Floor)

(fs=96kHz)

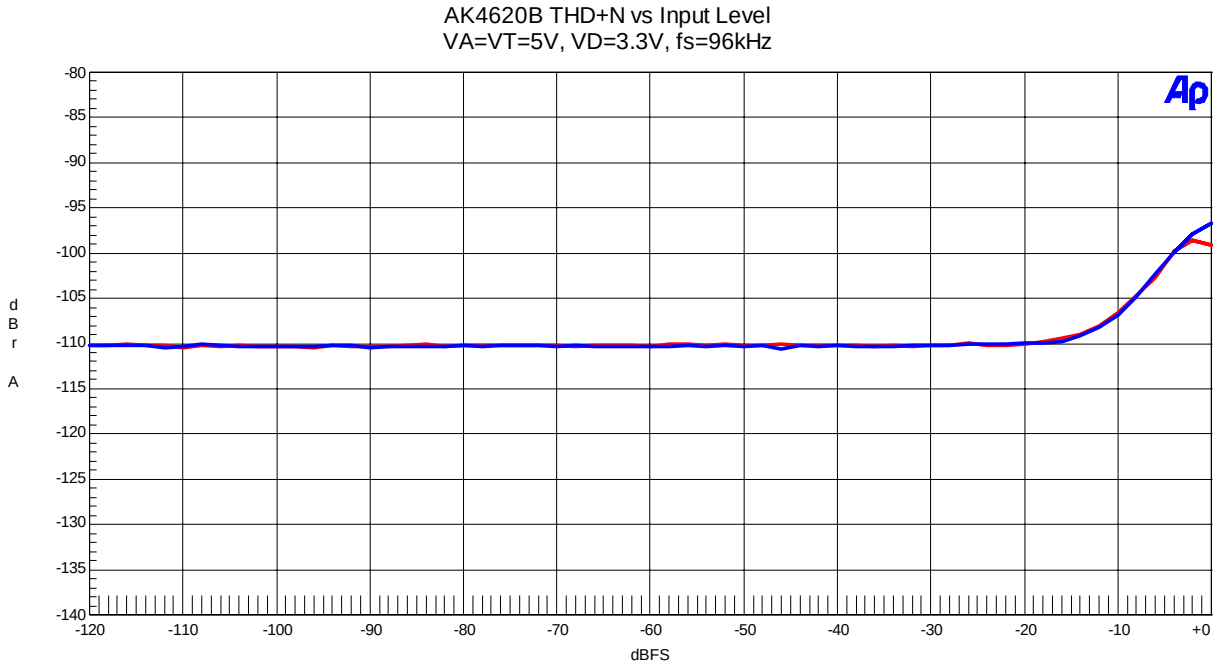


Figure 72. THD +N vs. Input level (fin=1kHz)

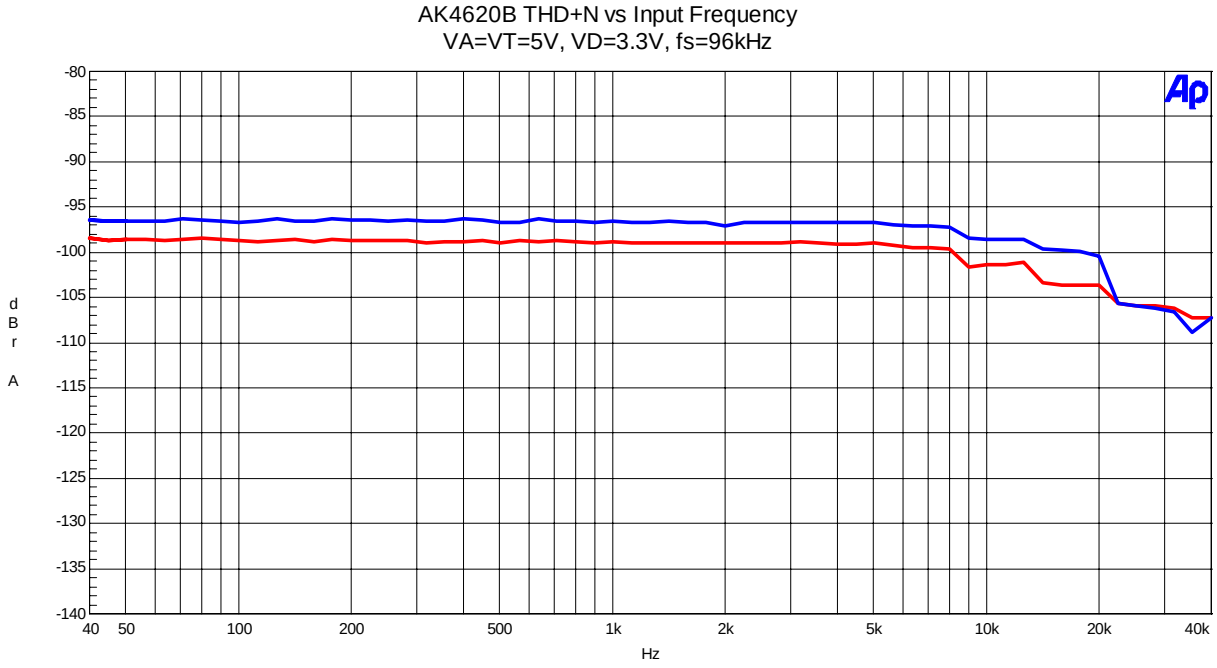


Figure 73. THD +N vs. Input Frequency (Input level=0dBFS)

(fs=96kHz)

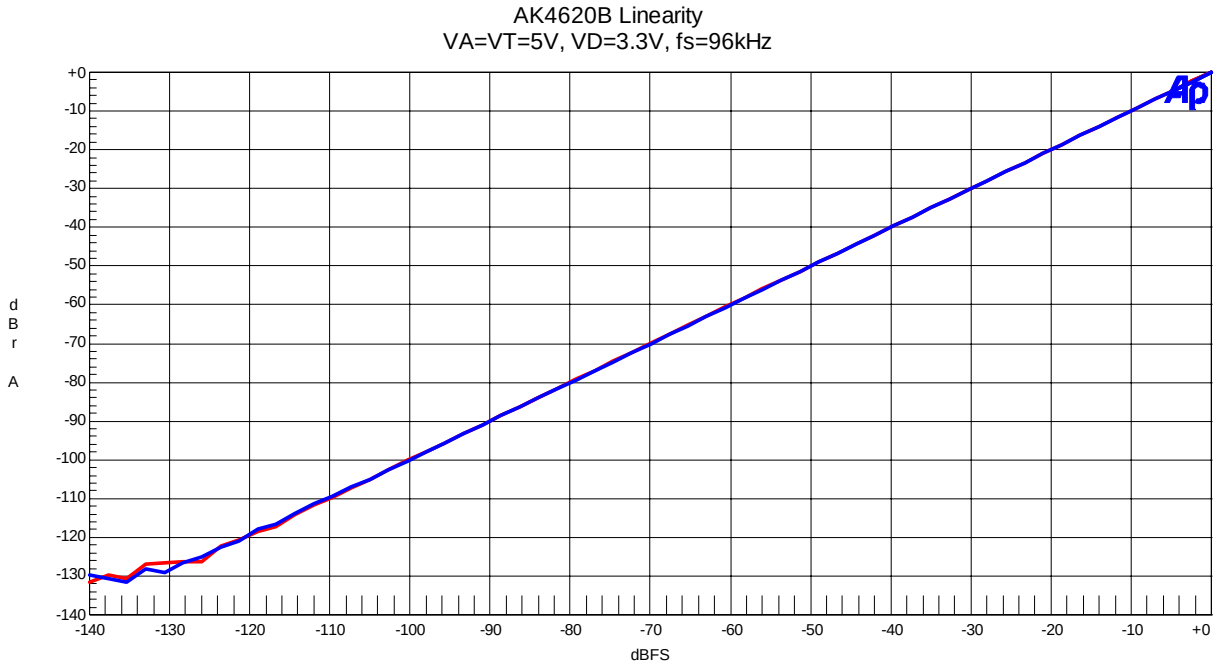


Figure 74. Linearity (fin=1kHz)

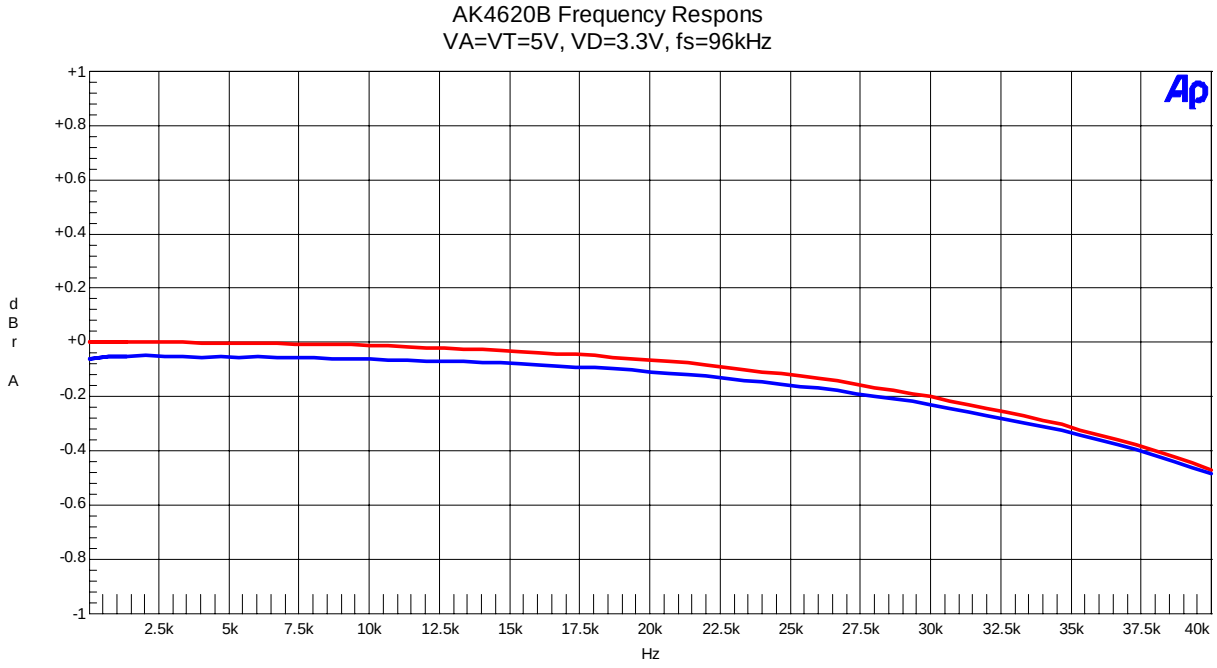


Figure 75. Frequency Response (Input level=0dBFS)

(fs=96kHz)

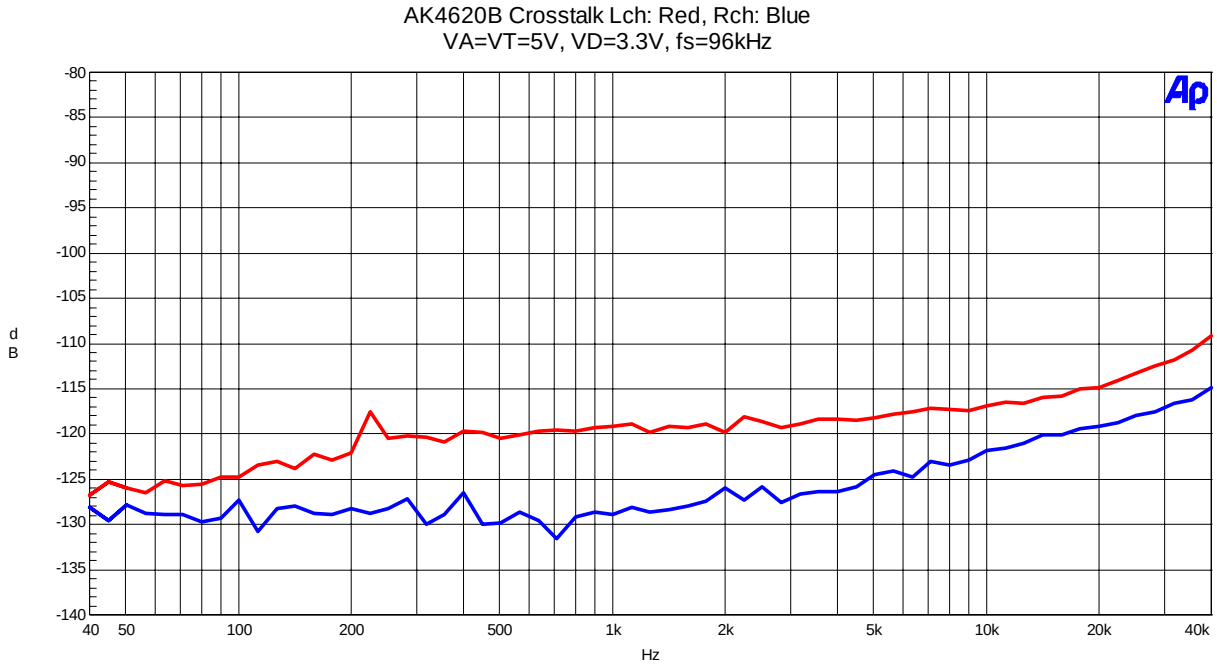


Figure 76. Crosstalk

(fs=192kHz)

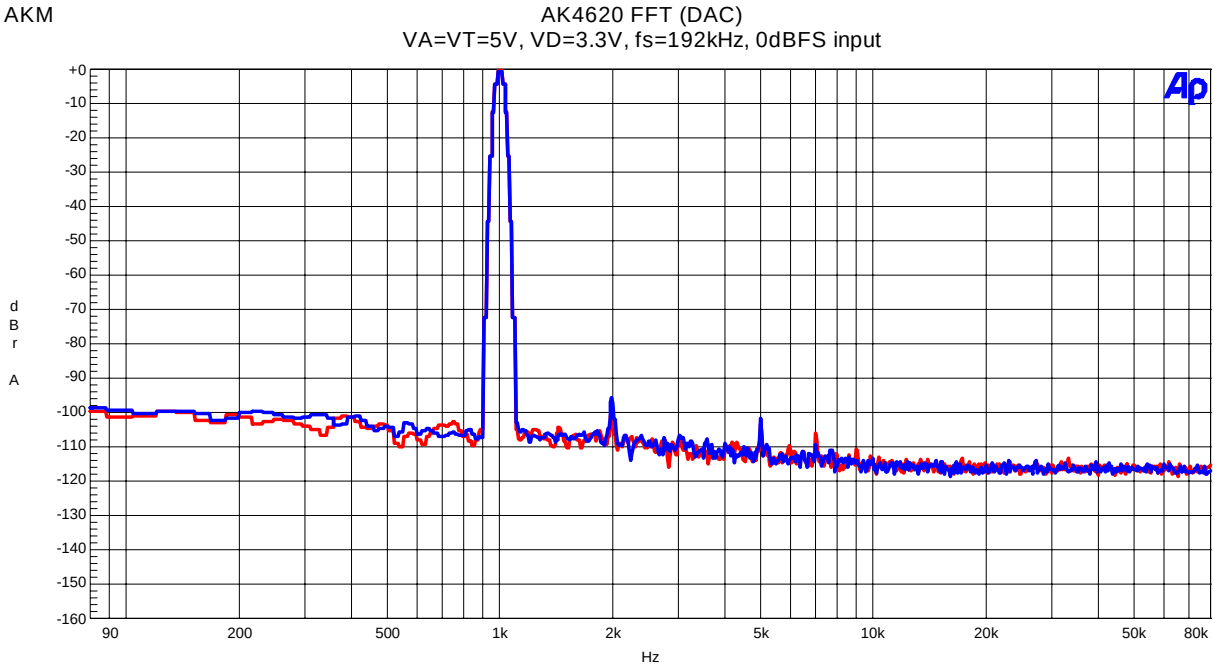


Figure 77. FFT (fin=1kHz, Input Level=0dBFS)

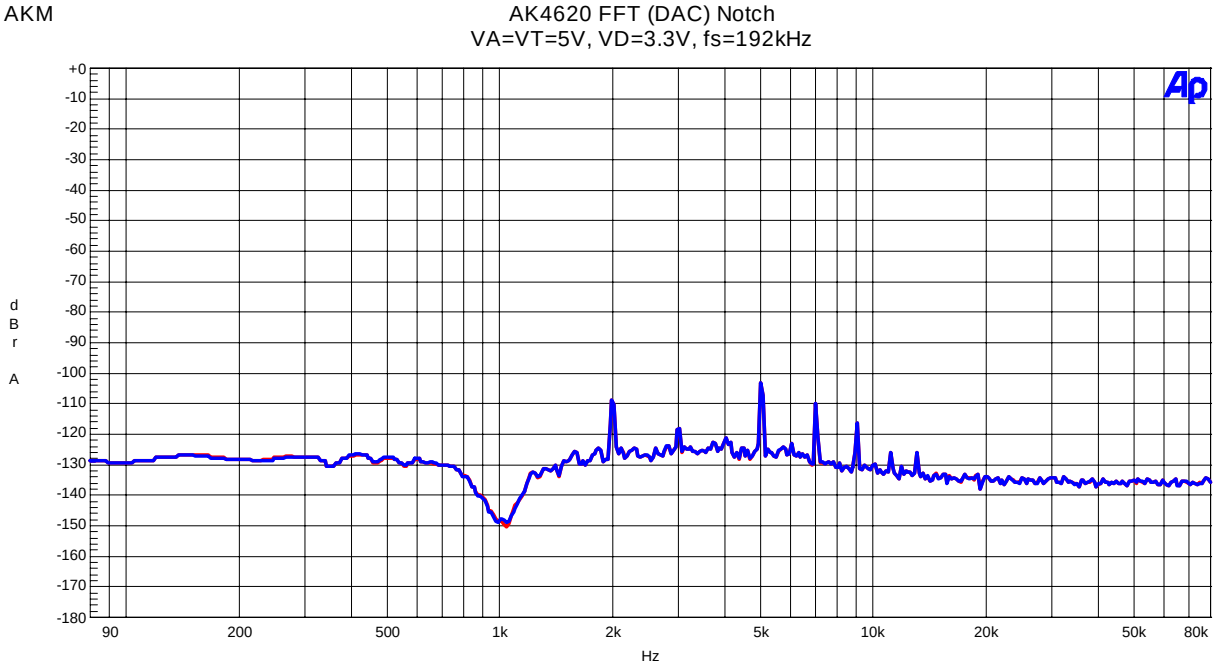


Figure 78. FFT (fin=1kHz, Input Level=0dBFS, Notch Filter)

(fs=192kHz)

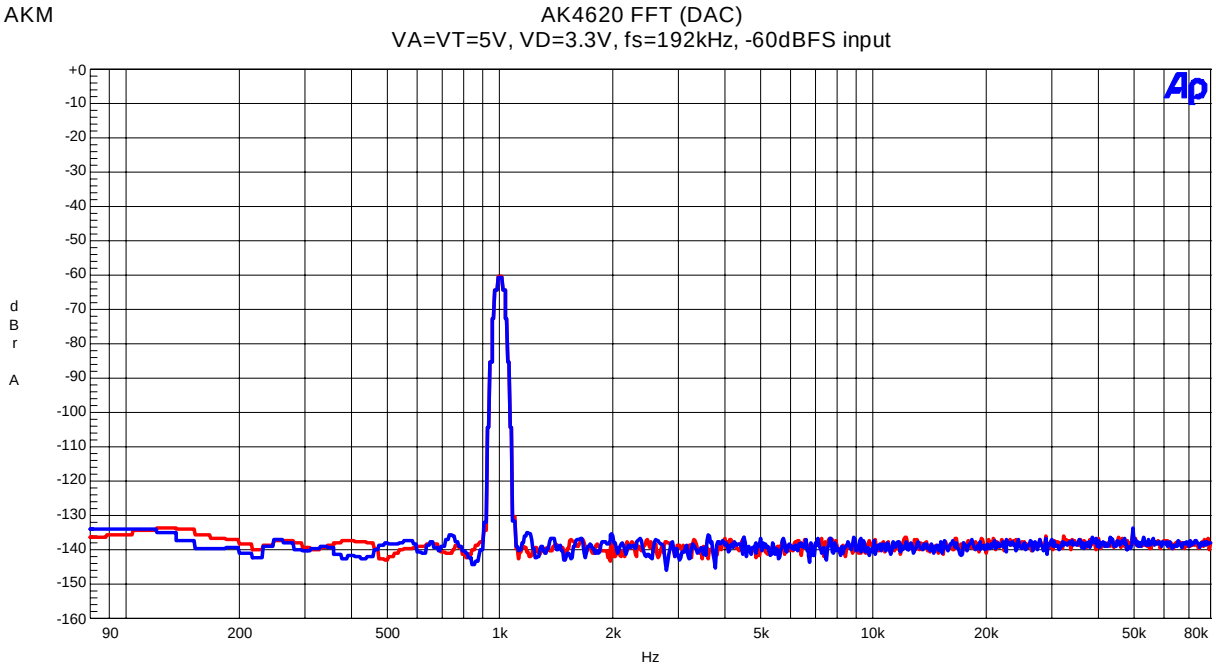


Figure 79. FFT (fin=1kHz, Input Level=-60dBFS)

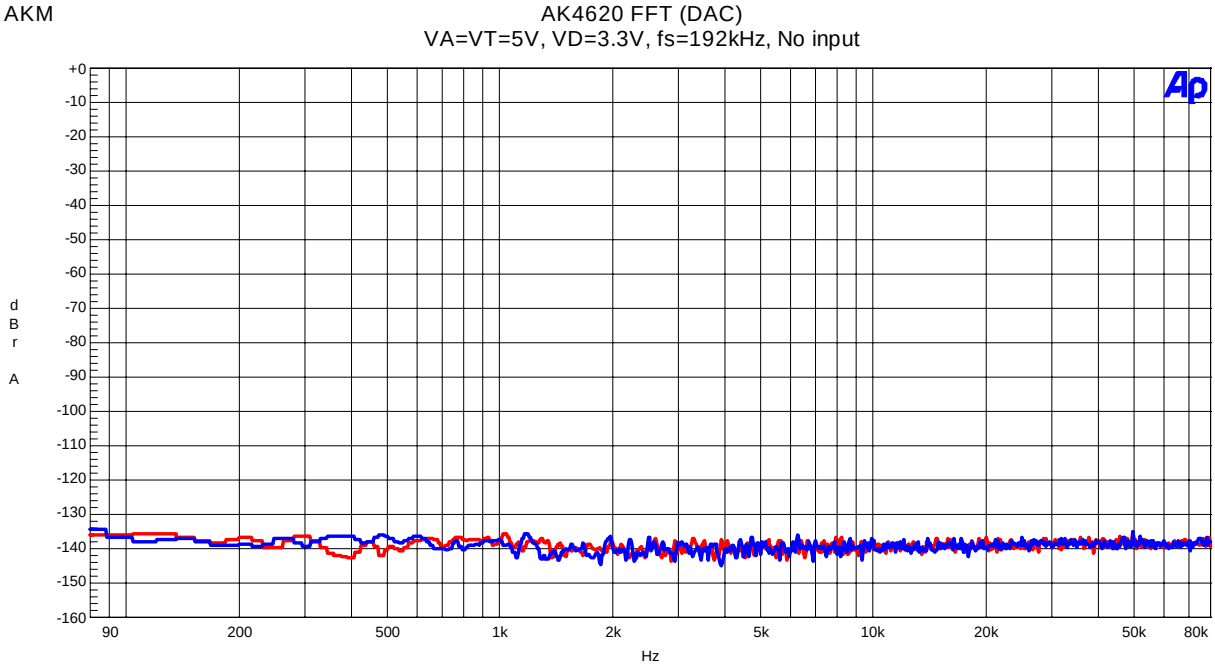


Figure 80. FFT (Noise Floor)

(fs=192kHz)

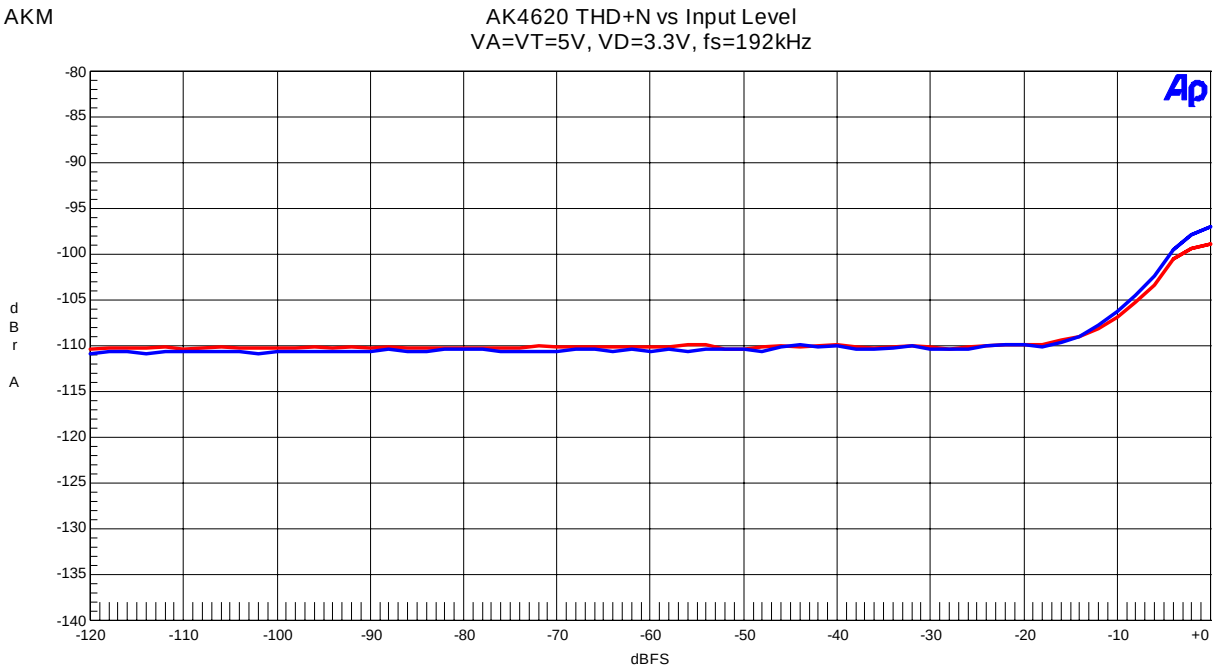


Figure 81. THD+N vs. Input level (fin=1kHz)

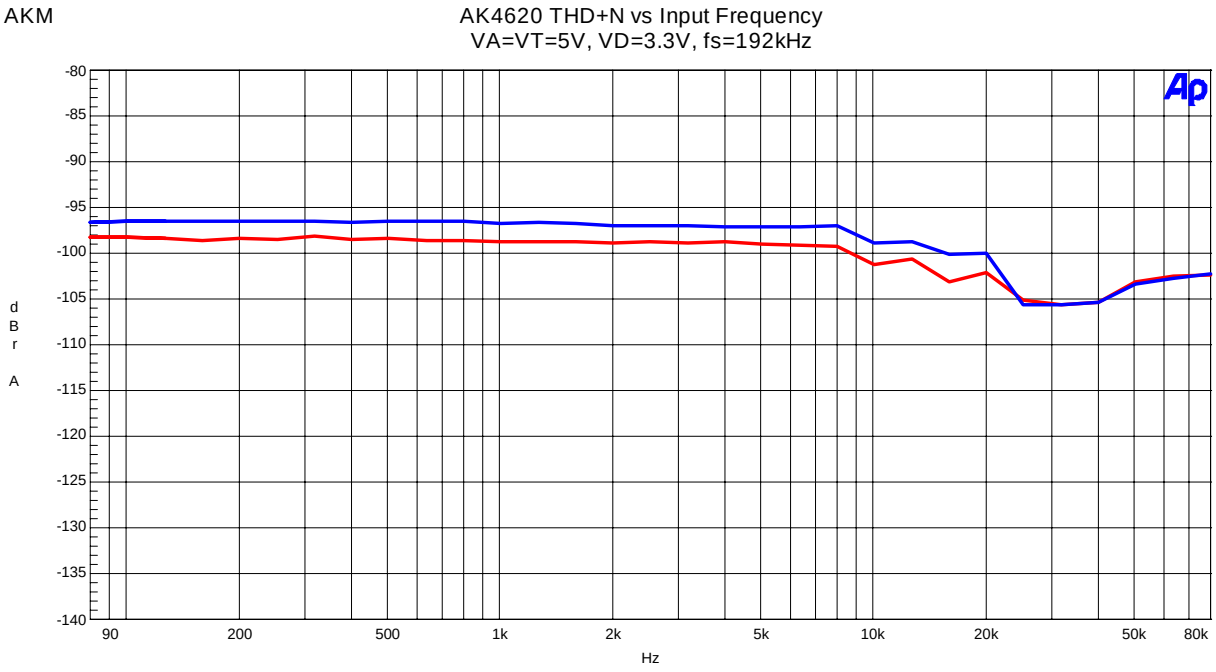


Figure 82. THD+N vs. Input Frequency (Input level=0dBFS)

(fs=192kHz)

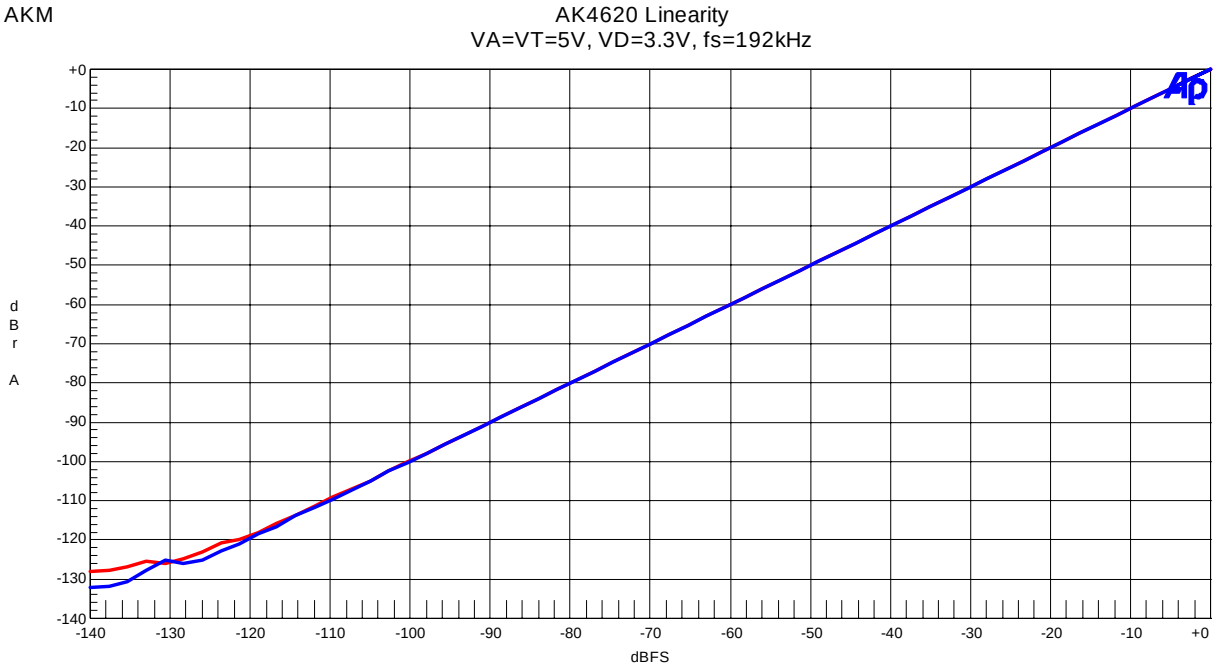


Figure 83. Linearity (fin=1kHz)

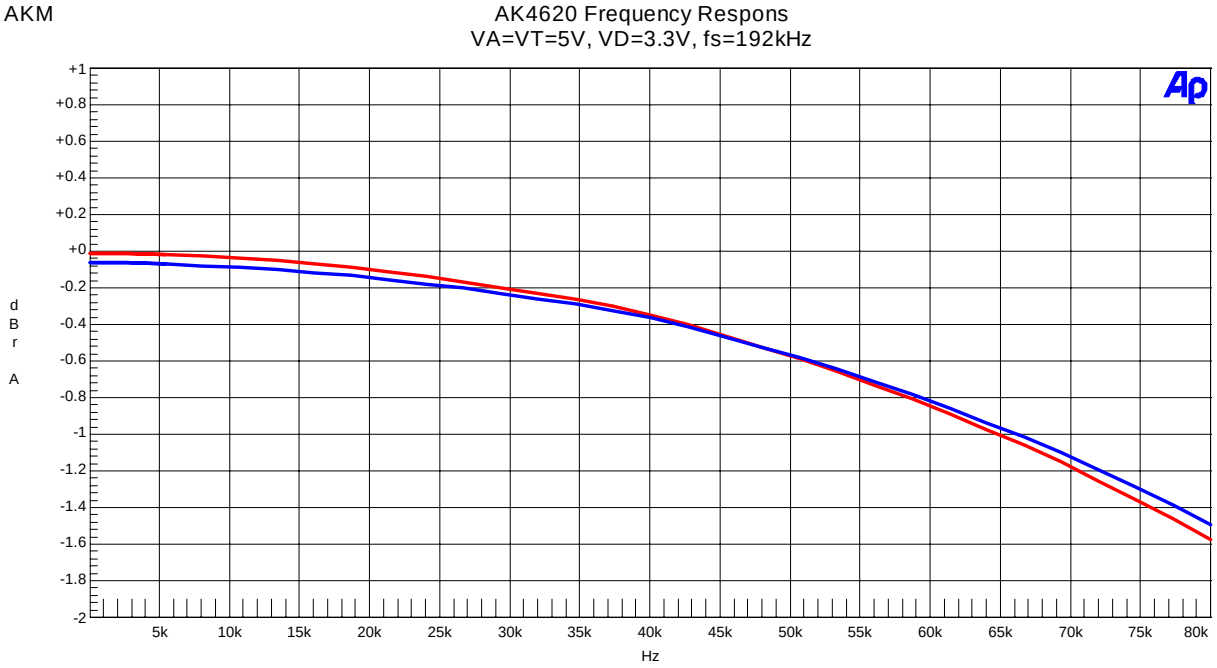


Figure 84. Frequency Response (Input level=0dBFS)

(fs=192kHz)

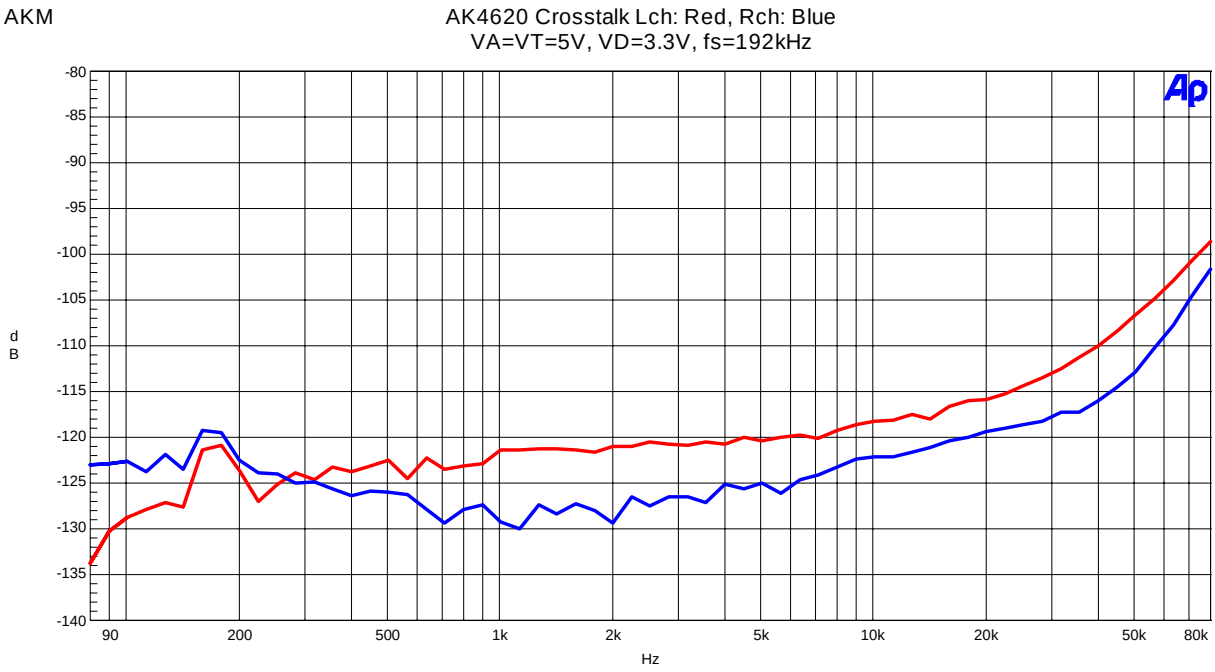
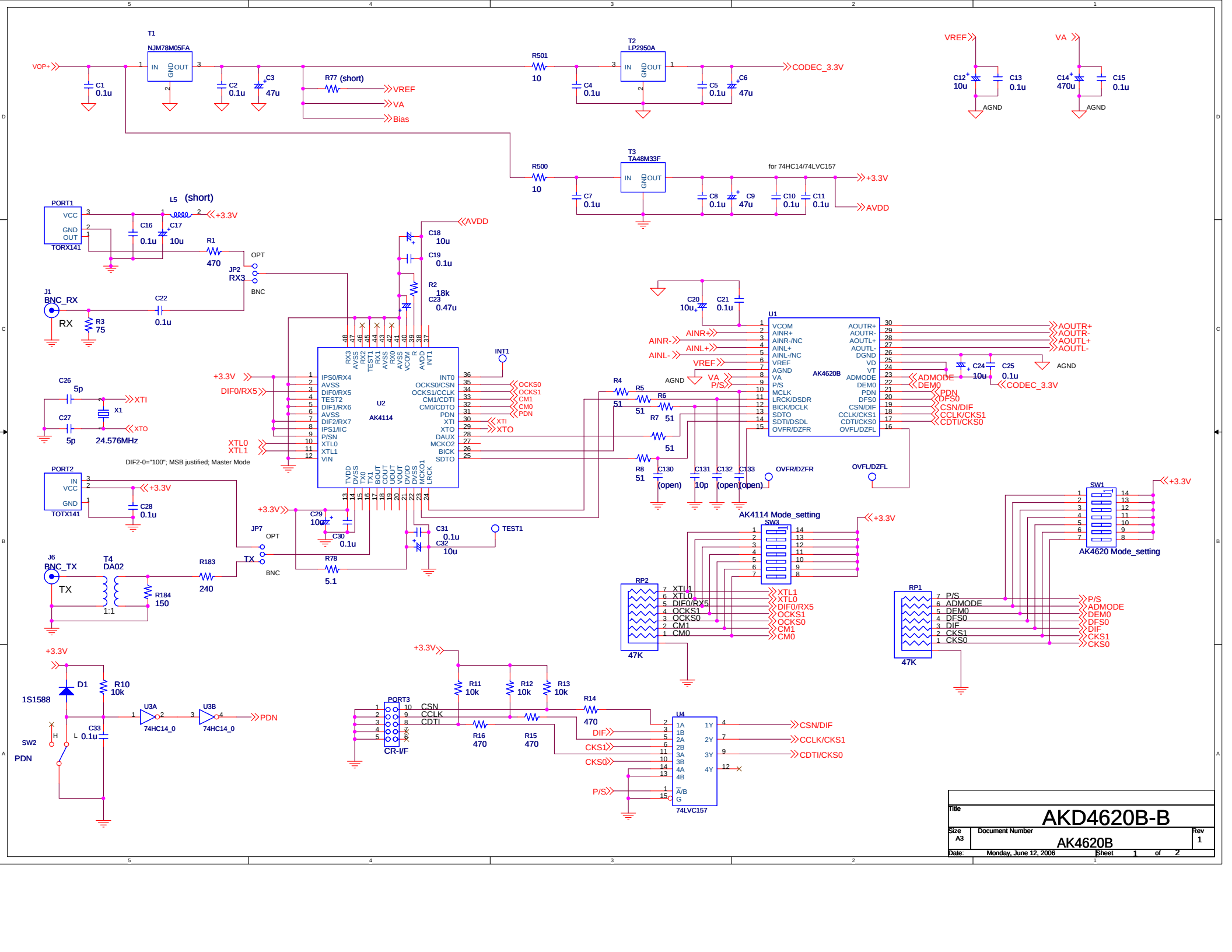
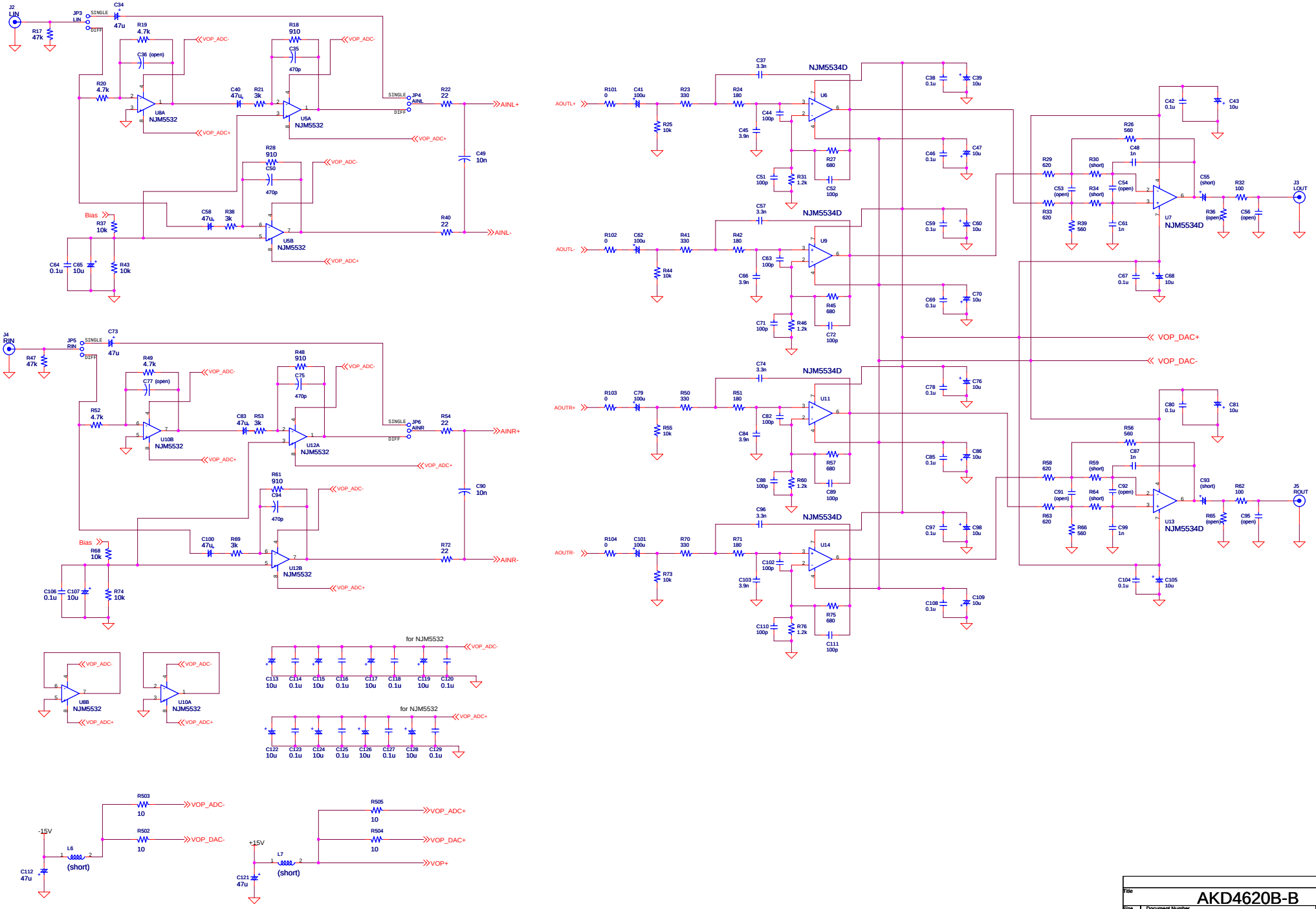


Figure 85. Crosstalk

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
05/05/26	KM078900	0	First Edition	
06/06/12	KM078901	1	Change control software	Control software was updated: 1.0 → 2.0 Control software manual was changed: P12-14 → P12-19
			Error Correct	Circuit diagram was changed. • U1: AK4620A →AK4620B • Document Number: AK4620A →AK4620B • Circuit diagram name: AKD4620A-B → AKD4620B-B


T1
NJM78M05FA
VOP+
C1 0.1u
C2 0.1u
C3 47u
R77 (short)
VREF
VA
Bias
R501 10
T2
LP2950A
C4 0.1u
C5 0.1u
C6 47u
CODEC_3.3V
VREF
VA
C12 10u
C13 0.1u
C14 470u
C15 0.1u
AGND
R500 10
T3
TA48M33F
C7 0.1u
C8 0.1u
C9 47u
C10 0.1u
C11 0.1u
for 74HC14/74LVC157
+3.3V
AVDD
L5 (short)
PORT1
TORX141
C16 0.1u
C17 10u
R1 470
JP2
RX3
OPT
BNC
J1
BNC_RX
RX
R3 75
C22 0.1u
C18 10u
C19 0.1u
R2 18k
C23 0.47u
INT1
U2
AK4114
IPS0/RX4
AVSS
DIF0/RX5
TEST2
DIF1/RX6
AVSS
DIF2/RX7
IPS1/IIC
P/SN
XTL0
XTL1
VIN
INT0
OCKS0/CSN
OCKS1/CCLK
CM1/CDTI
CM0/CDTO
PDN
XTI
XTO
DAUX
MCKO2
BICK
SDTO
OCKS0
OCKS1
CM1
CM0
PDN
XTI
XTO
DIF0/RX5
XTL0
XTL1
C26 5p
C27 5p
X1
24.576MHz
DIF2-0="100"; MSB justified; Master Mode
PORT2
TOTX141
C28 0.1u
C29 100u
C30 0.1u
C31 0.1u
C32 10u
TEST1
JP7
OPT
TX
BNC
J6
BNC_TX
TX
T4
DA02
1:1
R183 240
R184 150
R78 5.1
C20 10u
C21 0.1u
U1
AK4620B
VCOM
AINR+
AINR-/NC
AINL+
AINL-/NC
VREF
AGND
VA
P/S
MCLK
LRCK/DSDR
BICK/DCLK
SDTO
SDTI/DSDL
OVFR/DZFR
AOUTR+
AOUTR-
AOUTL+
AOUTL-
DGND
VD
VT
ADMODE
DEM0
PDN
DFS0
CSN/DIF
CCLK/CKS1
CDTI/CKS0
OVFL/DZFL
AINR+
AINR-
AINL+
AINL-
C24 10u
C25 0.1u
ADMODE
DEM0
PDN
DFS0
CSN/DIF
CCLK/CKS1
CDTI/CKS0
R4 51
R5 51
R6 51
R7 51
R8 51
C130 (open)
C131 10p
C132 (open)
C133 (open)
OVFR/DZFR
OVFL/DZFL
AK4114 Mode_setting
SW3
RP2
47K
XTL1
XTL0
DIF0/RX5
OCKS1
OCKS0
CM1
CM0
SW1
AK4620 Mode_setting
RP1
47K
P/S
ADMODE
DEM0
DFS0
DIF
CKS1
CKS0
D1
1S1588
R10 10k
U3A
U3B
74HC14_0
C33 0.1u
SW2
PDN
R11 10k
R12 10k
R13 10k
R14 470
R16 470
R15 470
PORT3
CR-I/F
CSN
CCLK
CDTI
U4
74LVC157
DIF
CKS1
CKS0
P/S
CSN/DIF
CCLK/CKS1
CDTI/CKS0
Title
AKD4620B-B
Size A3
Document Number
AK4620B
Rev 1
Date: Monday, June 12, 2006
Sheet 1 of 2



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Size A2	Document Number Analog_I/O		Rev 1
Date: Monday, June 12, 2006	Sheet 2 of 2		