1. Overview

1.1 Features

The M16C Family offers a robust platform of 32-/16-bit CISC microcomputers (MCUs) featuring high ROM code efficiency, extensive EMI/EMS noise immunity, ultra-low power consumption, high-speed processing in actual applications, and numerous and varied integrated peripherals. Extensive device scalability from low- to high-end, featuring a single architecture as well as compatible pin assignments and peripheral functions, provides support for a vast range of application fields.

The R32C/100 Series is a high-end microcontroller series in the M16C Family. With a 4-Gbyte memory space, it achieves maximum code efficiency and high-speed processing with 32-bit CISC architecture, multiplier, multiply-accumulate unit, and floating point unit. The selection from the broadest choice of on-chip peripheral devices — UART, CRC, DMAC, A/D and D/A converters, timers, I^2C, and WDT enables to minimize external components.

The R32C/100 Series, in particular, provides the R32C/111 Group as a standard product. This product, provided as 100-pin plastic molded LGA, and 100-/80-/64-pin plastic molded LQFP package, configures a maximum of nine channels of serial interface.

1.1.1 Applications

Audio, cameras, television, home appliance, printer, meter, office/industrial equipment, communication/ portable devices

1.1.2 Performance Overview

Table 1.1 to Table 1.6 show the performance overview of the R32C/111 Group.

Table 1.1 R32C/111 Group Performance for the 100-pin Package (1/2)

Unit	Function	Performance
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 20 ns (f(CPU) = 50 MHz) • Multiplier: 32-bit × 32-bit → 64-bit • Multiply-accumulate unit: 32-bit × 32-bit + 64-bit → 64-bit • IEEE-754 floating point standard: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional (1))
Memory		Flash memory: 256 to 512 Kbytes RAM: 32 to 63 Kbytes Data flash: 4 Kbytes × 2 blocks Refer to Table 1.7 for memory size of each product group
Voltage Detector	Low voltage detector	Optional (1) Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/re-oscillation detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
External Bus Expansion	Bus and memory expansion	• Address space: 4 Gbytes (of which up to 64 Mbytes is user accessible) • External bus Interface: Support for wait-state insertion, 4 chip select outputs, 3V/5V interface • Bus format: Separate bus/Multiplexed bus selectable, data bus width selectable (8/16 bits)
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4 Interrupt priority levels: 7 levels
Watchdog Timer		15 bits × 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 51 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Can be activated by any peripheral interrupt source • 3 transfer functions: Immediate data transfer, calculation transfer, chained transfer
I/O Ports	Programmable I/O ports	• 2 input-only ports • 82 CMOS inputs/outputs • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:
1. Please contact a Renesas sales office to use the optional feature.

Table 1.2 R32C/111 Group Performance for the 100-pin Package (2/2)

Unit	Function	Performance
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer ×1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART8	Asynchronous/synchronous serial interface × 9 channels • I^2C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (1) (optional (2)) (UART0 to UART6)
A/D Converter		10-bit resolution × 26 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 19 Serial interface: Variable-length synchronous serial I/O mode, IEBus (1) mode (optional (2))
Flash Memory		Programming and erasure supply voltage: VCC1 = VCC2 = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		50 MHz/VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Operating Temperature		-20°C to 85°C (version N) -40°C to 85°C (version D)
Current Consumption		32 mA (VCC1 = VCC2 = 5.0 V, f(CPU) = 50 MHz) 8 µA (VCC1 = VCC2 = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		100-pin plastic molded LQFP (PLQP0100KB-A) 100-pin plastic molded TFLGA (PTLG0100KA-A)

Notes:
1. IEBus is a trademark of NEC Electronics Corporation.
2. Please contact a Renesas sales office to use the optional feature.

Table 1.3 R32C/111 Group Performance for the 80-pin Package (1/2)

Unit	Function	Performance
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 20 ns (f(CPU) = 50 MHz) • Multiplier: 32-bit × 32-bit → 64-bit • Multiply-accumulate unit: 32-bit × 32-bit + 64-bit → 64-bit • IEEE-754 floating point standard: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional (1))
Memory		Flash memory: 128/256 Kbytes RAM: 32 Kbytes Data flash: 4 Kbytes × 2 blocks Refer to Table 1.7 for memory size of each product group
Voltage Detector	Low voltage detector	Optional (1) Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/re-oscillation detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4 Interrupt priority levels: 7 levels
Watchdog Timer		15 bits × 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 47 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Can be activated by any peripheral interrupt source • 3 transfer functions: Immediate data transfer, calculation transfer, chained transfer
I/O Ports	Programmable I/O ports	• 1 input-only port • 65 CMOS inputs/outputs • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:
1. Please contact a Renesas sales office to use the optional feature.

Table 1.4 R32C/111 Group Performance for the 80-pin Package (2/2)

Unit	Function	Performance
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 (1) Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer ×1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART5, UART8	Asynchronous/synchronous serial interface × 7 channels • I^2C-bus (UART0 to UART5) • Special mode 2 (UART0 to UART3, UART5) • IEBus (2) (optional (3)) (UART0 to UART5)
A/D Converter		10-bit resolution × 26 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 1
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 19 Serial interface: Variable-length synchronous serial I/O mode, IEBus (2) mode (optional (3))
Flash Memory		Programming and erasure supply voltage: VCC1 = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		50 MHz/VCC1 = 3.0 to 5.5 V
Operating Temperature		-20°C to 85°C (version N) -40°C to 85°C (version D)
Current Consumption		32 mA (VCC1 = 5.0 V, f(CPU) = 50 MHz) 8 µA (VCC1 = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		80-pin plastic molded LQFP (PLQP0080KB-A)

Notes:
1. Timer B4 is available in timer mode only.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Please contact a Renesas sales office to use the optional feature.

Table 1.5 R32C/111 Group Performance for the 64-pin Package (1/2)

Unit	Function	Performance
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 20 ns (f(CPU) = 50 MHz) • Multiplier: 32-bit × 32-bit → 64-bit • Multiply-accumulate unit: 32-bit × 32-bit + 64-bit → 64-bit • IEEE-754 floating point standard: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional (1))
Memory		Flash memory: 128/256 Kbytes RAM: 32 Kbytes Data flash: 4 Kbytes × 2 blocks Refer to Table 1.7 for memory size of each product group
Voltage Detector	Low voltage detector	Optional (1) Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/re-oscillation detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4 Interrupt priority levels: 7 levels
Watchdog Timer		15 bits × 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 45 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Can be activated by any peripheral interrupt source • 3 transfer functions: Immediate data transfer, calculation transfer, chained transfer
I/O Ports	Programmable I/O ports	• 1 input-only port • 49 CMOS inputs/outputs • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:
1. Please contact a Renesas sales office to use the optional feature.

Table 1.6 R32C/111 Group Performance for the 64-pin Package (2/2)

Unit	Function	Performance
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 (1) Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer ×1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART3, UART5, UART8	Asynchronous/synchronous serial interface × 6 channels • I^2C-bus (UART0 to UART3, UART5) • Special mode 2 (UART0 to UART3, UART5) • IEBus (2) (optional (3)) (UART0 to UART3, UART5)
A/D Converter		10-bit resolution × 20 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 1
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 19 Serial interface: Variable-length synchronous serial I/O mode, IEBus (2) mode (optional (3))
Flash Memory		Programming and erasure supply voltage: VCC1 = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		50 MHz/VCC1 = 3.0 to 5.5 V
Operating Temperature		-20°C to 85°C (version N) -40°C to 85°C (version D)
Current Consumption		32 mA (VCC1 = 5.0 V, f(CPU) = 50 MHz) 8 µA (VCC1 = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		64-pin plastic molded LQFP (PLQP0080KB-A)

Notes:
1. Timer B4 is available in timer mode only.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Please contact a Renesas sales office to use the optional feature.

1.2 Product Information

Table 1.7 lists the product information and Figure 1.1 shows the details of the part number.

Table 1.7 R32C/111 Group Product List **As of September, 2009**

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F64110NFB (P)	PLQP0100KB-A	256 Kbytes +8 Kbyts	63 Kbytes	-20°C to 85°C (version N)
R5F64110DFB				-40°C to 85°C (version D)
R5F64111NFB (P)		384 Kbytes +8 Kbytes		-20°C to 85°C (version N)
R5F64111DFB				-40°C to 85°C (version D)
R5F64112NFB (P)		512 Kbytes +8 Kbytes		-20°C to 85°C (version N)
R5F64112DFB				-40°C to 85°C (version D)
R5F64114NFB (P)		256 Kbytes +8 Kbytes	40 Kbytes	-20°C to 85°C (version N)
R5F64114DFB				-40°C to 85°C (version D)
R5F64115NFB (P)		384 Kbytes +8 Kbytes		-20°C to 85°C (version N)
R5F64115DFB				-40°C to 85°C (version D)
R5F64116NFB (P)		512 Kbytes +8 Kbytes		-20°C to 85°C (version N)
R5F64116DFB				-40°C to 85°C (version D)
R5F64111NLG	PTLG0100KA-A	384 Kbytes +8 Kbytes	63 Kbytes	-20°C to 85°C (version N)
R5F64111DLG (P)				-40°C to 85°C (version D)
R5F64112NLG		512 Kbytes +8 Kbytes		-20°C to 85°C (version N)
R5F64112DLG (P)				-40°C to 85°C (version D)
R5F6411FNLG		256 Kbytes +8 Kbytes	32 Kbytes	-20°C to 85°C (version N)
R5F6411FDLG (P)				-40°C to 85°C (version D)
R5F6411ENFP (P)	PLQP080KB-A	128 Kbytes +8 Kbyts	32 Kbytes	-20°C to 85°C (version N)
R5F6411EDFP (P)				-40°C to 85°C (version D)
R5F6411FNFP (P)		256 Kbytes +8 Kbyts		-20°C to 85°C (version N)
R5F6411FDFP (P)				-40°C to 85°C (version D)
R5F6411ENFN (P)	PLQP064KB-A	128 Kbytes +8 Kbyts	32 Kbytes	-20°C to 85°C (version N)
R5F6411EDFN (D)				-40°C to 85°C (version D)
R5F6411FNFN (P)		256 Kbytes +8 Kbyts		-20°C to 85°C (version N)
R5F6411FDFN				-40°C to 85°C (version D)

(D): Under development (P): On planning phase

Notes:

1. The old package codes are as follows:
   PLQP0100KB-A: 100P6Q-A
   PTLG0100KA-A: 100F0M
   PLQP0080KB-A: 80P6Q-A
   PLQP0064KB-A: 64P6Q-A
2. Data flash memory provides an additional 8 Kbytes of ROM capacity.

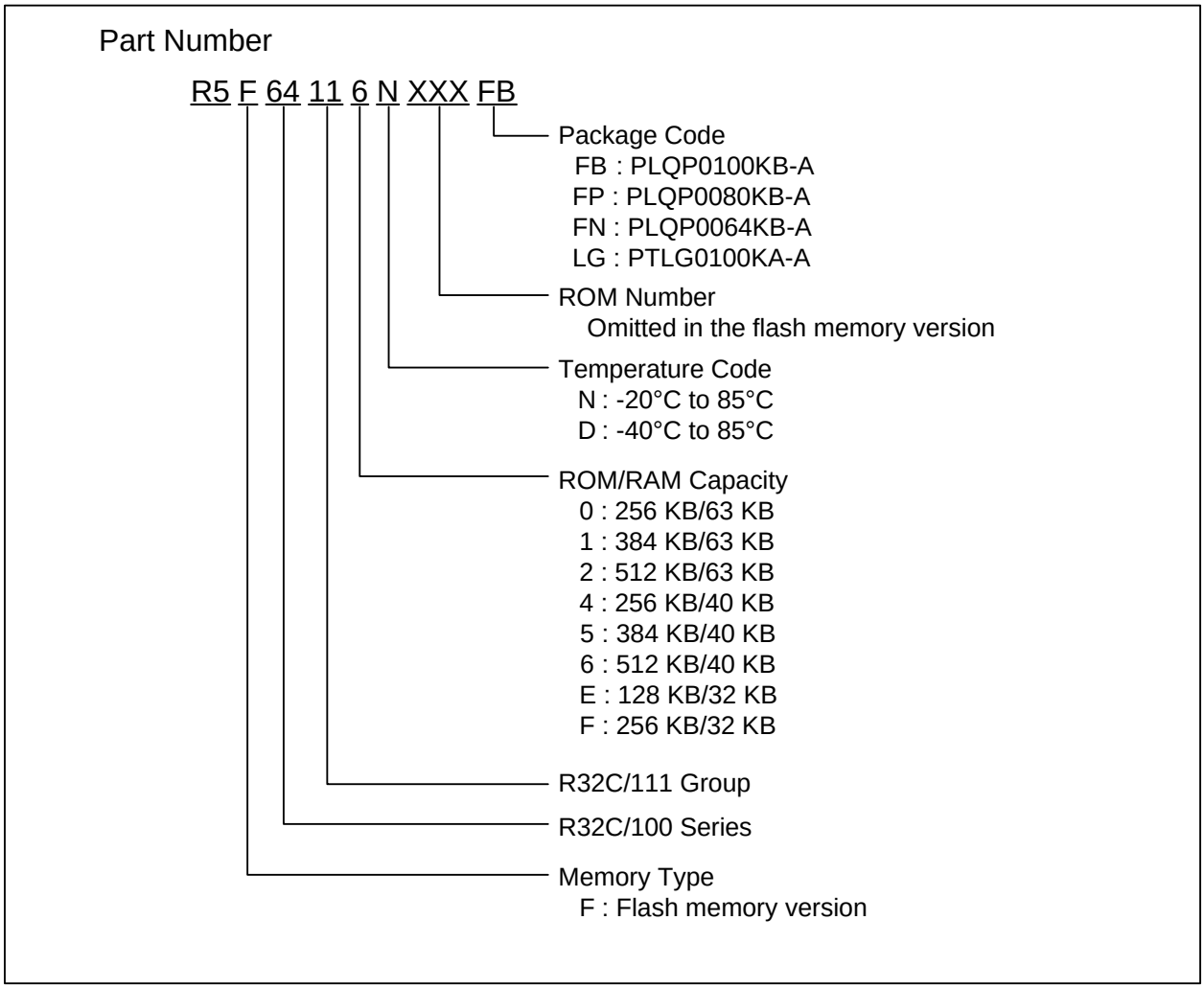
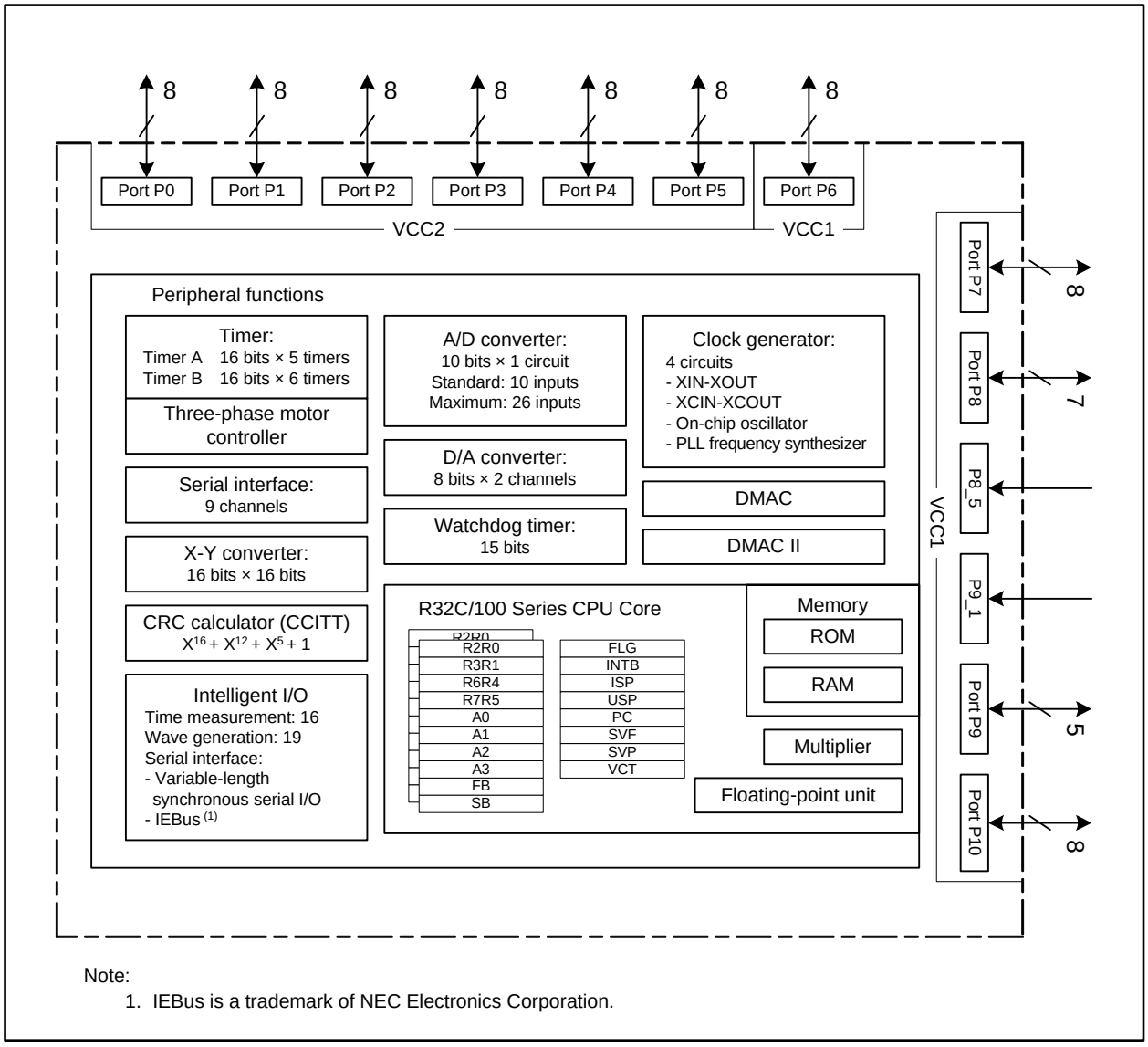


Figure 1.1 Part Numbering of Product

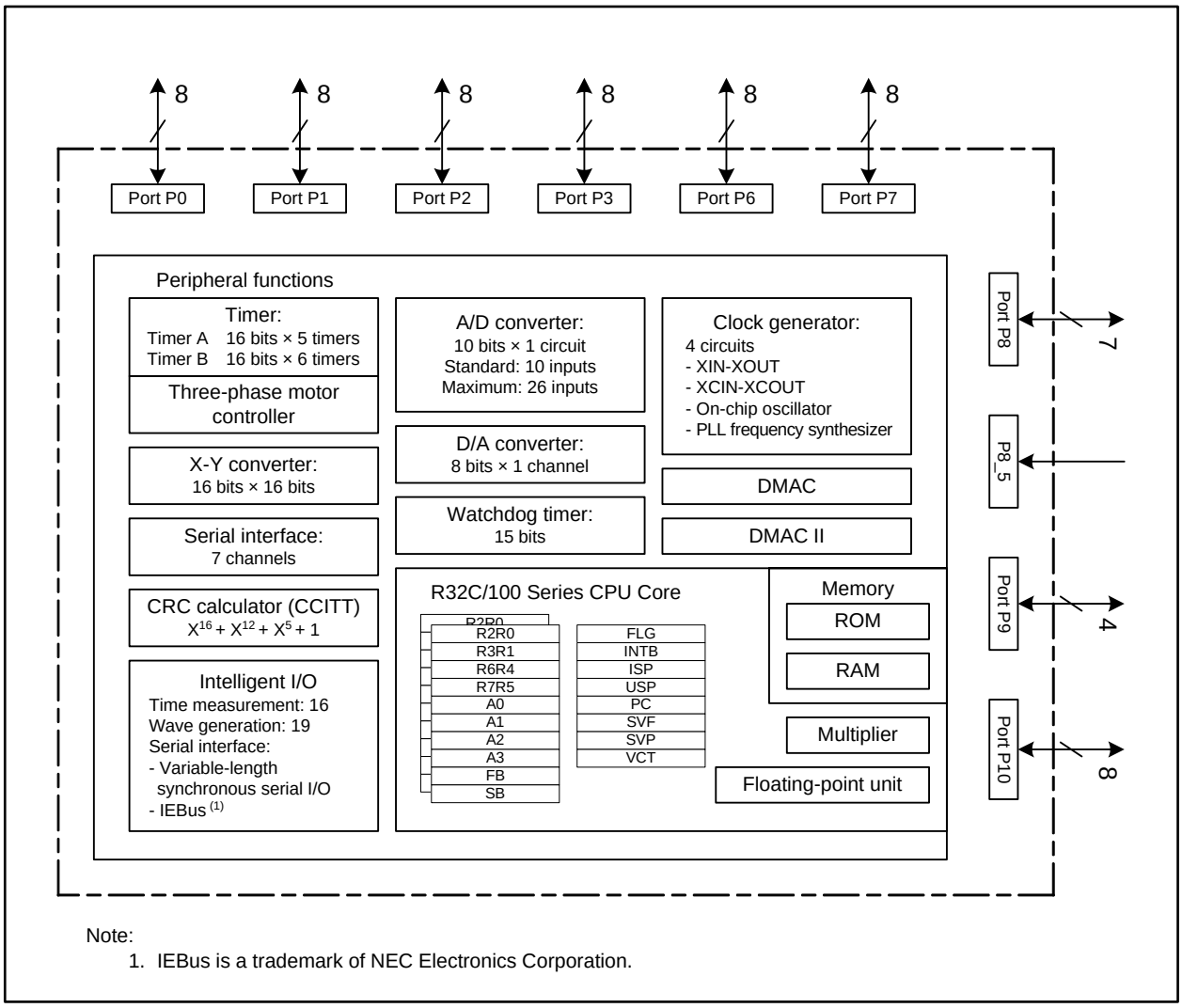
1.3 Block Diagram

Figure 1.2 to Figure 1.4 show block diagram of the R32C/111 Group.



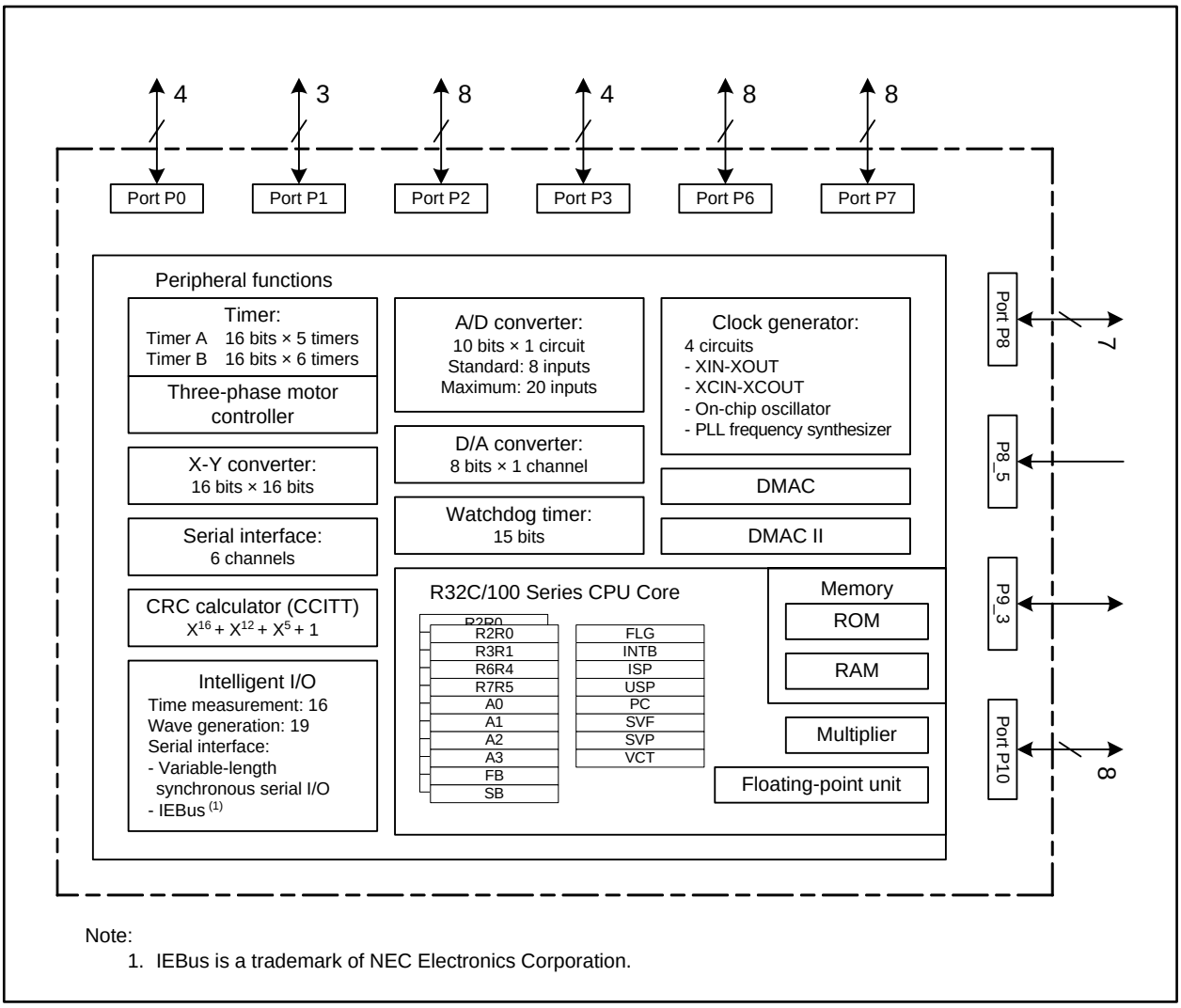
Note:
1. IEBus is a trademark of NEC Electronics Corporation.

Figure 1.2 R32C/111 Group Block Diagram for the 100-pin Package



Note:
1. IEBus is a trademark of NEC Electronics Corporation.

Figure 1.3 R32C/111 Group Block Diagram for the 80-pin Package

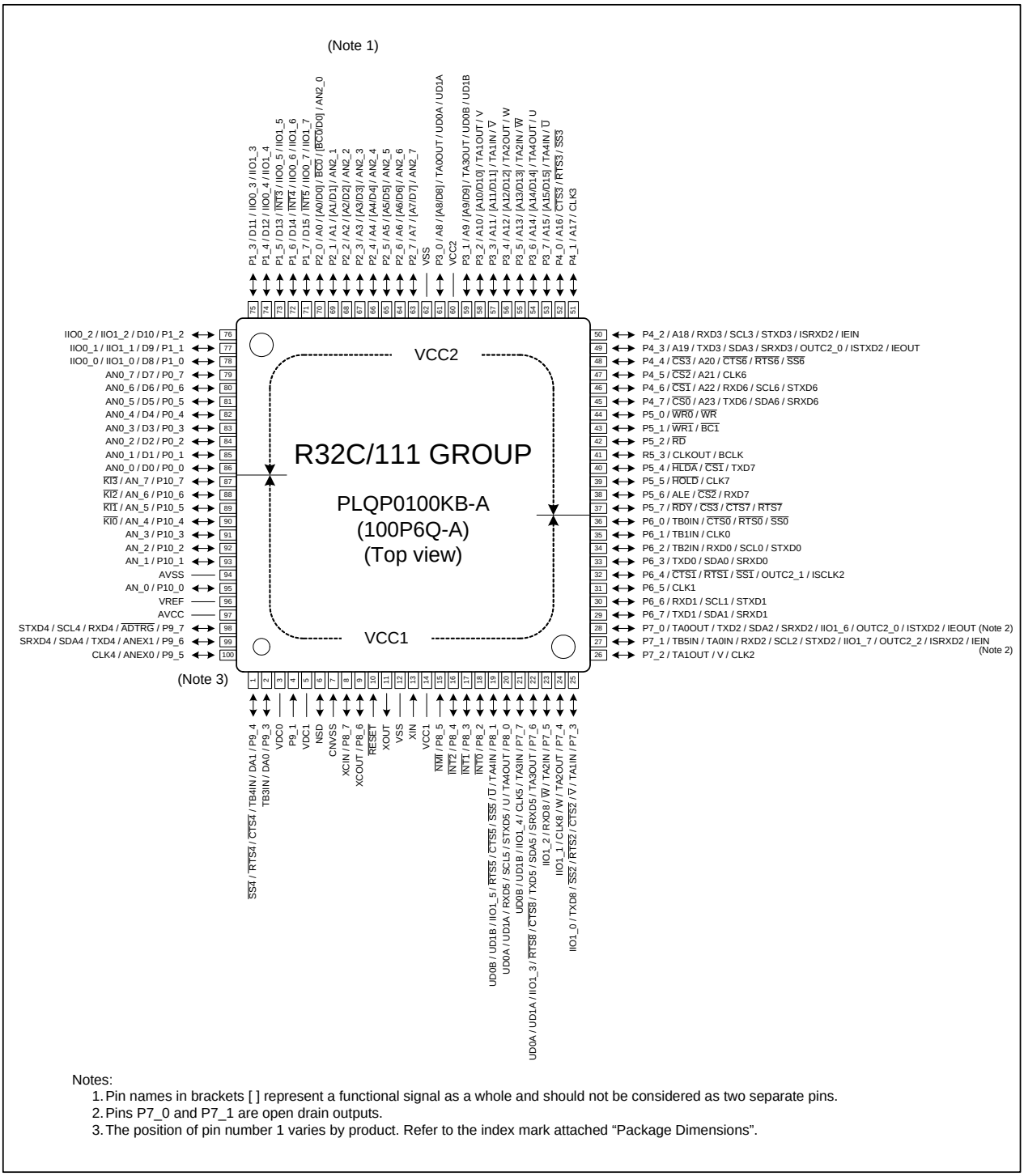


Note:
1. IEBus is a trademark of NEC Electronics Corporation.

Figure 1.4 R32C/111 Group Block Diagram for the 64-pin Package

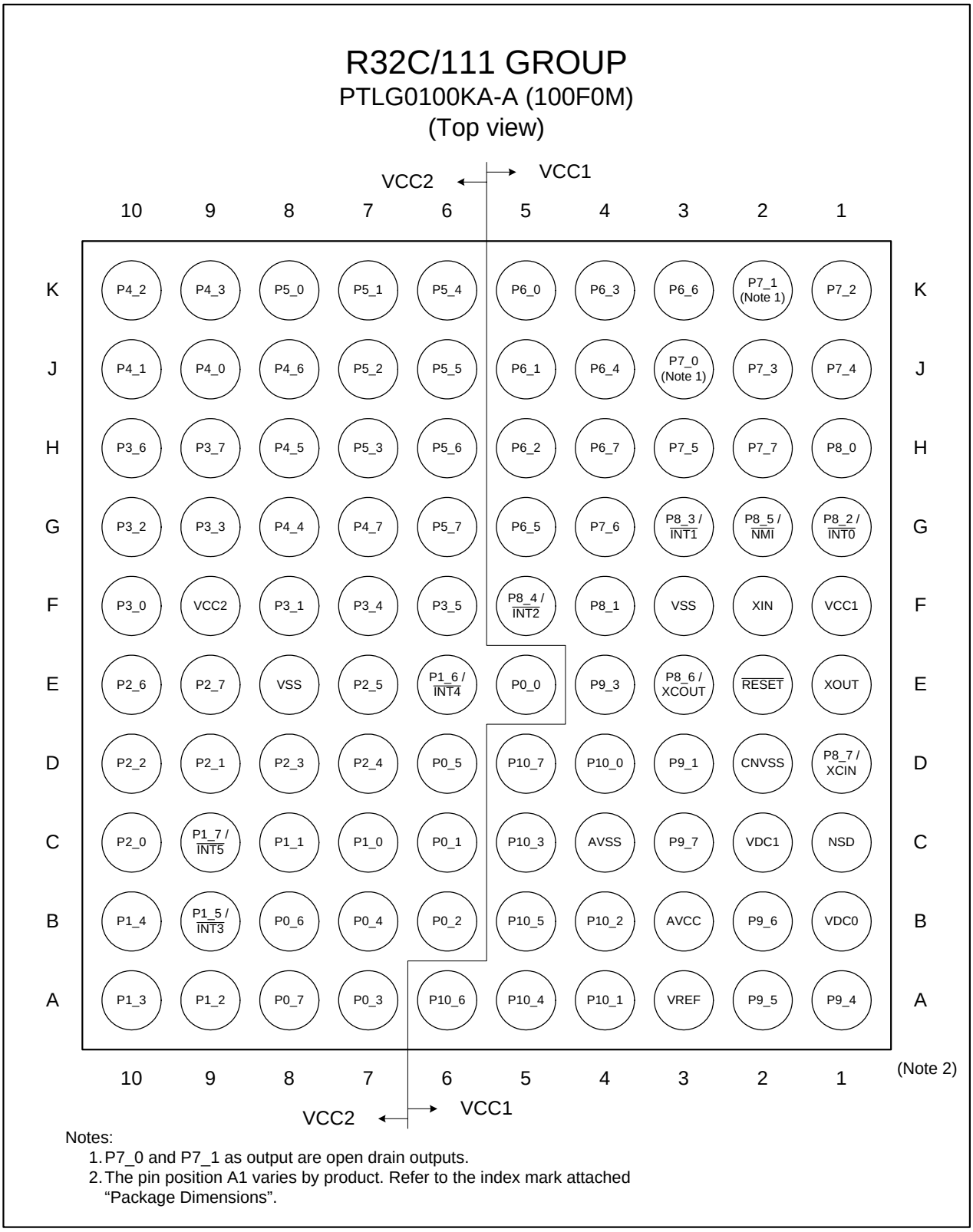
1.4 Pin Assignments

Figure 1.5 to Figure 1.8 show the pin assignments (top view) and Table 1.8 to Table 1.14 show the pin characteristics.



Notes:
1. Pin names in brackets [ ] represent a functional signal as a whole and should not be considered as two separate pins.
2. Pins P7_0 and P7_1 are open drain outputs.
3. The position of pin number 1 varies by product. Refer to the index mark attached “Package Dimensions”.

Figure 1.5 Pin Assignment for the 100-pin Package (top view)



Notes:
1. P7_0 and P7_1 as output are open drain outputs.
2. The pin position A1 varies by product. Refer to the index mark attached "Package Dimensions".

Figure 1.6 Pin Assignment for the 100-pin LGA Package (top view)

Table 1.8 Pin Characteristics for the 100-pin Package (1/3)

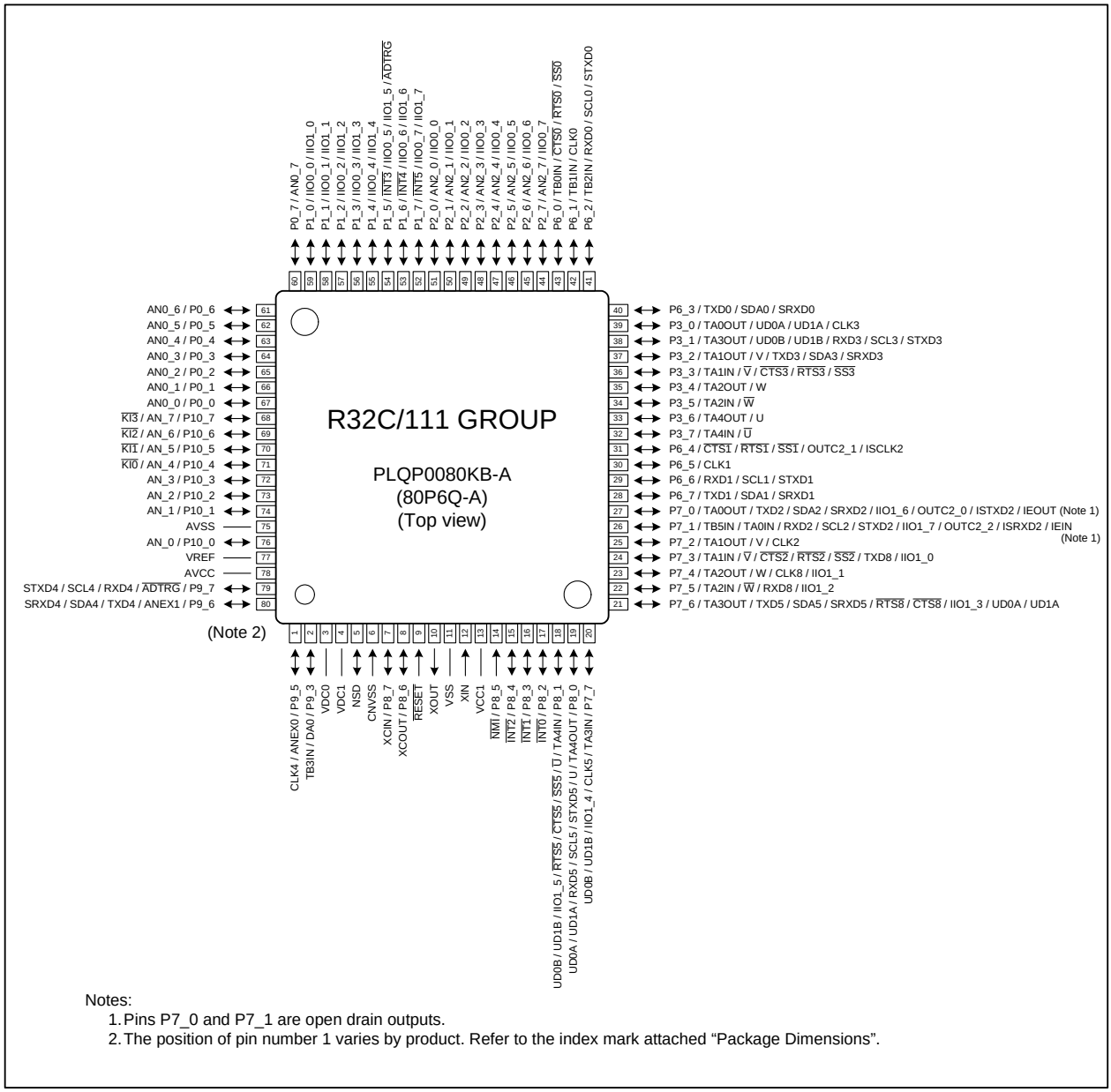
Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
1	A1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
2	E4		P9_3		TB3IN			DA0	
3	B1	VDC0							
4	D3		P9_1						
5	C2	VDC1							
6	C1	NSD							
7	D2	CNVSS							
8	D1	XCIN	P8_7						
9	E3	XCOUT	P8_6						
10	E2	RESET							
11	E1	XOUT							
12	F3	VSS							
13	F2	XIN							
14	F1	VCC1							
15	G2		P8_5	NMI					
16	F5		P8_4	INT2					
17	G3		P8_3	INT1					
18	G1		P8_2	INT0					
19	F4		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
20	H1		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
21	H2		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B		
22	G4		P7_6		TA3OUT	TXD5/SDA5/ SRXD5/CTS8/RTS8	IIO1_3/UD0A/UD1A		
23	H3		P7_5		TA2IN/W	RXD8	IIO1_2		
24	J1		P7_4		TA2OUT/W	CLK8	IIO1_1		
25	J2		P7_3		TA1IN/V	CTS2/RTS2/SS2/ TXD8	IIO1_0		
26	K1		P7_2		TA1OUT/V	CLK2			
27	K2		P7_1		TB5IN/ TA0IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN		
28	J3		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
29	H4		P6_7			TXD1/SDA1/SRXD1			
30	K3		P6_6			RXD1/SCL1/STXD1			
31	G5		P6_5			CLK1			
32	J4		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
33	K4		P6_3			TXD0/SDA0/SRXD0			
34	H5		P6_2		TB2IN	RXD0/SCL0/STXD0			
35	J5		P6_1		TB1IN	CLK0			
36	K5		P6_0		TB0IN	CTS0/RTS0/SS0			
37	G6		P5_7			CTS7/RTS7			RDY/CS3
38	H6		P5_6			RXD7			ALE/CS2
39	J6		P5_5			CLK7			HOLD

Table 1.9 Pin Characteristics for the 100-pin Package (2/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
40	K6		P5_4			TXD7			HLDA/CS1
41	H7		P5_3						CLKOUT/ BCLK
42	J7		P5_2						RD
43	K7		P5_1						WR1/BC1
44	K8		P5_0						WR0/WR
45	G7		P4_7			TXD6/SDA6/SRXD6			CS0/A23
46	J8		P4_6			RXD6/SCL6/STXD6			CS1/A22
47	H8		P4_5			CLK6			CS2/A21
48	G8		P4_4			CTS6/RTS6/SS6			CS3/A20
49	K9		P4_3			TXD3/SDA3/SRXD3	OUTC2_0/ISTXD2/ IEOUT		A19
50	K10		P4_2			RXD3/SCL3/STXD3	ISRXD2/IEIN		A18
51	J10		P4_1			CLK3			A17
52	J9		P4_0			CTS3/RTS3/SS3			A16
53	H9		P3_7		TA4IN/U				A15(/D15)
54	H10		P3_6		TA4OUT/U				A14(/D14)
55	F6		P3_5		TA2IN/W				A13(/D13)
56	F7		P3_4		TA2OUT/W				A12(/D12)
57	G9		P3_3		TA1IN/V				A11(/D11)
58	G10		P3_2		TA1OUT/V				A10(/D10)
59	F8		P3_1		TA3OUT		UD0B/UD1B		A9(/D9)
60	F9	VCC2							
61	F10		P3_0		TA0OUT		UD0A/UD1A		A8(/D8)
62	E8	VSS							
63	E9		P2_7					AN2_7	A7(/D7)
64	E10		P2_6					AN2_6	A6(/D6)
65	E7		P2_5					AN2_5	A5(/D5)
66	D7		P2_4					AN2_4	A4(/D4)
67	D8		P2_3					AN2_3	A3(/D3)
68	D10		P2_2					AN2_2	A2(/D2)
69	D9		P2_1					AN2_1	A1(/D1)
70	C10		P2_0					AN2_0	A0(/D0)/ BC0(/D0)
71	C9		P1_7	INT5			IIO0_7/IIO1_7		D15
72	E6		P1_6	INT4			IIO0_6/IIO1_6		D14
73	B9		P1_5	INT3			IIO0_5/IIO1_5		D13
74	B10		P1_4				IIO0_4/IIO1_4		D12
75	A10		P1_3				IIO0_3/IIO1_3		D11
76	A9		P1_2				IIO0_2/IIO1_2		D10
77	C8		P1_1				IIO0_1/IIO1_1		D9
78	C7		P1_0				IIO0_0/IIO1_0		D8
79	A8		P0_7					AN0_7	D7

Table 1.10 Pin Characteristics for the 100-pin Package (3/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
80	B8		P0_6					AN0_6	D6
81	D6		P0_5					AN0_5	D5
82	B7		P0_4					AN0_4	D4
83	A7		P0_3					AN0_3	D3
84	B6		P0_2					AN0_2	D2
85	C6		P0_1					AN0_1	D1
86	E5		P0_0					AN0_0	D0
87	D5		P10_7	$\overline{KI3}$				AN_7	
88	A6		P10_6	$\overline{KI2}$				AN_6	
89	B5		P10_5	$\overline{KI1}$				AN_5	
90	A5		P10_4	$\overline{KI0}$				AN_4	
91	C5		P10_3					AN_3	
92	B4		P10_2					AN_2	
93	A4		P10_1					AN_1	
94	C4	AVSS							
95	D4		P10_0					AN_0	
96	A3	VREF							
97	B3	AVCC							
98	C3		P9_7			RXD4/SCL4/STXD4		$\overline{ADTRG}$	
99	B2		P9_6			TXD4/SDA4/SRXD4		ANEX1	
100	A2		P9_5			CLK4		ANEX0	



Notes:
1. Pins P7_0 and P7_1 are open drain outputs.
2. The position of pin number 1 varies by product. Refer to the index mark attached “Package Dimensions”.

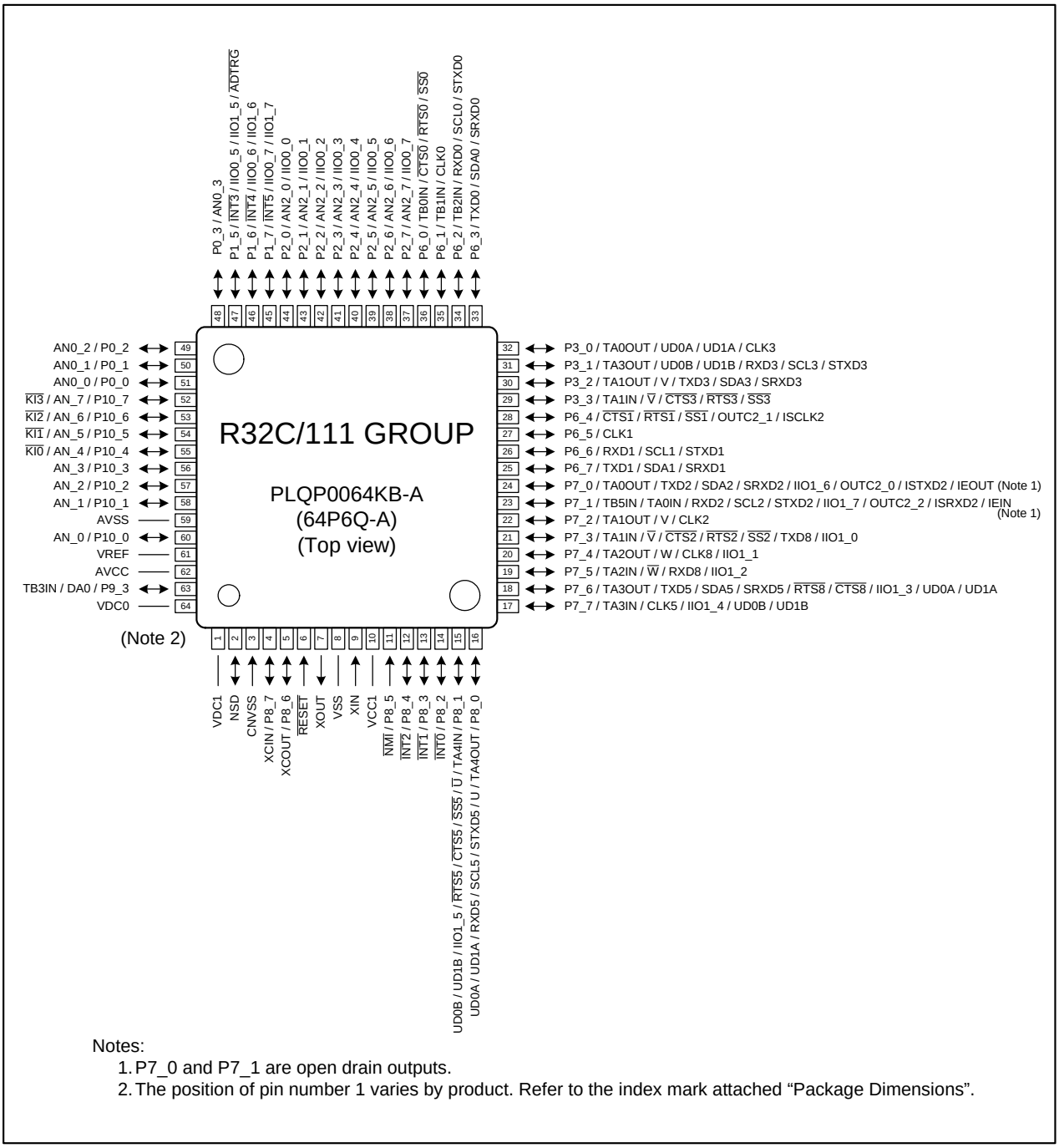
Figure 1.7 Pin Assignment for the 80-pin Package (top view)

Table 1.11 Pin Characteristics for the 80-pin Package (1/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin
1		P9_5			CLK4		ANEX0
2		P9_3		TB3IN			DA0
3	VDC0						
4	VDC1						
5	NSD						
6	CNVSS						
7	XCIN	P8_7					
8	XCOUT	P8_6					
9	$\overline{\text{RESET}}$						
10	XOUT						
11	VSS						
12	XIN						
13	VCC1						
14		P8_5	$\overline{\text{NMI}}$				
15		P8_4	$\overline{\text{INT2}}$				
16		P8_3	$\overline{\text{INT1}}$				
17		P8_2	$\overline{\text{INT0}}$				
18		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$	IIO1_5/UD0B/UD1B	
19		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A	
20		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B	
21		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ $\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$	IIO1_3/UD0A/UD1A	
22		P7_5		TA2IN/$\overline{\text{W}}$	RXD8	IIO1_2	
23		P7_4		TA2OUT/W	CLK8	IIO1_1	
24		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/TXD8	IIO1_0	
25		P7_2		TA1OUT/V	CLK2		
26		P7_1		TB5IN/TA0IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN	
27		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT	
28		P6_7			TXD1/SDA1/SRXD1		
29		P6_6			RXD1/SCL1/STXD1		
30		P6_5			CLK1		
31		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	OUTC2_1/ISCLK2	
32		P3_7		TA4IN/$\overline{\text{U}}$			
33		P3_6		TA4OUT/U			
34		P3_5		TA2IN/$\overline{\text{W}}$			
35		P3_4		TA2OUT/W			
36		P3_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$		
37		P3_2		TA1OUT/V	TXD3/SDA3/SRXD3		
38		P3_1		TA3OUT	RXD3/SCL3/STXD3	UD0B/UD1B	
39		P3_0		TA0OUT	CLK3	UD0A/UD1A	
40		P6_3			TXD0/SDA0/SRXD0		

Table 1.12 Pin Characteristics for the 80-pin Package (2/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin
41		P6_2		TB2IN	RXD0/SCL0/STXD0		
42		P6_1		TB1IN	CLK0		
43		P6_0		TB0IN	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$		
44		P2_7				IIO0_7	AN2_7
45		P2_6				IIO0_6	AN2_6
46		P2_5				IIO0_5	AN2_5
47		P2_4				IIO0_4	AN2_4
48		P2_3				IIO0_3	AN2_3
49		P2_2				IIO0_2	AN2_2
50		P2_1				IIO0_1	AN2_1
51		P2_0				IIO0_0	AN2_0
52		P1_7	$\overline{\text{INT5}}$			IIO0_7/IIO1_7	
53		P1_6	$\overline{\text{INT4}}$			IIO0_6/IIO1_6	
54		P1_5	$\overline{\text{INT3}}$			IIO0_5/IIO1_5	$\overline{\text{ADTRG}}$
55		P1_4				IIO0_4/IIO1_4	
56		P1_3				IIO0_3/IIO1_3	
57		P1_2				IIO0_2/IIO1_2	
58		P1_1				IIO0_1/IIO1_1	
59		P1_0				IIO0_0/IIO1_0	
60		P0_7					AN0_7
61		P0_6					AN0_6
62		P0_5					AN0_5
63		P0_4					AN0_4
64		P0_3					AN0_3
65		P0_2					AN0_2
66		P0_1					AN0_1
67		P0_0					AN0_0
68		P10_7	$\overline{\text{KI3}}$				AN_7
69		P10_6	$\overline{\text{KI2}}$				AN_6
70		P10_5	$\overline{\text{KI1}}$				AN_5
71		P10_4	$\overline{\text{KI0}}$				AN_4
72		P10_3					AN_3
73		P10_2					AN_2
74		P10_1					AN_1
75	AVSS						
76		P10_0					AN_0
77	VREF						
78	AVCC						
79		P9_7			RXD4/SCL4/STXD4		$\overline{\text{ADTRG}}$
80		P9_6			TXD4/SDA4/SRXD4		ANEX1



Notes:
1. P7_0 and P7_1 are open drain outputs.
2. The position of pin number 1 varies by product. Refer to the index mark attached “Package Dimensions”.

Figure 1.8 Pin Assignment for the 64-pin Package (top view)

Table 1.13 Pin Characteristics for the 64-pin Package (1/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin
1	VDC1						
2	NSD						
3	CNVSS						
4	XCIN	P8_7					
5	XCOUT	P8_6					
6	$\overline{\text{RESET}}$						
7	XOUT						
8	VSS						
9	XIN						
10	VCC1						
11		P8_5	$\overline{\text{NMI}}$				
12		P8_4	$\overline{\text{INT2}}$				
13		P8_3	$\overline{\text{INT1}}$				
14		P8_2	$\overline{\text{INT0}}$				
15		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$	IIO1_5/UD0B/UD1B	
16		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A	
17		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B	
18		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ $\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$	IIO1_3/UD0A/UD1A	
19		P7_5		TA2IN/$\overline{\text{W}}$	RXD8	IIO1_2	
20		P7_4		TA2OUT/W	CLK8	IIO1_1	
21		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/TXD8	IIO1_0	
22		P7_2		TA1OUT/V	CLK2		
23		P7_1		TB5IN/ TA0IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN	
24		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT	
25		P6_7			TXD1/SDA1/SRXD1		
26		P6_6			RXD1/SCL1/STXD1		
27		P6_5			CLK1		
28		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	OUTC2_1/ISCLK2	
29		P3_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$		
30		P3_2		TA1OUT/V	TXD3/SDA3/SRXD3		
31		P3_1		TA3OUT	RXD3/SCL3/STXD3	UD0B/UD1B	
32		P3_0		TA0OUT	CLK3	UD0A/UD1A	
33		P6_3			TXD0/SDA0/SRXD0		
34		P6_2		TB2IN	RXD0/SCL0/STXD0		
35		P6_1		TB1IN	CLK0		
36		P6_0		TB0IN	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$		
37		P2_7				IIO0_7	AN2_7
38		P2_6				IIO0_6	AN2_6
39		P2_5				IIO0_5	AN2_5
40		P2_4				IIO0_4	AN2_4

Table 1.14 Pin Characteristics for the 64-pin Package (2/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin
41		P2_3				IIO0_3	AN2_3
42		P2_2				IIO0_2	AN2_2
43		P2_1				IIO0_1	AN2_1
44		P2_0				IIO0_0	AN2_0
45		P1_7	$\overline{INT5}$			IIO0_7/IIO1_7	
46		P1_6	$\overline{INT4}$			IIO0_6/IIO1_6	
47		P1_5	$\overline{INT3}$			IIO0_5/IIO1_5	$\overline{ADTRG}$
48		P0_3					AN0_3
49		P0_2					AN0_2
50		P0_1					AN0_1
51		P0_0					AN0_0
52		P10_7	$\overline{KI3}$				AN_7
53		P10_6	$\overline{KI2}$				AN_6
54		P10_5	$\overline{KI1}$				AN_5
55		P10_4	$\overline{KI0}$				AN_4
56		P10_3					AN_3
57		P10_2					AN_2
58		P10_1					AN_1
59	AVSS						
60		P10_0					AN_0
61	VREF						
62	AVCC						
63		P9_3		TB3IN			DA0
64	VDC0						

1.5 Pin Definitions and Functions

Table 1.15 to Table 1.21 show the pin definitions and functions.

Table 1.15 Pin Definitions and Functions for the 100-pin Package (1/4)

Function	Symbol	I/O	Power Supply	Description
Power supply	VCC1, VCC2, VSS	I	—	Applicable as follows: VCC1 and VCC2 = 3.0 to 5.5 V (VCC1 ≥ VCC2), VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	VCC1	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC1 and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	VCC1	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	VCC1	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	VCC1	This pin is to communicate with a debugger. It should be connected to VCC1 via a resistor of 1 to 4.7 kΩ
Main clock input	XIN	I	VCC1	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOUT. An external clock should be input at the XCIN while leaving the XCOUT open
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	BCLK output
Clock output	CLKOUT	O	VCC2	Output of the clock with the same frequency as fC, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	VCC1 VCC2	Input for external interrupts
NMI input	P8_5/$\overline{\text{NMI}}$	I	VCC1	Input for NMI
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	VCC2	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	VCC2	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A23	O	VCC2	Output of address bits A0 to A23

Table 1.16 Pin Definitions and Functions for the 100-pin Package (2/4)

Function	Symbol	I/O	Power Supply	Description
Bus control pins	A0/D0 to A7/D7	I/O	VCC2	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit multiplexed bus
	$\overline{BC0}$/D0	I/O	VCC2	Output of byte control ($\overline{BC0}$) and input/output of data (D0) by time-division while accessing an external memory space with multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	VCC2	Chip select output
	$\overline{WR0}$/$\overline{WR1}$/$\overline{WR}$/ $\overline{BC0}$/$\overline{BC1}$/$\overline{RD}$	O	VCC2	Output of write, byte control, and read signals. Either $\overline{WRx}$ or $\overline{WR}$ and $\overline{BCx}$ can be selected by a program. Data is read when $\overline{RD}$ is low. • When $\overline{WR0}$, $\overline{WR1}$, and $\overline{RD}$ are selected, data is written to the following address: an even address, when $\overline{WR0}$ is low an odd address, when $\overline{WR1}$ is low on 16-bit external data bus • When $\overline{WR}$, $\overline{BC0}$, $\overline{BC1}$, and $\overline{RD}$ are selected, data is written, when $\overline{WR}$ is low and the following address is accessed: an even address, when $\overline{BC0}$ is low an odd address, when $\overline{BC1}$ is low on 16-bit external data bus
	ALE	O	VCC2	Latch enable signal in multiplexed bus format
	$\overline{HOLD}$	I	VCC2	The MCU is in a hold state while this pin is held low
	$\overline{HLDA}$	O	VCC2	This pin is driven low while the MCU is held in a hold state
	$\overline{RDY}$	I	VCC2	Bus cycle is extended by the CPU if this pin is low on the falling edge of the BCLK

Table 1.17 Pin Definitions and Functions for the 100-pin Package (3/4)

Function	Symbol	I/O	Power Supply	Description
I/O port	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7	I/O	VCC2	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Pull-up resistors are selected for following 4-pin units, but are enabled only for the input pins: Pi_0 to Pi_3 and Pi_4 to Pi_7 (i = 0 to 10). P7_0 and P7_1 outputs are N-channel open drain
	P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_4 P8_6, P8_7 P9_3 to P9_7 P10_0 to P10_7	I/O	VCC1	
Input port	P9_1	I	VCC1	Input port in CMOS. Pull-up resistors are selectable for P9_1 and P9_3
Timer A	TA0OUT to TA4OUT	I/O	VCC1 VCC2	Timers A0 to A4 input/output. TA0OUT output assigned for port P7_0 is N-channel open drain
	TA0IN to TA4IN	I	VCC1 VCC2	Timers A0 to A4 input
Timer B	TB0IN to TB5IN	I	VCC1	Timers B0 to B5 input
Three-phase motor control timer output	U,$\overline{U}$,V,$\overline{V}$,W,$\overline{W}$	O	VCC1 VCC2	Three-phase motor control timer output
Serial interface	$\overline{CTS0}$ to $\overline{CTS8}$	I	VCC1 VCC2	Handshake input
	$\overline{RTS0}$ to $\overline{RTS8}$	O	VCC1 VCC2	Handshake output
	CLK0 to CLK8	I/O	VCC1 VCC2	Transmit/receive clock input/output
	RXD0 to RXD8	I	VCC1 VCC2	Serial data input
	TXD0 to TXD8	O	VCC1 VCC2	Serial data output. TXD2 output is N-channel open drain
I^2C bus (simplified)	SDA0 to SDA6	I/O	VCC1 VCC2	Serial data input/output. SDA2 output is N-channel open drain
	SCL0 to SCL6	I/O	VCC1 VCC2	Transmit/receive clock input/output. SCL2 output is N-channel open drain

Table 1.18 Pin Definitions and Functions for the 100-pin Package (4/4)

Function	Symbol	I/O	Power Supply	Description
Serial interface special functions	STXD0 to STXD6	O	VCC1 VCC2	Serial data output in slave mode. STXD2 is N-channel open drain
	SRXD0 to SRXD6	I	VCC1 VCC2	Serial data input in slave mode
	$\overline{SS0}$ to $\overline{SS6}$	I	VCC1 VCC2	Input to control serial interface special functions
A/D converter	AN_0 to AN_7	I	VCC1	Analog input for the A/D converter
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC2	
	$\overline{ADTRG}$	I	VCC1	External trigger input for the A/D converter
	ANEX0	I/O	VCC1	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	VCC1	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	VCC1	Output for the D/A converter
Reference voltage input	VREF	I	–	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	VCC1 VCC2	Input/output for the Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	VCC1 VCC2	Input/output for the Intelligent I/O group 1. Either input capture or output compare is selectable. IIO1_6 and IIO1_7 outputs assigned for ports P7_0 and P7_1 are N-channel open drain
	UD0A, UD0B, UD1A, UD1B	I	VCC1 VCC2	Input for the two-phase encoder
	OUTC2_0 to OUTC2_2	O	VCC1 VCC2	Output for OC (output compare) of the Intelligent I/O group 2. OUTC2_0 and OUTC2_2 assigned for ports P7_0 and P7_1 are N-channel open drain
	ISCLK2	I/O	VCC1 VCC2	Clock input/output for the serial interface
	ISRXD2	I		Receive data input for the serial interface
	ISTXD2	O		Transmit data output for the serial interface. ISTXD2 assigned for port P7_0 is N-channel open drain
	IEIN	I	VCC1 VCC2	Receive data input for the serial interface
	IEOUT	O		Transmit data output for the serial interface. IEOUT assigned for port P7_0 is N-channel open drain

Table 1.19 Pin Definitions and Functions for the 80-/64-pin Package (1/3)

Function	Symbol	I/O	Description
Power supply	VCC1, VSS	I	Applicable as follows: VCC1 = 3.0 to 5.5 V, VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC1 via a resistor of 1 to 4.7 kΩ
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOUT. An external clock should be input at the XCIN while leaving the XCOUT open
Sub clock output	XCOUT	O	
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input for external interrupts
NMI input	P8_5/$\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input for the key input interrupt
I/O port (1)	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_4 P8_6, P8_7 P9_3, P9_5 to P9_7, P10_0 to P10_7	I/O	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Pull-up resistors are selected for following 4-pin units, but are enabled only for the input pins: Pi_0 to Pi_3 and Pi_4 to Pi_7 (i = 0 to 3, 6 to 10). P7_0 and P7_1 outputs are N-channel open drain
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output. TA0OUT output assigned for port P7_0 is N-channel open drain
	TA0IN to TA4IN	I	Timers A0 to A4 input
Timer B	TB0IN to TB3IN, TB5IN	I	Timers B0 to B3, and B5 input
Three-phase motor control timer output	U,$\overline{\text{U}}$,V,$\overline{\text{V}}$,W,$\overline{\text{W}}$	O	Three-phase motor control timer output

Note:
1. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, and P9_5 to P9_7 are available in the 80-pin package only.

Table 1.20 Pin Definitions and Functions for the 80-/64-pin Package (2/3)

Function	Symbol	I/O	Description
Serial interface (1)	$\overline{CTS0}$ to $\overline{CTS3}$, $\overline{CTS5}$, $\overline{CTS8}$	I	Handshake input
	$\overline{RTS0}$ to $\overline{RTS3}$, $\overline{RTS5}$, $\overline{RTS8}$	O	Handshake output
	CLK0 to CLK5, CLK8	I/O	Transmit/receive clock input/output
	RXD0 to RXD5, RXD8	I	Serial data input
	TXD0 to TXD5, TXD8	O	Serial data output. TXD2 output is N-channel open drain
I^2C bus (simplified) (1)	SDA0 to SDA5	I/O	Serial data input/output. SDA2 output is N-channel open drain
	SCL0 to SCL5	I/O	Transmit/receive clock input/output. SCL2 output is N-channel open drain
Serial interface special functions (1)	STXD0 to STXD5	O	Serial data output in slave mode. STXD2 is N-channel open drain
	SRXD0 to SRXD5	I	Serial data input in slave mode
	$\overline{SS0}$ to $\overline{SS3}$, $\overline{SS5}$	I	Input to control serial interface special functions
A/D converter (2)	AN_0 to AN_7 AN0_0 to AN0_7 AN2_0 to AN2_7	I	Analog input for the A/D converter
	$\overline{ADTRG}$	I	External trigger input for the A/D converter
	ANEX0	I/O	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	Expanded analog input for the A/D converter
D/A converter	DA0	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter

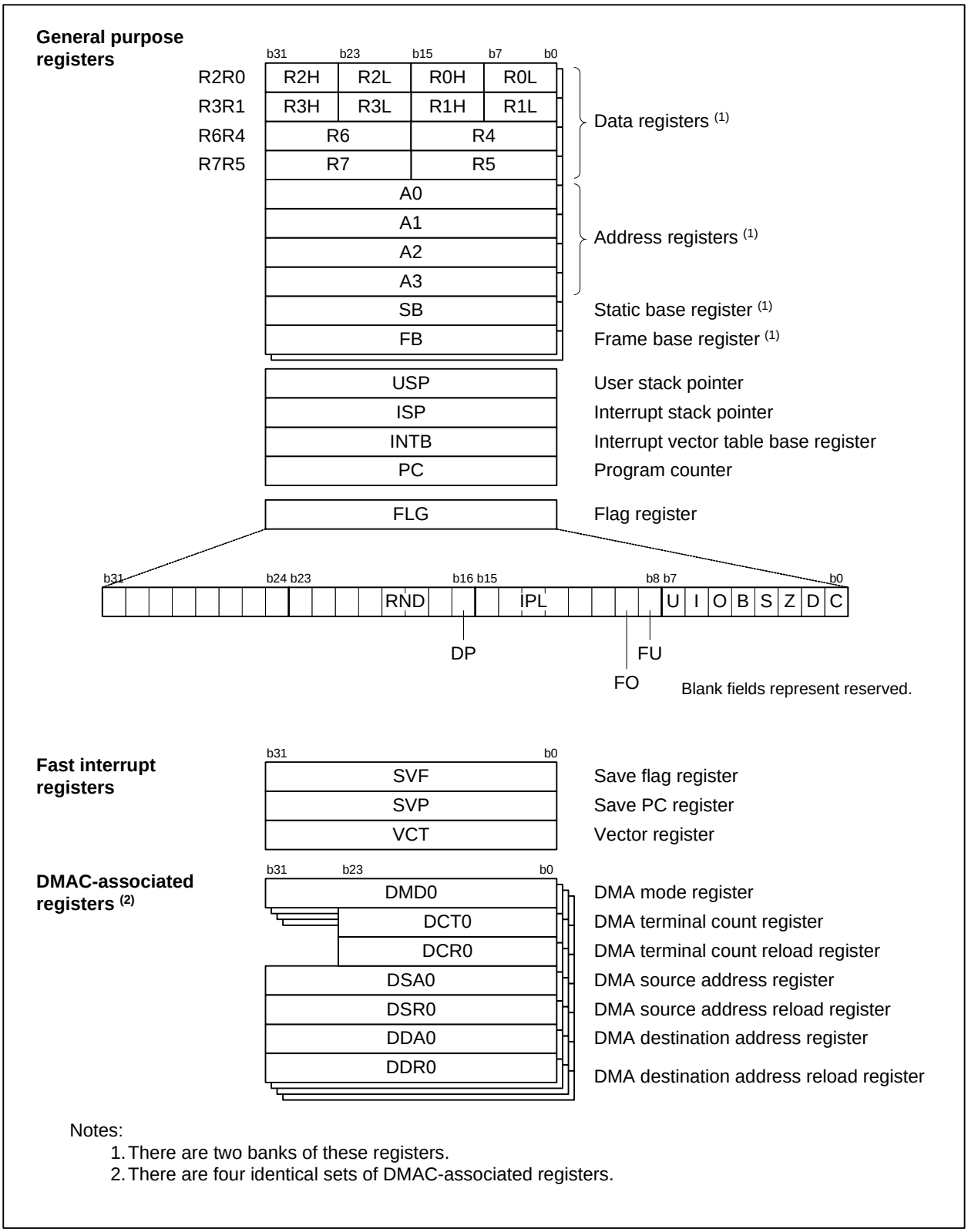
Notes:
1. Pins CLK4, RXD4, TXD4, SDA4, SCL4, SRXD4, and STXD4 are available in the 80-pin package only.
2. Pins AN0_4 to AN0_7, ANEX0 and ANEX1 are available in the 80-pin package only.

Table 1.21 Pin Definitions and Functions for the 80-/64-pin Package (3/3)

Function	Symbol	I/O	Description
Intelligent I/O	IIO0_0 to IIO0_7	I/O	Input/output for the Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	Input/output for the Intelligent I/O group 1. Either input capture or output compare is selectable. IIO1_6 and IIO1_7 outputs assigned for ports P7_0 and P7_1 are N-channel open drain
	UD0A, UD0B, UD1A, UD1B	I	Input for the two-phase encoder
	OUTC2_0 to OUTC2_2	O	Output for OC (output compare) of the Intelligent I/O group 2. OUTC2_0 and OUTC2_2 assigned for ports P7_0 and P7_1 are N-channel open drain
	ISCLK2	I/O	Clock input/output for the serial interface
	ISRXD2	I	Receive data input for the serial interface
	ISTXD2	O	Transmit data output for the serial interface. ISTXD2 assigned for port P7_0 is N-channel open drain
	IEIN	I	Receive data input for the serial interface
	IEOUT	O	Transmit data output for the serial interface. IEOUT assigned for port P7_0 is N-channel open drain

2. Central Processing Unit (CPU)

The CPU contains registers as shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.



Notes:
1. There are two banks of these registers.
2. There are four identical sets of DMAC-associated registers.

Figure 2.1 CPU Registers

2.1 General Purpose Registers

2.1.1 Data Registers (R2R0, R3R1, R6R4, and R7R5)

These 32-bit registers are primarily used for transfers and arithmetic/logic operations.
Each of the registers can be divided into upper and lower 16-bit registers, e.g. R2R0 can be divided into R2 and R0, R3R0 can be divided into R3 and R1, etc.
Moreover, data registers R2R0 and R3R1 can be divided into four 8-bit data registers: upper (R2H and R3H), mid-upper (R2L and R3L), mid-lower (R0H and R1H), and lower (R0L and R1L).

2.1.2 Address Registers (A0, A1, A2, and A3)

These 32-bit registers have functions similar to data registers. They are also used for address register indirect addressing and address register relative addressing.

2.1.3 Static Base Register (SB)

This 32-bit register is used for SB relative addressing.

2.1.4 Frame Base Register (FB)

This 32-bit register is used for FB relative addressing.

2.1.5 Program Counter (PC)

This 32-bit counter indicates the address of the instruction to be executed next.

2.1.6 Interrupt Vector Table Base Register (INTB)

This 32-bit register indicates the start address of a relocatable vector table.

2.1.7 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Two types of 32-bit stack pointers (SPs) are provided: user stack pointer (USP) and interrupt stack pointer (ISP).
Use the stack pointer select flag (U flag) to select either the user stack pointer (USP) or the interrupt stack pointer (ISP). The U flag is bit 7 in the flag register (FLG). Refer to 2.1.8 “Flag Register (FLG)” for details.
To minimize the overhead of interrupt sequence due to less memory access, set the user stack pointer (USP) or the interrupt stack pointer (ISP) to a multiple of 4.

2.1.8 Flag Register (FLG)

This 32-bit register indicates the CPU status.

2.1.8.1 Carry Flag (C flag)

This flag becomes 1 when any of the carry, borrow, shifted-out bit, etc. is generated in the arithmetic logic unit (ALU).

2.1.8.2 Debug Flag (D flag)

This flag is only for debugging. Only set this bit to 0.

2.1.8.3 Zero Flag (Z flag)

This flag becomes 1 when the result of an operation is 0; otherwise it is 0.

2.1.8.4 Sign Flag (S flag)

This flag becomes 1 when the result of an operation is a negative value; otherwise it is 0.

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when the register bank 0 is selected, and 1 when the register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 if an overflow occurs in an operation; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupts is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand has invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand has invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of three bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is acceptable when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to take. It is used in the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt is generated.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt is generated.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt is generated.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set DMA transfer counting.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded value for DMA source address register.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination address.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

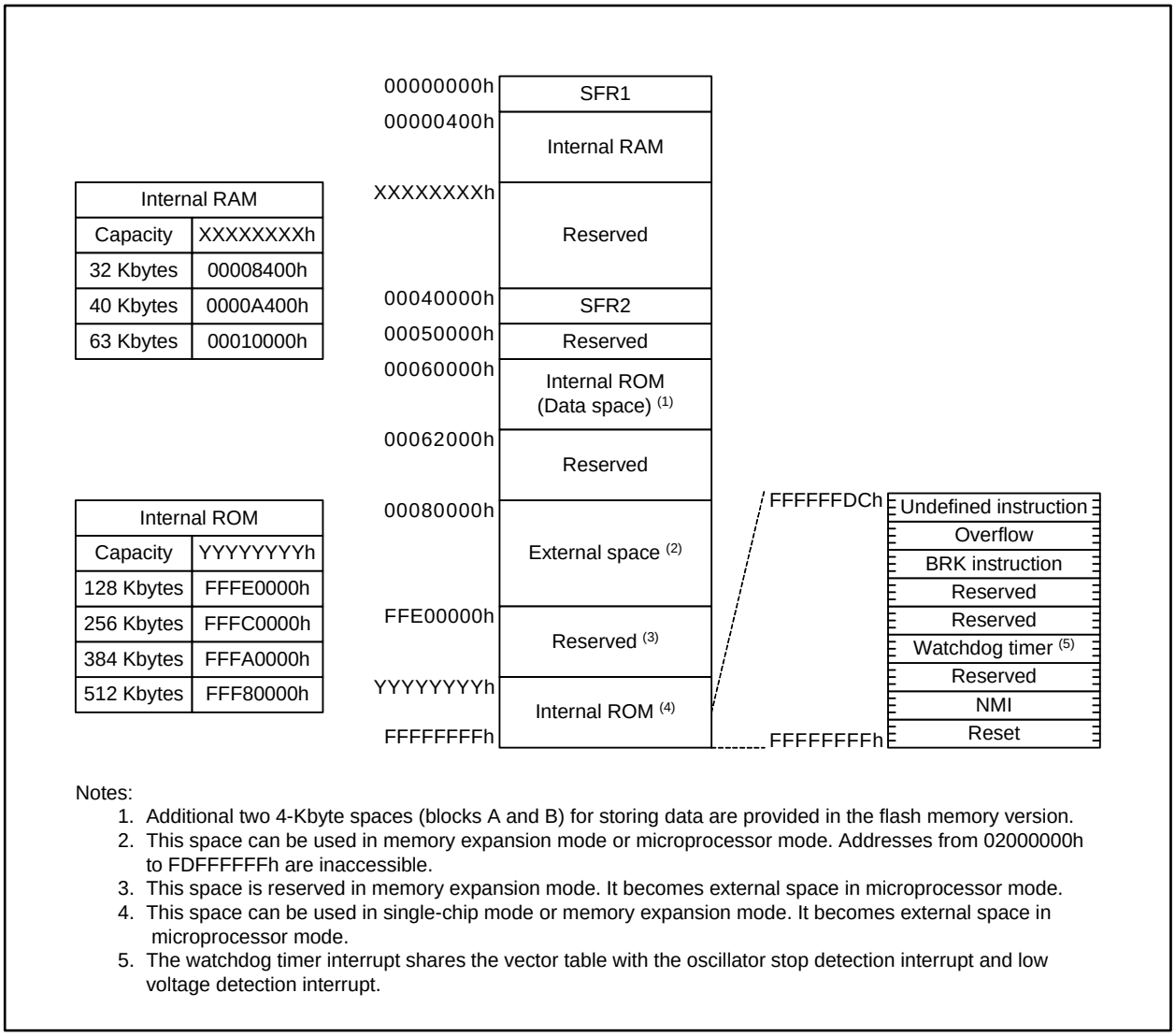
3. Memory

Figure 3.1 shows the memory map of the R32C/111 Group.
The R32C/111 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

The internal ROM is mapped to the end of the memory map with the ending address fixed at FFFFFFFFh. Therefore, the 512-Kbyte internal ROM is mapped from FFF80000h to FFFFFFFFh.
The fixed interrupt vector table which contains each start address of interrupt handlers is mapped from FFFFFFDCh to FFFFFFFFh.
The internal RAM is mapped to the beginning of the memory map with the starting address fixed at 00000400h. Therefore, the 63-Kbyte internal RAM is mapped from 00000400h to 0000FFFFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutines and/or interrupt handlers.

Special Function Registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved. No access is allowed.

In memory expansion mode or microprocessor mode, some spaces are reserved for internal use and should not be accessed.



Internal RAM	
Capacity	XXXXXXXXh
32 Kbytes	00008400h
40 Kbytes	0000A400h
63 Kbytes	00010000h

Internal ROM	
Capacity	YYYYYYYYh
128 Kbytes	FFFE0000h
256 Kbytes	FFFC0000h
384 Kbytes	FFFA0000h
512 Kbytes	FFF80000h

Notes:
1. Additional two 4-Kbyte spaces (blocks A and B) for storing data are provided in the flash memory version.
2. This space can be used in memory expansion mode or microprocessor mode. Addresses from 02000000h to FDFFFFFFh are inaccessible.
3. This space is reserved in memory expansion mode. It becomes external space in microprocessor mode.
4. This space can be used in single-chip mode or memory expansion mode. It becomes external space in microprocessor mode.
5. The watchdog timer interrupt shares the vector table with the oscillator stop detection interrupt and low voltage detection interrupt.

Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.24 SFR List (24) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h 000011h	External Bus Control Register 3/Flash Memory Rewrite Bus Control Register 3	EBC3/FEBC3	0000h
000012h	Chip Selects 2 and 3 Boundary Setting Register	CB23	00h
000013h			
000014h 000015h	External Bus Control Register 2	EBC2	0000h
000016h	Chip Selects 1 and 2 Boundary Setting Register	CB12	00h
000017h			
000018h 000019h	External Bus Control Register 1	EBC1	0000h
00001Ah	Chip selects 0 and 1 Boundary Setting Register	CB01	00h
00001Bh			
00001Ch 00001Dh	External Bus Control Register 0/Flash Memory Rewrite Bus Control Register 0	EBC0/FEBC0	0000h
00001Eh 00001Fh	Peripheral Bus Control Register	PBC	0504h
000020h to 00005Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h	UART5 Transmit/NACK Interrupt Control Register	S5TIC	XXXX X000b
000063h	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
000064h	UART6 Transmit/NACK Interrupt Control Register	S6TIC	XXXX X000b
000065h	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
000066h	UART5/6 Bus Collision, Start Condition/Stop Condition Detection Interrupt Control Register	BCN5IC/BCN6IC	XXXX X000b
000067h	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0/3 Bus Collision, Start Condition/Stop Condition Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h			
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh			
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh			
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh			
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
000082h	UART5 Receive/ACK Interrupt Control Register	S5RIC	XXXX X000b
000083h	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
000084h	UART6 Receive/ACK Interrupt Control Register	S6RIC	XXXX X000b
000085h	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
000086h			
000087h	UART2 Bus Collision, Start Condition/Stop Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.3 SFR List (3)

Address	Register	Symbol	Reset Value
000088h	DMA1 Transfer Complete Interrupt Control Register	DM1IC	XXXX X000b
000089h	UART1/4 Bus Collision, Start Condition/Stop Condition Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
00008Ah	DMA3 Transfer Complete Interrupt Control Register	DM3IC	XXXX X000b
00008Bh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
00008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
00008Dh	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000b
00008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
00008Fh	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000b
000090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
000091h	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X000b
000092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
000093h	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X000b
000094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
000095h	Intelligent I/O Interrupt Control Register 9	IIO9IC	XXXX X000b
000096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
000097h	Intelligent I/O Interrupt Control Register 11	IIO11IC	XXXX X000b
000098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
000099h			
00009Ah	INT4 Interrupt Control Register	INT4IC	XX00 X000b
00009Bh			
00009Ch	INT2 Interrupt Control Register	INT2IC	XX00 X000b
00009Dh			
00009Eh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
00009Fh			
0000A0h	Intelligent I/O Interrupt Request Register 0	IIO0IR	0000 0XX1b
0000A1h	Intelligent I/O Interrupt Request Register 1	IIO1IR	0000 0XX1b
0000A2h	Intelligent I/O Interrupt Request Register 2	IIO2IR	0000 0X01b
0000A3h	Intelligent I/O Interrupt Request Register 3	IIO3IR	0000 XXX1b
0000A4h	Intelligent I/O Interrupt Request Register 4	IIO4IR	000X 0XX1b
0000A5h	Intelligent I/O Interrupt Request Register 5	IIO5IR	000X 0XX1b
0000A6h	Intelligent I/O Interrupt Request Register 6	IIO6IR	000X 0XX1b
0000A7h	Intelligent I/O Interrupt Request Register 7	IIO7IR	X00X 0XX1b
0000A8h	Intelligent I/O Interrupt Request Register 8	IIO8IR	XX0X 0XX1b
0000A9h	Intelligent I/O Interrupt Request Register 9	IIO9IR	0000 0XX1b
0000AAh	Intelligent I/O Interrupt Request Register 10	IIO10IR	0000 0XX1b
0000ABh	Intelligent I/O Interrupt Request Register 11	IIO11IR	0000 0XX1b
0000ACh			
0000ADh			
0000AEh			
0000AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.4 SFR List (4)

Address	Register	Symbol	Reset Value
0000B0h	Intelligent I/O Interrupt Enable Register 0	IIO0IE	00h
0000B1h	Intelligent I/O Interrupt Enable Register 1	IIO1IE	00h
0000B2h	Intelligent I/O Interrupt Enable Register 2	IIO2IE	00h
0000B3h	Intelligent I/O Interrupt Enable Register 3	IIO3IE	00h
0000B4h	Intelligent I/O Interrupt Enable Register 4	IIO4IE	00h
0000B5h	Intelligent I/O Interrupt Enable Register 5	IIO5IE	00h
0000B6h	Intelligent I/O Interrupt Enable Register 6	IIO6IE	00h
0000B7h	Intelligent I/O Interrupt Enable Register 7	IIO7IE	00h
0000B8h	Intelligent I/O Interrupt Enable Register 8	IIO8IE	00h
0000B9h	Intelligent I/O Interrupt Enable Register 9	IIO9IE	00h
0000BAh	Intelligent I/O Interrupt Enable Register 10	IIO10IE	00h
0000BBh	Intelligent I/O Interrupt Enable Register 11	IIO11IE	00h
0000BCh			
0000BDh			
0000BEh			
0000BFh			
0000C0h			
0000C1h			
0000C2h			
0000C3h			
0000C4h			
0000C5h			
0000C6h			
0000C7h			
0000C8h			
0000C9h			
0000CAh			
0000CBh			
0000CCh			
0000CDh			
0000CEh			
0000CFh			
0000D0h			
0000D1h			
0000D2h			
0000D3h			
0000D4h			
0000D5h			
0000D6h			
0000D7h			
0000D8h			
0000D9h			
0000DAh			
0000DBh			
0000DCh			
0000DDh	UART7 Transmit Interrupt Control Register	S7TIC	XXXX X000b
0000DEh			
0000DFh	UART8 Transmit Interrupt Control Register	S8TIC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.5 SFR List (5)

Address	Register	Symbol	Reset Value
0000E0h			
0000E1h			
0000E2h			
0000E3h			
0000E4h			
0000E5h			
0000E6h			
0000E7h			
0000E8h			
0000E9h			
0000EAh			
0000EBh			
0000ECh			
0000EDh			
0000EEh			
0000EFh			
0000F0h			
0000F1h			
0000F2h			
0000F3h			
0000F4h			
0000F5h			
0000F6h			
0000F7h			
0000F8h			
0000F9h			
0000FAh			
0000FBh			
0000FCh			
0000FDh	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0000FEh			
0000FFh	UART8 Receive Interrupt Control Register	S8RIC	XXXX X000b
000100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
000101h			
000102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
000103h			
000104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
000105h			
000106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
000107h			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.6 SFR List (6)

Address	Register	Symbol	Reset Value
000108h	Group 1 Time Measurement/Waveform Generation Register 4	G1TM4/G1PO4	XXXXh
000109h			
00010Ah	Group 1 Time Measurement/Waveform Generation Register 5	G1TM5/G1PO5	XXXXh
00010Bh			
00010Ch	Group 1 Time Measurement/Waveform Generation Register 6	G1TM6/G1PO6	XXXXh
00010Dh			
00010Eh	Group 1 Time Measurement/Waveform Generation Register 7	G1TM7/G1PO7	XXXXh
00010Fh			
000110h	Group 1 Waveform Generation Control Register 0	G1POCR0	0000 X000b
000111h	Group 1 Waveform Generation Control Register 1	G1POCR1	0X00 X000b
000112h	Group 1 Waveform Generation Control Register 2	G1POCR2	0X00 X000b
000113h	Group 1 Waveform Generation Control Register 3	G1POCR3	0X00 X000b
000114h	Group 1 Waveform Generation Control Register 4	G1POCR4	0X00 X000b
000115h	Group 1 Waveform Generation Control Register 5	G1POCR5	0X00 X000b
000116h	Group 1 Waveform Generation Control Register 6	G1POCR6	0X00 X000b
000117h	Group 1 Waveform Generation Control Register 7	G1POCR7	0X00 X000b
000118h	Group 1 Time Measurement Control Register 0	G1TMCR0	00h
000119h	Group 1 Time Measurement Control Register 1	G1TMCR1	00h
00011Ah	Group 1 Time Measurement Control Register 2	G1TMCR2	00h
00011Bh	Group 1 Time Measurement Control Register 3	G1TMCR3	00h
00011Ch	Group 1 Time Measurement Control Register 4	G1TMCR4	00h
00011Dh	Group 1 Time Measurement Control Register 5	G1TMCR5	00h
00011Eh	Group 1 Time Measurement Control Register 6	G1TMCR6	00h
00011Fh	Group 1 Time Measurement Control Register 7	G1TMCR7	00h
000120h	Group 1 Base Timer Register	G1BT	XXXXh
000121h			
000122h	Group 1 Base Timer Control Register 0	G1BCR0	00h
000123h	Group 1 Base Timer Control Register 1	G1BCR1	0000 0000b
000124h	Group 1 Timer Measurement Prescaler Register 6	G1TPR6	00h
000125h	Group 1 Timer Measurement Prescaler Register 7	G1TPR7	00h
000126h	Group 1 Function Enable Register	G1FE	00h
000127h	Group 1 Function Select Register	G1FS	00h
000128h			
000129h			
00012Ah			
00012Bh			
00012Ch			
00012Dh			
00012Eh			
00012Fh			
000130h to 00013Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.7 SFR List (7)

Address	Register	Symbol	Reset Value
000140h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
000141h			
000142h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
000143h			
000144h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
000145h			
000146h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
000147h			
000148h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
000149h			
00014Ah	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
00014Bh			
00014Ch	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
00014Dh			
00014Eh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh
00014Fh			
000150h	Group 2 Waveform Generation Control Register 0	G2POCR0	0000 0000b
000151h	Group 2 Waveform Generation Control Register 1	G2POCR1	0000 0000b
000152h	Group 2 Waveform Generation Control Register 2	G2POCR2	0000 0000b
000153h	Group 2 Waveform Generation Control Register 3	G2POCR3	0000 0000b
000154h	Group 2 Waveform Generation Control Register 4	G2POCR4	0000 0000b
000155h	Group 2 Waveform Generation Control Register 5	G2POCR5	0000 0000b
000156h	Group 2 Waveform Generation Control Register 6	G2POCR6	0000 0000b
000157h	Group 2 Waveform Generation Control Register 7	G2POCR7	0000 0000b
000158h			
000159h			
00015Ah			
00015Bh			
00015Ch			
00015Dh			
00015Eh			
00015Fh			
000160h	Group 2 Base Timer Register	G2BT	XXXXh
000161h			
000162h	Group 2 Base Timer Control Register 0	G2BCR0	00h
000163h	Group 2 Base Timer Control Register 1	G2BCR1	0000 0000b
000164h	Base Timer Start Register	BTSR	XXXX 0000b
000165h			
000166h	Group 2 Function Enable Register	G2FE	00h
000167h	Group 2 RTP Output Buffer Register	G2RTP	00h
000168h			
000169h			
00016Ah	Group 2 Serial Interface Mode Register	G2MR	00XX X000b
00016Bh	Group 2 Serial Interface Control Register	G2CR	0000 X110b
00016Ch	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
00016Dh			
00016Eh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
00016Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.8 SFR List (8)

Address	Register	Symbol	Reset Value
000170h	Group 2 IE Bus Address Register	IEAR	XXXXh
000171h			
000172h	Group 2 IE Bus Control Register	IECR	00XX X000b
000173h	Group 2 IE Bus Transmit Interrupt Source Detect Register	IETIF	XXX0 0000b
000174h	Group 2 IE Bus Receive Interrupt Source Detect Register	IERIF	XXX0 0000b
000175h			
000176h			
000177h			
000178h			
000179h			
00017Ah			
00017Bh			
00017Ch			
00017Dh			
00017Eh			
00017Fh			
000180h	Group 0 Time Measurement/Waveform Generation Register 0	G0TM0/G0PO0	XXXXh
000181h			
000182h	Group 0 Time Measurement/Waveform Generation Register 1	G0TM1/G0PO1	XXXXh
000183h			
000184h	Group 0 Time Measurement/Waveform Generation Register 2	G0TM2/G0PO2	XXXXh
000185h			
000186h	Group 0 Time Measurement/Waveform Generation Register 3	G0TM3/G0PO3	XXXXh
000187h			
000188h	Group 0 Time Measurement/Waveform Generation Register 4	G0TM4/G0PO4	XXXXh
000189h			
00018Ah	Group 0 Time Measurement/Waveform Generation Register 5	G0TM5/G0PO5	XXXXh
00018Bh			
00018Ch	Group 0 Time Measurement/Waveform Generation Register 6	G0TM6/G0PO6	XXXXh
00018Dh			
00018Eh	Group 0 Time Measurement/Waveform Generation Register 7	G0TM7/G0PO7	XXXXh
00018Fh			
000190h	Group 0 Waveform Generation Control Register 0	G0POCR0	0000 X000b
000191h	Group 0 Waveform Generation Control Register 1	G0POCR1	0X00 X000b
000192h	Group 0 Waveform Generation Control Register 2	G0POCR2	0X00 X000b
000193h	Group 0 Waveform Generation Control Register 3	G0POCR3	0X00 X000b
000194h	Group 0 Waveform Generation Control Register 4	G0POCR4	0X00 X000b
000195h	Group 0 Waveform Generation Control Register 5	G0POCR5	0X00 X000b
000196h	Group 0 Waveform Generation Control Register 6	G0POCR6	0X00 X000b
000197h	Group 0 Waveform Generation Control Register 7	G0POCR7	0X00 X000b
000198h	Group 0 Time Measurement Control Register 0	G0TMCR0	00h
000199h	Group 0 Time Measurement Control Register 1	G0TMCR1	00h
00019Ah	Group 0 Time Measurement Control Register 2	G0TMCR2	00h
00019Bh	Group 0 Time Measurement Control Register 3	G0TMCR3	00h
00019Ch	Group 0 Time Measurement Control Register 4	G0TMCR4	00h
00019Dh	Group 0 Time Measurement Control Register 5	G0TMCR5	00h
00019Eh	Group 0 Time Measurement Control Register 6	G0TMCR6	00h
00019Fh	Group 0 Time Measurement Control Register 7	G0TMCR7	00h

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

Address	Register	Symbol	Reset Value
0001A0h	Group 0 Base Timer Register	G0BT	XXXXh
0001A1h			
0001A2h	Group 0 Base Timer Control Register 0	G0BCR0	00h
0001A3h	Group 0 Base Timer Control Register 1	G0BCR1	0000 0000b
0001A4h	Group 0 Timer Measurement Prescaler Register 6	G0TPR6	00h
0001A5h	Group 0 Timer Measurement Prescaler Register 7	G0TPR7	00h
0001A6h	Group 0 Function Enable Register	G0FE	00h
0001A7h	Group 0 Function Select Register	G0FS	00h
0001A8h			
0001A9h			
0001AAh			
0001ABh			
0001ACh			
0001ADh			
0001AEh			
0001AFh			
0001B0h			
0001B1h			
0001B2h			
0001B3h			
0001B4h			
0001B5h			
0001B6h			
0001B7h			
0001B8h			
0001B9h			
0001BAh			
0001BBh			
0001BCh			
0001BDh			
0001BEh			
0001BFh			
0001C0h			
0001C1h			
0001C2h			
0001C3h			
0001C4h	UART5 Special Mode Register 4	U5SMR4	00h
0001C5h	UART5 Special Mode Register 3	U5SMR3	00h
0001C6h	UART5 Special Mode Register 2	U5SMR2	00h
0001C7h	UART5 Special Mode Register	U5SMR	00h
0001C8h	UART5 Transmit/Receive Mode Register	U5MR	00h
0001C9h	UART5 Bit Rate Register	U5BRG	XXh
0001CAh	UART5 Transmit Buffer Register	U5TB	XXXXh
0001CBh			
0001CCh	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
0001CDh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
0001CEh	UART5 Receive Buffer Register	U5RB	XXXXh
0001CFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.10 SFR List (10)

Address	Register	Symbol	Reset Value
0001D0h			
0001D1h			
0001D2h			
0001D3h			
0001D4h	UART6 Special Mode Register 4	U6SMR4	00h
0001D5h	UART6 Special Mode Register 3	U6SMR3	00h
0001D6h	UART6 Special Mode Register 2	U6SMR2	00h
0001D7h	UART6 Special Mode Register	U6SMR	00h
0001D8h	UART6 Transmit/Receive Mode Register	U6MR	00h
0001D9h	UART6 Bit Rate Register	U6BRG	XXh
0001DAh	UART6 Transmit Buffer Register	U6TB	XXXXh
0001DBh			
0001DCh	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
0001DDh	UART6 Transmit/Receive Control Register 1	U6C1	0000 0010b
0001DEh	UART6 Receive Buffer Register	U6RB	XXXXh
0001DFh			
0001E0h	UART7 Transmit/Receive Mode Register	U7MR	00h
0001E1h	UART7 Bit Rate Register	U7BRG	XXh
0001E2h	UART7 Transmit Buffer Register	U7TB	XXXXh
0001E3h			
0001E4h	UART7 Transmit/Receive Control Register 0	U7C0	00X0 1000b
0001E5h	UART7 Transmit/Receive Control Register 1	U7C1	XXXX 0010b
0001E6h	UART7 Receive Buffer Register	U7RB	XXXXh
0001E7h			
0001E8h	UART8 Transmit/Receive Mode Register	U8MR	00h
0001E9h	UART8 Bit Rate Register	U8BRG	XXh
0001EAh	UART8 Transmit Buffer Register	U8TB	XXXXh
0001EBh			
0001ECh	UART8 Transmit/Receive Control Register 0	U8C0	00X0 1000b
0001EDh	UART8 Transmit/Receive Control Register 1	U8C1	XXXX 0010b
0001EEh	UART8 Receive Buffer Register	U8RB	XXXXh
0001EFh			
0001F0h	UART7, UART8 Transmit/Receive Control Register 2	U78CON	X000 0000b
0001F1h			
0001F2h			
0001F3h			
0001F4h			
0001F5h			
0001F6h			
0001F7h			
0001F8h			
0001F9h			
0001FAh			
0001FBh			
0001FCh			
0001FDh			
0001FEh			
0001FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.11 SFR List (11)

Address	Register	Symbol	Reset Value
000200h to 0002BFh			
0002C0h	X0 Register/Y0 Register	X0R/Y0R	XXXXh
0002C1h			
0002C2h	X1 Register/Y1 Register	X1R/Y1R	XXXXh
0002C3h			
0002C4h	X2 Register/Y2 Register	X2R/Y2R	XXXXh
0002C5h			
0002C6h	X3 Register/Y3 Register	X3R/Y3R	XXXXh
0002C7h			
0002C8h	X4 Register/Y4 Register	X4R/Y4R	XXXXh
0002C9h			
0002CAh	X5 Register/Y5 Register	X5R/Y5R	XXXXh
0002CBh			
0002CCh	X6 Register/Y6 Register	X6R/Y6R	XXXXh
0002CDh			
0002CEh	X7 Register/Y7 Register	X7R/Y7R	XXXXh
0002CFh			
0002D0h	X8 Register/Y8 Register	X8R/Y8R	XXXXh
0002D1h			
0002D2h	X9 Register/Y9 Register	X9R/Y9R	XXXXh
0002D3h			
0002D4h	X10 Register/Y10 Register	X10R/Y10R	XXXXh
0002D5h			
0002D6h	X11 Register/Y11 Register	X11R/Y11R	XXXXh
0002D7h			
0002D8h	X12 Register/Y12 Register	X12R/Y12R	XXXXh
0002D9h			
0002DAh	X13 Register/Y13 Register	X13R/Y13R	XXXXh
0002DBh			
0002DCh	X14 Register/Y14 Register	X14R/Y14R	XXXXh
0002DDh			
0002DEh	X15 Register/Y15 Register	X15R/Y15R	XXXXh
0002DFh			
0002E0h	XY Control Register	XYC	XXXX XX00b
0002E1h			
0002E2h			
0002E3h			
0002E4h	UART1 Special Mode Register 4	U1SMR4	00h
0002E5h	UART1 Special Mode Register 3	U1SMR3	00h
0002E6h	UART1 Special Mode Register 2	U1SMR2	00h
0002E7h	UART1 Special Mode Register	U1SMR	00h
0002E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
0002E9h	UART1 Bit Rate Register	U1BRG	XXh
0002EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
0002EBh			
0002ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
0002EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
0002EEh	UART1 Receive Buffer Register	U1RB	XXXXh
0002EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.12 SFR List (12)

Address	Register	Symbol	Reset Value
0002F0h			
0002F1h			
0002F2h			
0002F3h			
0002F4h	UART4 Special Mode Register 4	U4SMR4	00h
0002F5h	UART4 Special Mode Register 3	U4SMR3	00h
0002F6h	UART4 Special Mode Register 2	U4SMR2	00h
0002F7h	UART4 Special Mode Register	U4SMR	00h
0002F8h	UART4 Transmit/Receive Mode Register	U4MR	00h
0002F9h	UART4 Bit Rate Register	U4BRG	XXh
0002FAh	UART4 Transmit Buffer Register	U4TB	XXXXh
0002FBh			
0002FCh	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
0002FDh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
0002FEh	UART4 Receive Buffer Register	U4RB	XXXXh
0002FFh			
000300h	Count Start Register for Timers B3, B4 and B5	TBSR	000X XXXXb
000301h			
000302h	Timer A1-1 Register	TA11	XXXXh
000303h			
000304h	Timer A2-1 Register	TA21	XXXXh
000305h			
000306h	Timer A4-1 Register	TA41	XXXXh
000307h			
000308h	Three-phase PWM Control Register 0	INVC0	00h
000309h	Three-phase PWM Control Register 1	INVC1	00h
00030Ah	Three-phase Output Buffer Register 0	IDB0	XX11 1111b
00030Bh	Three-phase Output Buffer Register 1	IDB1	XX11 1111b
00030Ch	Dead Time Timer	DTT	XXh
00030Dh	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XXh
00030Eh			
00030Fh			
000310h	Timer B3 Register	TB3	XXXXh
000311h			
000312h	Timer B4 Register	TB4	XXXXh
000313h			
000314h	Timer B5 Register	TB5	XXXXh
000315h			
000316h			
000317h			
000318h			
000319h			
00031Ah			
00031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
00031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
00031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
00031Eh			
00031Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.13 SFR List (13)

Address	Register	Symbol	Reset Value
000320h			
000321h			
000322h			
000323h			
000324h	UART3 Special Mode Register 4	U3SMR4	00h
000325h	UART3 Special Mode Register 3	U3SMR3	00h
000326h	UART3 Special Mode Register 2	U3SMR2	00h
000327h	UART3 Special Mode Register	U3SMR	00h
000328h	UART3 Transmit/Receive Mode Register	U3MR	00h
000329h	UART3 Bit Rate Register	U3BRG	XXh
00032Ah	UART3 Transmit Buffer Register	U3TB	XXXXh
00032Bh			
00032Ch	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
00032Dh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
00032Eh	UART3 Receive Buffer Register	U3RB	XXXXh
00032Fh			
000330h			
000331h			
000332h			
000333h			
000334h	UART2 Special Mode Register 4	U2SMR4	00h
000335h	UART2 Special Mode Register 3	U2SMR3	00h
000336h	UART2 Special Mode Register 2	U2SMR2	00h
000337h	UART2 Special Mode Register	U2SMR	00h
000338h	UART2 Transmission/Receive Mode Register	U2MR	00h
000339h	UART2 Bit Rate Register	U2BRG	XXh
00033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
00033Bh			
00033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
00033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
00033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
00033Fh			
000340h	Count Start Register	TABSR	00h
000341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
000342h	One-shot Start Register	ONSF	00h
000343h	Trigger Select Register	TRGSR	00h
000344h	Increment/Decrement Counting Select Register	UDF	0000 0000b
000345h			
000346h	Timer A0 Register	TA0	XXXXh
000347h			
000348h	Timer A1 Register	TA1	XXXXh
000349h			
00034Ah	Timer A2 Register	TA2	XXXXh
00034Bh			
00034Ch	Timer A3 Register	TA3	XXXXh
00034Dh			
00034Eh	Timer A4 Register	TA4	XXXXh
00034Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.14 SFR List (14)

Address	Register	Symbol	Reset Value
000350h	Timer B0 Register	TB0	XXXXh
000351h			
000352h	Timer B1 Register	TB1	XXXXh
000353h			
000354h	Timer B2 Register	TB2	XXXXh
000355h			
000356h	Timer A0 Mode Register	TA0MR	0000 0000b
000357h	Timer A1 Mode Register	TA1MR	0000 0000b
000358h	Timer A2 Mode Register	TA2MR	0000 0000b
000359h	Timer A3 Mode Register	TA3MR	0000 0000b
00035Ah	Timer A4 Mode Register	TA4MR	0000 0000b
00035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
00035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
00035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
00035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
00035Fh	Count Source Prescaler Register	TCSPR	0000 0000b
000360h			
000361h			
000362h			
000363h			
000364h	UART0 Special Mode Register 4	U0SMR4	00h
000365h	UART0 Special Mode Register 3	U0SMR3	00h
000366h	UART0 Special Mode Register 2	U0SMR2	00h
000367h	UART0 Special Mode Register	U0SMR	00h
000368h	UART0 Transmit/Receive Mode Register	U0MR	00h
000369h	UART0 Bit Rate Register	U0BRG	XXh
00036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
00036Bh			
00036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
00036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
00036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
00036Fh			
000370h			
000371h			
000372h			
000373h			
000374h			
000375h			
000376h			
000377h			
000378h			
000379h			
00037Ah			
00037Bh			
00037Ch	CRC Data Register	CRCD	XXXXh
00037Dh			
00037Eh	CRC Input Register	CRCIN	XXh
00037Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h			
000394h	A/D0 Control Register 2	AD0CON2	X00X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.16 SFR List (16)

Address	Register	Symbol	Reset Value
0003B0h			
0003B1h			
0003B2h			
0003B3h			
0003B4h			
0003B5h			
0003B6h			
0003B7h			
0003B8h			
0003B9h			
0003BAh			
0003BBh			
0003BCh			
0003BDh			
0003BEh			
0003BFh			
0003C0h	Port P0 Register	P0	XXh
0003C1h	Port P1 Register	P1	XXh
0003C2h	Port P0 Direction Register	PD0	0000 0000b
0003C3h	Port P1 Direction Register	PD1	0000 0000b
0003C4h	Port P2 Register	P2	XXh
0003C5h	Port P3 Register	P3	XXh
0003C6h	Port P2 Direction Register	PD2	0000 0000b
0003C7h	Port P3 Direction Register	PD3	0000 0000b
0003C8h	Port P4 Register	P4	XXh
0003C9h	Port P5 Register	P5	XXh
0003CAh	Port P4 Direction Register	PD4	0000 0000b
0003CBh	Port P5 Direction Register	PD5	0000 0000b
0003CCh	Port P6 Register	P6	XXh
0003CDh	Port P7 Register	P7	XXh
0003CEh	Port P6 Direction Register	PD6	0000 0000b
0003CFh	Port P7 Direction Register	PD7	0000 0000b
0003D0h	Port P8 Register	P8	XXh
0003D1h	Port P9 Register	P9	XXh
0003D2h	Port P8 Direction Register	PD8	00X0 0000b
0003D3h	Port P9 Direction Register	PD9	0000 0000b
0003D4h	Port P10 Register	P10	XXh
0003D5h			
0003D6h	Port P10 Direction Register	PD10	0000 0000b
0003D7h			
0003D8h			
0003D9h			
0003DAh			
0003DBh			
0003DCh			
0003DDh			
0003DEh			
0003DFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX 0000b
0003F2h	Pull-up Control Register 2	PUR2	0000 0000b
0003F3h	Pull-up Control Register 3	PUR3	XXXX XX00b
0003F4h			
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	XXXX XXX0b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.18 SFR List (18)

Address	Register	Symbol	Reset Value
040000h	Flash Memory Control Register 0	FMR0	0X01 XX00b
040001h	Flash Memory Status Register 0	FMSR0	1000 0000b
040002h			
040003h			
040004h			
040005h			
040006h			
040007h			
040008h	Flash Register Protection Unlock Register 0	FPR0	00h
040009h	Flash Memory Control Register 1	FMR1	0000 0010b
04000Ah	Block Protect Bit Monitor Register 0	FBPM0	??X? ????b (1)
04000Bh	Block Protect Bit Monitor Register 1	FBPM1	XXX? ????b (1)
04000Ch			
04000Dh			
04000Eh			
04000Fh			
040010h			
040011h			
040012h			
040013h			
040014h			
040015h			
040016h			
040017h			
040018h			
040019h			
04001Ah			
04001Bh			
04001Ch			
04001Dh			
04001Eh			
04001Fh			
040020h	PLL Control Register 0	PLC0	0000 0001b
040021h	PLL Control Register 1	PLC1	0001 1111b
040022h			
040023h			
040024h			
040025h			
040026h			
040027h			
040028h			
040029h			
04002Ah			
04002Bh			
04002Ch			
04002Dh			
04002Eh			
04002Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The status of protect bit of each block in flash memory is reflected.

Table 4.19 SFR List (19)

Address	Register	Symbol	Reset Value
040030h to 04003Fh			
040040h			
040041h			
040042h			
040043h			
040044h	Processor Mode Register 0 (1)	PM0	1000 0000b (CNVSS pin = Low) 0000 0011b (CNVSS pin = High)
040045h			
040046h	System Clock Control Register 0	CM0	0000 1000b
040047h	System Clock Control Register 1	CM1	0010 0000b
040048h	Processor Mode Register 3	PM3	00h
040049h			
04004Ah	Protect Register	PRCR	XXXX X000b
04004Bh			
04004Ch	Protect Register 3	PRCR3	0000 0000b
04004Dh	Oscillator Stop Detection Register	CM2	00h
04004Eh			
04004Fh			
040050h			
040051h			
040052h			
040053h	Processor Mode Register 2	PM2	00h
040054h	Chip Select Output Pin Setting Register 0	CSOP0	1000 XXXXb
040055h	Chip Select Output Pin Setting Register 1	CSOP1	01X0 XXXXb
040056h			
040057h			
040058h			
040059h			
04005Ah	Low Speed Mode Clock Control Register	CM3	XXXX XX00b
04005Bh			
04005Ch			
04005Dh			
04005Eh			
04005Fh			
040060h	Voltage Regulator Control Register	VRCR	0000 0000b
040061h			
040062h	Low Voltage Detector Control Register	LVDC	0000 XX00b
040063h			
040064h	Detection Voltage Configuration Register	DVCR	0000 XXXXb
040065h			
040066h			
040067h			
040068h to 040093h			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The value in the PM0 register remains unchanged even after a software reset or watchdog timer reset.

Table 4.20 SFR List (20)

Address	Register	Symbol	Reset Value
040094h			
040095h			
040096h			
040097h	Three-phase Output Buffer Control Register	IOBC	0XXX XXXXb
040098h	Input Function Select Register 0	IFS0	X000 0000b (1)
040099h			
04009Ah	Input Function Select Register 2	IFS2	0000 00X0b (2)
04009Bh	Input Function Select Register 3	IFS3	XXXX XX00b
04009Ch			
04009Dh			
04009Eh			
04009Fh	Input Function Select Register 7 (3)	IFS7	XXXX XX0Xb
0400A0h	Port P0_0 Function Select Register	P0_0S	0XXX X000b
0400A1h	Port P1_0 Function Select Register	P1_0S	XXXX X000b
0400A2h	Port P0_1 Function Select Register	P0_1S	0XXX X000b
0400A3h	Port P1_1 Function Select Register	P1_1S	XXXX X000b
0400A4h	Port P0_2 Function Select Register	P0_2S	0XXX X000b
0400A5h	Port P1_2 Function Select Register	P1_2S	XXXX X000b
0400A6h	Port P0_3 Function Select Register	P0_3S	0XXX X000b
0400A7h	Port P1_3 Function Select Register	P1_3S	XXXX X000b
0400A8h	Port P0_4 Function Select Register	P0_4S	0XXX X000b
0400A9h	Port P1_4 Function Select Register	P1_4S	XXXX X000b
0400AAh	Port P0_5 Function Select Register	P0_5S	0XXX X000b
0400ABh	Port P1_5 Function Select Register	P1_5S	XXXX X000b
0400ACh	Port P0_6 Function Select Register	P0_6S	0XXX X000b
0400ADh	Port P1_6 Function Select Register	P1_6S	XXXX X000b
0400AEh	Port P0_7 Function Select Register	P0_7S	0XXX X000b
0400AFh	Port P1_7 Function Select Register	P1_7S	XXXX X000b
0400B0h	Port P2_0 Function Select Register	P2_0S	0XXX X000b
0400B1h	Port P3_0 Function Select Register	P3_0S	XXXX X000b
0400B2h	Port P2_1 Function Select Register	P2_1S	0XXX X000b
0400B3h	Port P3_1 Function Select Register	P3_1S	XXXX X000b
0400B4h	Port P2_2 Function Select Register	P2_2S	0XXX X000b
0400B5h	Port P3_2 Function Select Register	P3_2S	XXXX X000b
0400B6h	Port P2_3 Function Select Register	P2_3S	0XXX X000b
0400B7h	Port P3_3 Function Select Register	P3_3S	XXXX X000b
0400B8h	Port P2_4 Function Select Register	P2_4S	0XXX X000b
0400B9h	Port P3_4 Function Select Register	P3_4S	XXXX X000b
0400BAh	Port P2_5 Function Select Register	P2_5S	0XXX X000b
0400BBh	Port P3_5 Function Select Register	P3_5S	XXXX X000b
0400BCh	Port P2_6 Function Select Register	P2_6S	0XXX X000b
0400BDh	Port P3_6 Function Select Register	P3_6S	XXXX X000b
0400BEh	Port P2_7 Function Select Register	P2_7S	0XXX X000b
0400BFh	Port P3_7 Function Select Register	P3_7S	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Notes:
1. The reset value is 0000 0000b in the 80-/64-pin package.
2. The reset value is 0000 000Xb in the 80-/64-pin package.
3. This register is provided for the 80-64/pin package. No access is allowed in the 100-pin package.

Table 4.21 SFR List (21)

Address	Register	Symbol	Reset Value
0400C0h	Port P4_0 Function Select Register	P4_0S	XXXX X000b
0400C1h	Port P5_0 Function Select Register	P5_0S	XXXX X000b
0400C2h	Port P4_1 Function Select Register	P4_1S	XXXX X000b
0400C3h	Port P5_1 Function Select Register	P5_1S	XXXX X000b
0400C4h	Port P4_2 Function Select Register	P4_2S	XXXX X000b
0400C5h	Port P5_2 Function Select Register	P5_2S	XXXX X000b
0400C6h	Port P4_3 Function Select Register	P4_3S	XXXX X000b
0400C7h	Port P5_3 Function Select Register	P5_3S	XXXX X000b
0400C8h	Port P4_4 Function Select Register	P4_4S	XXXX X000b
0400C9h	Port P5_4 Function Select Register	P5_4S	XXXX X000b
0400CAh	Port P4_5 Function Select Register	P4_5S	XXXX X000b
0400CBh	Port P5_5 Function Select Register	P5_5S	XXXX X000b
0400CCh	Port P4_6 Function Select Register	P4_6S	XXXX X000b
0400CDh	Port P5_6 Function Select Register	P5_6S	XXXX X000b
0400CEh	Port P4_7 Function Select Register	P4_7S	XXXX X000b
0400CFh	Port P5_7 Function Select Register	P5_7S	XXXX X000b
0400D0h	Port P6_0 Function Select Register	P6_0S	XXXX X000b
0400D1h	Port P7_0 Function Select Register	P7_0S	XXXX X000b
0400D2h	Port P6_1 Function Select Register	P6_1S	XXXX X000b
0400D3h	Port P7_1 Function Select Register	P7_1S	XXXX X000b
0400D4h	Port P6_2 Function Select Register	P6_2S	XXXX X000b
0400D5h	Port P7_2 Function Select Register	P7_2S	XXXX X000b
0400D6h	Port P6_3 Function Select Register	P6_3S	XXXX X000b
0400D7h	Port P7_3 Function Select Register	P7_3S	XXXX X000b
0400D8h	Port P6_4 Function Select Register	P6_4S	XXXX X000b
0400D9h	Port P7_4 Function Select Register	P7_4S	XXXX X000b
0400DAh	Port P6_5 Function Select Register	P6_5S	XXXX X000b
0400DBh	Port P7_5 Function Select Register	P7_5S	XXXX X000b
0400DCh	Port P6_6 Function Select Register	P6_6S	XXXX X000b
0400DDh	Port P7_6 Function Select Register	P7_6S	XXXX X000b
0400DEh	Port P6_7 Function Select Register	P6_7S	XXXX X000b
0400DFh	Port P7_7 Function Select Register	P7_7S	XXXX X000b
0400E0h	Port P8_0 Function Select Register	P8_0S	XXXX X000b
0400E1h			
0400E2h	Port P8_1 Function Select Register	P8_1S	XXXX X000b
0400E3h			
0400E4h	Port P8_2 Function Select Register	P8_2S	XXXX X000b
0400E5h			
0400E6h	Port P8_3 Function Select Register	P8_3S	XXXX X000b
0400E7h	Port P9_3 Function Select Register	P9_3S	0XXX X000b
0400E8h	Port P8_4 Function Select Register	P8_4S	XXXX X000b
0400E9h	Port P9_4 Function Select Register	P9_4S	0XXX X000b
0400EAh			
0400EBh	Port P9_5 Function Select Register	P9_5S	0XXX X000b
0400ECh	Port P8_6 Function Select Register	P8_6S	XXXX X000b
0400EDh	Port P9_6 Function Select Register	P9_6S	0XXX X000b
0400EEh	Port P8_7 Function Select Register	P8_7S	XXXX X000b
0400EFh	Port P9_7 Function Select Register	P9_7S	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.22 SFR List (22)

Address	Register	Symbol	Reset Value
0400F0h	Port P10_0 Function Select Register	P10_0S	0XXX X000b
0400F1h			
0400F2h	Port P10_1 Function Select Register	P10_1S	0XXX X000b
0400F3h			
0400F4h	Port P10_2 Function Select Register	P10_2S	0XXX X000b
0400F5h			
0400F6h	Port P10_3 Function Select Register	P10_3S	0XXX X000b
0400F7h			
0400F8h	Port P10_4 Function Select Register	P10_4S	0XXX X000b
0400F9h			
0400FAh	Port P10_5 Function Select Register	P10_5S	0XXX X000b
0400FBh			
0400FCh	Port P10_6 Function Select Register	P10_6S	0XXX X000b
0400FDh			
0400FEh	Port P10_7 Function Select Register	P10_7S	0XXX X000b
0400FFh			
040100h			
040101h			
040102h			
040103h			
040104h			
040105h			
040106h			
040107h			
040108h			
040109h			
04010Ah			
04010Bh			
04010Ch			
04010Dh			
04010Eh			
04010Fh			
040110h			
040111h			
040112h			
040113h			
040114h			
040115h			
040116h			
040117h			
040118h			
040119h			
04011Ah			
04011Bh			
04011Ch			
04011Dh			
04011Eh			
04011Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.23 SFR List (23)

Address	Register	Symbol	Reset Value
040120h to 04403Fh			
044040h			
044041h			
044042h			
044043h			
044044h			
044045h			
044046h			
044047h			
044048h			
044049h			
04404Ah			
04404Bh			
04404Ch			
04404Dh			
04404Eh	Watchdog Timer Start Register	WDTS	XXXX XXXXb
04404Fh	Watchdog Timer Control Register	WDC	000X XXXXb
044050h			
044051h			
044052h			
044053h			
044054h			
044055h			
044056h			
044057h			
044058h			
044059h			
04405Ah			
04405Bh			
04405Ch			
04405Dh			
04405Eh			
04405Fh	Protect Register 2	PRCR2	0XXX XXXXb

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.24 SFR List (24)

Address	Register	Symbol	Reset Value
044060h			
044061h			
044062h			
044063h			
044064h			
044065h			
044066h			
044067h			
044068h			
044069h			
04406Ah			
04406Bh			
04406Ch			
04406Dh	External Interrupt Source Select Register 1	IFSR1	X0XX XXXXb
04406Eh			
04406Fh	External Interrupt Source Select Register 0	IFSR0	0000 0000b
044070h	DMA0 Request Source Select Register 2	DM0SL2	XX00 0000b
044071h	DMA1 Request Source Select Register 2	DM1SL2	XX00 0000b
044072h	DMA2 Request Source Select Register 2	DM2SL2	XX00 0000b
044073h	DMA3 Request Source Select Register 2	DM3SL2	XX00 0000b
044074h			
044075h			
044076h			
044077h			
044078h	DMA0 Request Source Select Register	DM0SL	XXX0 0000b
044079h	DMA1 Request Source Select Register	DM1SL	XXX0 0000b
04407Ah	DMA2 Request Source Select Register	DM2SL	XXX0 0000b
04407Bh	DMA3 Request Source Select Register	DM3SL	XXX0 0000b
04407Ch			
04407Dh	Wake-up IPL Setting Register 2	RIPL2	XX0X 0000b
04407Eh			
04407Fh	Wake-up IPL Setting Register 1	RIPL1	XX0X 0000b
044080h			
044081h			
044082h			
044083h			
044084h			
044085h			
044086h			
044087h			
044088h			
044089h			
04408Ah			
04408Bh			
04408Ch			
04408Dh			
04408Eh			
04408Fh			

X: Undefined
Blanks are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings (1)

Symbol	Characteristic		Condition	Value (2)	Unit
V_{CC1}, V_{CC2}	Supply voltage		$V_{CC1} = AV_{CC}$	-0.3 to 6.0	V
V_{CC2}	Supply voltage		—	-0.3 to V_{CC1}	V
AV_{CC}	Analog supply voltage		$V_{CC1} = AV_{CC}$	-0.3 to 6.0	V
V_I	Input voltage	XIN, $\overline{\text{RESET}}$, CNVSS, NSD, V_{REF}, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (3)		-0.3 to V_{CC1} +0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (3)		-0.3 to V_{CC2} +0.3	V
		P7_0, P7_1		-0.3 to 6.0	V
V_O	Output voltage	XOUT, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3)		-0.3 to V_{CC1} +0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (3)		-0.3 to V_{CC2} +0.3	V
		P7_0, P7_1		-0.3 to 6.0	V
P_d	Power consumption		T_a = 25°C	500	mW
—	Operating temperature range			-40 to 85	°C
T_{stg}	Storage temperature range			-65 to 150	°C

Notes:

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The V_{CC2} pin is available in the 100-pin package only. It should be considered as V_{CC1} in the 80-/64-pin package.
3. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, and P9_5 to P9_7 are available in the 100- and 80-pin packages. Ports P4, P5, P9_1, and P9_4 are available in the 100-pin package only.

Table 5.2 Operating Conditions (1) (1)

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Digital supply voltage ($V_{CC1} \geq V_{CC2}$)		3.0	5.0	5.5	V
AV_{CC}	Analog supply voltage			V_{CC1}		V
V_{REF}	Reference voltage		3.0		V_{CC1}	V
V_{SS}	Digital ground voltage			0		V
AV_{SS}	Analog ground voltage			0		V
dV_{CC1}/dt	V_{CC1} ramp up rate (V_{CC1} < 2.0 V)		0.05			V/ms
V_{IH}	High level input voltage	P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (4)	0.8 × V_{CC2}		V_{CC2}	V
		XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7 (3), P9_1, P9_3 to P9_7, P10_0 to P10_7 (4)	0.8 × V_{CC1}		V_{CC1}	V
		P7_0, P7_1	0.8 × V_{CC1}		6.0	V
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode) (4)	0.8 × V_{CC2}		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode or microprocessor mode) (4, 5)	0.5 × V_{CC2}		V_{CC2}	V
V_{IL}	Low level input voltage	P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (4)	0		0.2 × V_{CC2}	V
		XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (3), P9_1, P9_3 to P9_7, P10_0 to P10_7 (4)	0		0.2 × V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode) (4)	0		0.2 × V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode or microprocessor mode) (4, 5)	0		0.16 × V_{CC2}	V
T_{opr}	Operating temperature range	Version N	-20		85	°C
		Version D	-40		85	°C

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. The V_{CC2} pin is available in the 100-pin package only. It should be considered as V_{CC1} in the 80-/64-pin package.
3. V_{IH} and V_{IL} for P8_7 are specified for P8_7 as a programmable port. These values are not applicable to P8_7 as XCIN.
4. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, and P9_5 to P9_7 are available in the 100- and 80-pin packages. Ports P4, P5, P9_1, and P9_4 are available in the 100-pin package only.
5. Memory expansion mode and microprocessor mode are available in the 100-pin package only.

Table 5.3 Operating Conditions (2)

(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
C_{VDC}	Decoupling capacitance for voltage regulator	Inter-pin voltage: 1.5 V	2.4		10.0	µF

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. This value should be satisfied with due consideration of every condition as follows: operating temperature, DC bias, aging, etc.

Table 5.4 Operating Conditions (3)

(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	High level peak output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3)			-10.0	mA
$I_{OH(avg)}$	High level average output current (4)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3)			-5.0	mA
$I_{OL(peak)}$	Low level peak output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3)			10.0	mA
$I_{OL(avg)}$	Low level average output current (4)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3)			5.0	mA

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. The following conditions should be satisfied:
   - The sum of $I_{OL(peak)}$ of ports P0, P1, P2, P8_6, P8_7, P9, and P10 is 80 mA or less.
   - The sum of $I_{OL(peak)}$ of ports P3, P4, P5, P6, P7, and P8_0 to P8_4 is 80 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P0, P1, and P2 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P8_6, P8_7, P9, and P10 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P3, P4, and P5 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P6, P7, and P8_0 to P8_4 is -40 mA or less.
3. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, and P9_5 to P9_7 are available in the 100- and 80-pin packages. Ports P4, P5, and P9_4 are available in the 100-pin package only.
4. Average value within 100 ms.

Table 5.5 Operating Conditions (4)

(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock oscillator frequency	4		16	MHz
$f_{(XRef)}$	Reference clock frequency	2		4	MHz
$f_{(PLL)}$	PLL clock oscillator frequency	96		128	MHz
$f_{(Base)}$	Base clock frequency			50	MHz
$t_{c(Base)}$	Base clock cycle time	20			ns
$f_{(CPU)}$	CPU operating frequency			50	MHz
$t_{c(CPU)}$	CPU clock cycle time	20			ns
$f_{(BCLK)}$	Peripheral bus clock operating frequency			25	MHz
$t_{c(BCLK)}$	Peripheral bus clock cycle time	40			ns
$f_{(PER)}$	Peripheral clock source frequency			32	MHz
$f_{(XCIN)}$	Sub clock oscillator frequency		32.768	62.5	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

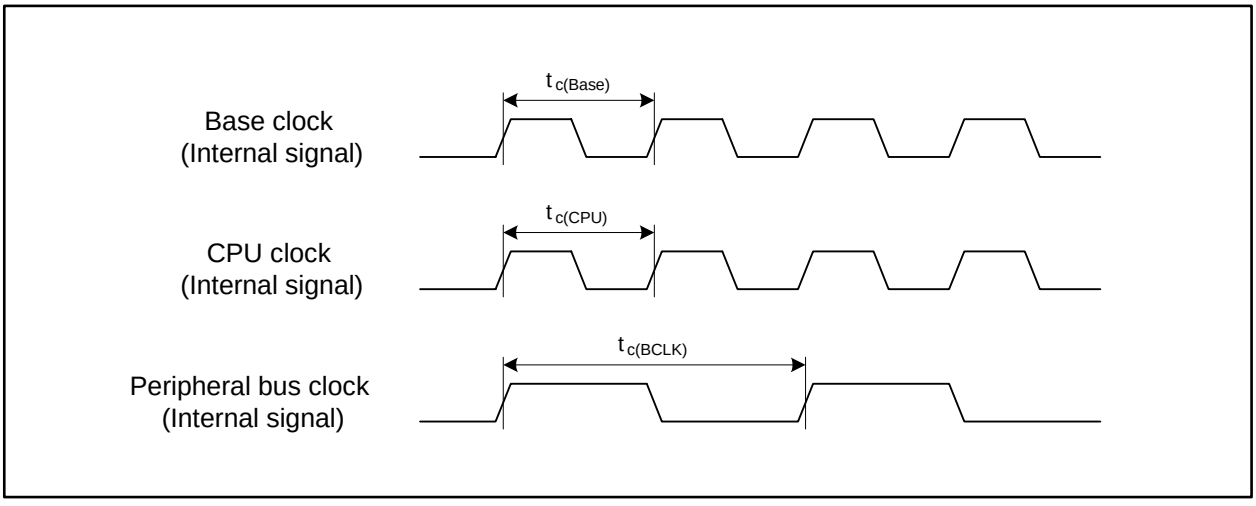


Figure 5.1 Clock Cycle Time

Table 5.6 Operating Conditions (5)
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$V_{r(VCC1)}$	Allowable ripple voltage	V_{CC1} = 5.0 V			0.5	Vp-p
		V_{CC1} = 3.0 V			0.3	Vp-p
$V_{r(VCC2)}$	Allowable ripple voltage	V_{CC2} = 5.0 V			0.5	Vp-p
		V_{CC2} = 3.0 V			0.3	Vp-p
$dV_{r(VCC1)}/dt$	Ripple voltage gradient	V_{CC1} = 5.0 V			±0.3	V/ms
		V_{CC1} = 3.0 V			±0.3	V/ms
$dV_{r(VCC2)}/dt$	Ripple voltage gradient	V_{CC2} = 5.0 V			±0.3	V/ms
		V_{CC2} = 3.0 V			±0.3	V/ms
$f_{r(VCC1)}$	Allowable ripple frequency				10	kHz
$f_{r(VCC2)}$	Allowable ripple frequency				10	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

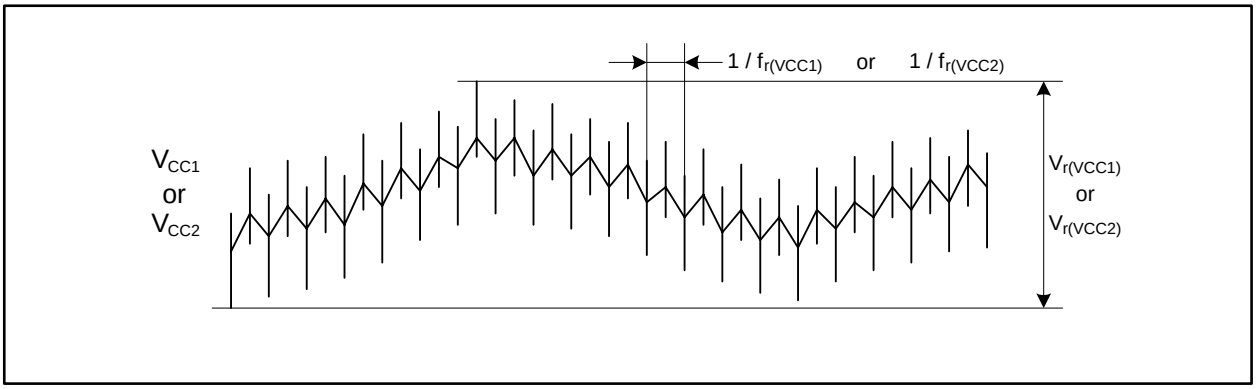


Figure 5.2 Ripple Waveform

Table 5.7 RAM Electrical Characteristics
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
V_{RDR}	RAM data retention voltage (1)	in stop mode	2.0			V

Note:
1. The value listed in the table is the minimum V_{CC1} to retain RAM data.

Table 5.8 Flash Memory Electrical Characteristics
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
—	Programming and erasure endurance of flash memory (1)	Program area	1000			times
		Data area	10000			times
—	4-word program time	Program area		150	900	µs
		Data area		300	1700	µs
—	Lock bit-program time	Program area		70	500	µs
		Data area		140	1000	µs
—	Block erasure time	4 Kbyte block		0.12	3.0	s
		32 Kbyte block		0.17	3.0	s
		64 Kbyte block		0.20	3.0	s
—	Data retention (2)	T_a = 55°C (3)	10			years

Notes:
1. Program/erase definition
   This value represents the number of erasures per block.
   If the flash memory is programmed/erased n times, each block can be erased n times.
   i.e. If 4-word write is performed in 512 different addresses in the block A of 4 Kbyte and then the block is erased, it is considered the programming/erasure is performed just once.
   However a write in the same address more than once for one erasure is disabled. (overwrite disabled).
2. The data retention time includes the periods when the supply voltage is not applied and no clock is provided.
3. Please contact a Renesas sales office regarding data retention time other than the above.

Table 5.9 Power Supply Circuit Timing Characteristics
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply start-up stabilization time after the main power supply is turned on				2	ms

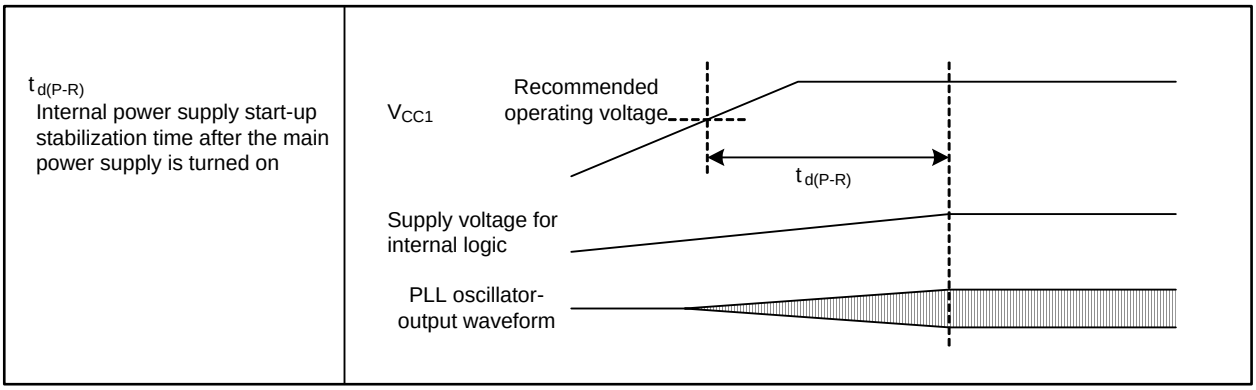


Figure 5.3 Power Supply Circuit Timing

Table 5.10 Electrical Characteristics of Voltage Regulator for Internal Logic
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
V_{VDC1}	Output voltage			1.5		V

Table 5.11 Electrical Characteristics of Low Voltage Detector
(V_{CC1} = V_{CC2} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
ΔVdet	Detected voltage error				±0.3	V
Vdet(R)-Vdet(F)	Hysteresis width		0			V
—	Self-consuming current	V_{CC1} = 5.0 V, low voltage detector enabled		4		μA
$t_{d(E-A)}$	Operation start time of low voltage detector				150	μs

Table 5.12 Electrical Characteristics of Oscillator
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
$f_{SO(PLL)}$	PLL clock self-oscillation frequency		35	55	80	MHz
$t_{LOCK(PLL)}$	PLL lock time (1)				1	ms
$t_{jitter(p-p)}$	PLL jitter period (p-p)				2.0	ns
$f_{(OCO)}$	On-chip oscillator frequency		62.5	125	250	kHz

Note:
1. This value is applicable only when the main clock oscillation is stable.

Table 5.13 Electrical Characteristics of Clock Circuitry
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
$t_{rec(STOP)}$	Recovery time from stop mode (1)				225	µs
$t_{rec(WAIT)}$	Recovery time from wait mode to low power mode				225	µs

Note:
1. This recovery time does not include the period until the main clock oscillator is stabilized. The CPU starts operating before the oscillator is stabilized.

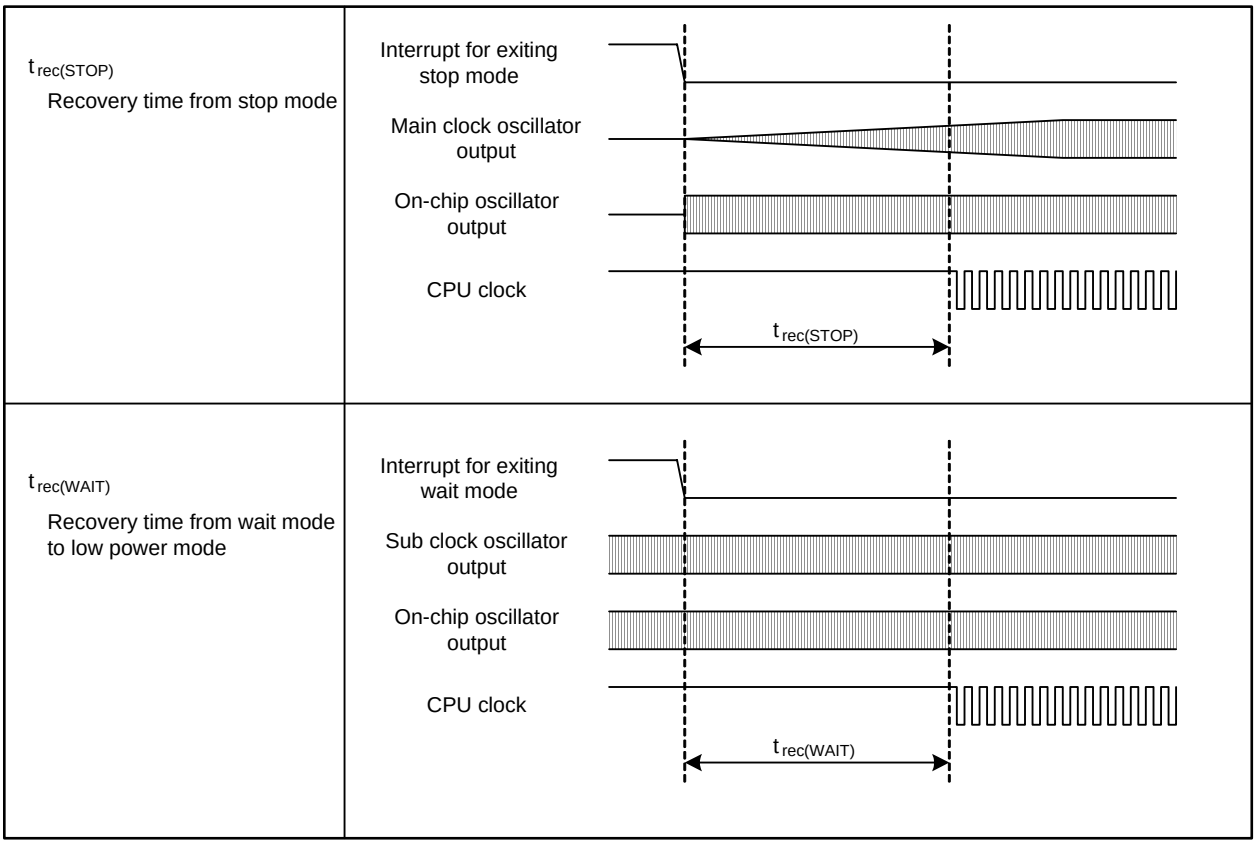


Figure 5.4 Clock Circuit Timing

Timing Requirements (V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.14 Flash Memory CPU Rewrite Mode Timing

Symbol	Characteristics	Value		Unit
		Min.	Max.	
t_{cR}	Read cycle time	200		ns
$t_{su(S-R)}$	Chip-select setup time for read	200		ns
$t_{h(R-S)}$	Chip-select hold time after read	0		ns
$t_{su(A-R)}$	Address setup time for read	200		ns
$t_{h(R-A)}$	Address hold time after read	0		ns
$t_{w(R)}$	Read pulse width	100		ns
t_{cW}	Write cycle time	200		ns
$t_{su(S-W)}$	Chip-select setup time for write	0		ns
$t_{h(W-S)}$	Chip-select hold time after write	30		ns
$t_{su(A-W)}$	Address setup time for write	0		ns
$t_{h(W-A)}$	Address hold time after write	30		ns
$t_{w(W)}$	Write pulse width	50		ns

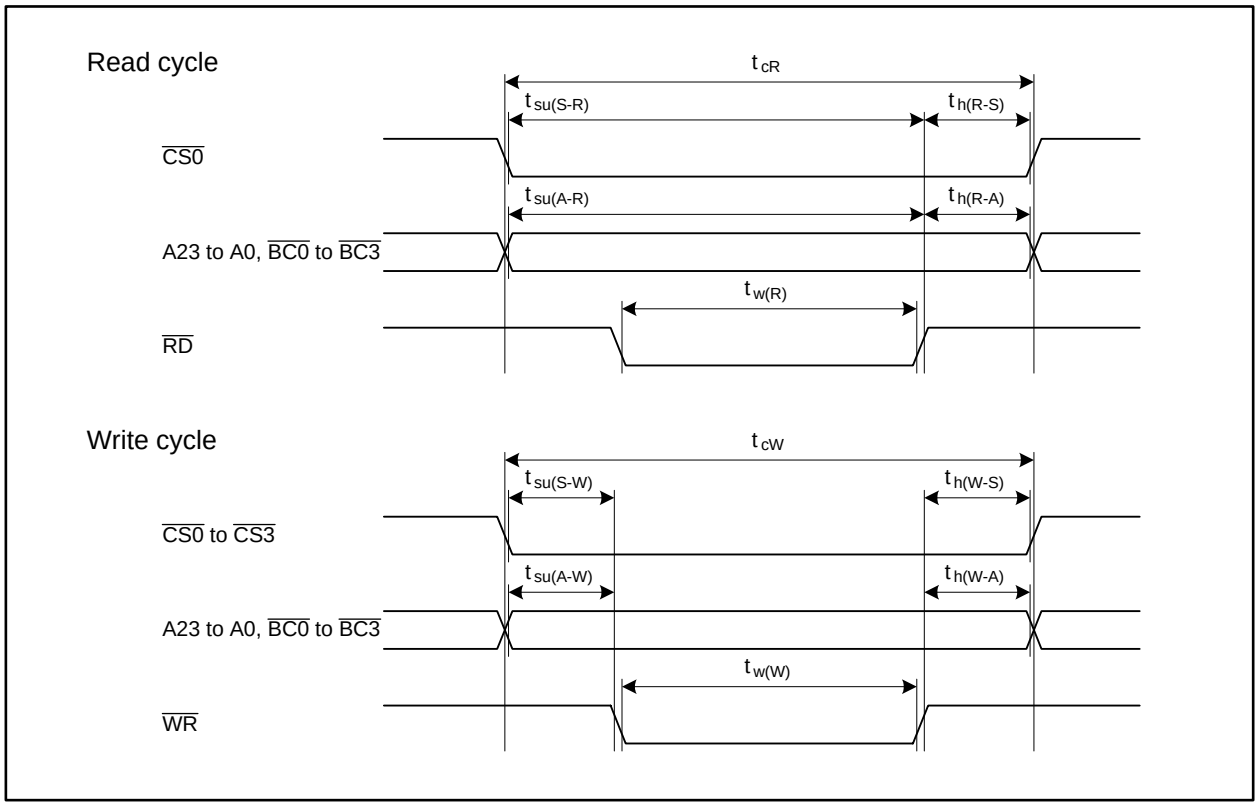


Figure 5.5 Flash Memory CPU Rewrite Mode Timing

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.15 Electrical Characteristics (1)
($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)

Symbol	Characteristic		Measurement condition	Value (2)			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1)	I_{OH} = -5 mA	V_{CC2} -2.0		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OH} = -5 mA	V_{CC1} -2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1)	I_{OH} = -200 µA	V_{CC2} -0.3		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OH} = -200 µA	V_{CC1} -0.3		V_{CC1}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OL} = 200 µA			0.45	V

Notes:
1. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, and P9_5 to P9_7 are available in the 100- and 80-pin packages. Ports P4, P5, and P9_4 are available in the 100-pin package only.
2. The V_{CC2} pin is available in the 100-pin package only. It should be considered as V_{CC1} in the 80-/64-pin package.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.16 Electrical Characteristics (2) ($V_{CC1} = V_{CC2}$ = 4.2 to 5.5 V, V_{SS} = 0 V, $T_a = T_{opr}$, and $f_{(CPU)}$ = 50 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	HOLD, RDY, NMI, INT0 to INT5, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS8, CLK0 to CLK8, RXD0 to RXD8, SCL0 to SCL6, SDA0 to SDA6, SS0 to SS6, SRXD0 to SRXD6, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN(1)		0.2		1.0	V
		RESET		0.2		1.8	V
I_{IH}	High level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	V_I = 5 V			5.0	µA
I_{IL}	Low level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	V_I = 0 V			-5.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistor	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistor	XCIN			15		MΩ

Notes:
1. Pins CLK4, RXD4, TXD4, SDA4, SCL4, STXD4, and SRXD4 are available in the 100- and 80-pin package only. Pins TB4IN, CTS4, RTS4, SS4, UART6, and UART7 are available in the 100-pin package only.
2. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, and P9_5 to P9_7 are available in the 100- and 80-pin packages. Ports P4, P5, P9_1, and P9_4 are available in the 100-pin package only.

$V_{CC1} = V_{CC2} = 5$ V

Table 5.17 Electrical Characteristics (3)
($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement condition		Value			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS} XIN-XOUT Drive power: low XCIN-XCOUT Drive power: low	$f_{(CPU)}$ = 50 MHz, $f_{(BCLK)}$ = 25 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		32	45	mA
			$f_{(CPU)} = f_{SO(PLL)}$/24 MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		10		mA
			$f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		1.2		mA
			$f_{(CPU)} = f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		220		µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		230		µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T_a = 25°C, Wait mode		960	1600	µA
			$f_{(CPU)} = f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T_a = 25°C, Wait mode		8	140	µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T_a = 25°C, Wait mode		10	150	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 25°C		5	70	µA

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.18 A/D Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF}$ = 4.2 to 5.5 V, $V_{SS} = AV_{SS}$ = 0 V, $T_a = T_{opr}$, and $f_{(BCLK)}$ = 25 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC1}$				10	Bits
—	Absolute error	$V_{REF} = V_{CC1} = V_{CC2}$ = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1 (1)			±3	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	$V_{REF} = V_{CC1} = V_{CC2}$ = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1 (1)			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error					±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	$V_{REF} = V_{CC1}$		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		2.06			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.69			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		1.75			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.06			µs
t_{SAMP}	Sample time	ϕ_{AD} = 16 MHz		0.188			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	without sample and hold function		0.25		16	MHz
		with sample and hold function		1		16	MHz

Note:
1. Pins AN0_4 to AN0_7, ANEX0, and ANEX1 are available in the 100- and 80-pin package only.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.19 D/A Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF}$ = 4.2 to 5.5 V, $V_{SS} = AV_{SS}$ = 0 V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	(1)			1.5	mA

Note:

1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for A/D converter is not considered.
   Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.20 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(X)}$	External clock input period	62.5	250	ns
$t_{w(XH)}$	External clock input high level pulse width	25		ns
$t_{w(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_w / t_c	External clock input duty	40	60	%

Table 5.21 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time for read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{c(Base)} + 10$	ns

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.22 Timer A Input (Counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock period	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.23 Timer A Input (Gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock period	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.24 Timer A Input (External trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock period	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.25 Timer A Input (External trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.26 Timer A Input (Increment/decrement count switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock period	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements ($V_{CC1} = V_{CC2}$ = 4.2 to 5.5 V, V_{SS} = 0 V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.27 Timer B Input (Counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock period (one edge counting)	200		ns
$t_{W(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{W(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{C(TB)}$	TBiIN input clock period (both edges counting)	200		ns
$t_{W(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{W(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.28 Timer B Input (Pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock period	400		ns
$t_{W(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{W(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.29 Timer B Input (Pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock period	400		ns
$t_{W(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{W(TBL)}$	TBiIN input low level pulse width	180		ns

$V_{CC1} = V_{CC2} = 5$ V

Timing requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.30 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input clock period	200		ns
$t_{w(CKH)}$	CLKi input high level pulse width	80		ns
$t_{w(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.31 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(ADH)}$	$\overline{\text{ADTRG}}$ input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.32 External Interrupt INTi Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ input high level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)} + 200$		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ input low level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)} + 200$		ns

Table 5.33 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(ISCLK2)}$	ISCLK2 input clock period	600		ns
$t_{w(ISCLK2H)}$	ISCLK2 input high level pulse width	270		ns
$t_{w(ISCLK2L)}$	ISCLK2 input low level pulse width	270		ns
$t_{su(RXD-ISCLK2)}$	ISRXD2 input setup time	150		ns
$t_{h(ISCLK2-RXD)}$	ISRXD2 input hold time	100		ns

$V_{CC1} = V_{CC2} = 5$ V

Switching Characteristics ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.34 External Bus Timing (Separate bus)

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{su(S-R)}$	Chip-select setup time for read	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$t_{c(Base)}$ - 10		ns
$t_{su(A-R)}$	Address setup time for read		(1)		ns
$t_{h(R-A)}$	Address hold time after read		$t_{c(Base)}$ - 10		ns
$t_{W(R)}$	Read pulse width		(1)		ns
$t_{su(S-W)}$	Chip-select setup time for write		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{su(A-W)}$	Address setup time for write		(1)		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{W(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time for write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0		ns

Note:

1. The value is calculated by the following formulas based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For the details of how to set values, refer to the Hardware manual.

   $t_{su(S-R)} = t_{su(A-R)} = Tsu(A-R) \times t_{c(Base)} - 15$ [ns]

   $t_{W(R)} = Tw(R) \times t_{c(Base)} - 10$ [ns]

   $t_{su(S-W)} = t_{su(A-W)} = Tsu(A-W) \times t_{c(Base)} - 15$ [ns]

   $t_{W(W)} = t_{su(D-W)} = Tw(W) \times t_{c(Base)} - 10$ [ns]

$V_{CC1} = V_{CC2} = 5$ V

Switching Characteristics ($V_{CC1} = V_{CC2}$ = 4.2 to 5.5 V, V_{SS} = 0 V, $T_a = T_{opr}$, and unless otherwise noted)

Table 5.35 External Bus Timing (Multiplexed bus)

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time for ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		1.5 × $t_{c(Base)}$ - 10		ns
$t_{su(A-ALE)}$	Address setup time for ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		0.5 × $t_{c(Base)}$ - 5		ns
$t_{h(R-A)}$	Address hold time after read		1.5 × $t_{c(Base)}$ - 10		ns
$t_{d(ALE-R)}$	ALE-read delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{d(ALE-W)}$	ALE-write delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time for write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0.5 × $t_{c(Base)}$		ns

Note:

1. The value is calculated by the following formulas based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For the details of how to set values, refer to the Hardware manual.

   $t_{su(S-ALE)} = t_{su(A-ALE)} = t_{w(ALE)} = (Tsu(A-R) - 0.5) \times t_{c(Base)} - 15$ [ns]

   $t_{w(R)} = Tw(R) \times t_{c(Base)} - 10$ [ns]

   $t_{w(W)} = t_{su(D-W)} = Tw(W) \times t_{c(Base)} - 10$ [ns]

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics ($V_{CC1} = V_{CC2}$ = 4.2 to 5.5 V, V_{SS} = 0 V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.36 Serial Interface

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.37 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{d(ISCLK2-TXD)}$	ISTXD2 output delay time		180	ns
$t_{h(ISCLK2-RXD)}$	ISTXD2 output hold time	0		ns

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.38 Electrical Characteristics (1) ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)

Symbol	Characteristic		Measurement condition	Value (2)			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1)	I_{OH} = -1 mA	V_{CC2} - 0.6		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OH} = -1 mA	V_{CC1} - 0.6		V_{CC1}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OL} = 1 mA			0.5	V

Notes:
1. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, and P9_5 to P9_7 are available in the 100- and 80-pin packages. Ports P4, P5, and P9_4 are available in the 100-pin package only.
2. The V_{CC2} pin is available in the 100-pin package only. It should be considered as V_{CC1} in the 80-/64-pin package.

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.39 Electrical Characteristics (2) ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)

Symbol	Characteristic		Measurement condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $\overline{NMI}$, $\overline{INT0}$ to $\overline{INT5}$, $\overline{KI0}$ to $\overline{KI3}$, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, $\overline{CTS0}$ to $\overline{CTS8}$, CLK0 to CLK8, RXD0 to RXD8, SCL0 to SCL6, SDA0 to SDA6, $\overline{SS0}$ to $\overline{SS6}$, SRXD0 to SRXD6, $\overline{ADTRG}$, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN(1)		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	High level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 3.3$ V			4.0	µA
I_{IL}	Low level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 0$ V			-4.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 0$ V	50	100	500	kΩ
R_{fXIN}	Feedback resistor	XIN			3		MΩ
R_{fXCIN}	Feedback resistor	XCIN			25		MΩ

Notes:
1. Pins CLK4, RXD4, TXD4, SDA4, SCL4, STXD4, and SRXD4 are available in the 100- and 80-pin package only. Pins TB4IN, $\overline{CTS4}$, $\overline{RTS4}$, $\overline{SS4}$, UART6, and UART7 are available in the 100-pin package only.
2. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, and P9_5 to P9_7 are available in the 100- and 80-pin packages. Ports P4, P5, P9_1, and P9_4 are available in the 100-pin package only.

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.40 Electrical Characteristics (3)
($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement condition		Value			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS} XIN-XOUT Drive power: low XCIN-XCOUT Drive power: low	$f_{(CPU)}$ = 50 MHz, $f_{(BCLK)}$ = 25 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		28	40	mA
			$f_{(CPU)} = f_{SO(PLL)}/24$ MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		7		mA
			$f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256$ MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		670		µA
			$f_{(CPU)} = f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		180		µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4$ kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		190		µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256$ MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T_a = 25°C, Wait mode		500	900	µA
			$f_{(CPU)} = f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T_a = 25°C, Wait mode		8	140	µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4$ kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T_a = 25°C, Wait mode		10	150	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 25°C		5	70	µA

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.41 A/D Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF}$ = 3.0 to 3.6 V, $V_{SS} = AV_{SS}$ = 0 V, $T_a = T_{opr}$, and $f_{(BCLK)}$ = 25 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC1}$				10	Bits
—	Absolute error	$V_{REF} = V_{CC1} = V_{CC2}$ = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1 (1)			±5	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	$V_{REF} = V_{CC1} = V_{CC2}$ = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1 (1)			±5	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error	$V_{REF} = V_{CC1} = V_{CC2}$ = 3.3 V				±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	$V_{REF} = V_{CC1}$		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		3.3			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		2.8			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 10 MHz		0.3			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	without sample and hold function		0.25		10	MHz
		with sample and hold function		1		10	MHz

Note:
1. Pins AN0_4 to AN0_7, ANEX0, and ANEX1 are available in the 100- and 80-pin package only.

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.42 D/A Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF}$ = 3.0 to 3.6 V, $V_{SS} = AV_{SS}$ = 0 V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	(1)			1.0	mA

Note:

1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for A/D converter is not considered.
   Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

$V_{CC1} = V_{CC2} = 3.3$ V

Timing Requirements ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.43 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(X)}$	External clock input period	62.5	250	ns
$t_{w(XH)}$	External clock input high level pulse width	25		ns
$t_{w(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_w / t_c	External clock input duty	40	60	%

Table 5.44 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time for read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{c(Base)} + 10$	ns

$V_{CC1} = V_{CC2} = 3.3$ V

Timing Requirements ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.45 Timer A Input (Counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock period	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.46 Timer A Input (Gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock period	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.47 Timer A Input (External trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock period	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.48 Timer A Input (External trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.49 Timer A Input (Increment/decrement count switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock period	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

$V_{CC1} = V_{CC2} = 3.3\ V$

Timing Requirements ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.50 Timer B Input (Counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock period (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock period (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.51 Timer B Input (Pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock period	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.52 Timer B Input (Pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock period	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

$V_{CC1} = V_{CC2} = 3.3$ V

Timing Requirements ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.53 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input clock period	200		ns
$t_{w(CKH)}$	CLKi input high level pulse width	80		ns
$t_{w(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.54 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(ADH)}$	$\overline{\text{ADTRG}}$ input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.55 External Interrupt INTi Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ input high level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)} + 200$		ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input low level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)} + 200$		ns

Table 5.56 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(ISCLK2)}$	ISCLK2 input clock period	600		ns
$t_{W(ISCLK2H)}$	ISCLK2 input high level pulse width	270		ns
$t_{W(ISCLK2L)}$	ISCLK2 input low level pulse width	270		ns
$t_{su(RXD-ISCLK2)}$	ISRXD2 input setup time	150		ns
$t_{h(ISCLK2-RXD)}$	ISRXD2 input hold time	100		ns

$V_{CC1} = V_{CC2} = 3.3$ V

Switching Characteristics ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.57 External Bus Timing (Separate bus)

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{su(S-R)}$	Chip-select setup time for read	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$t_{c(Base)}$ - 10		ns
$t_{su(A-R)}$	Address setup time for read		(1)		ns
$t_{h(R-A)}$	Address hold time after read		$t_{c(Base)}$ - 10		ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{su(S-W)}$	Chip-select setup time for write		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{su(A-W)}$	Address setup time for write		(1)		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time for write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0		ns

Note:

1. The value is calculated by the following formulas based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For the details of how to set values, refer to the Hardware manual.

   $t_{su(S-R)} = t_{su(A-R)} = Tsu(A-R) \times t_{c(Base)} - 15$ [ns]

   $t_{w(R)} = Tw(R) \times t_{c(Base)} - 10$ [ns]

   $t_{su(S-W)} = t_{su(A-W)} = Tsu(A-W) \times t_{c(Base)} - 15$ [ns]

   $t_{w(W)} = t_{su(D-W)} = Tw(W) \times t_{c(Base)} - 10$ [ns]

$V_{CC1} = V_{CC2} = 3.3$ V

Switching Characteristics ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.58 External Bus Timing (Multiplexed bus)

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time for ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$1.5 \times t_{c(Base)} - 10$		ns
$t_{su(A-ALE)}$	Address setup time for ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		$0.5 \times t_{c(Base)} - 5$		ns
$t_{h(R-A)}$	Address hold time after read		$1.5 \times t_{c(Base)} - 10$		ns
$t_{d(ALE-R)}$	ALE-read delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{W(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		$1.5 \times t_{c(Base)} - 10$		ns
$t_{h(W-A)}$	Address hold time after write		$1.5 \times t_{c(Base)} - 10$		ns
$t_{d(ALE-W)}$	ALE-write delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time for write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		$0.5 \times t_{c(Base)}$		ns

Note:

1. The value is calculated by the following formulas based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For the details of how to set values, refer to the Hardware manual.

   $t_{su(S-ALE)} = t_{su(A-ALE)} = t_{w(ALE)} = (Tsu(A-R) - 0.5) \times t_{c(Base)} - 15$ [ns]

   $t_{w(R)} = Tw(R) \times t_{c(Base)} - 10$ [ns]

   $t_{w(W)} = t_{su(D-W)} = Tw(W) \times t_{c(Base)} - 10$ [ns]

$V_{CC1} = V_{CC2} = 3.3$ V

Switching Characteristics ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.59 Serial Interface

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.60 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{d(ISCLK2-TXD)}$	ISTXD2 output delay time		180	ns
$t_{h(ISCLK2-RXD)}$	ISTXD2 output hold time	0		ns

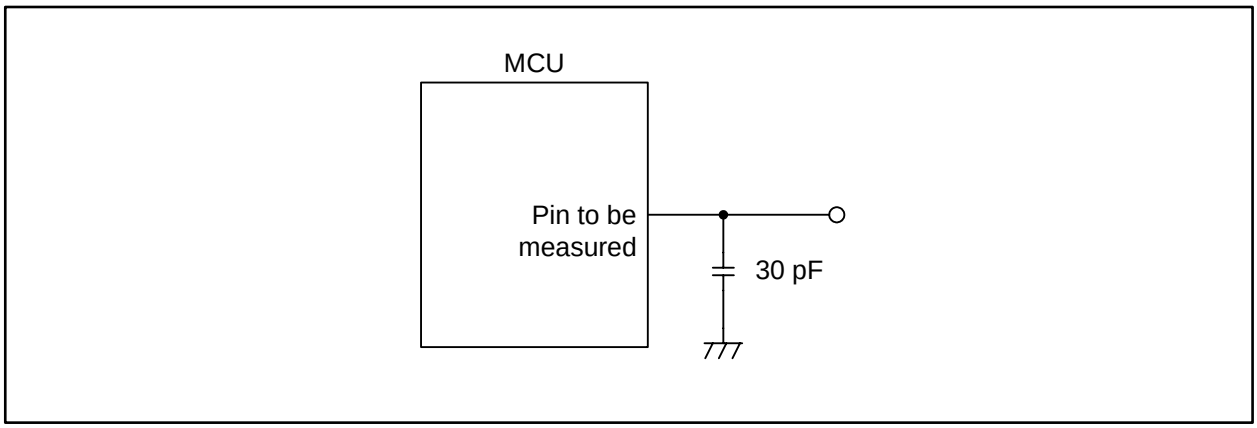


Figure 5.6 Switching Characteristic Measurement Circuit

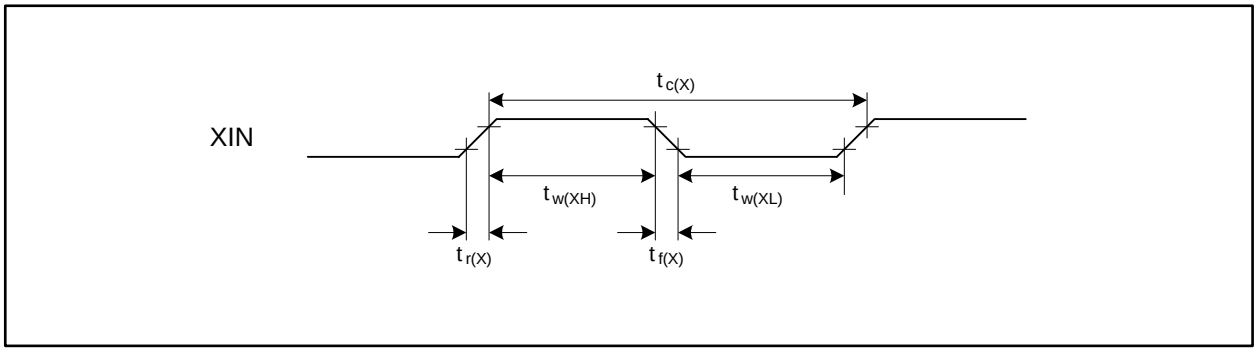
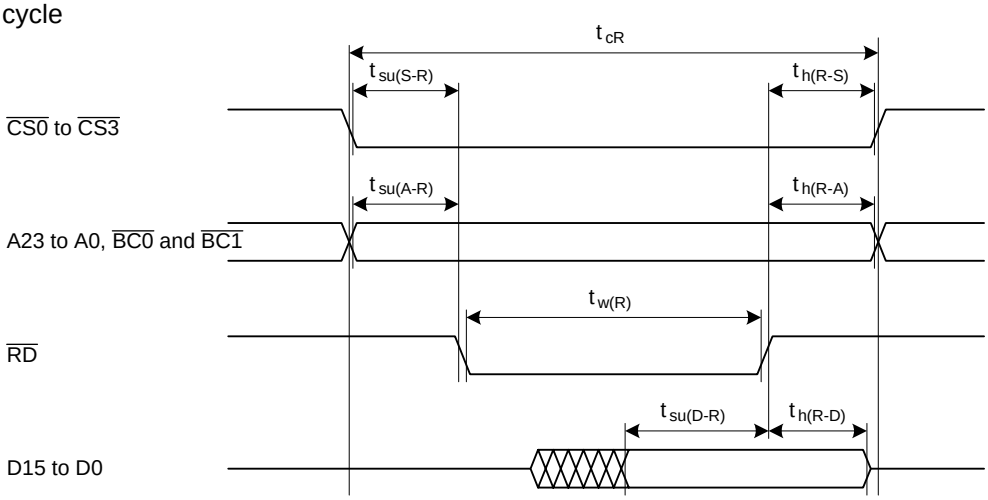


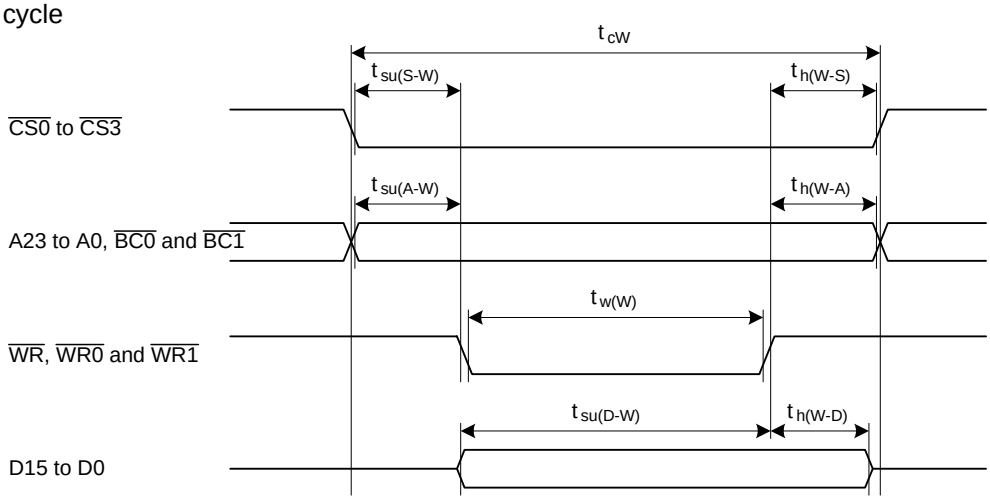
Figure 5.7 External Clock Input Timing

External bus timing (Separate bus)

Read cycle



Write cycle



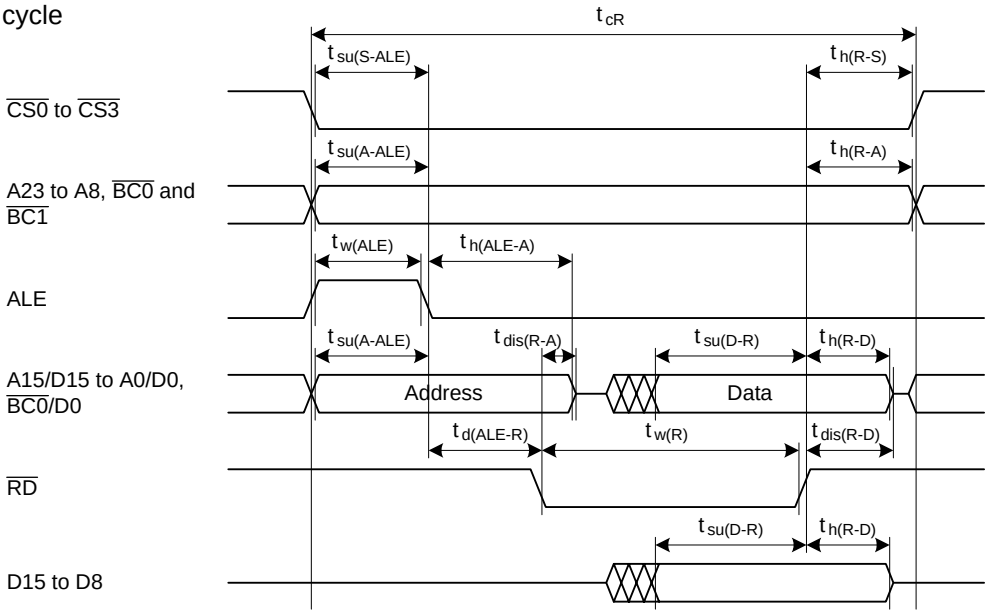
Measurement conditions

Item		$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V	$V_{CC1} = V_{CC2} = 3.0$ to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

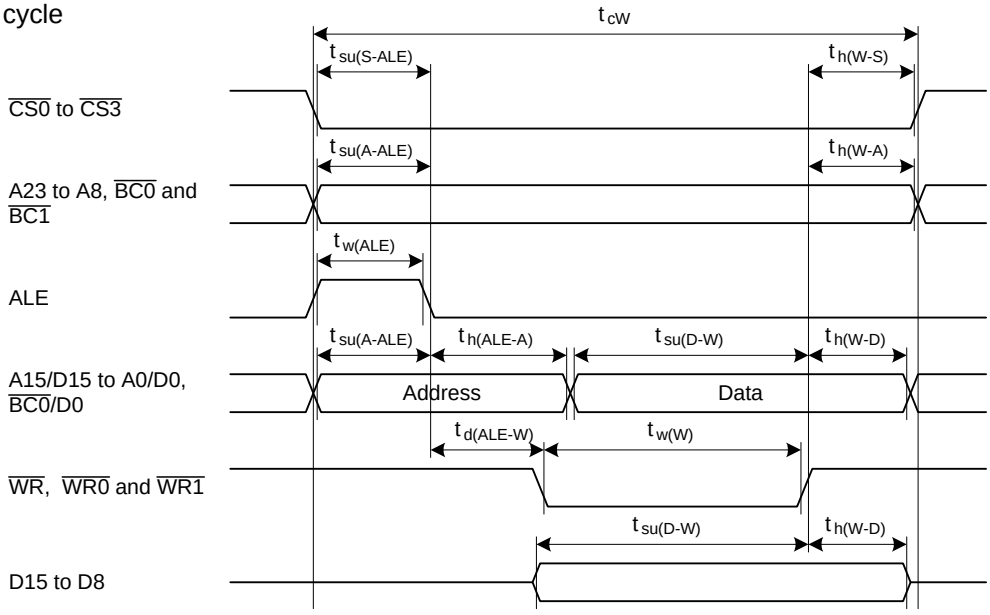
Figure 5.8 External Bus Timing (Separate Bus)

External bus timing (Multiplexed bus)

Read cycle



Write cycle



Measurement conditions

Item		V_{CC1} = V_{CC2} = 4.2 to 5.5 V	V_{CC1} = V_{CC2} = 3.0 to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.9 External Bus Timing (Multiplexed Bus)

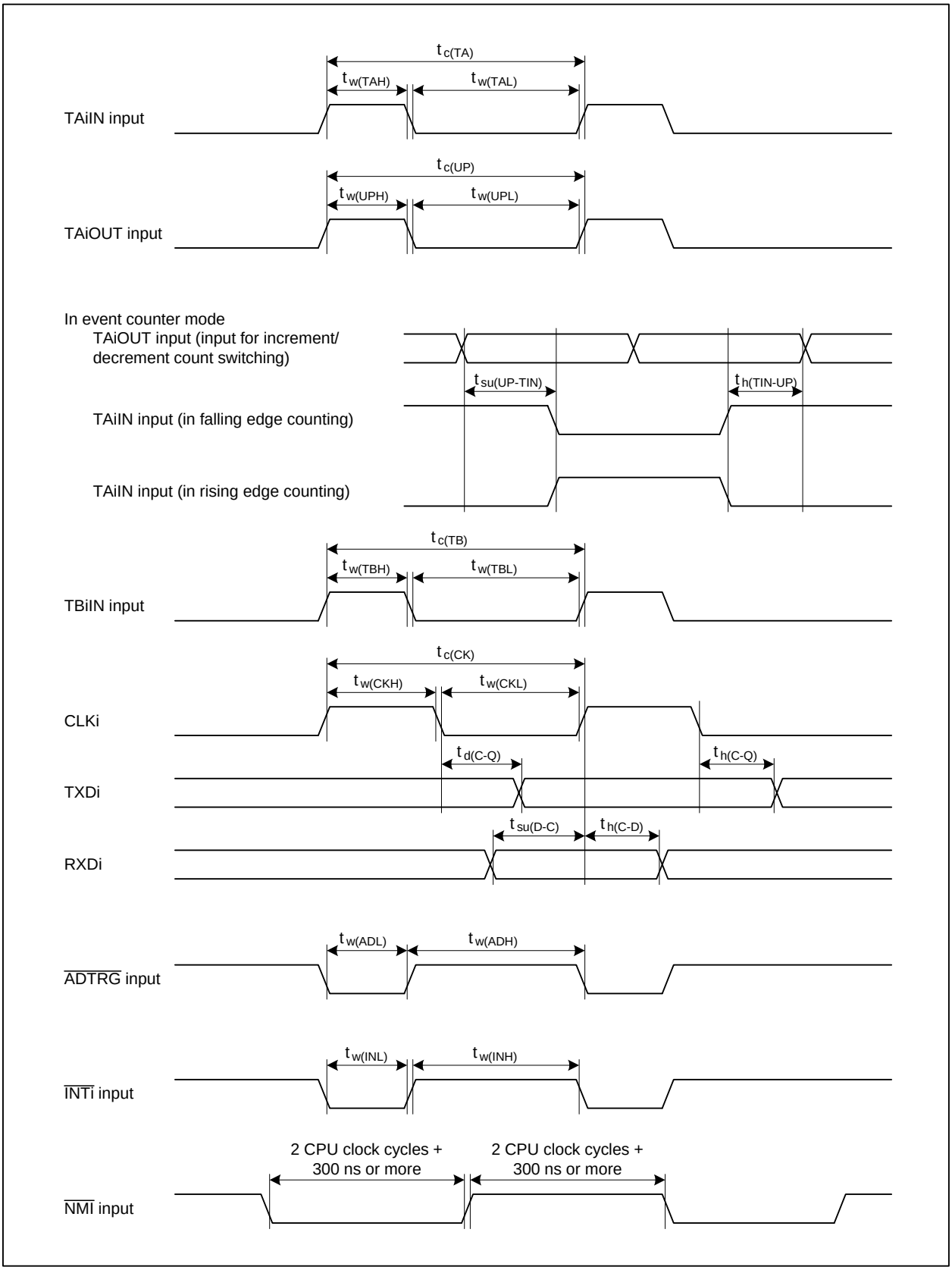
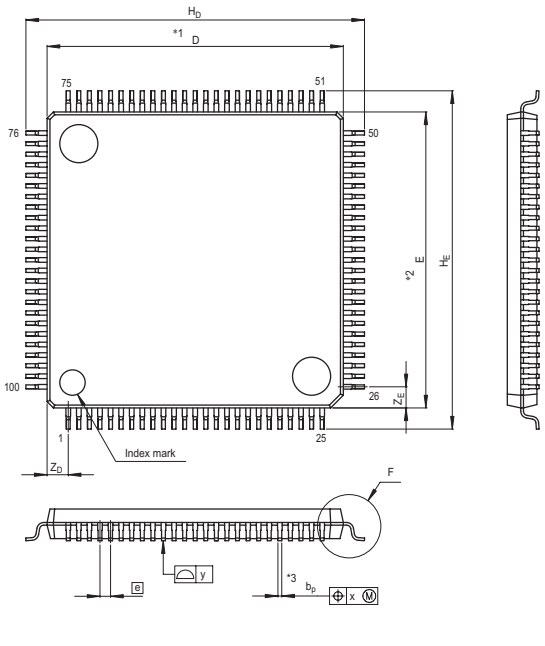


Figure 5.10 Timing of Peripheral Functions

Appendix 1. Package Dimensions

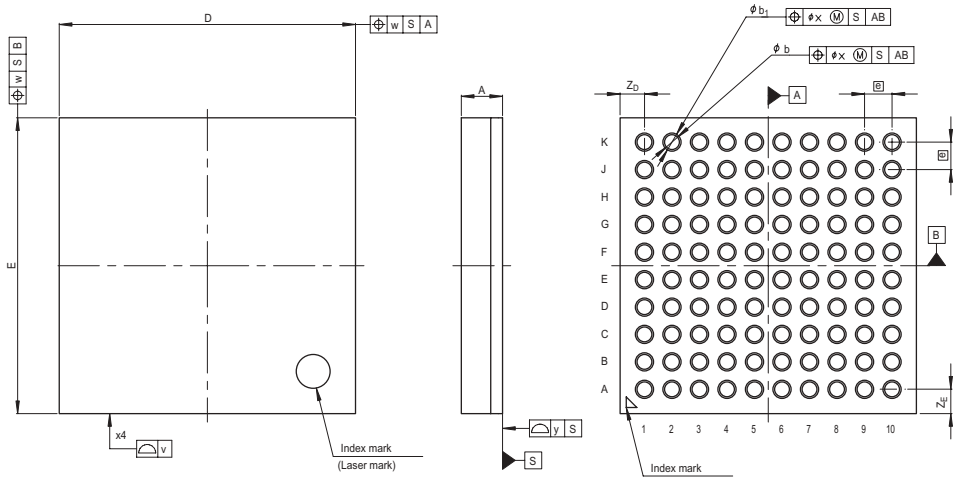
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

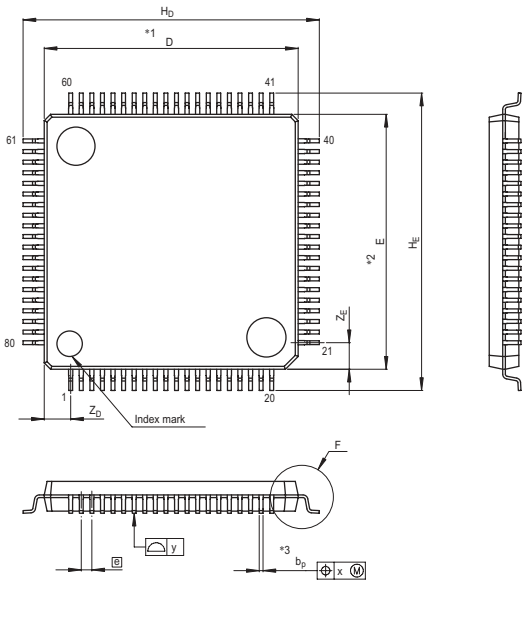
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

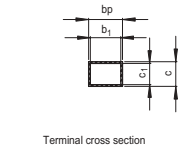
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-5.5x5.5-0.5	PTLG0100KA-A	100F0M	0.1g

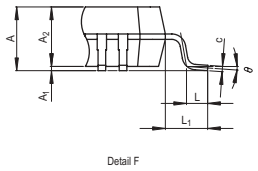


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.5	—
E	—	5.5	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.5	—
Z_E	—	0.5	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



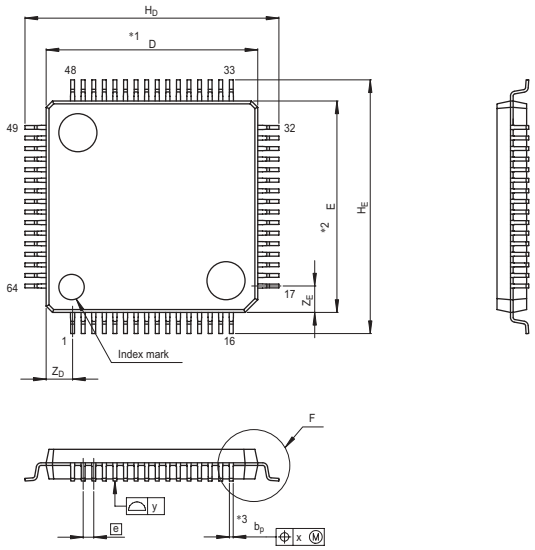


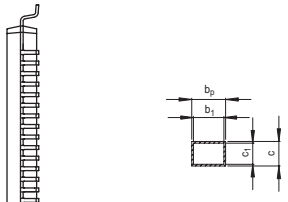


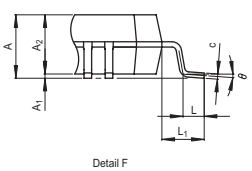
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY — R32C/111 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.03	Oct 17, 2007	—	Initial release
0.30	Aug 19, 2008	—	Second edition released
		—	The manual in general • Maximum operating frequency changed from 48 MHz to 50 MHz • Specification of on-chip oscillator disclosed • Microprocessor mode becomes optional • “memory-expanded mode” changed to “memory expansion mode”
			Chapter 1
		1	• “(MCUs)” added to line 1 of **1.1** • Applications in **1.1.1** revised and modified • “Attention Users” below **1.1.1** modified to “Notes to users”; “The specification” in this box changed to “Specifications”
		2	• “instructions” in “CPU” of **Table 1.1** deleted • Minimum instruction execution time in “CPU” of **Table 1.1** changed • Microprocessor mode in CPU” of **Table 1.1** changed to optional • “TBD” for “Voltage Detection” in **Table 1.1** deleted • “3 circuits” for “Clock” in **Table 1.1** changed to “4 circuits” • “Total interrupt vectors” in **Table 1.1** changed to “Interrupt vectors” • Trigger sources” for DMA in **Table 1.1** modified to “Request sources”; Request sources for “DMA” defined as 51 • Scribal error: “peripheral interrupt sources” for “DMACII” in **Table 1.1** corrected to “peripheral interrupt source”
		3	• Unit names in **Table 1.2** sorted in chapter order • Description for “A/D Converter” in **Table 1.2** changed • “Operating frequency” in **Table 1.2** changed from “48 MHz” to “50 MHz” • “version N” and “version D” added to “Operating Temperature” in **Table 1.2**; “optional” deleted • Values for “Current Consumption” in **Table 1.2** added
		4	• “version N” and “version D” added to **Table 1.3** • All “version N”s in **Table 1.3** become on planning phase
		6	• **Figure 1.2** modified
		7	• Note 2 for **Figure 1.3** modified
		8	• Scribal error: “CLK5/” (pin No. 21) in **Table 1.4** corrected to “CLK5”
		11	• Description for “Connecting pins for decoupling capacitor”, “CNVSS”, and “Debug port” in **Table 1.7** modified
		12	• Some descriptions for “$\overline{WR0}$/$\overline{WR1}$/$\overline{WR}$/$\overline{BC0}$/$\overline{BC1}$/$\overline{RD}$” of “Bus control pins” in **Table 1.8** modified
		13, 14	• Functional category items in **Tables 1.9 and 1.10** sorted in chapter order; Descriptions modified
			Chapter 2
		—	• Descriptions for this chapter modified; Expression “DMAC-related registers”s modified to “DMAC-associated registers”s
		15	• “Data register” and “Address register” in **Figure 2.1** pluralized; Explanation in Notes 1 and 2 for this figure revised

Rev.	Date	Description	
		Page	Summary
		15, 16	• "Interrupt table register" in **Figure 2.1** and **2.1.6** changed to "Interrupt vector table base register"
		18	• Scribal error: "24 bit" in **2.2.2** corrected to "32 bit"
			Chapter 3
		19	• Descriptions for this chapter and **Figure 3.1** modified
			Chapter 4
		20	• "(SFR)" of chapter title changed to "(SFRs)"
			• Description for initial paragraph of **Chapter 4** modified
			• Reset value for CCR and PBC in **Table 4.1** changed
		21, 22	• "UARTi Bus Collision Detection Interrupt Control Register" (i = 0 to 6) in **Tables 4.2 and 4.3** changed to "UARTi Bus Collision, Start/Stop Condition Detection Interrupt Control Register"
			• "DMAi interrupt" in **Tables 4.2 and 4.3** changed to "DMAi transfer complete interrupt"
		22	• Reset value for IIO3IR and IIO8IR to IIO11R in **Table 4.3** modified
		25	• Scribal error: address "00010Fh" added to **Table 4.6**
		32	• "Upward/Downward Counting Select Register" in **Table 4.13** changed to "Increment/Decrement Counting Select Register"
		38	• CSOP2 for address 040056h in **Table 4.19** deleted
			• Reset value for CM3 in **Table 4.19** changed
		43	• "DMAi Source Select Register i" in **Table 4.24** changed to "DMAi Request Source Select Register i"
			Chapter 5
		—	• This chapter newly added
			Appendix 1
		81	• "Package Dimension" as title changed to "Package Dimensions"
1.10	Sep 17, 2009	—	Third edition released
		—	The manual in general • Added 100-pin plastic molded LGA and 80- and 64-pin plastic molded LQFP packages • When new tables/figures are added for 80-/64-pin packages, add the following description: "(for the 100-pin package)" to the title of corresponding current tables/figures
			Chapter 1. Overview
		1	• Added description for 100-pin LGA and 80-/64-pin packages to lines 12 and 13 of **1.1**; Added description "a maximum of" to "nine channels of serial interface"; Deleted the whole description of "Notes to users"
		2	• Changed minimum RAM size "40" in **Table 1.1**, to "32"
			• Modified description for "External Bus Expansion", to **Table 1.1**; Moved this unit below "Clock"
		3	• Added "(optional)" for IEBus mode for "Intelligent I/O" in **Table 1.2**
			• Modified description for "Flash memory" in **Tables 1.2**
			• Added "100-pin plastic molded TFLGA (PTLG0100KA-A)" to **Table 1.2**
		4-7	• Added **Tables 1.3 to 1.6** to provide specifications for 80-/64-pin packages

Rev.	Date	Description	
		Page	Summary
		8	• Completed “under development” phase of part numbers R5F64110DFB, R5F64111DFB, R5F64112DFB, R5F64114DFB, R5F64115DFB, and R5F64116DFB in **Table 1.7** • Added product information for 100-pin LGA and 80-/64-pin packages to **Table 1.7**
		9	• Added product information for 100-pin LGA and 80-/64-pin packages, and 32-Kbyte RAM to **Figure 1.1** • Deleted hyphenation for part number in **Figure 1.1**
		11, 12, 14, 18, 21	• Added **Figures 1.3, 1.4, and 1.6 to 1.8** to provide block diagrams and pin assignment for 100-pin LGA and 80-/64-pin packages
		13	• Changed the order of Notes in **Figures 1.5**
		15-17	• Added pin No. for 100-pin LGA package to **Tables 1.8 to 1.10**
		19, 20, 22, 23	• Added **Tables 1.11 to 1.14** to provide pin characteristics for 80-/64-pin packages.
		24	• Changed the following expression: “A ceramic resonator or a crystal oscillator” for “Main clock input/output” in **Table 1.15**, to “A crystal, or a ceramic resonator”
		25	• Modified descriptions for $\overline{\text{HLDA}}$ and $\overline{\text{RDY}}$ of “Bus control pins” in **Table 1.16**
		26	• Changed the following expression: “selected” for “Input port” in **Table 1.17**, to “selectable” • Modified description “TXD2” for TXD0 to TXD8 of “Serial interface” in **Table 1.17**, to “TXD2 output”
		28-30	• Added **Tables 1.19 to 1.21** to provide pin definitions and functions for 80-/64-pin packages
			Chapter 2. CPU
		—	• Made major text modifications to this chapter
		33	• Changed the following expression: “a requested interrupt’s priority level” in line 2 of **2.1.8.11**, to “the interrupt request level”
			Chapter 3. Memory
		35	• Made major text modifications to this chapter • Changed RAM size “40” in line 7 of this chapter, to “63”, and address “0000A3FFh” in line 8, to “0000FFFFh” • Added descriptions for 32-Kbyte RAM and 128-Kbyte ROM to **Figure 3.1** • Changed two “can be”s in Notes 3 and 4 of **Figure 3.1**, to “becomes”s
			Chapter 4. SFRs
		36	• Changed hexadecimal format of reset values for registers CCR and FMCR in **Table 4.1**, to binary • Added FEBC3 register to addresses 000010h-000011h in **Table 4.1** • Changed FEBC register for addresses 00001Ch-00001Dh, to FEBC0 in **Table 4.1** • Modified the following register name in **Table 4.1**: “Chip-select Boundary (between n and n + 1) Setting Register”, to “Chip-select n and n + 1 Boundary Setting Register”

Rev.	Date	Description	
		Page	Summary
		37, 38	• Changed register names associated with “Start/Stop Condition” for BCNiIC in **Tables 4.2 and 4.3**, to “Start Condition/Stop Condition”
		45	• Modified reset values “XXXX XXXXb” and “XXXX 000Xb” for registers U7RB and U8RB in **Table 4.10**, to “XXXXh”
		46	• Changed expression of register name “Xi Register Yi Register” (i = 0 to 15) and register symbol “XiR, YiR” in **Table 4.11**, to “Xi Register/Yi Register” and “XiR/YiR”, respectively
		51	• Changed hexadecimal format of reset values for PDi in **Table 4.16**, to binary
		54	• Modified Note 1 in **Table 4.19**
		55	• Merged addresses 40090h to 40093h in **Table 4.20**, into previous page • Modified reset values for IFS0 and IFS2 in **Table 4.20**; Added Notes 1 to 3 for 80-/64-pin packages and IFS7 register
		55-57	• Modified the following register name in **Tables 4.20 to 4.22**: “Port Pi_j Port Function Select Register”, to “Port Pi_j Function Select Register”
		59	• Modified register name “DMAi Request Source Select Register 1” in **Table 4.24**, to “DMAi Request Source Select Register” • Changed register names “Wake-up Interrupt Priority Level Control Register 2” and “Wake-up Interrupt Priority Level Control Register 1” in **Table 4.24**, to “Wake-up IPL Setting Register 2” and “Wake-up IPL Setting Register 1”, respectively
			Chapter 5. Electrical Characteristics
		60	• Added Notes 2 and 3 for 80-/64-pin packages to **Table 5.1**
		61	• Added specification of “dV_{CC1}/dt” to **Table 5.2**; Added Notes 2, 4, and 5 for 80-/64-pin packages
		62	• Added Note 2 for **Table 5.3**
		63	• Added Note 3 for 80-/64-pin packages to **Table 5.4**
		65	• Modified description “V_{CC}”s in **Table 5.6**, to “V_{CC1}”s and “V_{CC2}”s
		66	• Added **Table 5.7** to provide RAM electrical characteristics • Deleted specification of “t_{PS}” from **Table 5.8**
		67	• Deleted measurement condition for power supply circuit timing characteristics in **Table 5.9** • Added “Supply voltage for internal logic” to **Figure 5.3** and deleted “CPU clock” from the figure • Changed voltage condition for **Table 5.11**, from “V_{CC1} = V_{CC2} = 3.3 to 5.5 V” to “V_{CC1} = V_{CC2} = 4.2 to 5.5 V”; Clarified maximum value for “ΔVdet” in **Table 5.11**; Modified self-consuming current “V_{CC}”, to “V_{CC1}”
		68	• Changed typical value and maximum value for $f_{SO(PLL)}$ in **Table 5.12**, to “55” and “80” respectively • Changed the following expressions: “PLL frequency synthesizer stabilization time” in **Table 5.12**, to “PLL lock time” and “$t_{OSC(PLL)}$”, to “$t_{LOCK(PLL)}$” • Modified description for Note1 of **Table 5.13**

Rev.	Date	Description	
		Page	Summary
		70, 82	• Added Notes 1 and 2 for 80-/64-pin packages to **Tables 5.15 and 5.38**
		71, 83	• Deleted ports P7_0, P7_1, and P8_5 for R_{PULLUP} from **Tables 5.16 and 5.39**; Added Notes 1 and 2 for 80-/64-pin packages
		72, 84	• Added "XIN" as "Active" to first, third, and sixth rows of **Tables 5.17 and 5.40**
			• Deleted specification of ICC under condition "Ta = 85°C" from **Tables 5.17 and 5.40**
		73, 85	• Modified minimum value "0.125" for ϕ_{AD} in **Tables 5.18 and 5.41**, to "0.25"; Added Note 1 for 80-/64-pin packages
		75, 87	• Clarified three "TBD"s for external bus timing in **Tables 5.21 and 5.44**
		78	• Corrected a typo "$t_{h(C-Q)}$" in **Table 5.30**, to "$t_{h(C-D)}$"
		78, 90	• Modified maximum value for $t_{h(C-D)}$ "30" in **Tables 5.30 and 5.53**, to "80"
			• Modified minimum value for $t_{w(ADH)}$ in **Tables 5.31 and 5.54**, to "$\frac{3}{\phi_{AD}}$"
			• Added **Tables 5.33 and 5.56** to provide intelligent I/O timing requirements
		79, 91	• Changed the third formula of Note 1 in **Tables 5.34 and 5.57**
		80, 92	• Modified minimum value of $t_{h(W-D)}$ "0" in **Tables 5.35 and 5.58**, to "0.5 x $t_{c(Base)}$"; Changed the first formula of Note 1
		81, 93	• Modified "Characteristic" for $t_{h(C-Q)}$ in **Tables 5.36 and 5.59**, from "TXDi hold time" to "TXDi output hold time"
			• Added **Tables 5.37 and 5.60** to provide intelligent switching characteristics
		83	• Changed measurement condition for "High level input current" in **Table 5.39**, from "V_I = 3 V" to "V_I = 3.3 V"
		85	• Added a skipped word "error" after "Differential non-linearity" in **Table 5.41**
		87	• Corrected typos "$t_{w(H)}$," "$t_{w(L)}$", "t_r", and "t_f" in **Table 5.43**, to "$t_{w(XH)}$", "$t_{w(XL)}$", "$t_{r(X)}$", and "$t_{f(X)}$", respectively
		95	• Changed D15 to D0 output period of write cycle in **Figures 5.8**
		96	• Changed D15 to D8 output period of write cycle in **Figures 5.9**
			Appendix 1
		98, 99	• Added figures for 100-pin plastic molded LGA, and 80-/64-pin plastic molded LQFP packages

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