



PIC32MX3XX/4XX Family Data Sheet

**64/100-Pin General Purpose and USB
32-Bit Flash Microcontrollers**

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PIC32MX3XX/4XX

High-Performance 80 MHz MIPS-Based 32-bit Flash Microcontroller 64/100-Pin General Purpose and USB

High-Performance 32-bit RISC CPU:

- MIPS32® M4K™ 32-bit Core with 5-Stage Pipeline
- 80 MHz Maximum Frequency
- 1.56 DMIPS/MHz (Dhrystone 2.1) Performance at 0 Wait State Flash Access
- Single-Cycle Multiply and High-Performance Divide Unit
- MIPS16e™ Mode for Up to 40% Smaller Code Size
- Two Sets of 32 Core Register Files (32-bit) to Reduce Interrupt Latency
- Prefetch Cache Module to Speed Execution from Flash

Microcontroller Features:

- Operating Voltage Range of 2.3V to 3.6V
- 32K to 512K Flash Memory (plus an additional 12KB of Boot Flash)
- 8K to 32K SRAM Memory
- Pin-Compatible with Most PIC24/dsPIC® Devices
- Multiple Power Management Modes
- Multiple Interrupt Vectors with Individually Programmable Priority
- Fail-Safe Clock Monitor Mode
- Configurable Watchdog Timer with On-Chip Low-Power RC Oscillator for Reliable Operation

Peripheral Features:

- Atomic SET, CLEAR and INVERT Operation on Select Peripheral Registers
- Up to 4-Channel Hardware DMA with Automatic Data Size Detection
- USB 2.0 Compliant Full Speed Device and On-The-Go (OTG) Controller
- USB has a Dedicated DMA Channel
- 10 MHz to 40 MHz Crystal Oscillator
- Internal 8 MHz and 32 kHz Oscillators

- Separate PLLs for CPU and USB Clocks
- Two I²C™ Modules
- Two UART Modules with:
 - RS-232, RS-485 and LIN 1.2 support
 - IrDA® with On-Chip Hardware Encoder and Decoder
- Parallel Master and Slave Port (PMP/PSP) with 8-bit and 16-bit Data and Up to 16 Address Lines
- Hardware Real-Time Clock/Calendar (RTCC)
- Five 16-bit Timers/Counters (two 16-bit pairs combine to create two 32-bit timers)
- Five Capture Inputs
- Five Compare/PWM Outputs
- Five External Interrupt Pins
- High-Speed I/O Pins Capable of Toggling at Up to 80 MHz
- High-Current Sink/Source (18 mA/18 mA) on All I/O Pins
- Configurable Open-Drain Output on Digital I/O Pins

Debug Features:

- Two Programming and Debugging Interfaces:
 - 2-Wire Interface with Unintrusive Access and Real-time Data Exchange with Application
 - 4-wire MIPS® Standard Enhanced JTAG interface
- Unintrusive Hardware-Based Instruction Trace
- IEEE Std 1149.2 Compatible (JTAG) Boundary Scan

Analog Features:

- Up to 16-Channel 10-bit Analog-to-Digital Converter:
 - 1000 ksp/s Conversion Rate
 - Conversion Available During Sleep, Idle
- Two Analog Comparators
- 5V Tolerant Input Pins (digital pins only)

PIC32MX3XX/4XX

TABLE 1: PIC32MX GENERAL PURPOSE – FEATURES

GENERAL PURPOSE														
Device	Pins	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	VREG	Trace	EUART/SPI/I ² C™	10-bit A/D (ch)	Comparators	PMP/PSP	JTAG	Packages ⁽²⁾
PIC32MX320F032H	64	40	32 + 12 ⁽¹⁾	8	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes	PT, MR
PIC32MX320F064H	64	80	64 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes	PT, MR
PIC32MX320F128H	64	80	128 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes	PT, MR
PIC32MX340F128H	64	80	128 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes	PT, MR
PIC32MX340F256H	64	80	256 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes	PT, MR
PIC32MX340F512H	64	80	512 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes	PT, MR
PIC32MX320F128L	100	80	128 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes	PT
PIC32MX340F128L	100	80	128 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes	PT
PIC32MX360F256L	100	80	256 + 12 ⁽¹⁾	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes	PT
PIC32MX360F512L	100	80	512 + 12 ⁽¹⁾	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes	PT

Legend: PT = TQFP MR = QFN

Note 1: This device features 12 KB Boot Flash memory.

Note 2: See Legend for an explanation of the acronyms. See **Section 29.0 “Packaging Information”** for details.

TABLE 2: PIC32MX USB – FEATURES

USB															
Device	Pins	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	Dedicated USB DMA Channels	VREG	Trace	EUART/SPI/I ² C™	10-bit A/D (ch)	Comparators	PMP/PSP	JTAG	Packages ⁽²⁾
PIC32MX420F032H	64	80	32 + 12 ⁽¹⁾	8	5/5/5	0	2	Yes	No	2/1/2	16	2	Yes	Yes	PT, MR
PIC32MX440F128H	64	80	128 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes	PT, MR
PIC32MX440F256H	64	80	256 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes	PT, MR
PIC32MX440F512H	64	80	512 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes	PT, MR
PIC32MX440F128L	100	80	128 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	No	2/2/2	16	2	Yes	Yes	PT
PIC32MX460F256L	100	80	256 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	Yes	2/2/2	16	2	Yes	Yes	PT
PIC32MX460F512L	100	80	512 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	Yes	2/2/2	16	2	Yes	Yes	PT

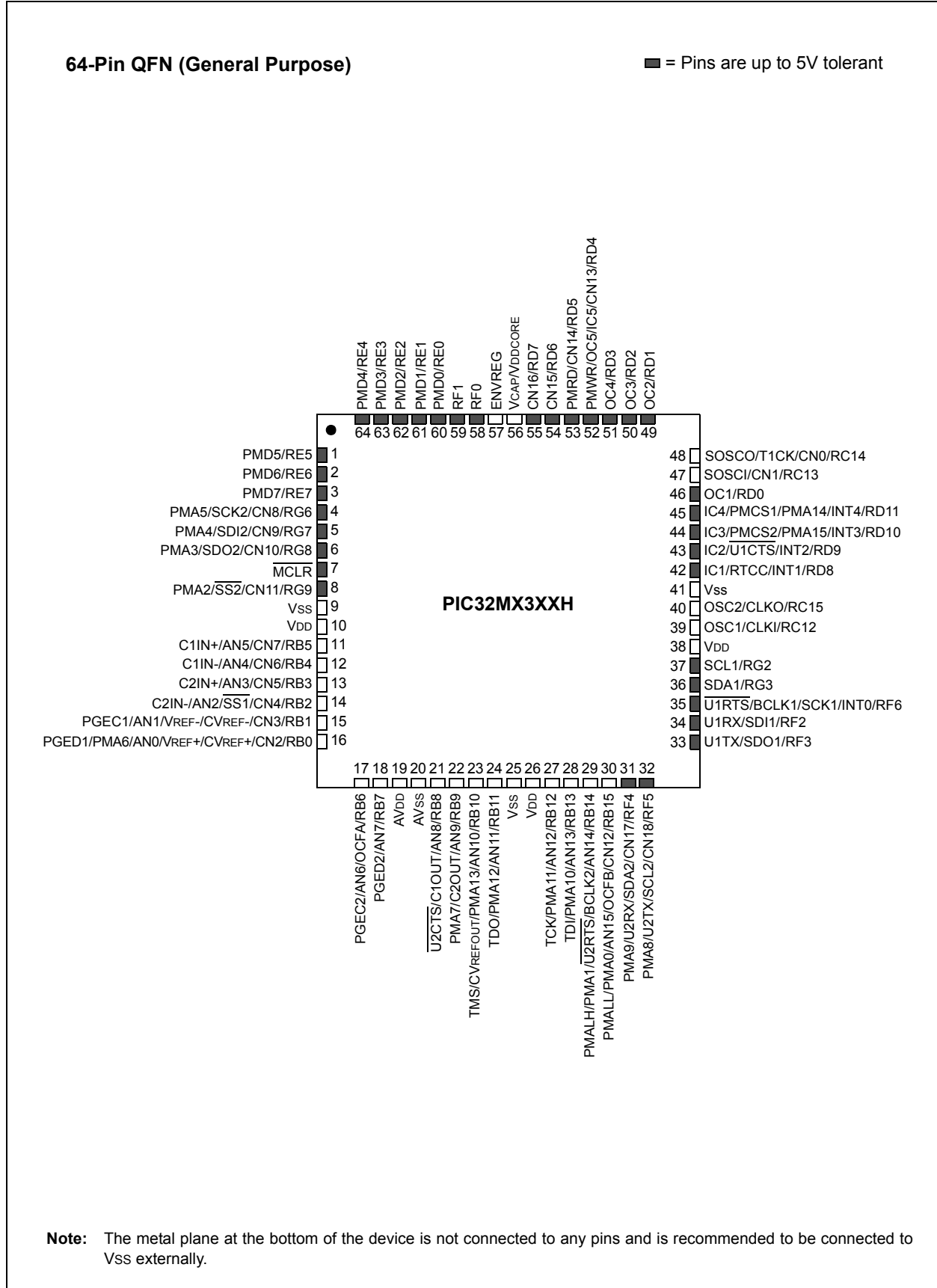
Legend: PT = TQFP MR = QFN

Note 1: This device features 12 KB Boot Flash memory.

Note 2: See Legend for an explanation of the acronyms. See **Section 29.0 “Packaging Information”** for details.

PIC32MX3XX/4XX

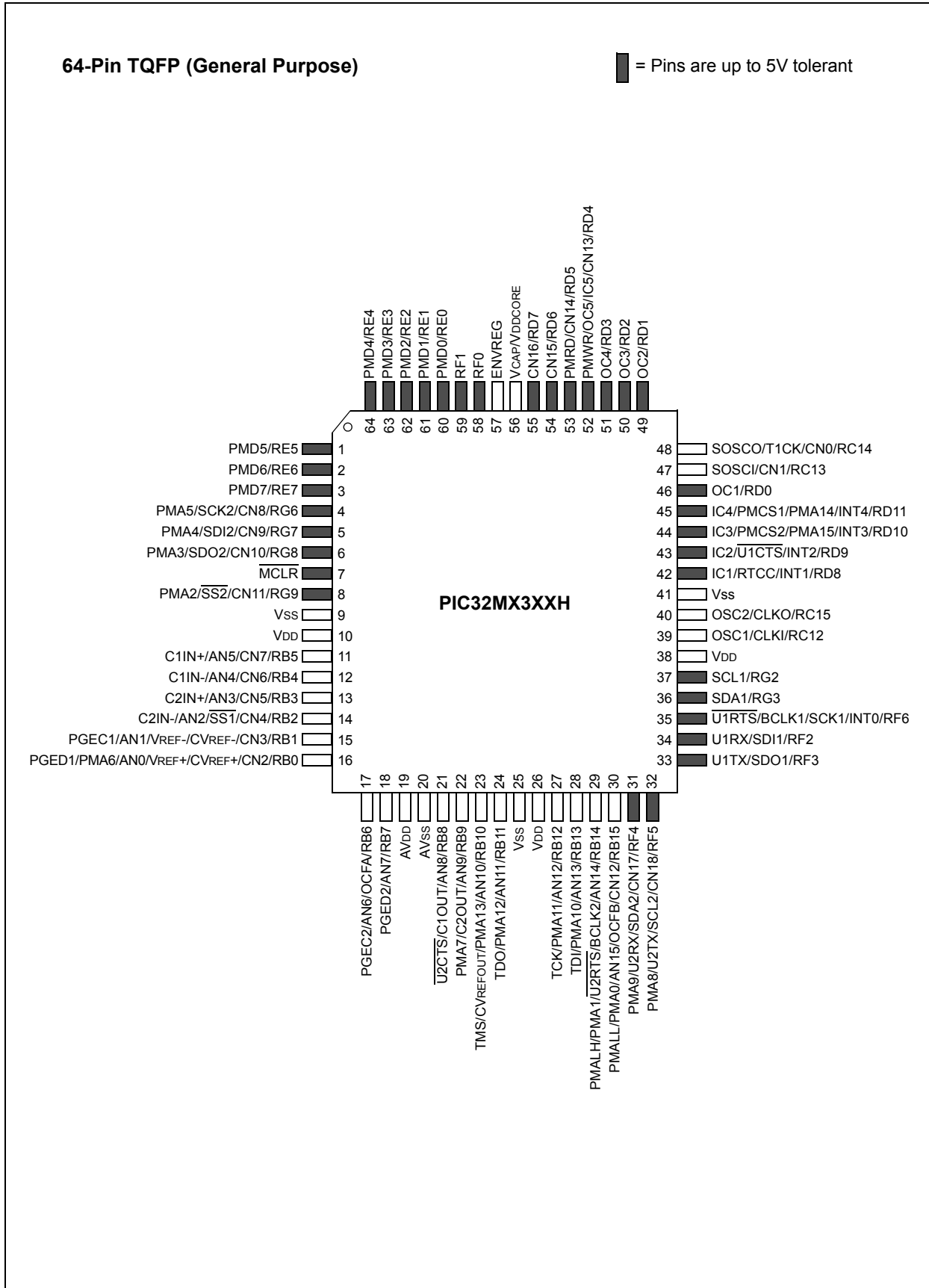
PIN DIAGRAM: 64-PIN QFN – GENERAL PURPOSE



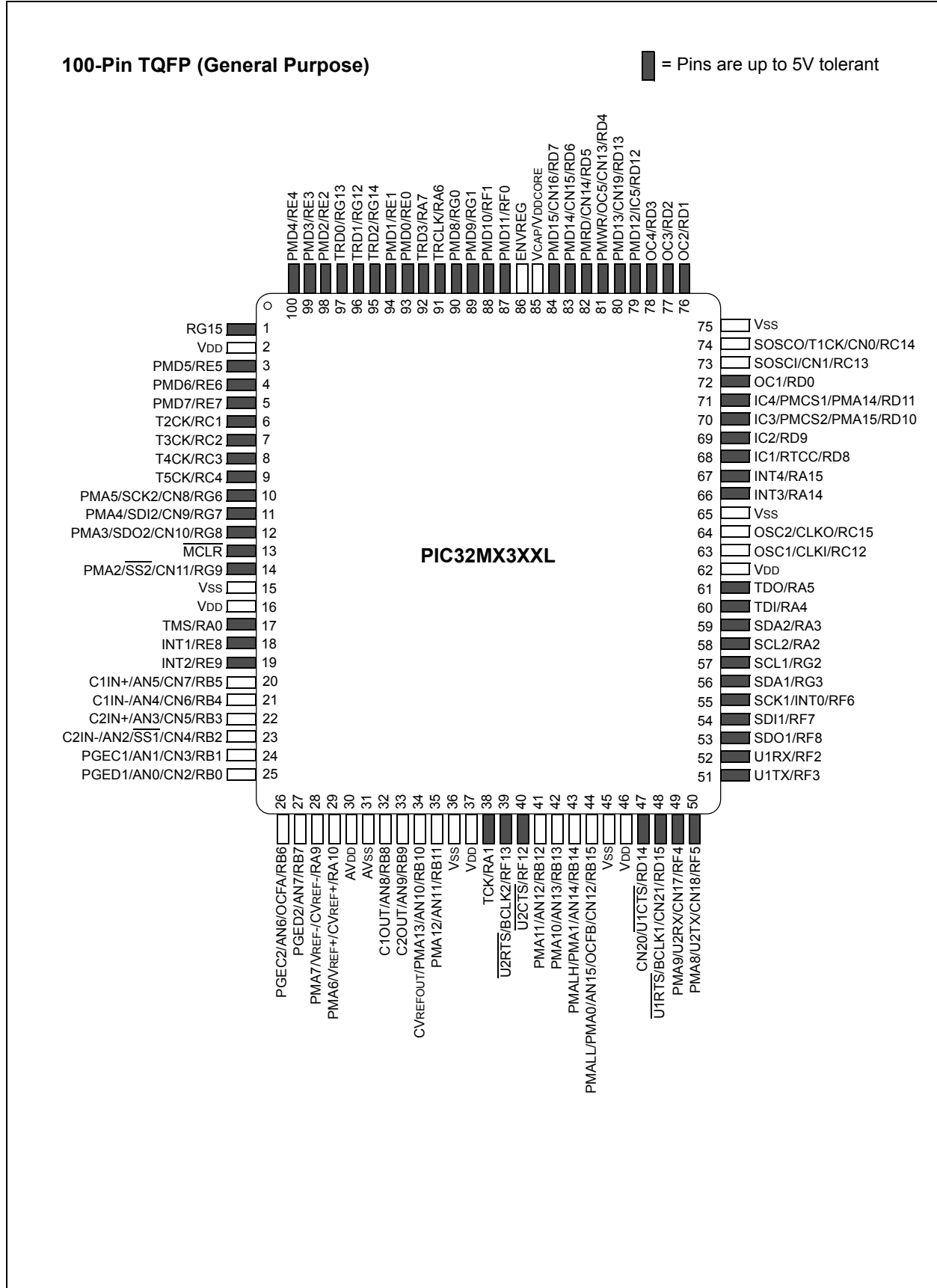
Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

PIC32MX3XX/4XX

PIN DIAGRAM: 64-PIN TQFP – GENERAL PURPOSE

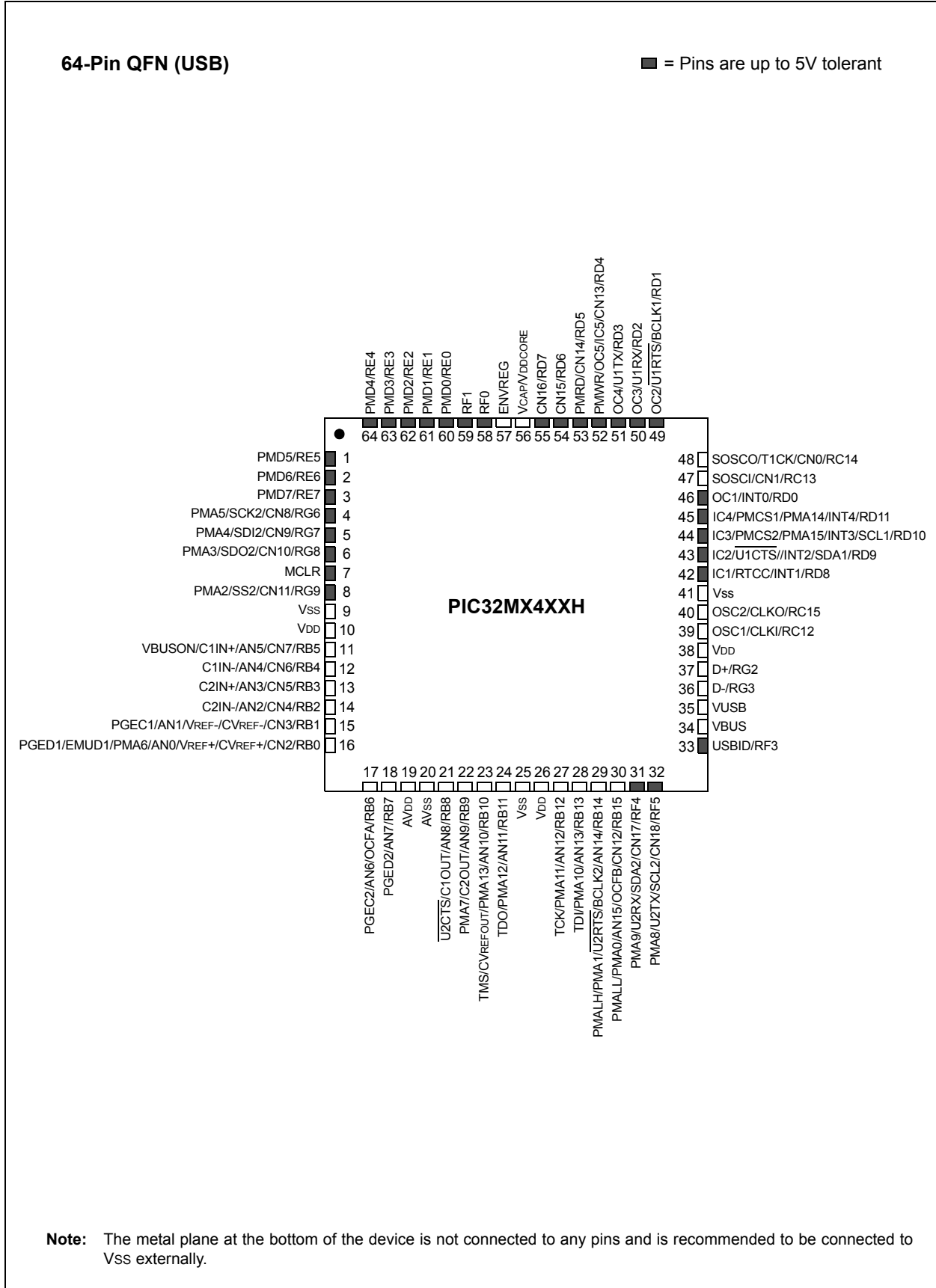


PIN DIAGRAM: 100-PIN TQFP – GENERAL PURPOSE



PIC32MX3XX/4XX

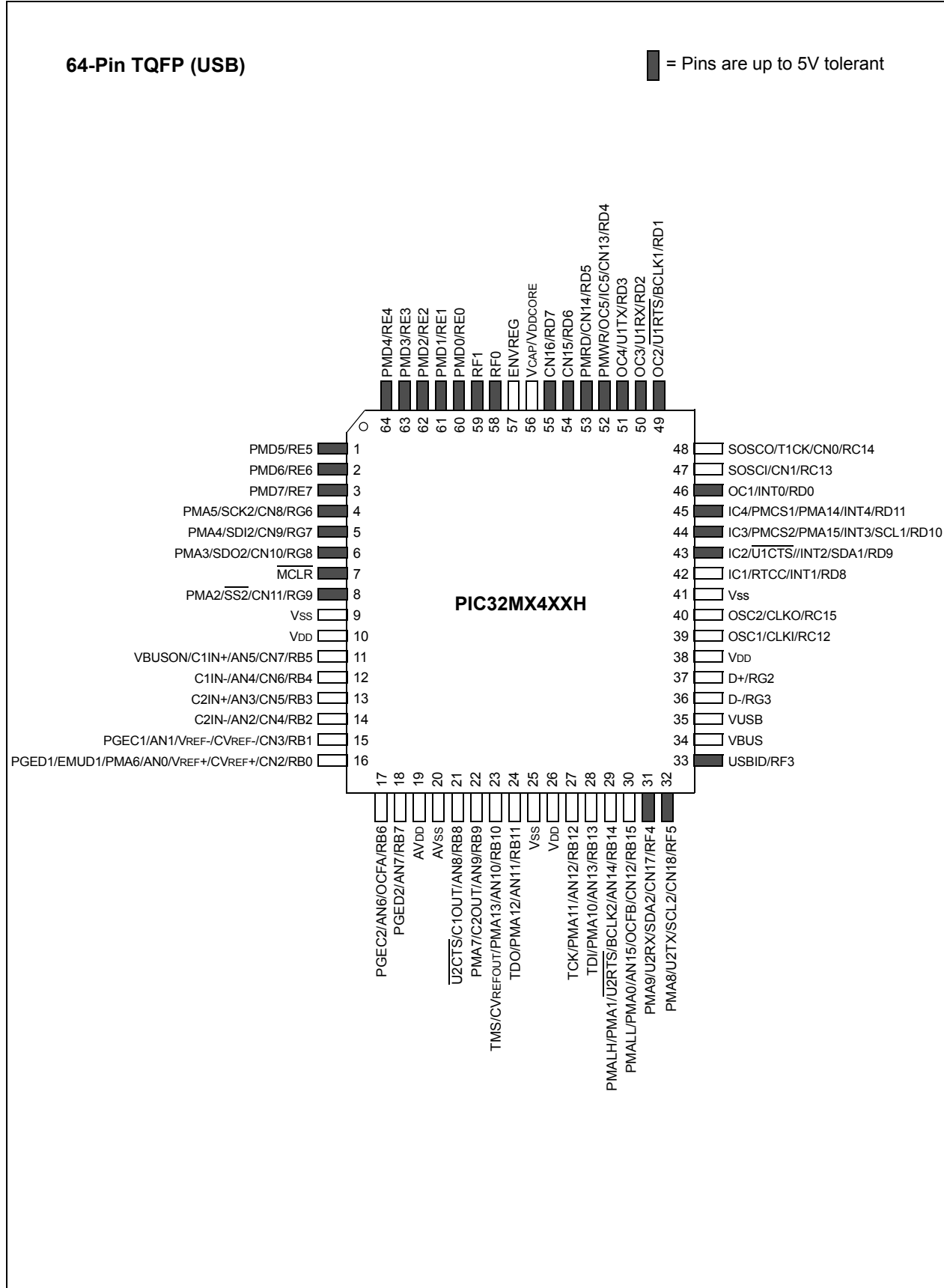
PIN DIAGRAM: 64-PIN QFN – USB



Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

PIC32MX3XX/4XX

PIN DIAGRAM: 64-PIN TQFP – USB



PIC32MX3XX/4XX

PIN DIAGRAM: 100-PIN TQFP – USB

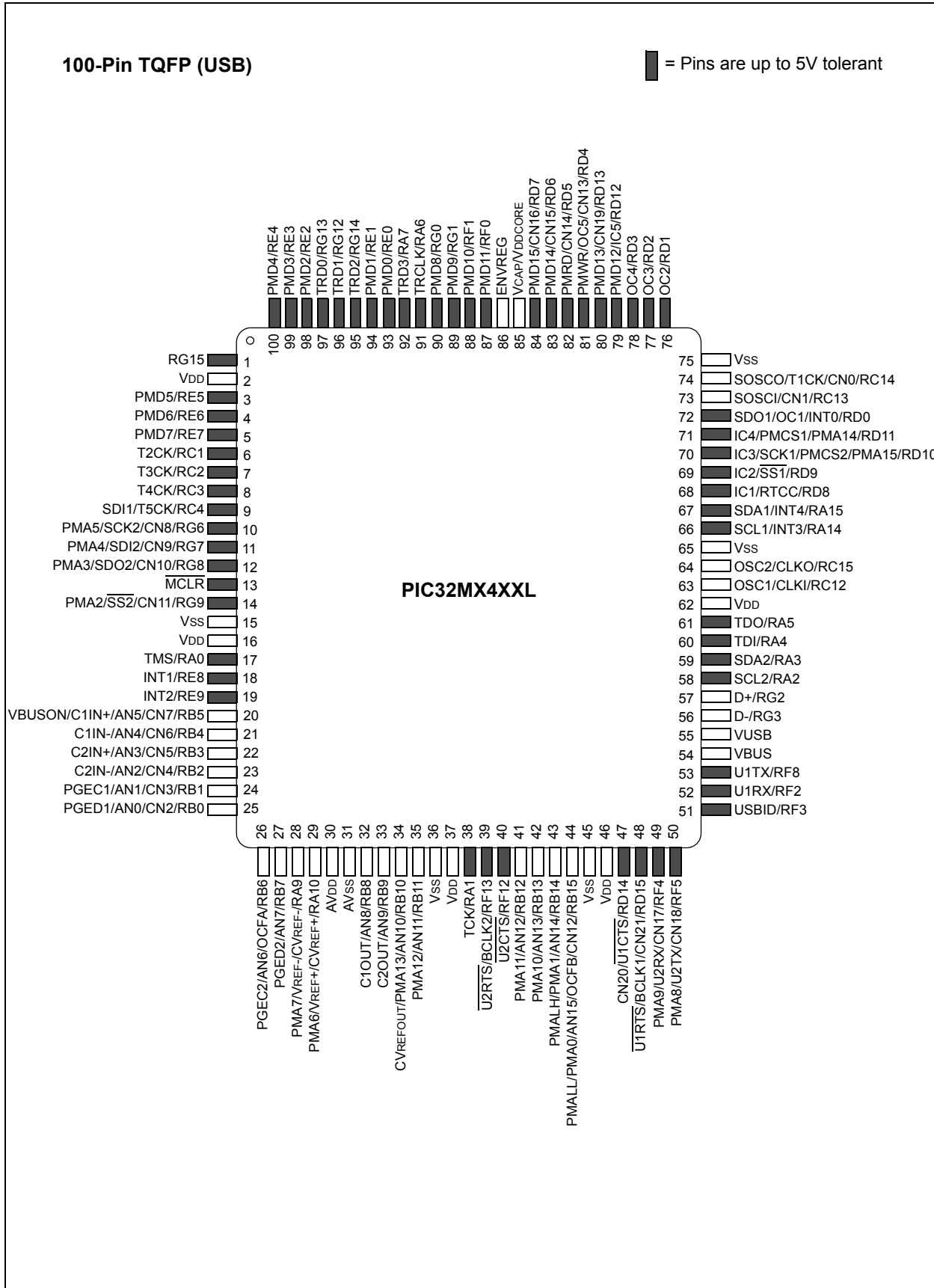


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1.0 DEVICE OVERVIEW

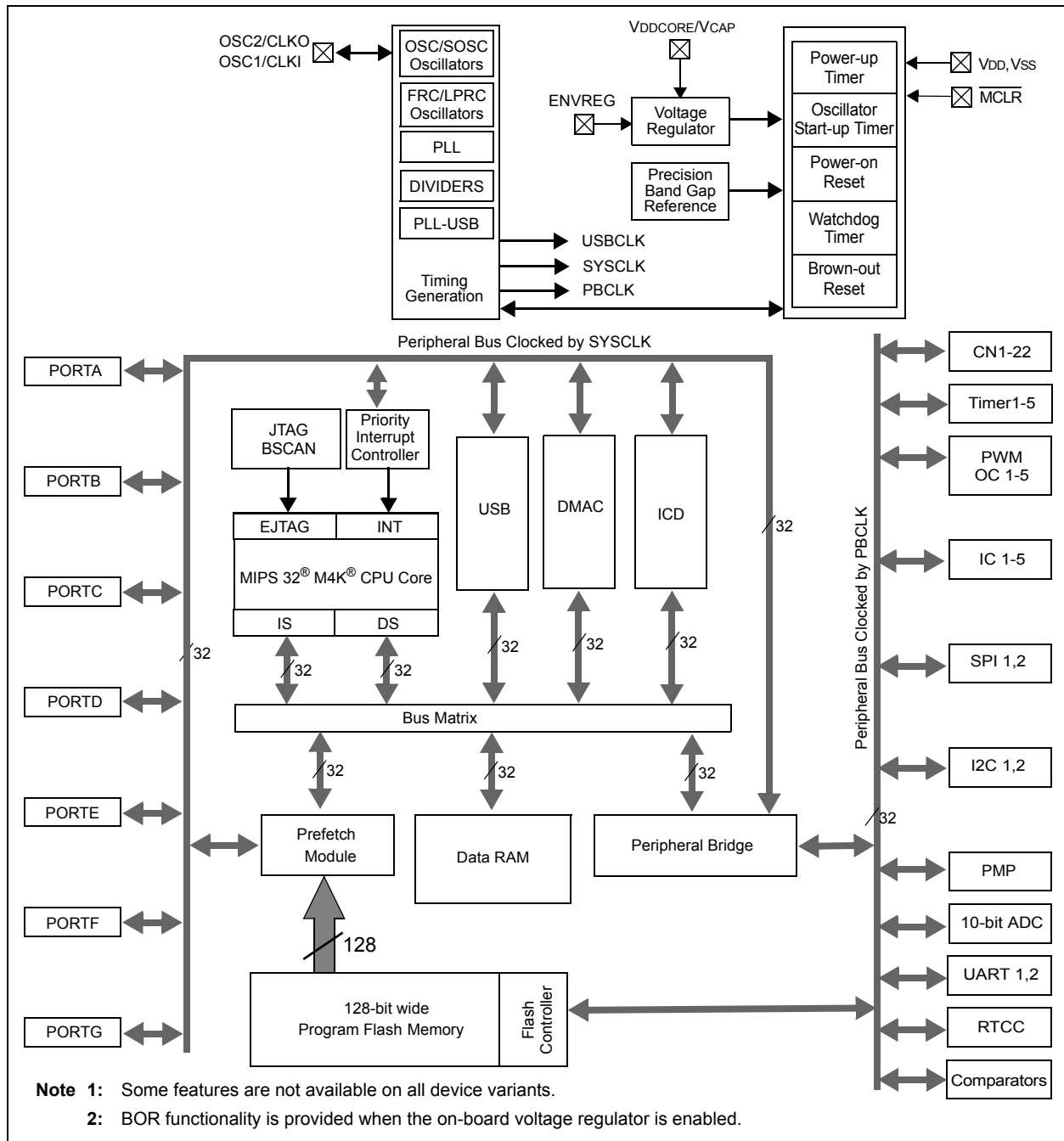
Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the appropriate section of the “PIC32MX Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32)

This document contains device-specific information for the PIC32MX3XX/4XX devices.

Figure 1-1 shows a general block diagram of the core and peripheral modules in the PIC32MX3XX/4XX families of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM^(1,2)



PIC32MX3XX/4XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	Description
AN0-AN15	I	Analog	Analog input channels.
CLKI	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	32.768 kHz low-power oscillator crystal output.
CN0-CN21	I	ST	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
IC1-IC5	I	ST	Capture inputs 1-5.
OCFA	I	ST	Compare Fault A input.
OC1-OC5	O	—	Compare outputs 1 through 5.
OCFB	I	ST	Output Compare Fault B Input.
INT0	I	ST	External interrupt 0.
INT1	I	ST	External interrupt 1.
INT2	I	ST	External interrupt 2.
INT3	I	ST	External interrupt 3.
INT4	I	ST	External interrupt 4.
RA0-RA15	I/O	ST	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC0-RC15	I/O	ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE15	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF15	I/O	ST	PORTF is a bidirectional I/O port.
RG0, RG1, RG4-RG15	I/O	ST	PORTG is a bidirectional I/O port.
RG2, RG3	I	ST	PORTG input pins.
T1CK	I	ST	Timer1 external clock input.
T2CK	I	ST	Timer2 external clock input.
T3CK	I	ST	Timer3 external clock input.
T4CK	I	ST	Timer4 external clock input.
T5CK	I	ST	Timer5 external clock input.
U1CTS	I	ST	UART1 clear to send.
U1RTS	O	—	UART1 ready to send.
U1RX	I	ST	UART1 receive.
U1TX	O	—	UART1 transmit.
U2CTS	I	ST	UART2 clear to send.
U2RTS	O	—	UART2 ready to send.
U2RX	I	ST	UART2 receive.
U2TX	O	—	UART2 transmit.

Legend: CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = TTL input buffer

Analog = Analog input
 O = Output
 P = Power
 I = Input

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
SCK1	I/O	ST	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	SPI1 data in.
SDO1	O	—	SPI1 data out.
SS1	I/O	ST	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	SPI2 data in.
SDO2	O	—	SPI2 data out.
SS2	I/O	ST	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	Synchronous serial data input/output for I2C1.
TMS	I	ST	JTAG Test mode select pin.
TCK	I	ST	JTAG test clock input pin.
TDI	I	ST	JTAG test data input pin.
TDO	O	—	JTAG test data output pin.
RTCC	O	—	Real-Time Clock Alarm Output.
CVREF-	I	ANA	Comparator Voltage Reference (low).
CVREF+	I	ANA	Comparator Voltage Reference (high).
CVREFOUT	O	ANA	Comparator Voltage Reference Output.
C1IN-	I	ANA	Comparator 1 Negative Input.
C1IN+	I	ANA	Comparator 1 Positive Input.
C1OUT	O	—	Comparator 1 Output.
C2IN-	I	ANA	Comparator 2 Negative Input.
C2IN+	I	ANA	Comparator 2 Positive Input.
C2OUT	O	—	Comparator 2 Output.
PMA0	I/O	TTL/ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	I/O	TTL/ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2-PMPA15	O	—	Parallel Master Port Address (Demultiplexed Master Modes).
PMENB	O	—	Parallel Master Port Enable Strobe (Master mode 1).
PMCS1	O	—	Parallel Master Port Chip Select 1 Strobe.
PMCS2	O	—	Parallel Master Port Chip Select 2 Strobe.
PMD0-PMD15	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMRD	O	—	Parallel Master Port Read Strobe.
PMWR	O	—	Parallel Master Port Write Strobe.
PMALL	O	—	Parallel Master Port Address Latch Enable low-byte (Multiplexed Master modes).
PMALH	O	—	Parallel Master Port Address Latch Enable high-byte (Multiplexed Master modes).
PMRD/PMWR	O	—	Parallel Master Port Read/Write Strobe (Master mode 1).
PMALL	O	—	Parallel Master Port Address Latch Enable low-byte (Multiplexed Master modes).
PMALH	O	—	Parallel Master Port Address Latch Enable high-byte (Multiplexed Master modes).
PMRD/PMWR	O	—	Parallel Master Port Read/Write Strobe (Master mode 1).

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 TTL = TTL input buffer

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
VBUS	I	ANA	USB Bus Power Monitor.
VUSB	P	—	USB Internal Transceiver Supply.
VBUSON	O	—	USB Host and OTG Bus Power Control Output.
D+	I/O	ANA	USB D+.
D-	I/O	ANA	USB D-.
USBID	I	ST	USB OTG ID Detect.
ENVREG	I	ST	Enable for On-Chip Voltage Regulator.
TRCLK	O	—	Trace Clock.
TRD0-TRD3	O	—	Trace Data Bits 0-3
PGED1	I/O	ST	Data I/O pin for programming/debugging communication channel 1.
PGEC1	I	ST	Clock input pin for programming/debugging communication channel 1.
PGED2	I/O	ST	Data I/O pin for programming/debugging communication channel 2.
PGEC2	I	ST	Clock input pin for programming/debugging communication channel 2.
MCLR	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVdd	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVss	P	P	Ground reference for analog modules.
Vdd	P	—	Positive supply for peripheral logic and I/O pins.
Vcap/Vddcore	P	—	CPU logic filter capacitor connection.
Vss	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog voltage reference (high) input.
VREF-	I	Analog	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 TTL = TTL input buffer

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” for a detailed description of the PIC32MX MCU. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX3XX/4XX family of 32-bit Microcontrollers (MCU) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see Section 2.2)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see Section 2.2)
- VCAP/VDDCORE (see Section 2.3)
- MCLR pin (see Section 2.4)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see Section 2.5)
- OSC1 and OSC2 pins when external oscillator source is used (see Section 2.8)

Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of ADC use and ADC voltage reference source.

2.2 Decoupling Capacitors

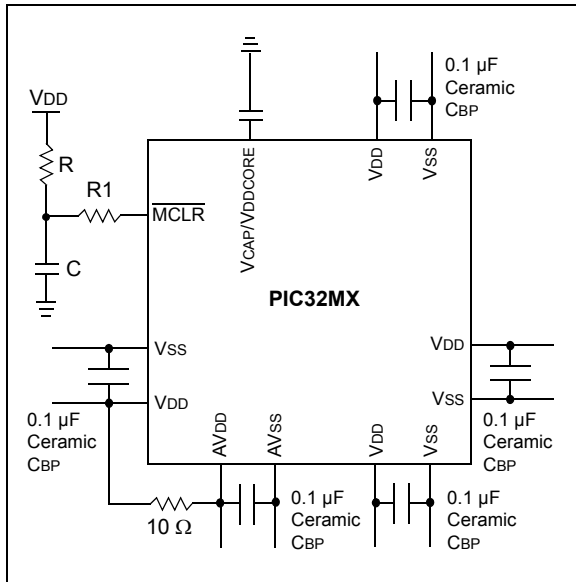
The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD, and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 μF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

PIC32MX3XX/4XX

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 μF to 47 μF . This capacitor should be located as close to the device as possible.

2.3 Capacitor on Internal Voltage Regulator (VCAP/VDDCORE)

2.3.1 INTERNAL REGULATOR MODE

A low-ESR ($< 5 \text{ Ohms}$) capacitor is required on the VCAP/VDDCORE pin, which is used to stabilize the internal voltage regulator output. The VCAP/VDDCORE pin must not be connected to VDD, and must have a 10 μF capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 28.0 "Electrical Characteristics"** for additional information. This mode is enabled by connecting the ENVREG pin to VDD.

2.3.2 EXTERNAL REGULATOR MODE

In this mode the core voltage is supplied externally through the VDDCORE pin. A low-ESR capacitor of 10 μF is recommended on the VDDCORE pin. This mode is enabled by grounding the ENVREG pin.

The placement of this capacitor should be close to the VCAP/VDDCORE. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 26.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

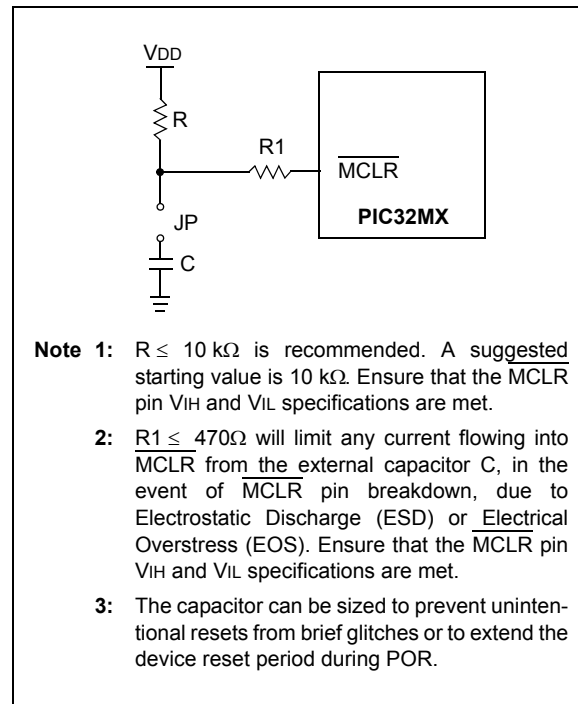
- Device Reset
- Device Programming and Debugging

Pulling The MCLR pin low generates a device reset. Figure 2-2 shows a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 2, MPLAB® ICD 3, or MPLAB® REAL ICE™.

For more information on ICD 2, ICD 3, and REAL ICE connection requirements, refer to the following documents that are available on the Microchip website.

- “MPLAB® ICD 2 In-Circuit Debugger User’s Guide” DS51331
- “Using MPLAB® ICD 2” (poster) DS51265
- “MPLAB® ICD 2 Design Advisory” DS51566
- “Using MPLAB® ICD 3” (poster) DS51765
- “MPLAB® ICD 3 Design Advisory” DS51764
- “MPLAB® REAL ICE™ In-Circuit Debugger User’s Guide” DS51616
- “Using MPLAB® REAL ICE™” (poster) DS51749

2.6 JTAG

The TMS, TDO, TDI, and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the TMS, TDO, TDI, and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.7 Trace

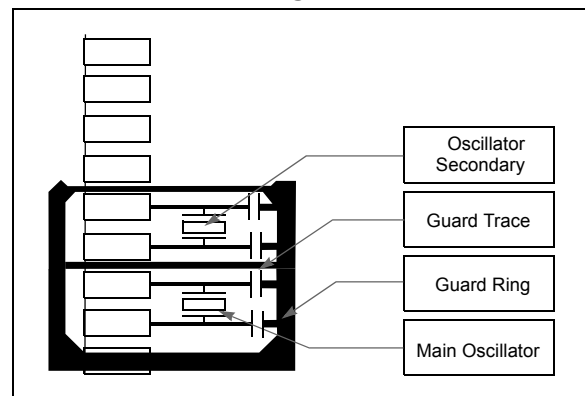
The trace pins can be connected to a hardware-trace-enabled programmer to provide a compressed real time instruction trace. When used for trace the TRD3, TRD2, TRD1, TRD0, and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 “Oscillator Configuration”** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



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2.9 Configuration of Analog and Digital Pins During ICSP Operations

If MPLAB ICD 2, ICD 3, or REAL ICE is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as “digital” pins by setting all bits in the ADPCFG register.

The bits in this register that correspond to the A/D pins that are initialized by MPLAB ICD 2, ICD 3, or REAL ICE, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, the user application must clear the corresponding bits in the ADPCFG register during initialization of the ADC module.

When MPLAB ICD 2, ICD 3, or REAL ICE is used as a programmer, the user application firmware must correctly configure the ADPCFG register. Automatic initialization of this register is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic '0', which may affect user application functionality.

2.10 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternately, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

3.0 PIC32MX MCU

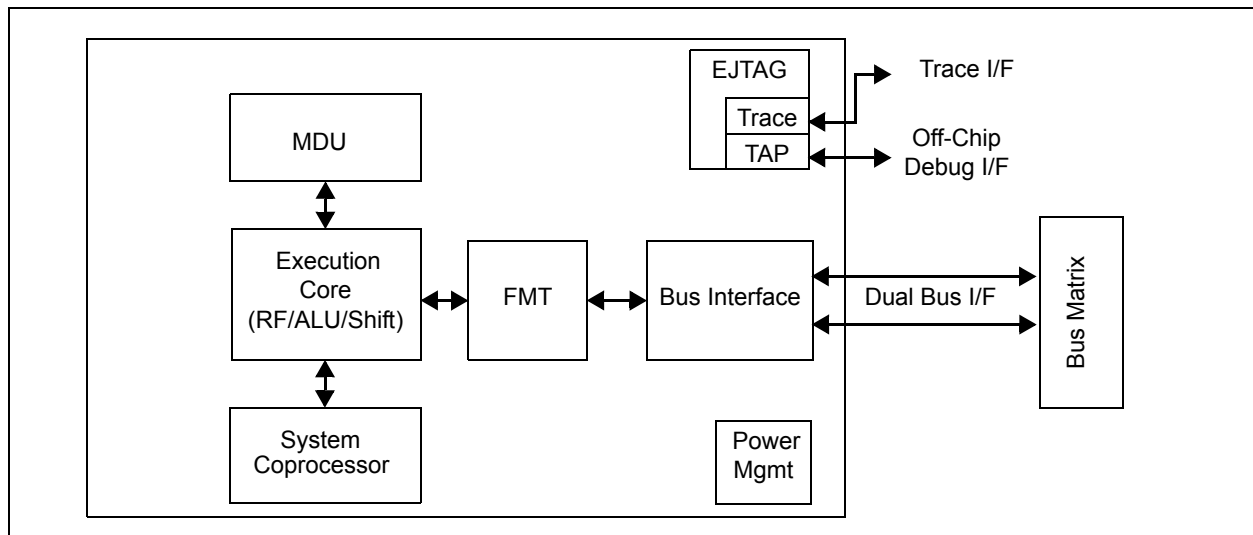
Note: This data sheet summarizes the features of the PIC32MX3XX/4XX Family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” **Section 2. “MCU”** (DS61113) for a detailed description of the PIC32MX MCU. The manual is available from the Microchip web site (www.Microchip.com/PIC32). Resources for the MIPS32® M4K® Processor Core are available at www.mips.com/products/cores/32-bit-cores/mips32-m4k/#.

The MCU module is the heart of the PIC32MX3XX/4XX Family processor. The MCU fetches instructions, decodes each instruction, fetches source operands, executes each instruction, and writes the results of instruction execution to the proper destinations.

3.1 Features

- 5-stage pipeline
- 32-bit Address and Data Paths
- MIPS32 Enhanced Architecture (Release 2)
 - Multiply-Accumulate and Multiply-Subtract Instructions
 - Targeted Multiply Instruction
 - Zero/One Detect Instructions
 - WAIT Instruction
 - Conditional Move Instructions (MOVN, MOVZ)
 - Vectored interrupts
 - Programmable exception vector base
 - Atomic interrupt enable/disable
 - GPR shadow registers to minimize latency for interrupt handlers
 - Bit field manipulation instructions
- MIPS16e™ Code Compression
 - 16-bit encoding of 32-bit instructions to improve code density
 - Special PC-relative instructions for efficient loading of addresses and constants
 - SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines
 - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- Simple Dual Bus Interface
 - Independent 32-bit address and data busses
 - Transactions can be aborted to improve interrupt latency
- Autonomous Multiply/Divide Unit
 - Maximum issue rate of one 32x16 multiply per clock
 - Maximum issue rate of one 32x32 multiply every other clock
 - Early-in iterative divide. Minimum 11 and maximum 34 clock latency (dividend (rs) sign extension-dependent)
- Power Control
 - Minimum frequency: 0 MHz
 - Low-Power mode (triggered by WAIT instruction)
 - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace
 - Support for single stepping
 - Virtual instruction and data address/value breakpoints
 - PC tracing with trace compression

FIGURE 3-1: MCU BLOCK DIAGRAM



PIC32MX3XX/4XX

3.2 Architecture Overview

The PIC32MX3XX/4XX Family core contains several logic blocks working together in parallel, providing an efficient high performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CPO)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The PIC32MX3XX/4XX Family core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit general purpose registers used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instructions streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and Store Aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The PIC32MX3XX/4XX Family core includes a multiply/divide unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the integer unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32MX core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit-wide *rs*, 15 iterations are skipped, and for a 24-bit-wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32MX core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: PIC32MX3XX/4XX FAMILY CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul <i>rt</i>) (div <i>rs</i>)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU, MSUB/MSUBU	16 bits	1	1
	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the general purpose register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, multiply-add (MADD) and multiply-subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds

the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (kernel, user, and debug), and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX3XX/4XX Family core
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers
8	BadVAddr ⁽¹⁾	Reports the address for the most recent address-related exception
9	Count ⁽¹⁾	Processor cycle count
10	Reserved	Reserved in the PIC32MX3XX/4XX Family core
11	Compare ⁽¹⁾	Timer interrupt control
12	Status ⁽¹⁾	Processor status and control
12	IntCtl ⁽¹⁾	Interrupt system status and control
12	SRSCtl ⁽¹⁾	Shadow register set status and control
12	SRSMap ⁽¹⁾	Provides mapping from vectored interrupt to a shadow set
13	Cause ⁽¹⁾	Cause of last general exception
14	EPC ⁽¹⁾	Program counter at last exception
15	PRId	Processor identification and revision
15	EBASE	Exception vector base register
16	Config	Configuration register
16	Config1	Configuration register 1
16	Config2	Configuration register 2
16	Config3	Configuration register 3

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TABLE 3-2: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
17-22	Reserved	Reserved in the PIC32MX3XX/4XX Family core
23	Debug ⁽²⁾	Debug control and exception status
24	DEPC ⁽²⁾	Program counter at last debug exception
25-29	Reserved	Reserved in the PIC32MX3XX/4XX Family core
30	ErrorEPC ⁽¹⁾	Program counter at last error
31	DESAVE ⁽²⁾	Debug handler scratchpad register

Note 1: Registers used in exception processing.

2: Registers used during debug.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events, or program errors. Table 3-3 shows the exception types in order of priority.

TABLE 3-3: PIC32MX3XX/4XX FAMILY CORE EXCEPTION TYPES

Exception	Description
Reset	Assertion MCLR or a Power-On Reset (POR)
DSS	EJTAG Debug Single Step
DINT	EJTAG Debug Interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input, or by setting the <i>EjtagBrk</i> bit in the ECR register
NMI	Assertion of NMI signal
Interrupt	Assertion of unmasked hardware or software interrupt signal
DIB	EJTAG debug hardware instruction break matched
AdEL	Fetch address alignment error Fetch reference to protected address
IBE	Instruction fetch bus error
DBp	EJTAG Breakpoint (execution of <i>SDBBP</i> instruction)
Sys	Execution of <i>SYSCALL</i> instruction
Bp	Execution of <i>BREAK</i> instruction
RI	Execution of a Reserved Instruction
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled
CEU	Execution of a CorExtend instruction when CorExtend is not enabled
Ov	Execution of an arithmetic instruction that overflowed
Tr	Execution of a trap (when trap condition is true)
DDBL / DDBS	EJTAG Data Address Break (address only) or EJTAG Data Value Break on Store (address + value)
AdEL	Load address alignment error Load reference to protected address
AdES	Store address alignment error Store to protected address
DBE	Load or store bus error
DDBL	EJTAG data hardware breakpoint matched in load data compare

3.3 Power Management

The PIC32MX3XX/4XX Family core offers a number of power management features, including low-power design, active power management, and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking power-down mode is through execution of the `WAIT` instruction. For more information on power management, see **Section 25.0 “Power-Saving Features”**.

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX3XX/4XX Family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The PIC32MX3XX/4XX Family core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard user mode and kernel modes of operation, the PIC32MX3XX/4XX Family core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a debug exception return (`DERET`) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the PIC32MX3XX/4XX Family core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define what registers are selected and how they are used.

PIC32MX3XX/4XX

NOTES:

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “*PIC32MX Family Reference Manual*” **Section 3. “Memory Organization”** (DS61115) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

PIC32MX3XX/4XX microcontrollers provide 4 GB of unified virtual memory address space. All memory regions including program, data memory, SFRs, and Configuration registers reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX3XX/4XX to execute from data memory.

Key Features:

- 32-bit native data width
- Separate User and Kernel mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code.
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable and non-cacheable address regions

4.1 PIC32MX3XX/4XX Memory Layout

PIC32MX3XX/4XX microcontrollers implement two address spaces: Virtual and Physical. All hardware resources such as program memory, data memory, and peripherals are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by peripherals such as DMA and Flash controller that access memory independently of CPU.

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FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX320F032H, PIC32MX420F032H DEVICES⁽¹⁾

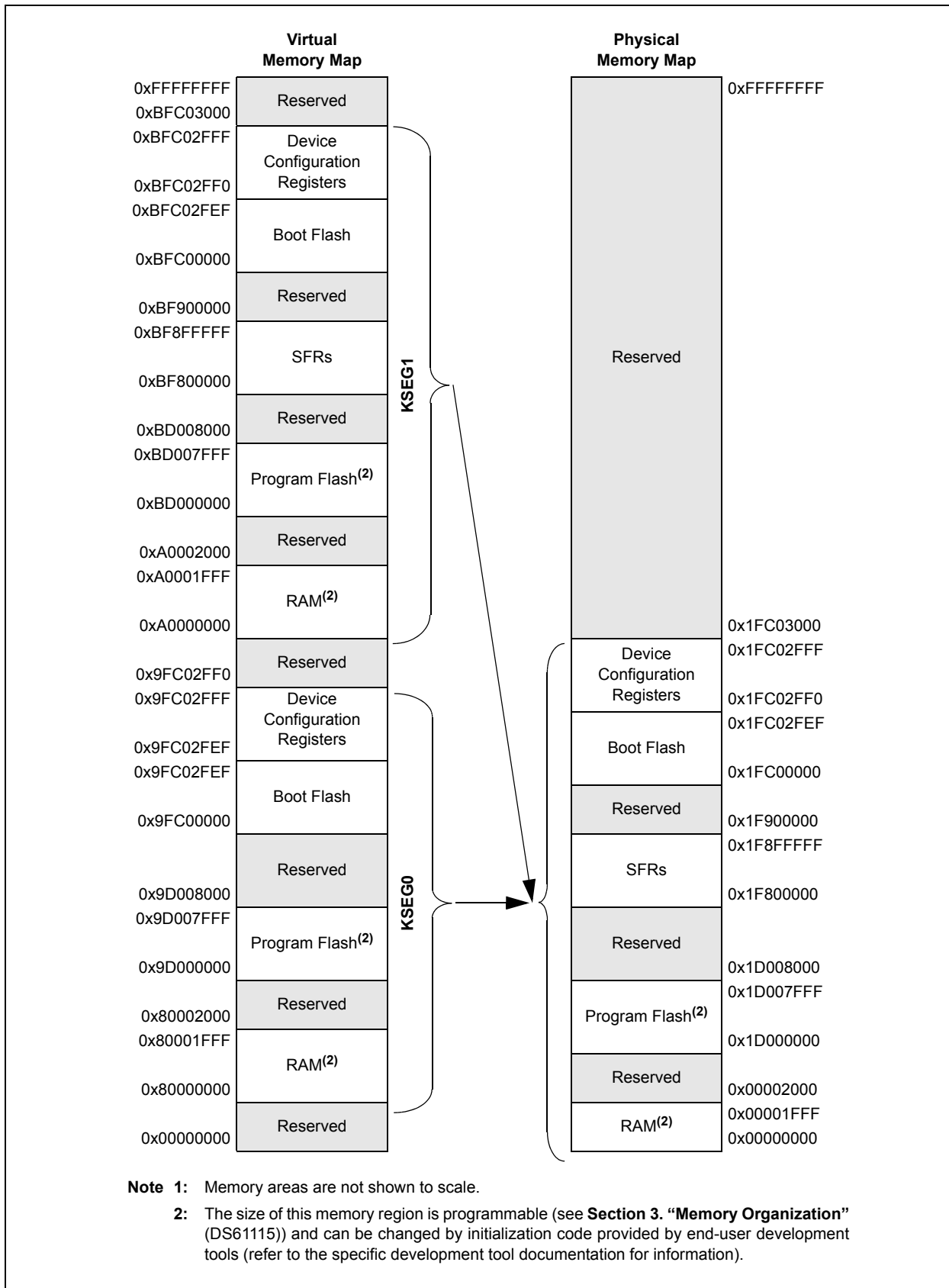
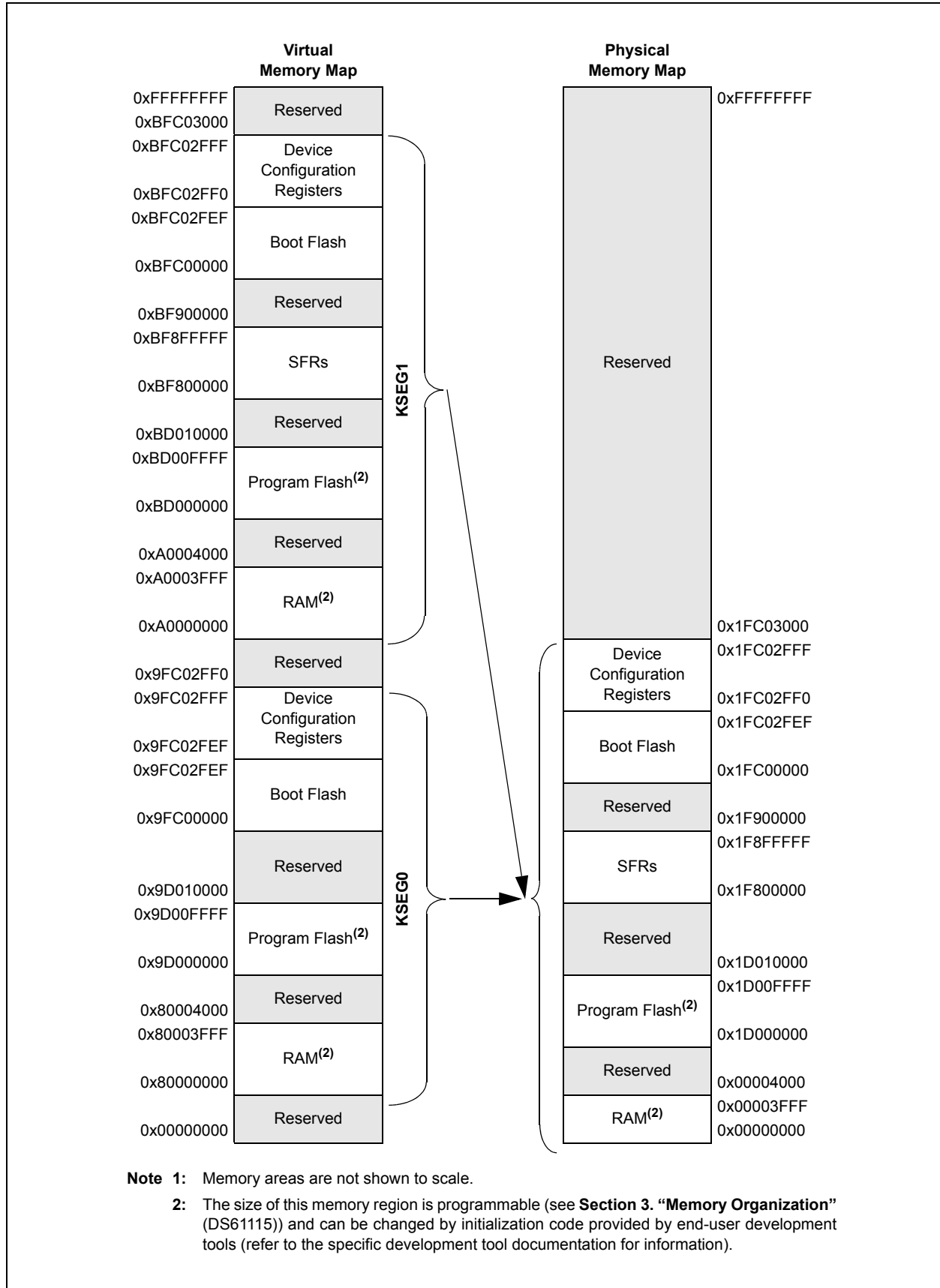


FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX320F064H DEVICES⁽¹⁾



PIC32MX3XX/4XX

FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX320F128H, PIC32MX320F128L DEVICES⁽¹⁾

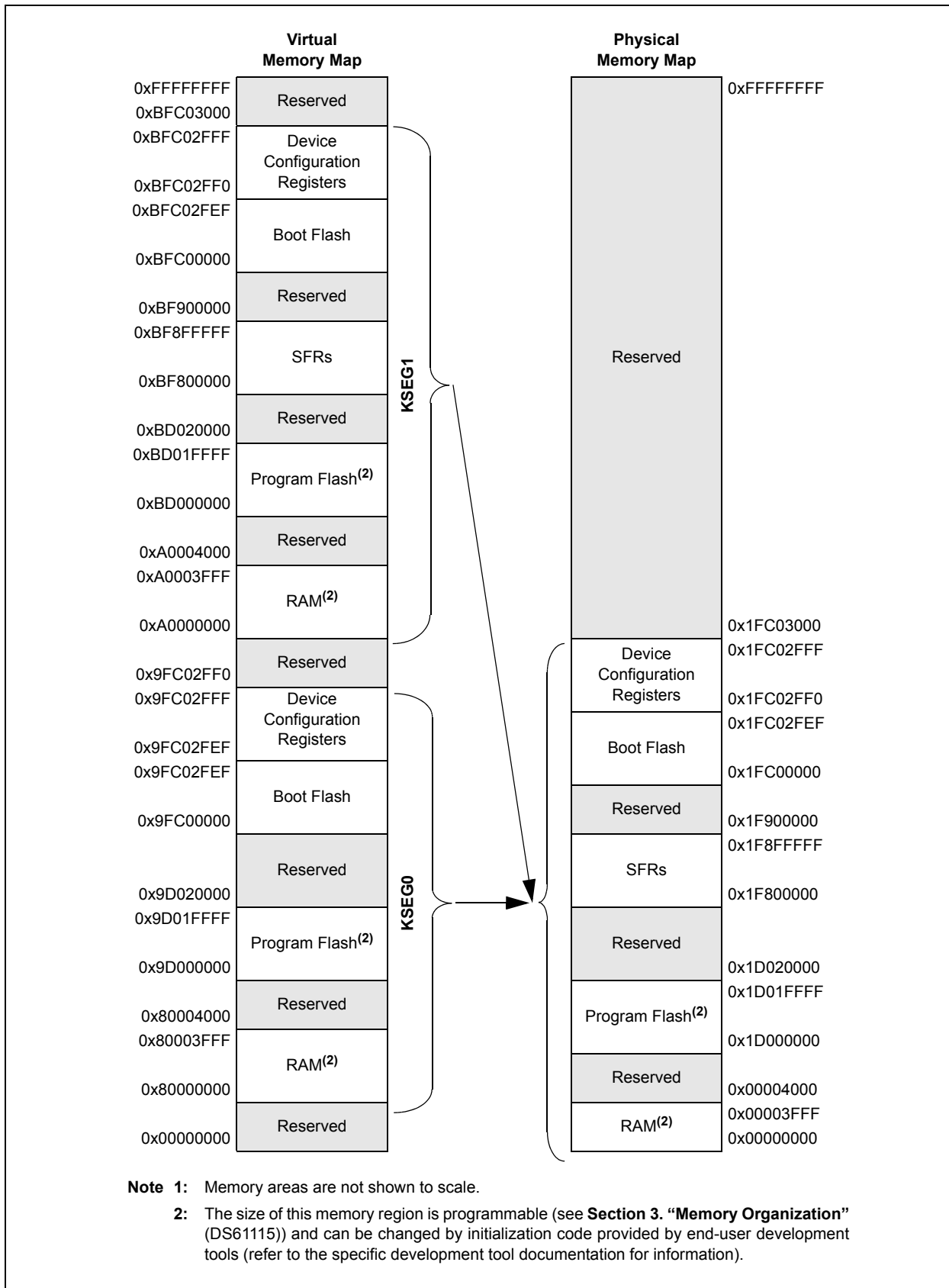
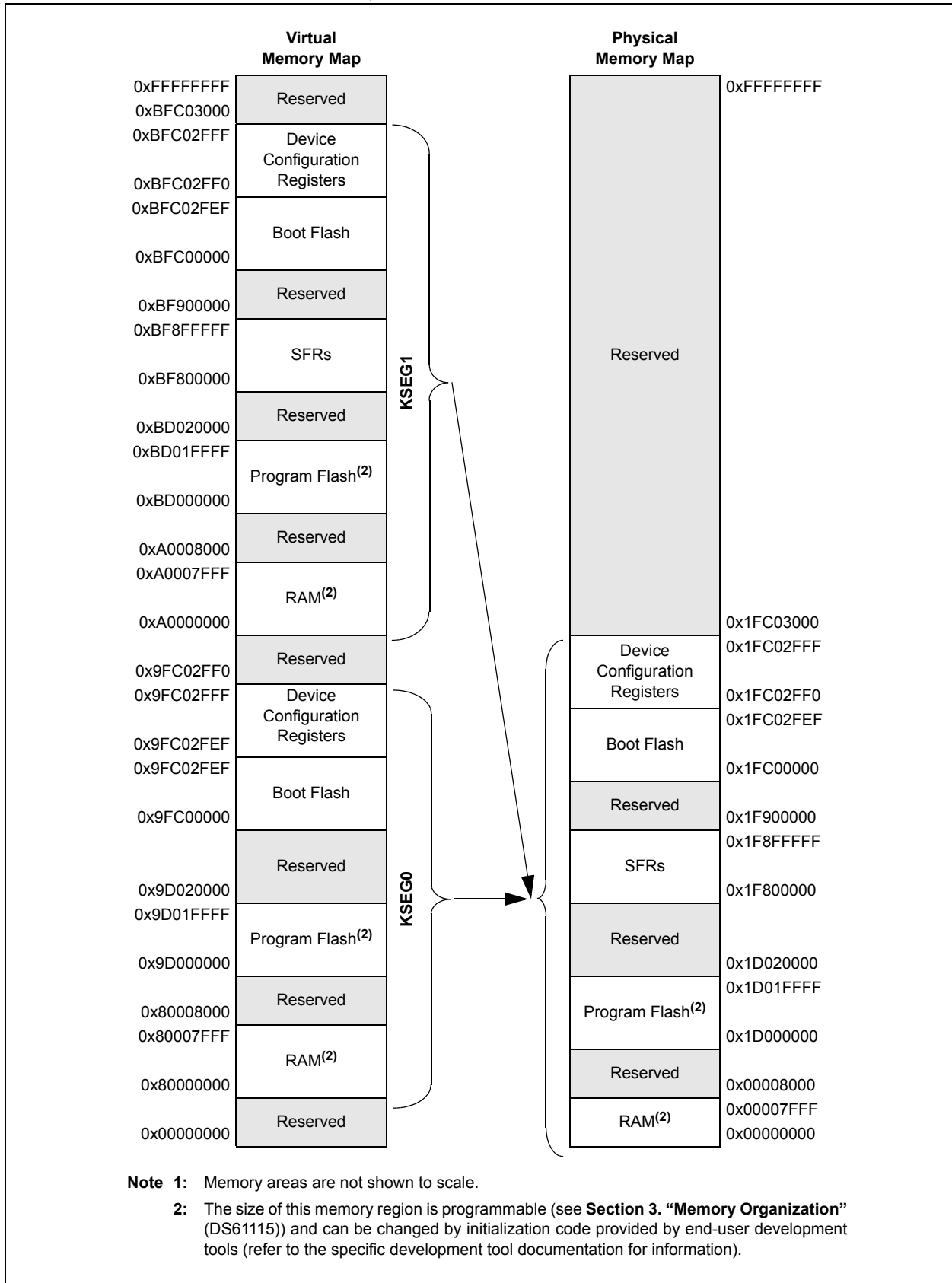


FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX340F128H, PIC32MX340F128L, PIC32MX440F128H, PIC32MX440F128L DEVICES⁽¹⁾



PIC32MX3XX/4XX

FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX340F256H, PIC32MX360F256L, PIC32MX440F256H, PIC32MX460F256L DEVICES⁽¹⁾

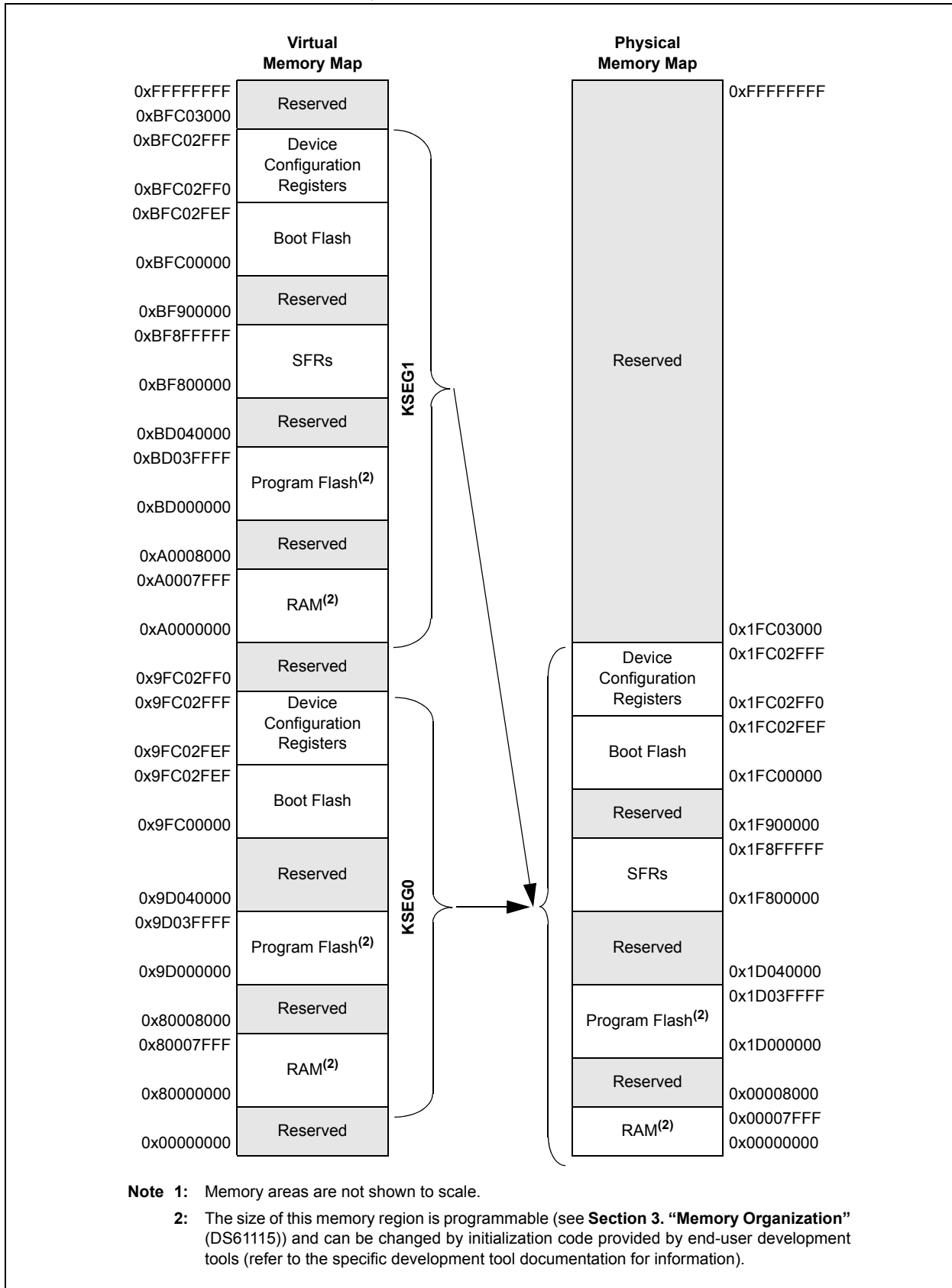
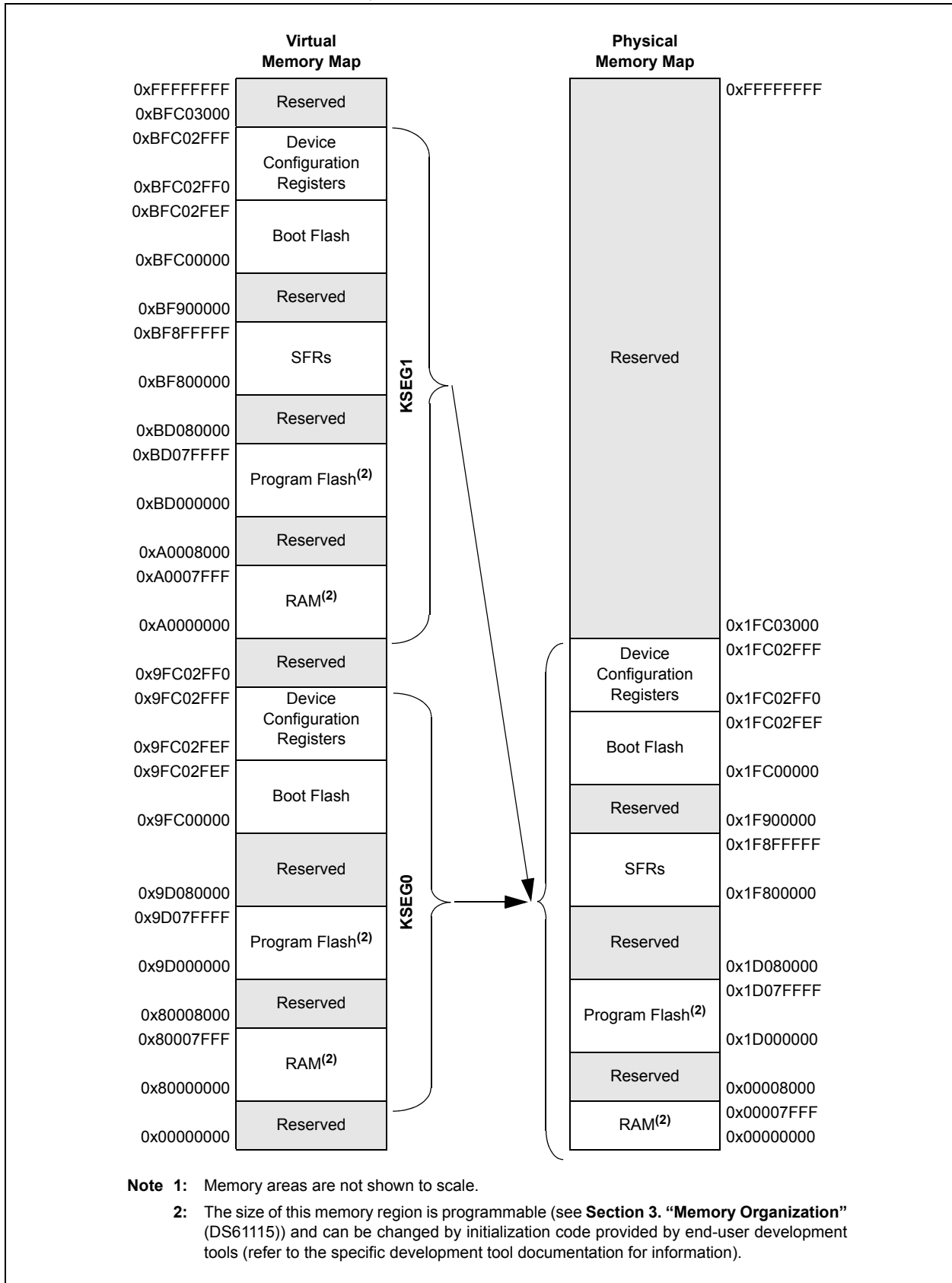


FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX340F512H, PIC32MX360F512L, PIC32MX440F512H, PIC32MX460F512L DEVICES⁽¹⁾



PIC32MX3XX/4XX

4.1.1 PERIPHERAL REGISTERS LOCATIONS

Table 4-1 through Table 4-25 contain the peripheral address maps for the PIC32MX3XX/4XX device. Peripherals located on the PB Bus are mapped to 512 byte boundaries. Peripherals on the FPB Bus are mapped to 4 Kbyte boundaries.

TABLE 4-1: BUS MATRIX REGISTERS MAP

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0	
BF88_2000	BMXCON ⁽¹⁾	31:16	—	—	—	—	—	BMX CHEDMA	—	—	—	—	—	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS	
		15:0	—	—	—	—	—	—	—	—	—	—	BMX WSDRM	—	—	—	BMXARB<2:0>		
BF88_2010	BMX DKPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	BMXDKPBA<15:0>																
BF88_2020	BMX DUDBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	BMXDUDBA<15:0>																
BF88_2030	BMX DUPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	BMXDUPBA<15:0>																
BF88_2040	BMXDRMSZ	31:16	BMXDRMSZ<31:0>																
BF88_2050	BMX PUPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	BMXPUPBA<19:16>			
		15:0	BMXPUPBA<15:0>																
BF88_2060	BMXPFMSZ	31:16	BMXPFMSZ<31:0>																
BF88_2070	BMX BOOTSZ	31:16	BMXBOOTSZ<31:0>																
		15:0																	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-2: INTERRUPT REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0	
BF88_1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	
		15:0	—	FRZ	—	MVEC	—	TRC<2:0>					—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
BF88_1010	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	RIPL<2:0>					—	—	VEC<5:0>				
BF88_1020	IPTMR	31:16	IPTMR<31:0>																
BF88_1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	
BF88_1040	IFS1	31:16	—	—	—	—	—	—	USBIF ⁽⁴⁾	FCEIF	—	—	—	—	DMA3IF ⁽²⁾	DMA2IF ⁽²⁾	DMA1IF ⁽²⁾	DMA0IF ⁽²⁾	
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF ⁽³⁾	SPI2TXIF ⁽³⁾	SPI2EIF ⁽³⁾	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

- 2:** These bits are not present on PIC32MX320FXXXX/420FXXXX devices.
- 3:** These bits are not present on PIC32MX420FXXXX/440FXXXX devices.
- 4:** These bits are not present on PIC32MX320FXXXX/340FXXXX/360FXXXX devices.

TABLE 4-2: INTERRUPT REGISTERS MAP⁽¹⁾ (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE
BF88_1070	IEC1	31:16	—	—	—	—	—	—	USBIE	FCEIE	—	—	—	—	DMA3IE ⁽²⁾	DMA2IE ⁽²⁾	DMA1IE ⁽²⁾	DMA0IE ⁽²⁾
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2RXIE ⁽³⁾	SPI2TXIE ⁽³⁾	SPI2EIE ⁽³⁾	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE
BF88_1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>			—	—	—	CS1IP<2:0>		CS1IS<1:0>	
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>			—	—	—	CTIP<2:0>		CTIS<1:0>	
BF88_10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>			—	—	—	OC1IP<2:0>		OC1IS<1:0>	
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>			—	—	—	T1IP<2:0>		T1IS<1:0>	
BF88_10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>			—	—	—	OC2IP<2:0>		OC2IS<1:0>	
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>			—	—	—	T2IP<2:0>		T2IS<1:0>	
BF88_10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>			—	—	—	OC3IP<2:0>		OC3IS<1:0>	
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>			—	—	—	T3IP<2:0>		T3IS<1:0>	
BF88_10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>			—	—	—	OC4IP<2:0>		OC4IS<1:0>	
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>			—	—	—	T4IP<2:0>		T4IS<1:0>	
BF88_10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>			—	—	—	OC5IP<2:0>		OC5IS<1:0>	
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>			—	—	—	T5IP<2:0>		T5IS<1:0>	
BF88_10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>			—	—	—	CNIP<2:0>		CNIS<1:0>	
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>			—	—	—	U1IP<2:0>		U1IS<1:0>	
BF88_1100	IPC7	31:16	—	—	—	SPI2IP<2:0> ⁽³⁾			SPI2IS<1:0> ⁽³⁾			—	—	—	CMP2IP<2:0>		CMP2IS<1:0>	
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>			—	—	—	PMPIP<2:0>		PMPIS<1:0>	
BF88_1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>			—	—	—	FSCMIP<2:0>		FSCMIS<1:0>	
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>			—	—	—	U2IP<2:0>		U2IS<1:0>	
BF88_1120	IPC9	31:16	—	—	—	DMA3IP<2:0> ⁽²⁾			DMA3IS<1:0> ⁽²⁾			—	—	—	DMA2IP<2:0> ⁽²⁾		DMA2IS<1:0> ⁽²⁾	
		15:0	—	—	—	DMA1IP<2:0> ⁽²⁾			DMA1IS<1:0> ⁽²⁾			—	—	—	DMA0IP<2:0> ⁽²⁾		DMA0IS<1:0> ⁽²⁾	
BF88_1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	USBIP<2:0> ⁽⁴⁾			USBIS<1:0> ⁽⁴⁾			—	—	—	FCEIP<2:0>		FCEIS<1:0>	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: These bits are not present on PIC32MX320FXXX/420FXXX devices.

3: These bits are not present on PIC32MX420FXXX/440FXXX devices.

4: These bits are not present on PIC32MX320FXXX/340FXXX/360FXXX devices.

TABLE 4-3: TIMER1-5 REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_0600	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>	—	—	TSYNC	TCS	—
BF80_0610	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TMR1<15:0>															
BF80_0620	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	PR1<15:0>															
BF80_0800	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	—	—	TGATE	—	TCKPS<2:0>	—	—	T32	—	TCS
BF80_0810	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TMR2<15:0>															
BF80_0820	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	PR2<15:0>															
BF80_0A00	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	—	—	TGATE	—	TCKPS<2:0>	—	—	—	—	TCS
BF80_0A10	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TMR3<15:0>															
BF80_0A20	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	PR3<15:0>															
BF80_0C00	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	—	—	TGATE	—	TCKPS<2:0>	—	—	T32	—	TCS
BF80_0C10	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TMR4<15:0>															
BF80_0C20	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	PR4<15:0>															
BF80_0E00	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	—	—	TGATE	—	TCKPS<2:0>	—	—	—	—	TCS
BF80_0E10	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TMR5<15:0>															
BF80_0E20	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	PR5<15:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-4: INPUT CAPTURE1-5 REGISTERS MAP

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_2000	IC1CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	ICFEDGE	ICC32	ICTMR	IC1<1:0>		ICOV	ICBNE	ICM<2:0>		
BF80_2010	IC1BUF	31:16 15:0	IC1BUF<31:0>															
BF80_2200	IC2CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	ICFEDGE	ICC32	ICTMR	IC1<1:0>		ICOV	ICBNE	ICM<2:0>		
BF80_2210	IC2BUF	31:16 15:0	IC2BUF<31:0>															
BF80_2400	IC3CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	ICFEDGE	ICC32	ICTMR	IC1<1:0>		ICOV	ICBNE	ICM<2:0>		
BF80_2410	IC3BUF	31:16 15:0	IC3BUF<31:0>															
BF80_2600	IC4CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	ICFEDGE	ICC32	ICTMR	IC1<1:0>		ICOV	ICBNE	ICM<2:0>		
BF80_2610	IC4BUF	31:16 15:0	IC4BUF<31:0>															
BF80_2800	IC5CON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	ICFEDGE	ICC32	ICTMR	IC1<1:0>		ICOV	ICBNE	ICM<2:0>		
BF80_2810	IC5BUF	31:16 15:0	IC5BUF<31:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-5: OUTPUT COMPARE 1-5 REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_3000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>	
BF80_3010	OC1R	31:16 15:0	OC1R<31:0>															
BF80_3020	OC1RS	31:16 15:0	OC1RS<31:0>															
BF80_3200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>	
BF80_3210	OC2R	31:16 15:0	OC2R<31:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-5: OUTPUT COMPARE 1-5 REGISTERS MAP⁽¹⁾ (CONTINUED)

SFR Virtual Addr	SFR Name	Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0	
BF80_3220	OC2RS	31:16 15:0	OC2RS<31:0>															
BF80_3400	OC3CON	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
			ON	FRZ	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>		
BF80_3410	OC3R	31:16 15:0	OC3R<31:0>															
BF80_3420	OC3RS	31:16 15:0	OC3RS<31:0>															
BF80_3600	OC4CON	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
			ON	FRZ	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>		
BF80_3610	OC4R	31:16 15:0	OC4R<31:0>															
BF80_3620	OC4RS	31:16 15:0	OC4RS<31:0>															
BF80_3800	OC5CON	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
			ON	FRZ	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>		
BF80_3810	OC5R	31:16 15:0	OC5R<31:0>															
BF80_3820	OC5RS	31:16 15:0	OC5RS<31:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-6: I2C1-2 REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name	Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0	
BF80_5000	I2C1CON	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
			ON	FRZ	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
BF80_5010	I2C1STAT	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
			ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF
BF80_5020	I2C1ADD	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
			ADD<9:0>															
BF80_5030	I2C1MSK	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
			MSK<9:0>															
BF80_5040	I2C1BRG	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
			I2C1BRG<11:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-6: I2C1-2 REGISTERS MAP⁽¹⁾ (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_5050	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	I2CT1DATA<7:0>						
BF80_5260	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	I2CR1DATA<7:0>						
BF80_5200	I2C2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
BF80_5210	I2C2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ACKSTAT	TRSTAT	—	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF
BF80_5220	I2C2ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	ADD<9:0>									
BF80_5230	I2C2MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	MSK<9:0>									
BF80_5240	I2C2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	I2C2BRG<11:0>										
BF80_5250	I2C2TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	I2CT1DATA<7:0>								
BF80_5260	I2C2RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	I2CR1DATA<7:0>								

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-7: UART1-2 REGISTERS MAP

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_6000	U1MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	IREN	RTSMD	—	UEN<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>	STSEL	—	—
BF80_6010	U1STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>							
		15:0	UTXISEL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	—	—
BF80_6020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register							
BF80_6030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	RX8	Receive Register							
BF80_6040	U1BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	BRG<15:0>															
BF80_6200	U2MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	IREN	RTSMD	—	UEN<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>	STSEL	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-7: UART1-2 REGISTERS MAP (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_6210	U2STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>							
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
BF80_6220	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register							
BF80_6230	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	RX8	Receive Register							
BF80_6240	U2BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	BRG<15:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-8: SPI1-2 REGISTERS MAP^(1,2)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0		
BF80_5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	
		15:0	ON	FRZ	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	—	
BF80_5810	SPI1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPIITBE	—	—	—	SPIRBF	
BF80_5820	SPI1BUF	31:16	DATA<31:0>																	
BF80_5830	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
BF80_5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—
		15:0	ON	FRZ	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	—	
BF80_5A10	SPI2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPIITBE	—	—	—	SPIRBF	
BF80_5A20	SPI2BUF	31:16	DATA<31:0>																	
BF80_5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

2: SPI2 Module is not present on PIC32MX420FXXXX/440FXXXX devices.

TABLE 4-9: ADC REGISTERS MAP

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_9000	AD1CON1 ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE
BF80_9010	AD1CON2 ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS
BF80_9020	AD1CON3 ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>							
BF80_9040	AD1CHS ⁽¹⁾	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>			
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BF80_9060	AD1PCFG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
BF80_9050	AD1CSSL ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0
BF80_9070	ADC1BUF0	31:16 15:0	ADC Result Word 0 (ADC1BUF0<31:0>)															
BF80_9080	ADC1BUF1	31:16 15:0	ADC Result Word 1 (ADC1BUF1<31:0>)															
BF80_9090	ADC1BUF2	31:16 15:0	ADC Result Word 2 (ADC1BUF2<31:0>)															
BF80_90A0	ADC1BUF3	31:16 15:0	ADC Result Word 3 (ADC1BUF3<31:0>)															
BF80_90B0	ADC1BUF4	31:16 15:0	ADC Result Word 4 (ADC1BUF4<31:0>)															
BF80_90C0	ADC1BUF5	31:16 15:0	ADC Result Word 5 (ADC1BUF5<31:0>)															
BF80_90D0	ADC1BUF6	31:16 15:0	ADC Result Word 6 (ADC1BUF6<31:0>)															
BF80_90E0	ADC1BUF7	31:16 15:0	ADC Result Word 7 (ADC1BUF7<31:0>)															
BF80_90F0	ADC1BUF8	31:16 15:0	ADC Result Word 8 (ADC1BUF8<31:0>)															
BF80_9100	ADC1BUF9	31:16 15:0	ADC Result Word 9 (ADC1BUF9<31:0>)															
BF80_9110	ADC1BUFA	31:16 15:0	ADC Result Word A (ADC1BUFA<31:0>)															
BF80_9120	ADC1BUFB	31:16 15:0	ADC Result Word B (ADC1BUFB<31:0>)															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-9: ADC REGISTERS MAP (CONTINUED)

SFR Virtual Addr	SFR Name	Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_9130	ADC1BUFC	31:16 15:0	ADC Result Word C (ADC1BUFC<31:0>)														
BF80_9140	ADC1BUFD	31:16 15:0	ADC Result Word D (ADC1BUFD<31:0>)														
BF80_9150	ADC1BUFE	31:16 15:0	ADC Result Word E (ADC1BUFE<31:0>)														
BF80_9160	ADC1BUFF	31:16 15:0	ADC Result Word F (ADC1BUFF<31:0>)														

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-10: DMA GLOBAL REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY

SFR Virtual Addr	SFR Name	Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0	
BF88_3000	DMACON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	ON	FRZ	SIDL	SUSPEND	—	—	—	—	—	—	—	—	—	—	—	—
BF88_3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	—	—	DMACH<1:0>
BF88_3020	DMAADDR	31:16	DMAADDR<31:0>															
		15:0																

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-11: DMA CRC REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY⁽¹⁾

SFR Virtual Addr	SFR Name	Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_3030	DCRCCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	PLEN<3:0>			—	—	CRCCEN	CRCCAPP	—	—	—	—
BF88_3040	DCRCDATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	DCRCDATA<15:0>														
BF88_3050	DCRCXOR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	DCRCXOR<15:0>														

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-12: DMA CHANNELS 0-3 REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>
BF88_3070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>							
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—
BF88_3080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF
BF88_3090	DCH0SSA	31:16	CHSSA<31:0>															
BF88_30A0	DCH0DSA	31:16	CHDSA<31:0>															
		15:0																
BF88_30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHSSIZ<7:0>															
BF88_30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHDSIZ<7:0>															
BF88_30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHSTR<7:0>															
BF88_30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHDPTR<7:0>															
BF88_30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHCSIZ<7:0>															
BF88_3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHCPTR<7:0>															
BF88_3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHPDAT<7:0>															
BF88_3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>
BF88_3130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>							
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—
BF88_3140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF
BF88_3150	DCH1SSA	31:16	CHSSA<31:0>															
BF88_3160	DCH1DSA	31:16	CHDSA<31:0>															
		15:0																

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR, and DCHxCPTR have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-12: DMA CHANNELS 0-3 REGISTERS MAP (CONTINUED) FOR PIC32MX340FXXX/360FXXX/440FXXX/460XXX DEVICES ONLY⁽¹⁾ (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_3170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>							
BF88_3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>							
BF88_3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHSPTR<7:0>							
BF88_31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>							
BF88_31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>							
BF88_31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>							
BF88_31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>							
BF88_31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>
BF88_31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHSIRQ<7:0>									CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—
BF88_3200	DCH2INT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE
BF88_3210	DCH2SSA	31:16																
		15:0	CHSSA<31:0>															
BF88_3220	DCH2DSA	31:16																
		15:0	CHDSA<31:0>															
BF88_3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>							
BF88_3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>							
BF88_3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHSPTR<7:0>							
BF88_3260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>							
BF88_3270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>							

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR, and DCHxCPTR have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-12: DMA CHANNELS 0-3 REGISTERS MAP (CONTINUED) FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY⁽¹⁾ (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>							
BF88_3290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>							
BF88_32A0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	
BF88_32B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CHSIRQ<7:0>									CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—
BF88_32C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE
BF88_32D0	DCH3SSA	31:16	CHSSA<31:0>															
		15:0	CHSSA<31:0>															
BF88_32E0	DCH3DSA	31:16	CHDSA<31:0>															
		15:0	CHDSA<31:0>															
BF88_32F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>							
BF88_3300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>							
BF88_3310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHSTR<7:0>							
BF88_3320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>							
BF88_3330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>							
BF88_3340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>							
BF88_3350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>							

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR, and DCHxCPTR have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-13: COMPARATOR REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_A000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	COE	CPOL	—	—	—	—	COUT	—	—	—	—	—	—	—	—
BF80_A010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	COE	CPOL	—	—	—	—	COUT	—	—	—	—	—	—	—	—
BF80_A060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	FRZ	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-14: COMPARATOR VOLTAGE REFERENCE REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_9800	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	—	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	—	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-15: FLASH CONTROLLER REGISTERS MAP

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_F400	NVMCON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	NVMWR	NVMWREN	NVMERR	LVDERR	LVDSTAT	—	—	—	—	—	—	—	—	—	—	—
BF80_F410	NVMKEY	31:16 15:0	NVMKEY<31:0>															
BF80_F420	NVMADDR ⁽¹⁾	31:16 15:0	NVMADDR<31:0>															
BF80_F430	NVMDATA	31:16 15:0	NVMDATA<31:0>															
BF80_F440	NVMSRC ADDR	31:16 15:0	NVMSRCADDR<31:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-16: SYSTEM CONTROL REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_F000	OSCCON	31:16	—	—	PLLODIV<2:0>			RCDIV<2:0>			—	SOSCRDY	—	PBDIV<1:0>		PLLMULT<2:0>		
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK	LOCK	SLPEN	CF	UFRGEN	SOSCEN	OSWEN
BF80_F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>					
BF80_0000	WDTCN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	—	—	—	—	—	—	—	—	—	SWDTPS<4:0>				—	WDTCCLR
BF80_F600	RCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	CM	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR
BF80_F610	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-17: PORT A-G REGISTERS MAP⁽¹¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_6000	TRISA ^(1,2,3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA<7:0>							
BF88_6010	PORTA ^(1,2,3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	RA15	RA14	—	—	—	RA10	RA9	—	RA<7:0>							
BF88_6020	LATA ^(1,2,3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA<7:0>							
BF88_6030	ODCA ^(1,2,3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ODCA15	ODCA14	—	—	—	ODCA10	ODCA9	—	ODCA<7:0>							
BF88_6040	TRISB ^(4,5)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TRISB<15:0>															
BF88_6050	PORTB ^(4,5)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	RB<15:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: TRISA, PORTA, LATA and ODCA registers are not implemented on 64-pin devices, and read as '0'.
Note 2: JTAG program/debug port is multiplexed with port pins RA0, RA1, RA4 and RA5 on 100-pin devices. At power-on-reset, these pins are controlled by the JTAG port. To use these pins for general purpose I/O, the user's application code must clear JTAGEN (DDPCON<3>) bit = 0. To use these pins for JTAG program/debug, the user's application code must maintain JTAGEN bit = 1.
Note 3: On specific 100-pin devices, the instruction TRACE port is multiplexed with PORTA pins RA6, RA7; PORTG pins RG12, RG13 and RG14. At Power-on Reset, these pins are general purpose I/O pins. To maintain these pins as general purpose I/O pins, the user's application code must maintain TROEN (DDPCON<2>) bit = 0. To use these pins as instruction TRACE pins, TROEN must be set = 1.
Note 4: JTAG program/debug port is multiplexed with port pins RB10, RB11, RB12 and RB13 on 64-pin devices. At power-on-reset, these pins are controlled by the JTAG port. To use these pins for general purpose I/O, the user's application code must clear JTAGEN (DDPCON<3>) bit = 0. To use these pins for JTAG program/debug, the user's application code must maintain JTAGEN bit = 1.
Note 5: Port Pin RB3 is not available as a general purpose I/O pin when the USB module is enabled.
Note 6: Not implemented on 64-pin devices. Read as '0'.
Note 7: Not implemented on 64-pin USB devices. Read as '0'.
Note 8: Not implemented on 100-pin USB devices. Read as '0'.
Note 9: Not available as a general purpose I/O pin when USB module is enabled.
Note 10: Not available as a general purpose I/O pin when USB module is enabled. Input only when the USB module is disabled.
Note 11: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-17: PORT A-G REGISTERS MAP⁽¹¹⁾ (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_6060	LATB ^(4,5)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	LATB<15:0>															
BF88_6070	ODCB ^(4,5)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ODCB<15:0>															
BF88_6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	TRISC4 ⁽⁶⁾	TRISC3 ⁽⁶⁾	TRISC2 ⁽⁶⁾	TRISC1 ⁽⁶⁾
BF88_6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	RC4 ⁽⁶⁾	RC3 ⁽⁶⁾	RC2 ⁽⁶⁾	RC1 ⁽⁶⁾
BF88_60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	LATC4 ⁽⁶⁾	LATC3 ⁽⁶⁾	LATC2 ⁽⁶⁾	LATC1 ⁽⁶⁾
BF88_60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	ODCC4 ⁽⁶⁾	ODCC3 ⁽⁶⁾	ODCC2 ⁽⁶⁾	ODCC1 ⁽⁶⁾
BF88_60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TRISD15 ⁽⁶⁾	TRISD14 ⁽⁶⁾	TRISD13 ⁽⁶⁾	TRISD12 ⁽⁶⁾	TRISD<11:8>					TRISD<7:0>						
BF88_60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	RD15 ⁽⁶⁾	RD14 ⁽⁶⁾	RD13 ⁽⁶⁾	RD12 ⁽⁶⁾	RD<11:8>					RD<7:0>						
BF88_60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	LATD15 ⁽⁶⁾	LATD14 ⁽⁶⁾	LATD13 ⁽⁶⁾	LATD12 ⁽⁶⁾	LATD<11:8>					LATD<7:0>						
BF88_60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ODCD15 ⁽⁶⁾	ODCD14 ⁽⁶⁾	ODCD13 ⁽⁶⁾	ODCD12 ⁽⁶⁾	ODCD<11:8>					ODCD<7:0>						
BF88_6100	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	TRISE9 ⁽⁶⁾	TRISE8 ⁽⁶⁾	TRISE<7:0>						
BF88_6110	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	RE9 ⁽⁶⁾	RE8 ⁽⁶⁾	RE<7:0>						
BF88_6120	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	LATE9 ⁽⁶⁾	LATE8 ⁽⁶⁾	LATE<7:0>						

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: TRISA, PORTA, LATA and ODCA registers are not implemented on 64-pin devices, and read as '0'.
 - 2: JTAG program/debug port is multiplexed with port pins RA0, RA1, RA4 and RA5 on 100-pin devices. At power-on-reset, these pins are controlled by the JTAG port. To use these pins for general purpose I/O, the user's application code must clear JTAGEN (DDPCON<3>) bit = 0. To use these pins for JTAG program/debug, the user's application code must maintain JTAGEN bit = 1.
 - 3: On specific 100-pin devices, the instruction TRACE port is multiplexed with PORTA pins RA6, RA7; PORTG pins RG12, RG13 and RG14. At Power-on Reset, these pins are general purpose I/O pins. To maintain these pins as general purpose I/O pins, the user's application code must maintain TROEN (DDPCON<2>) bit = 0. To use these pins as instruction TRACE pins, TROEN must be set = 1.
 - 4: JTAG program/debug port is multiplexed with port pins RB10, RB11, RB12 and RB13 on 64-pin devices. At power-on-reset, these pins are controlled by the JTAG port. To use these pins for general purpose I/O, the user's application code must clear JTAGEN (DDPCON<3>) bit = 0. To use these pins for JTAG program/debug, the user's application code must maintain JTAGEN bit = 1.
 - 5: Port Pin RB3 is not available as a general purpose I/O pin when the USB module is enabled.
 - 6: Not implemented on 64-pin devices. Read as '0'.
 - 7: Not implemented on 64-pin USB devices. Read as '0'.
 - 8: Not implemented on 100-pin USB devices. Read as '0'.
 - 9: Not available as a general purpose I/O pin when USB module is enabled.
 - 10: Not available as a general purpose I/O pin when USB module is enabled. Input only when the USB module is disabled.
 - 11: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-17: PORT A-G REGISTERS MAP⁽¹¹⁾ (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_6130	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	ODCE9 ⁽⁶⁾	ODCE8 ⁽⁶⁾	ODCE<7:0>						
BF88_6140	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	TRISF13 ⁽⁶⁾	TRISF12 ⁽⁶⁾	—	—	—	—	TRISF8 ⁽⁶⁾	TRISF7 ^(6,8)	TRISF6 ^(7,8)	TRISF5	TRISF4	TRISF3	TRISF2 ⁽⁷⁾	TRISF1
BF88_6150	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	RF13 ⁽⁶⁾	RF12 ⁽⁶⁾	—	—	—	—	RF8 ⁽⁶⁾	RF7 ^(6,8)	RF6 ^(7,8)	RF5	RF4	RF3 ⁽⁹⁾	RF2 ⁽⁷⁾	RF1
BF88_6160	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	LATF13 ⁽⁶⁾	LATF12 ⁽⁶⁾	—	—	—	—	LATF8 ⁽⁶⁾	LATF7 ^(6,8)	LATF6 ^(7,8)	LATF5	LATF4	LATF3	LATF2 ⁽⁷⁾	LATF1
BF88_6170	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	ODCF13 ⁽⁶⁾	ODCF12 ⁽⁶⁾	—	—	—	—	ODCF8 ⁽⁶⁾	ODCF7 ^(6,8)	ODCF6 ^(7,8)	ODCF5	ODCF4	ODCF3	ODCF2 ⁽⁷⁾	ODCF1
BF88_6180	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	TRISG15 ⁽⁶⁾	TRISG14 ⁽⁶⁾	TRISG13 ⁽⁶⁾	TRISG12 ⁽⁶⁾	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	TRISG1 ⁽⁶⁾
BF88_6190	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	RG15 ⁽⁶⁾	RG14 ⁽⁶⁾	RG13 ⁽⁶⁾	RG12 ⁽⁶⁾	—	—	—	RG9	RG8	RG7	RG6	—	—	RG3 ⁽¹⁰⁾	RG2 ⁽¹⁰⁾	RG1 ⁽⁶⁾
BF88_61A0	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	LATG15 ⁽⁶⁾	LATG14 ⁽⁶⁾	LATG13 ⁽⁶⁾	LATG12 ⁽⁶⁾	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	LATG1 ⁽⁶⁾
BF88_61B0	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ODCG15 ⁽⁶⁾	ODCG14 ⁽⁶⁾	ODCG13 ⁽⁶⁾	ODCG12 ⁽⁶⁾	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	ODCG3	ODCG2	ODCG1 ⁽⁶⁾

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** TRISA, PORTA, LATA and ODCA registers are not implemented on 64-pin devices, and read as '0'.
- 2:** JTAG program/debug port is multiplexed with port pins RA0, RA1, RA4 and RA5 on 100-pin devices. At power-on-reset, these pins are controlled by the JTAG port. To use these pins for general purpose I/O, the user's application code must clear JTAGEN (DDPCON<3>) bit = 0. To use these pins for JTAG program/debug, the user's application code must maintain JTAGEN bit = 1.
- 3:** On specific 100-pin devices, the instruction TRACE port is multiplexed with PORTA pins RA6, RA7; PORTG pins RG12, RG13 and RG14. At Power-on Reset, these pins are general purpose I/O pins. To maintain these pins as general purpose I/O pins, the user's application code must maintain TROEN (DDPCON<2>) bit = 0. To use these pins as instruction TRACE pins, TROEN must be set = 1.
- 4:** JTAG program/debug port is multiplexed with port pins RB10, RB11, RB12 and RB13 on 64-pin devices. At power-on-reset, these pins are controlled by the JTAG port. To use these pins for general purpose I/O, the user's application code must clear JTAGEN (DDPCON<3>) bit = 0. To use these pins for JTAG program/debug, the user's application code must maintain JTAGEN bit = 1.
- 5:** Port Pin RB3 is not available as a general purpose I/O pin when the USB module is enabled.
- 6:** Not implemented on 64-pin devices. Read as '0'.
- 7:** Not implemented on 64-pin USB devices. Read as '0'.
- 8:** Not implemented on 100-pin USB devices. Read as '0'.
- 9:** Not available as a general purpose I/O pin when USB module is enabled.
- 10:** Not available as a general purpose I/O pin when USB module is enabled. Input only when the USB module is disabled.
- 11:** All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-18: CHANGE NOTICE AND PULL-UP REGISTERS MAP⁽²⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_61C0	CNCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** CNEN and CNPUE bit(s) are not implemented on 64-pin devices, and read as '0'.
- 2:** All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-18: CHANGE NOTICE AND PULL-UP REGISTERS MAP⁽²⁾ (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0	
BF88_61D0	CNEN	31:16	—	—	—	—	—	—	—	—	—	—	—	CNEN21 ⁽¹⁾	CNEN20 ⁽¹⁾	CNEN19 ⁽¹⁾	CNEN18	CNEN17	CNEN16
		15:0	CNEN<15:0>																
BF88_61E0	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	CNPUE21 ⁽¹⁾	CNPUE20 ⁽¹⁾	CNPUE19 ⁽¹⁾	CNPUE18	CNPUE17	CNPUE16
		15:0	CNPUE<15:0>																

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: CNEN and CNPUE bit(s) are not implemented on 64-pin devices, and read as '0'.

Note 2: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-19: PARALLEL MASTER PORT REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_7000	PMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	ADRMUX<1:0>		PMP TTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP
BF80_7010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>			WAITE<1:0>		
BF80_7020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	CS2EN/A15	CS1EN/A14	ADDR<13:0>													
BF80_7030	PMDOUT	31:16	DATAOUT<31:0>															
BF80_7040	PMDIN	31:16	DATAIN<31:0>															
		15:0																
BF80_7050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	PTEN<15:0>															
BF80_7060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-20: PROGRAMMING AND DIAGNOSTICS REGISTERS MAP

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_F200	DDPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	DDPUSB	DDPU1	DDPU2	DDPSPI1	JTAGEN	TROEN	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-21: PREFETCH REGISTERS MAP

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_4000	CHECON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHECOH
		15:0	—	—	—	—	—	—	—	DCSZ<1:0>	—	—	—	PREFEN<1:0>	—	—	—	—
BF88_4010	CHEACC ⁽¹⁾	31:16	CHEWEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BF88_4020	CHETAG ⁽¹⁾	31:16	LTAG BOOT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BF88_4030	CHEMSK ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BF88_4040	CHEW0	31:16	CHEW0<31:0>															
BF88_4050	CHEW1	31:16	CHEW1<31:0>															
BF88_4060	CHEW2	31:16	CHEW2<31:0>															
BF88_4070	CHEW3	31:16	CHEW3<31:0>															
BF88_4080	CHELRU	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BF88_4090	CHEHIT	31:16	CHEHIT<31:0>															
BF88_40A0	CHEMIS	31:16	CHEMIS<31:0>															
BF88_40C0	CHEPFABT	31:16	CHEPFABT<31:0>															
		15:0																

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV Registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-22: RTCC REGISTERS MAP⁽¹⁾

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_0200	RTCCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	RTSEC SEL	RTC CLKON	—	—	RTCWREN	RTCSYNC	HALFSEC
BF80_0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	ALRMEN	CHIME	PIV	ALRM SYNC	AMASK<3:0>					ARPT<7:0>						

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-22: RTCC REGISTERS MAP⁽¹⁾ (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_0220	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>			
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—
BF80_0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>			
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>			
BF80_0240	ALRMTIME	31:16	MIN10<3:0>				MIN01<3:0>				MIN10<3:0>				MIN01<3:0>			
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—
BF80_0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>			
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>			

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-23: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BFC0_2FF0	DEVCFG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	USERID15	USERID14	USERID13	USERID12	USERID11	USERID10	USERID9	USERID8	USERID7	USERID6	USERID5	USERID4	USERID3	USERID2	USERID1	USERID0
BFC0_2FF4	DEVCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>			
		15:0	FUPLLEN ⁽¹⁾	—	—	—	—	FUPLLDIV<2:0> ⁽¹⁾				—	FPLLMULT<2:0>		FPLLDIV<2:0>			
BFC0_2FF8	DEVCFG1	31:16	—	—	—	—	—	—	—	—	FWDTEN	—	—	WDTPS<4:0>				
		15:0	FCKSM<1:0>		FPBDIV<1:0>		—	OSC IOFNC	POSCMD<1:0>		IESO	—	FSOSCEN	—	—	FNOSC<2:0>		
BFC0_2FFC	DEVCFG0	31:16	—	—	—	CP	—	—	—	BWP	—	—	—	—	PWP19	PWP18	PWP17	PWP16
		15:0	PWP15	PWP14	PWP13	PWP12	—	—	—	—	—	—	—	—	ICSESEL	—	DEBUG<1:0>	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are only available on PIC32MX4XX devices.

TABLE 4-24: DEVICE AND REVISION ID SUMMARY

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF80_F220	DEVID	31:16	VER<3:0>				DEVID<27:16>											
		15:0	DEVID<15:0>															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: USB REGISTERS MAP

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_5040	U1OTGIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—
BF88_5050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—
BF88_5060	U1OTG STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—
BF88_5070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPUL DWN	DMPUL DWN	VBUSON	OTGEN	VBUSCHG
BF88_5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	UACTPND	—	—	USLPGRD	—	—	USUS PEND
BF88_5200	U1IR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUME IF	IDLEIF	TRNIF	SOFIF	UERRIF
BF88_5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUME IE	IDLEIE	TRNIE	SOFIE	UERRIE
BF88_5220	U1EIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF
BF88_5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE EOFEE
BF88_5240	U1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BF88_5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	JSTATE	SE0	PKTDIS TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST
BF80_5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	LSPDEN	—	—	—	—	—	—
BF88_5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BF88_5280	U1FRML	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BF88_5290	U1FRMH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: USB REGISTERS MAP (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_52A0	U1TOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	PID<3:0>			EP<3:0>				
BF88_52B0	U1SOF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	CNT<7:0>							
BF88_52C0	U1BDTP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	BDTPTRH<7:0>							
BF88_52D0	U1BDTP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	BDTPTRU<7:0>							
BF88_52E0	U1CNFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	UTEYE	UOEMON	USBFRZ	USBSIDL	—	—	—	—
BF88_5300	U1EP0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	LSPD	RETRYDIS	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5310	U1EP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5320	U1EP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5330	U1EP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5340	U1EP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5350	U1EP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5360	U1EP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5370	U1EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5380	U1EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
BF88_5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: USB REGISTERS MAP (CONTINUED)

SFR Virtual Addr	SFR Name		Bits 31/15	Bits 30/14	Bits 29/13	Bits 28/12	Bits 27/11	Bits 26/10	Bits 25/9	Bits 24/8	Bits 23/7	Bits 22/6	Bits 21/5	Bits 20/4	Bits 19/3	Bits 18/2	Bits 17/1	Bits 16/0
BF88_53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL
BF88_53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL
BF88_53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL
BF88_53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL
BF88_53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL
BF88_53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	EPCON DIS	EPRXEN	EPTXEN	EPSTALL

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the *"PIC32MX Family Reference Manual"* **Section 5. "Flash Program Memory"** (DS61121) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

PIC32MX3XX/4XX devices contain an internal program Flash memory for executing user code. There are three methods by which the user can program this memory:

1. Run-Time Self Programming (RTSP)
2. In-Circuit Serial Programming™ (ICSP™)
3. EJTAG Programming

RTSP is performed by software executing from either Flash or RAM memory. EJTAG is performed using the EJTAG port of the device and a EJTAG capable programmer. ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP. RTSP techniques are described in this chapter. The ICSP and EJTAG methods are described in the *"PIC32MX3XX/4XX Programming Specification"* (DS61145) document, which may be downloaded from the Microchip web site.

PIC32MX3XX/4XX

NOTES:

6.0 RESETS

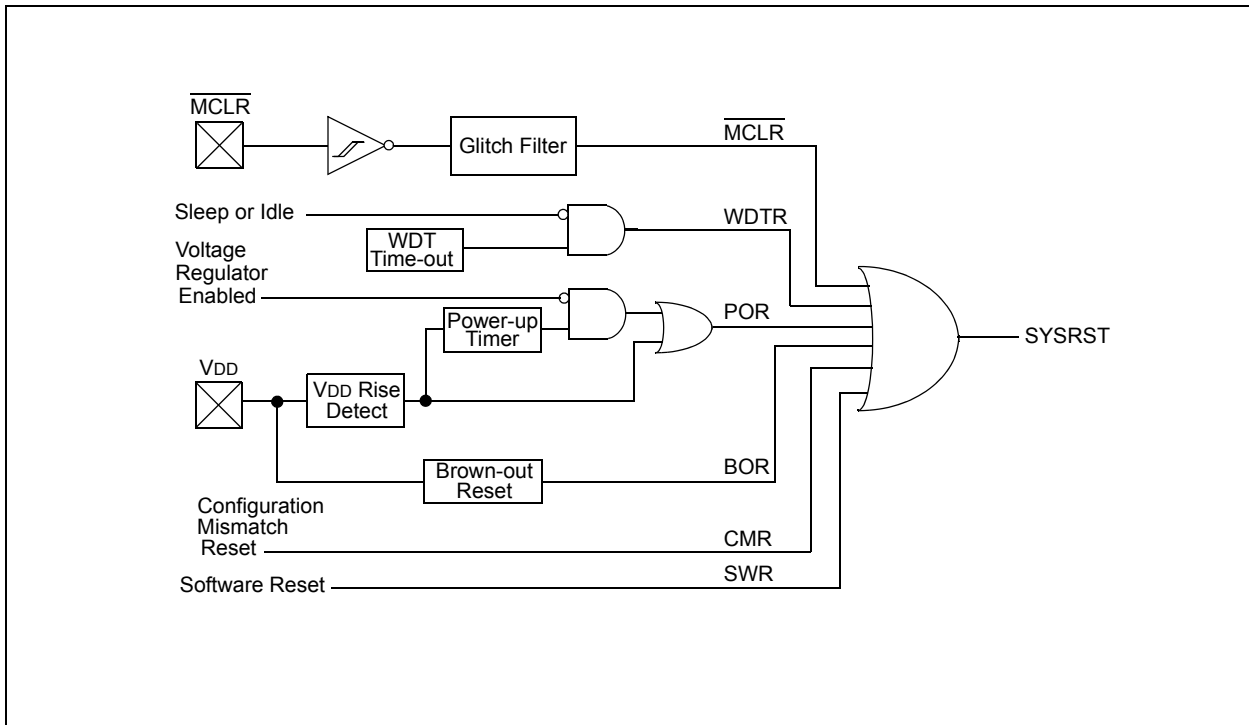
Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” **Section 7. “Resets”** (DS61118) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Master Clear Reset Pin
- SWR: Software Reset
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

7.0 INTERRUPT CONTROLLER

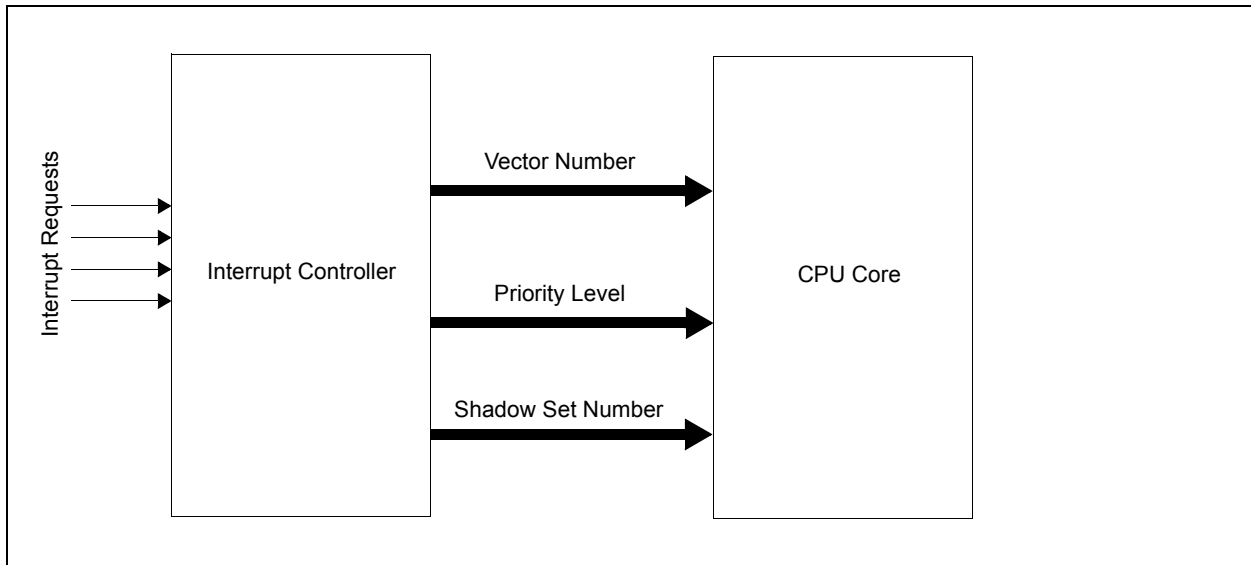
Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” **Section 8. “Interrupt Controller”** (DS61108) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

PIC32MX3XX/4XX devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX3XX/4XX interrupts module includes the following features:

- Up to 96 interrupt sources
- Up to 64 interrupt vectors
- Single and Multi-Vector mode operations
- 5 external interrupts with edge polarity control
- Interrupt proximity timer
- Module Freeze in Debug mode
- 7 user-selectable priority levels for each vector
- 4 user-selectable subpriority levels within each priority
- Dedicated shadow set for highest priority level
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

FIGURE 7-1: INTERRUPT CONTROLLER MODULE



Note: Several of the registers cited in this section are not in the interrupt controller module. These registers (and bits) are associated with the CPU. Details about them are available in **Section 3.0 “PIC32MX MCU”**.

To avoid confusion, a typographic distinction is made for registers in the CPU. The register names in this section, and all other sections of this manual, are signified by uppercase letters only. CPU register names are signified by upper and lowercase letters. For example, INTSTAT is an Interrupts register; whereas, IntCtl is a CPU register.

PIC32MX3XX/4XX

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION

Interrupt Source ⁽¹⁾	IRQ	Vector Number	Interrupt Bit Location			
			Flag	Enable	Priority	Subpriority
Highest Natural Order Priority						
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>
INT0 – External Interrupt 0	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>
IC1 – Input Capture 1	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>
OC1 – Output Compare 1	6	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>
INT1 – External Interrupt 1	7	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>
T2 – Timer2	8	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>
IC2 – Input Capture 2	9	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>
OC2 – Output Compare 2	10	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>
INT2 – External Interrupt 2	11	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>
T3 – Timer3	12	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>
IC3 – Input Capture 3	13	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>
OC3 – Output Compare 3	14	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>
INT3 – External Interrupt 3	15	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>
T4 – Timer4	16	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>
IC4 – Input Capture 4	17	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>
OC4 – Output Compare 4	18	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>
INT4 – External Interrupt 4	19	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>
T5 – Timer5	20	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>
IC5 – Input Capture 5	21	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>
OC5 – Output Compare 5	22	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>
SPI1E – SPI1 Fault	23	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>
SPI1TX – SPI1 Transfer Done	24	23	IFS0<24>	IEC0<24>	IPC5<28:26>	IPC5<25:24>
SPI1RX – SPI1 Receive Done	25	23	IFS0<25>	IEC0<25>	IPC5<28:26>	IPC5<25:24>
U1E – UART1 Error	26	24	IFS0<26>	IEC0<26>	IPC6<4:2>	IPC6<1:0>
U1RX – UART1 Receiver	27	24	IFS0<27>	IEC0<27>	IPC6<4:2>	IPC6<1:0>
U1TX – UART1 Transmitter	28	24	IFS0<28>	IEC0<28>	IPC6<4:2>	IPC6<1:0>
I2C1B – I2C1 Bus Collision Event	29	25	IFS0<29>	IEC0<29>	IPC6<12:10>	IPC6<9:8>
I2C1S – I2C1 Slave Event	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>
I2C1M – I2C1 Master Event	31	25	IFS0<31>	IEC0<31>	IPC6<12:10>	IPC6<9:8>
CN – Input Change Interrupt	32	26	IFS1<0>	IEC1<0>	IPC6<20:18>	IPC6<17:16>
AD1 – ADC1 Convert Done	33	27	IFS1<1>	IEC1<1>	IPC6<28:26>	IPC6<25:24>
PMP – Parallel Master Port	34	28	IFS1<2>	IEC1<2>	IPC7<4:2>	IPC7<1:0>
CMP1 – Comparator Interrupt	35	29	IFS1<3>	IEC1<3>	IPC7<12:10>	IPC7<9:8>
CMP2 – Comparator Interrupt	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>

Note 1: Not all interrupt sources are available on all devices.

See Table 1: “PIC32MX General Purpose – Features” and Table 2: “PIC32MX USB – Features” for available peripherals.

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	IRQ	Vector Number	Interrupt Bit Location			
			Flag	Enable	Priority	Subpriority
Highest Natural Order Priority						
SPI2E – SPI2 Fault	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>
SPI2TX – SPI2 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>
SPI2RX – SPI2 Receive Done	39	31	IFS1<7>	IEC1<7>	IPC7<28:26>	IPC7<25:24>
U2E – UART2 Error	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>
U2RX – UART2 Receiver	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>
U2TX – UART2 Transmitter	42	32	IFS1<10>	IEC1<10>	IPC8<4:2>	IPC8<1:0>
I2C2B – I2C2 Bus Collision Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>
I2C2S – I2C2 Slave Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>
I2C2M – I2C2 Master Event	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>
FSCM – Fail-Safe Clock Monitor	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>
RTCC – Real-Time Clock	47	35	IFS1<15>	IEC1<15>	IPC8<28:26>	IPC8<25:24>
DMA0 – DMA Channel 0	48	36	IFS1<16>	IEC1<16>	IPC9<4:2>	IPC9<1:0>
DMA1 – DMA Channel 1	49	37	IFS1<17>	IEC1<17>	IPC9<12:10>	IPC9<9:8>
DMA2 – DMA Channel 2	50	38	IFS1<18>	IEC1<18>	IPC9<20:18>	IPC9<17:16>
DMA3 – DMA Channel 3	51	39	IFS1<19>	IEC1<19>	IPC9<28:26>	IPC9<25:24>
FCE – Flash Control Event	56	44	IFS1<24>	IEC1<24>	IPC11<4:2>	IPC11<1:0>
USB	57	45	IFS1<25>	IEC1<25>	IPC11<12:10>	IPC11<9:8>
(Reserved)						
Lowest Natural Order Priority						

Note 1: Not all interrupt sources are available on all devices.
See Table 1: “PIC32MX General Purpose – Features” and Table 2: “PIC32MX USB – Features” for available peripherals.

PIC32MX3XX/4XX

NOTES:

8.0 OSCILLATOR CONFIGURATION

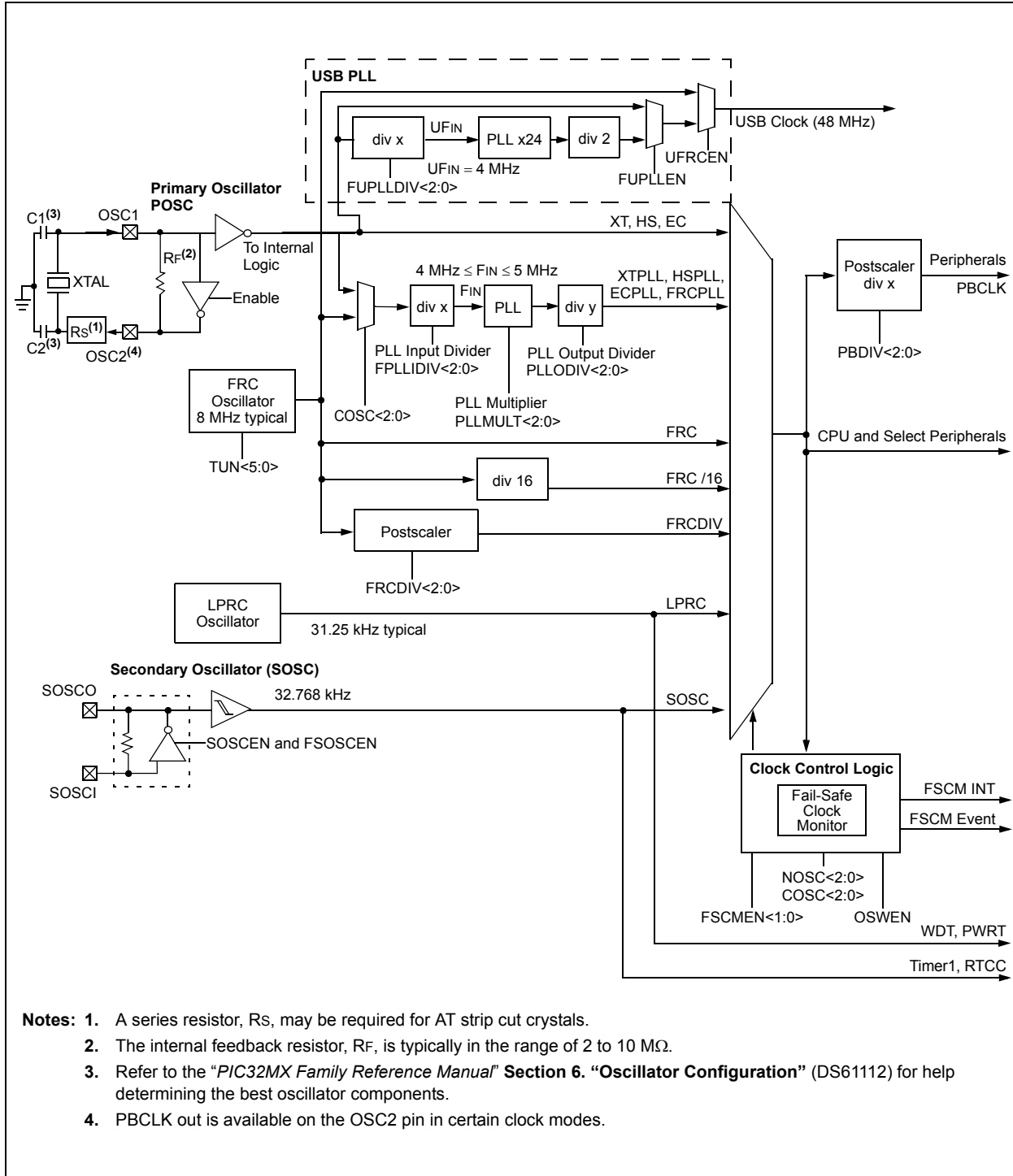
Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “*PIC32MX Family Reference Manual*” **Section 6. “Oscillator Configuration”** (DS61112) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

The PIC32MX oscillator system has the following modules and features:

- A total of four external and internal oscillator options as clock sources
- On-chip PLL (phase-locked loop) with user-selectable input divider, multiplier, and output divider to boost operating frequency on select internal and external oscillator sources
- On-chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated on-chip PLL for USB peripheral

PIC32MX3XX/4XX

FIGURE 8-1: PIC32MX3XX/4XX FAMILY CLOCK DIAGRAM



- Notes:**
1. A series resistor, Rs, may be required for AT strip cut crystals.
 2. The internal feedback resistor, RF, is typically in the range of 2 to 10 MΩ.
 3. Refer to the "PIC32MX Family Reference Manual" Section 6. "Oscillator Configuration" (DS61112) for help determining the best oscillator components.
 4. PBCLK out is available on the OSC2 pin in certain clock modes.

9.0 PREFETCH CACHE

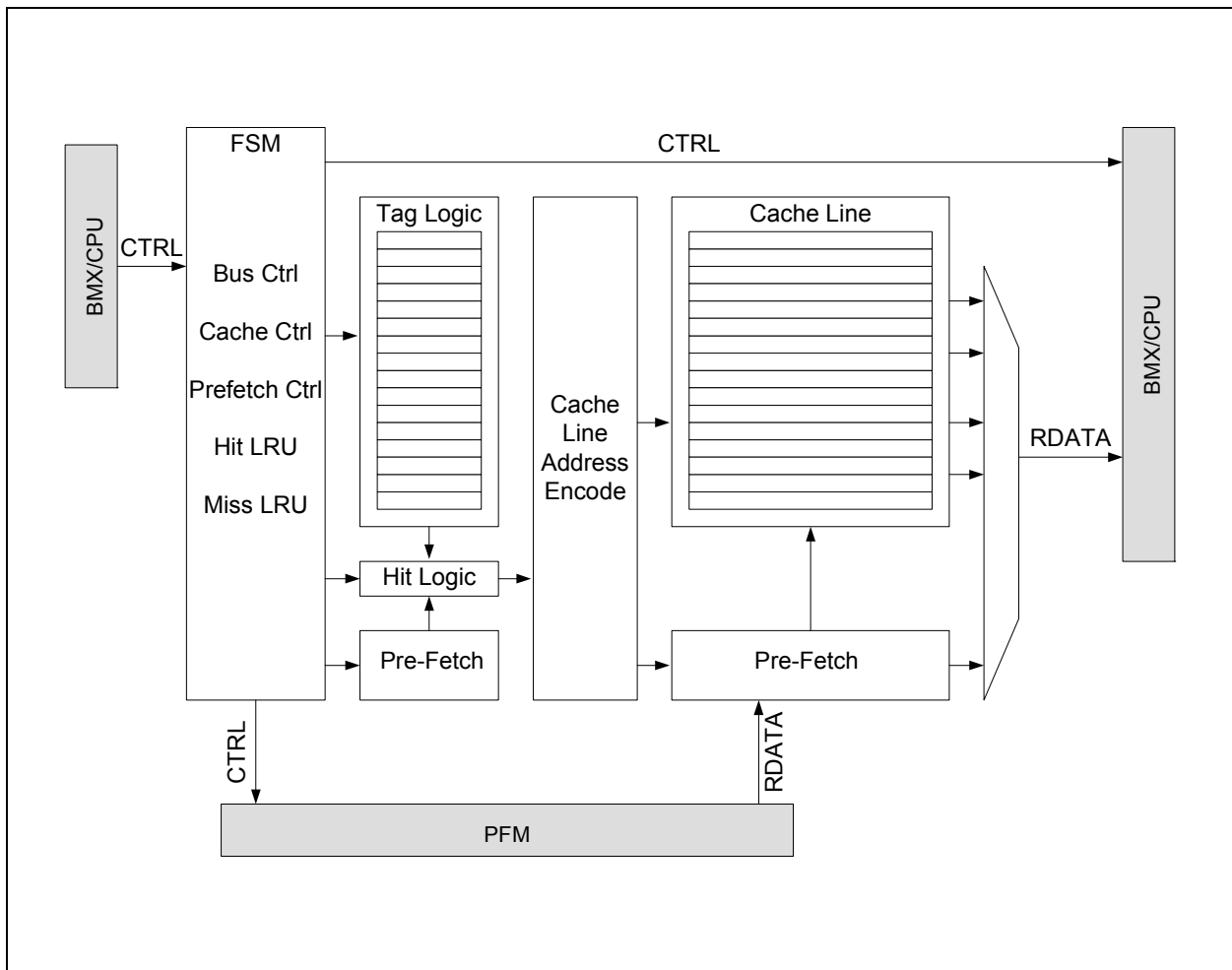
Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” **Section 4. “Prefetch Cache”** (DS61119) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

Prefetch cache increases performance for applications executing out of the cacheable program flash memory regions by implementing instruction caching, constant data caching, and instruction prefetching.

9.1 Features

- 16 Fully Associative Lockable Cache Lines
- 16-byte Cache Lines
- Up to 4 Cache Lines Allocated to Data
- 2 Cache Lines with Address Mask to hold repeated instructions
- Pseudo LRU replacement policy
- All Cache Lines are software writable
- 16-byte parallel memory fetch
- Predictive Instruction Prefetch

FIGURE 9-1: PREFETCH MODULE BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 31. “Direct Memory Access (DMA) Controller” (DS61117) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

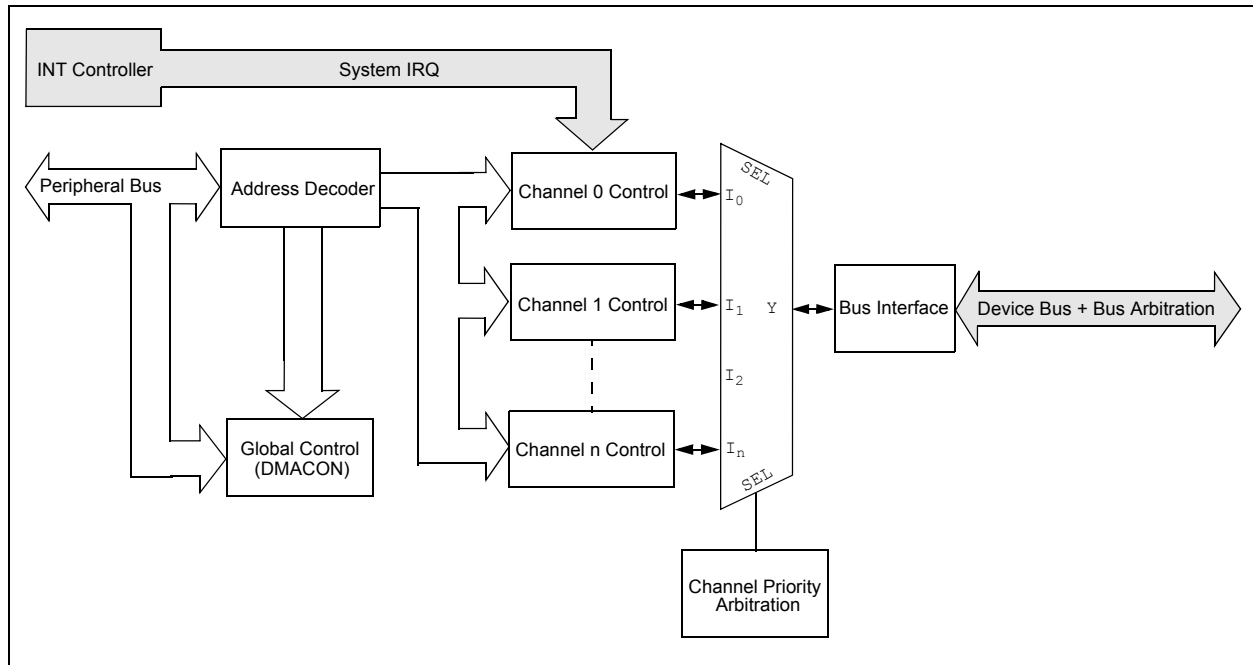
The PIC32MX Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32MX (such as Peripheral Bus (PBUS) devices: SPI, UART, I²C™, etc.) or memory itself.

Following are some of the key features of the DMA controller module:

- Four Identical Channels, each featuring:
 - Auto-Increment Source and Destination Address Registers
 - Source and Destination Pointers
 - Memory to Memory and Memory to Peripheral Transfers
- Automatic Word-Size Detection:
 - Transfer Granularity, down to byte level
 - Bytes need not be word-aligned at source and destination

- Fixed Priority Channel Arbitration
- Flexible DMA Channel Operating Modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- Flexible DMA Requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Pattern (data) match transfer termination
- Multiple DMA Channel Status Interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half-full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA Debug Support Features:
 - Most recent address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- CRC Generation Module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

11.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “*PIC32MX Family Reference Manual*” **Section 27. “USB On-The-Go (OTG)”** (DS61126) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device, or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32MX USB OTG module is presented in Figure 11-1.

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers, and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

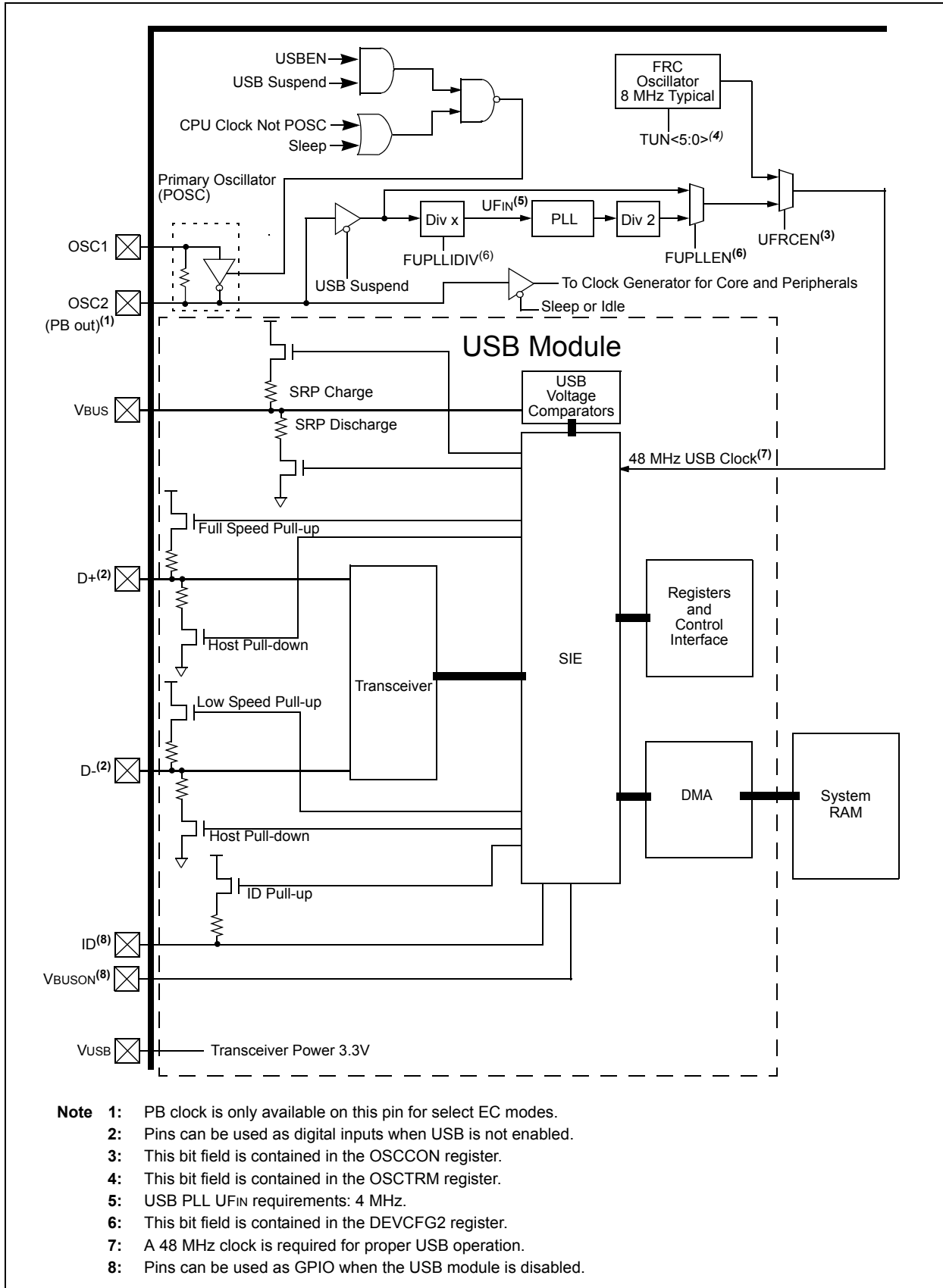
The PIC32MX USB module includes the following features:

- USB Full-Speed Support for Host and Device
- Low-Speed Host Support
- USB OTG Support
- Integrated Signaling Resistors
- Integrated Analog Comparators for VBUS Monitoring
- Integrated USB Transceiver
- Transaction Handshaking Performed by Hardware
- Endpoint Buffering Anywhere in System RAM
- Integrated DMA to Access System RAM and Flash

Note: IMPORTANT: The implementation and use of the USB specifications, as well as other third-party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

PIC32MX3XX/4XX

FIGURE 11-1: PIC32MX3XX/4XX FAMILY USB INTERFACE DIAGRAM



12.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 12. “I/O Ports” (DS61120) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s).

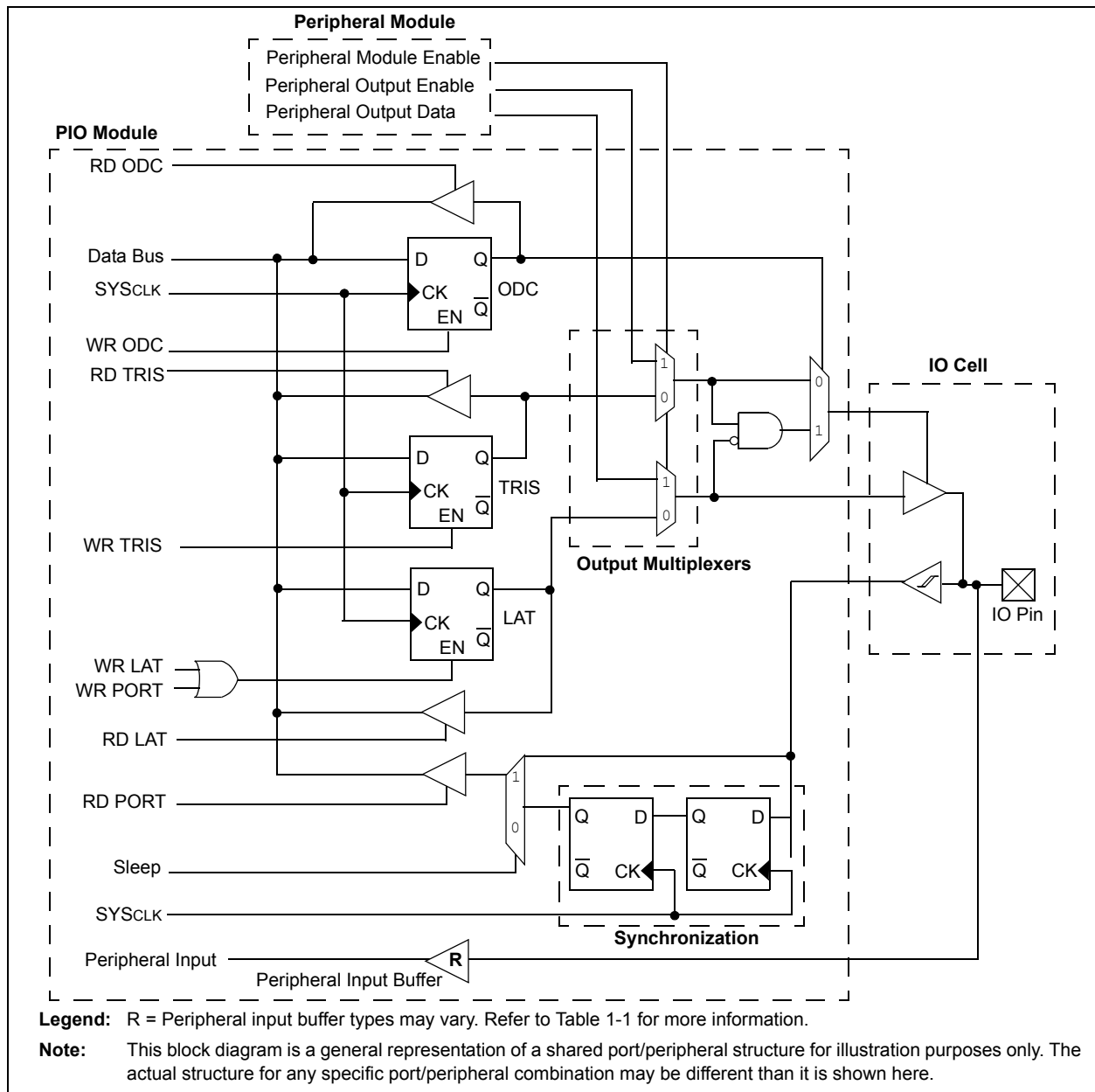
These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Following are some of the key features of this module:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up enable/disable
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Figure 12-1 shows a block diagram of a typical multiplexed I/O port.

FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



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12.1 Parallel I/O (PIO) Ports

All port pins have three registers (TRIS, LAT, and PORT) that are directly associated with their operation.

TRIS is a data direction or tri-state control register that determines whether a digital pin is an input or an output. Setting a TRISx register bit = 1 configures the corresponding I/O pin as an input; setting a TRISx register bit = 0 configures the corresponding I/O pin as an output. All port I/O pins are defined as inputs after a device Reset. Certain I/O pins are shared with analog peripherals and default to analog inputs after a device Reset.

PORT is a register used to read the current state of the signal applied to the port I/O pins. Writing to a PORTx register performs a write to the port's latch, LATx register, latching the data to the port's I/O pins.

LAT is a register used to write data to the port I/O pins. The LATx latch register holds the data written to either the LATx or PORTx registers. Reading the LATx latch register reads the last value written to the corresponding port or latch register.

Not all port I/O pins are implemented on some devices, therefore, the corresponding PORTx, LATx and TRISx register bits will read as zeros.

12.1.1 CLR, SET AND INV REGISTERS

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

To set PORTC bit 0, write to the LATSET register:

```
LATCSET = 0x0001;
```

To clear PORTC bit 0, write to the LATCLR register:

```
LATCCLR = 0x0001;
```

To toggle PORTC bit 0, write to the LATINV register:

```
LATCINV = 0x0001;
```

Note: Using a PORTxINV register to toggle a bit is recommended because the operation is performed in hardware atomically, using fewer instructions as compared to the traditional read-modify-write method shown below:

```
PORTC ^= 0x0001;
```

12.1.2 DIGITAL INPUTS

Pins are configured as digital inputs by setting the corresponding TRIS register bits = 1. When configured as inputs, they are either TTL buffers or Schmitt Triggers. Several digital pins share functionality with analog inputs and default to the analog inputs at POR. Setting the corresponding bit in the AD1PCFG register = 1 enables the pin as a digital pin.

Digital only pins are capable of input voltages up to 5.5V. Any pin that shares digital and analog functionality is limited to voltages up to $V_{DD} + 0.3V$.

TABLE 12-1: MAXIMUM INPUT PIN VOLTAGES

Input Pin Mode(s)	V_{IH} (max)
Digital Only	$V_{IH} = 5.5v$
Digital + Analog	$V_{IH} = V_{DD} + 0.03v$
Analog	$V_{IH} = V_{DD} + 0.03v$

Note: Refer to **Section 28.0 "Electrical Characteristics"** regarding the V_{IH} specification.

Note: Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

12.1.3 ANALOG INPUTS

Certain pins can be configured as analog inputs used by the ADC and Comparator modules. Setting the corresponding bits in the AD1PCFG register = 0 enables the pin as an analog input pin and must have the corresponding TRIS bit set = 1 (input). If the TRIS bit is cleared = 0 (output), the digital output level (V_{OH} or V_{OL}) will be converted. Any time a port I/O pin is configured as analog, its digital input is disabled and the corresponding PORTx register bit will read '0'. The AD1PCFG Register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

12.1.4 DIGITAL OUTPUTS

Pins are configured as digital outputs by setting the corresponding TRIS register bits = 0. When configured as digital outputs, these pins are CMOS drivers or can be configured as open drain outputs by setting the corresponding bits in the ODCx Open-Drain Configuration register.

Digital output pin voltage is limited to V_{DD} .

12.1.5 ANALOG OUTPUTS

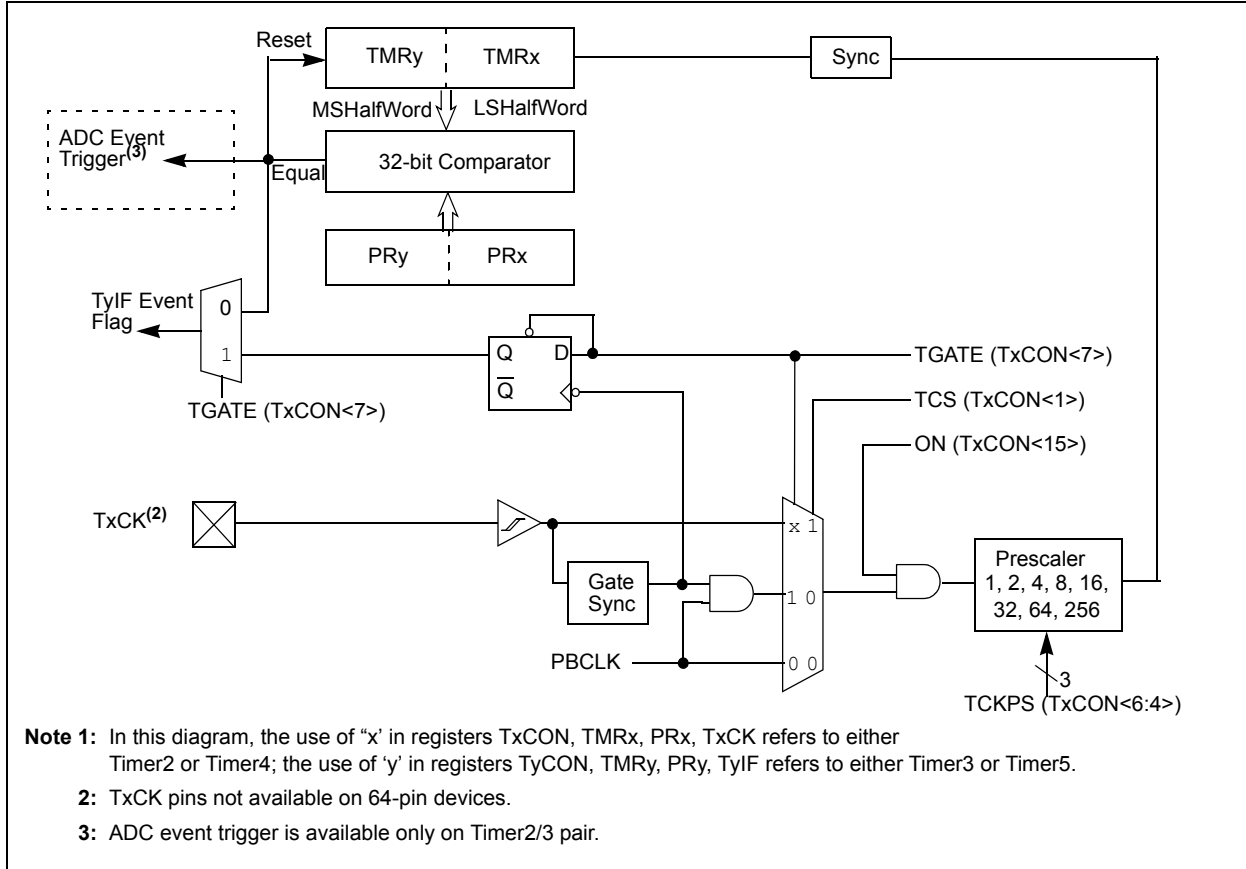
Certain pins can be configured as analog outputs, such as the CVREF output voltage used by the comparator module. Configuring the Comparator Reference module to provide this output will present the analog output voltage on the pin, independent of the TRIS register setting for the corresponding pin.

PIC32MX3XX/4XX

NOTES:

PIC32MX3XX/4XX

FIGURE 14-2: TIMER2/3, 4/5 BLOCK DIAGRAM (32-BIT)



15.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 15. “Input Capture” (DS61122) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement. The PIC32MX3XX/4XX devices support up to five input capture channels.

The input capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

1. Simple Capture Event modes
 - Capture timer value on every falling edge of input at ICx pin
 - Capture timer value on every rising edge of input at ICx pin

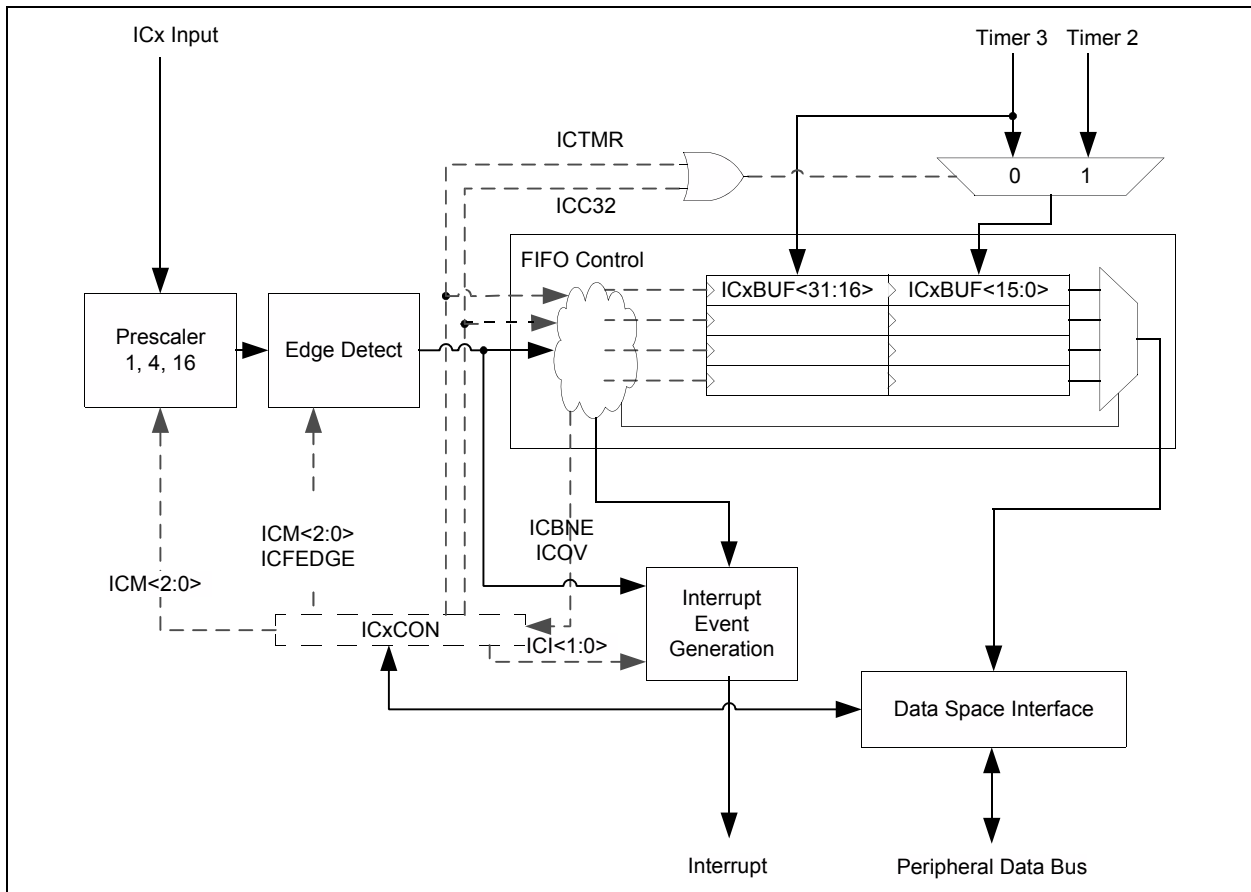
2. Capture timer value on every edge (rising and falling)
3. Capture timer value on every edge (rising and falling), specified edge first.
4. Prescaler Capture Event modes
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
 - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

PIC32MX3XX/4XX

NOTES:

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

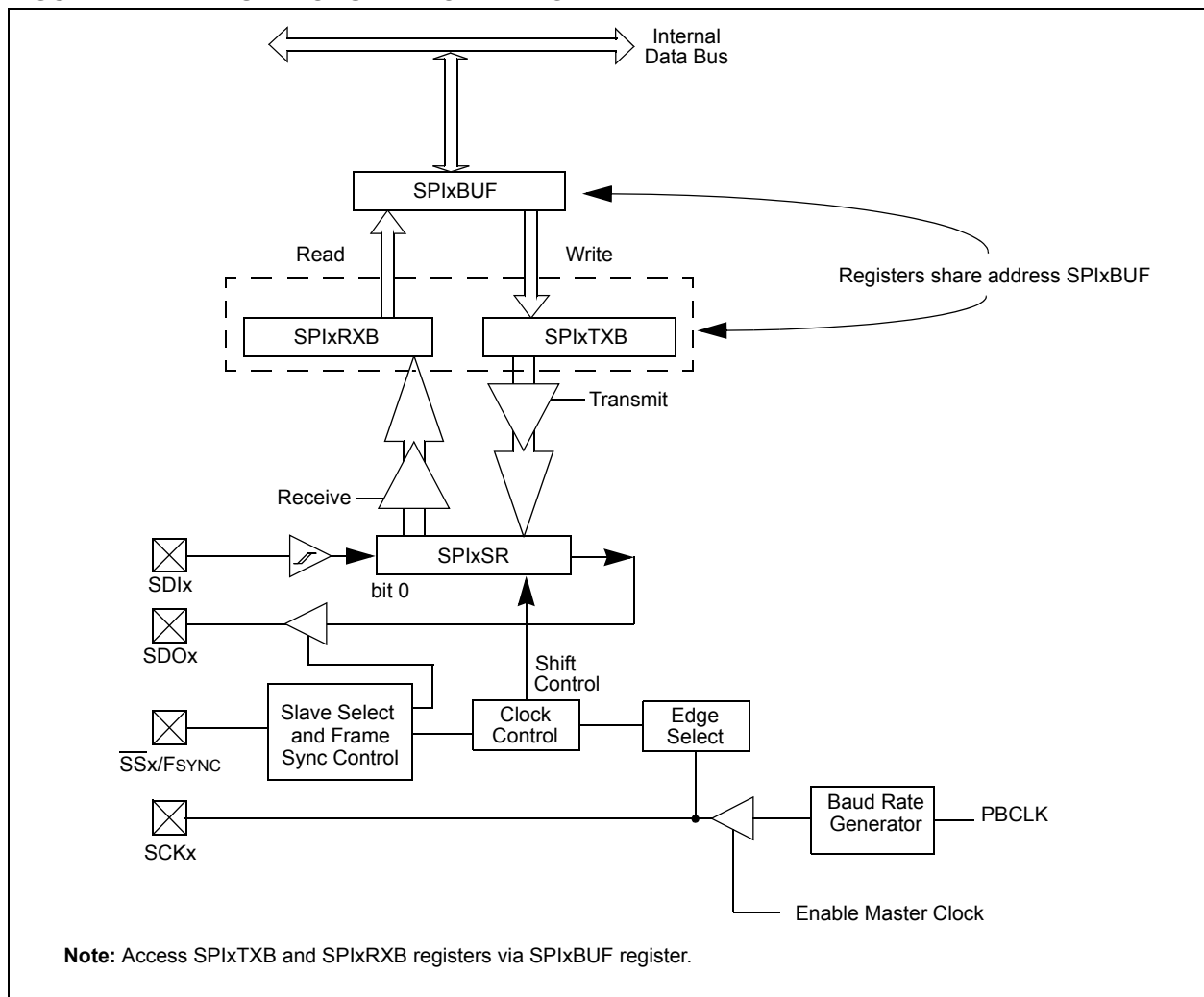
Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 23. “Serial Peripheral Interface (SPI)” (DS61106) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

The SPI module is a synchronous serial interface useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The PIC32MX SPI module is compatible with Motorola® SPI and SIOP interfaces.

Following are some of the key features of this module:

- Master and Slave Modes Support
- Four Different Clock Formats
- Framed SPI Protocol Support
- User Configurable 8-bit, 16-bit and 32-bit Data Width
- Separate SPI Data Registers for Receive and Transmit
- Programmable Interrupt Event on every 8-bit, 16-bit and 32-bit Data Transfer
- Operation during CPU Sleep and Idle Mode
- Fast Bit Manipulation using CLR, SET and INV Registers

FIGURE 17-1: SPI MODULE BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

18.0 INTER-INTEGRATED CIRCUIT (I²C™)

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” **Section 24**, “Inter-Integrated Circuit (I²C)” (DS61116) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard. Figure 18-1 shows the I²C module block diagram.

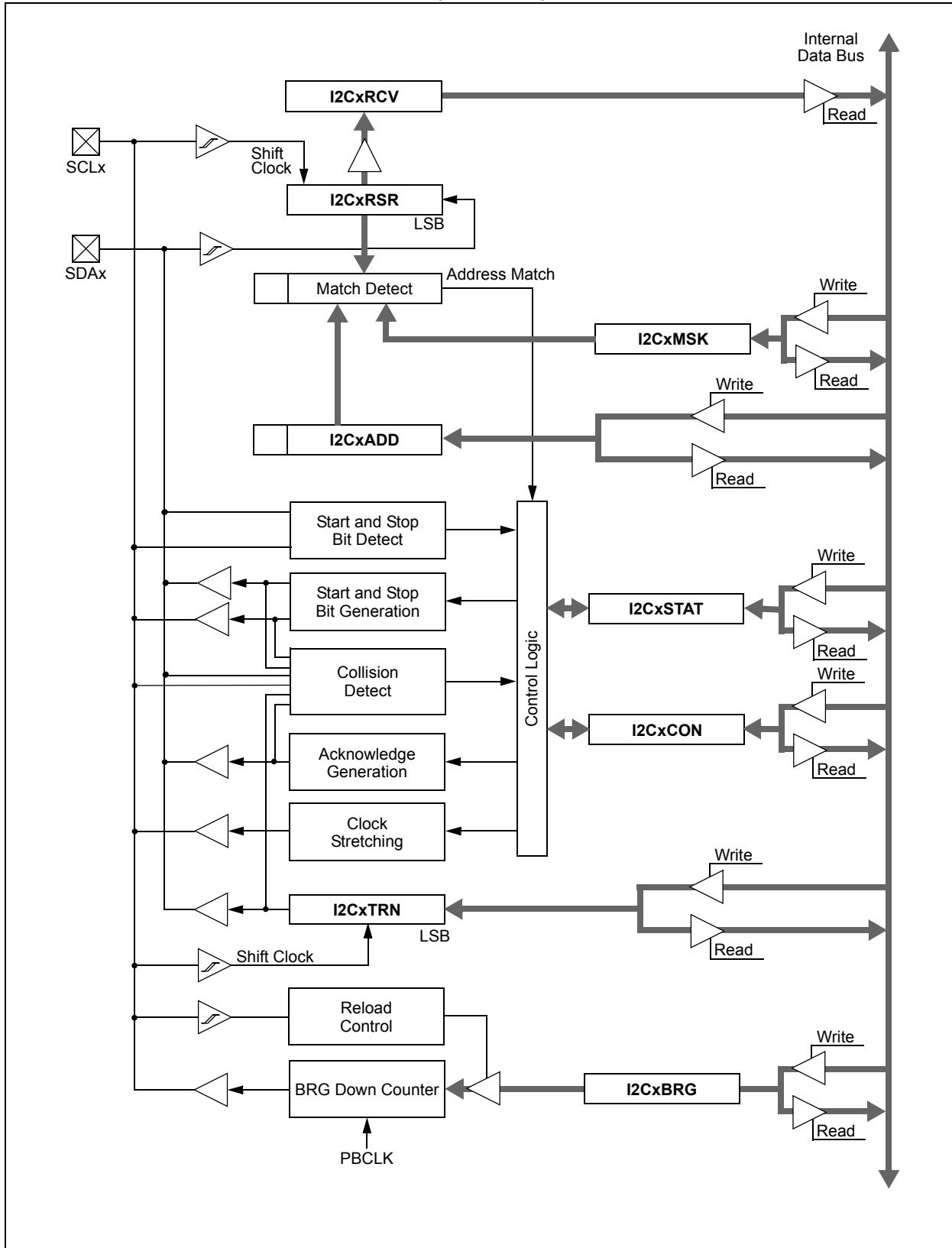
The PIC32MX3XX/4XX devices have up to two I²C interface modules, denoted as I2C1 and I2C2. Each I²C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module ‘I2Cx’ (x = 1 or 2) offers the following key features:

- I²C Interface Supporting both Master and Slave Operation.
- I²C Slave Mode Supports 7 and 10-bit Address.
- I²C Master Mode Supports 7 and 10-bit Address.
- I²C Port allows Bidirectional Transfers between Master and Slaves.
- Serial Clock Synchronization for I²C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control).
- I²C Supports Multi-master Operation; Detects Bus Collision and Arbitrates Accordingly.
- Provides Support for Address Bit Masking.

PIC32MX3XX/4XX

FIGURE 18-1: I²C™ BLOCK DIAGRAM (x = 1 OR 2)



19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 21. “Universal Asynchronous Receiver Transmitter (UART)” (DS61107) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

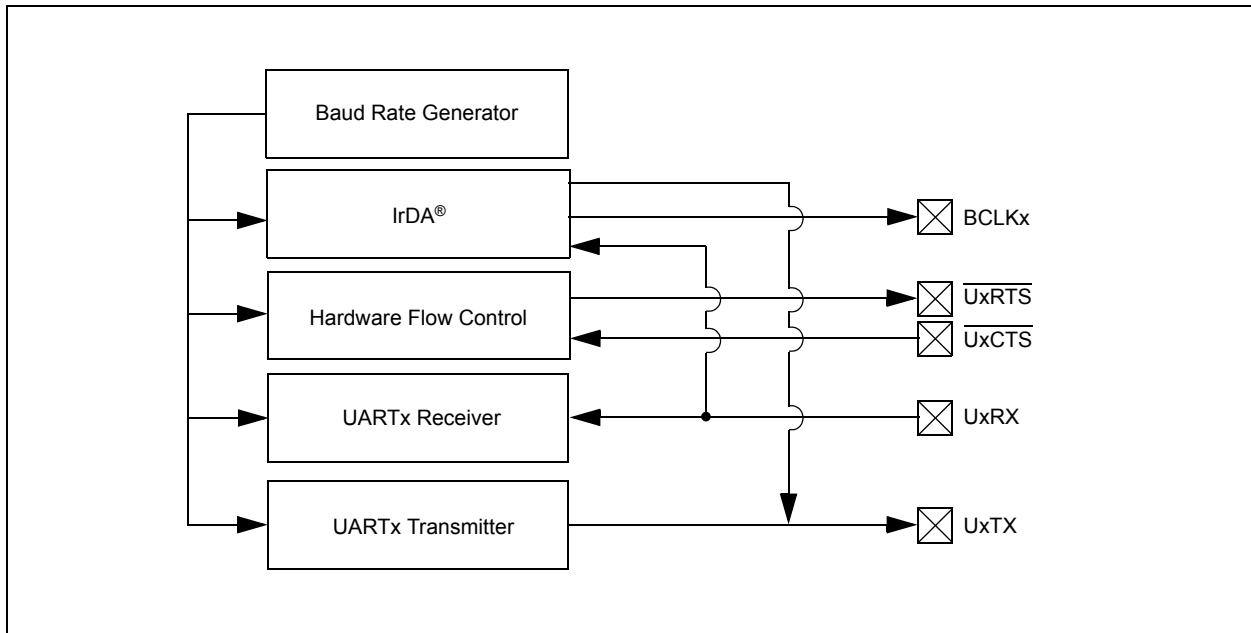
The UART module is one of the serial I/O modules available in PIC32MX3XX/4XX family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols such as RS-232, RS-485, LIN 1.2 and IrDA®. The module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 20 Mbps at 80 MHz
- 4-level-deep First-In-First-Out (FIFO) Transmit Data Buffer
- 4-level-deep FIFO Receive Data Buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN 1.2 protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 19-1 shows a simplified block diagram of the UART.

FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM



PIC32MX3XX/4XX

FIGURE 19-2: TRANSMISSION (8-BIT OR 9-BIT DATA)

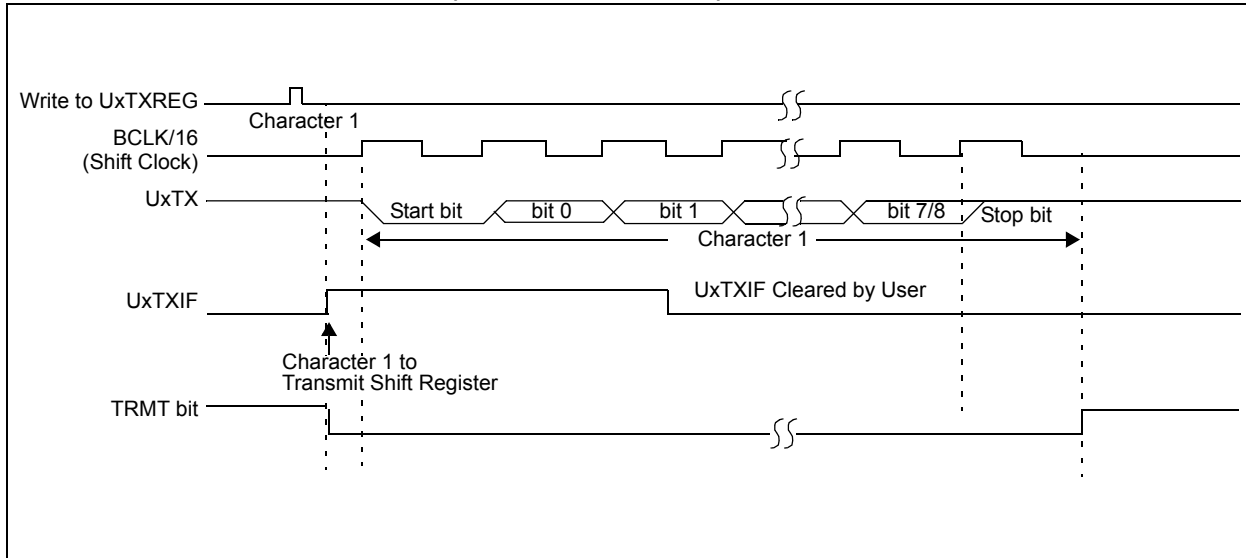


FIGURE 19-3: TWO CONSECUTIVE TRANSMISSIONS

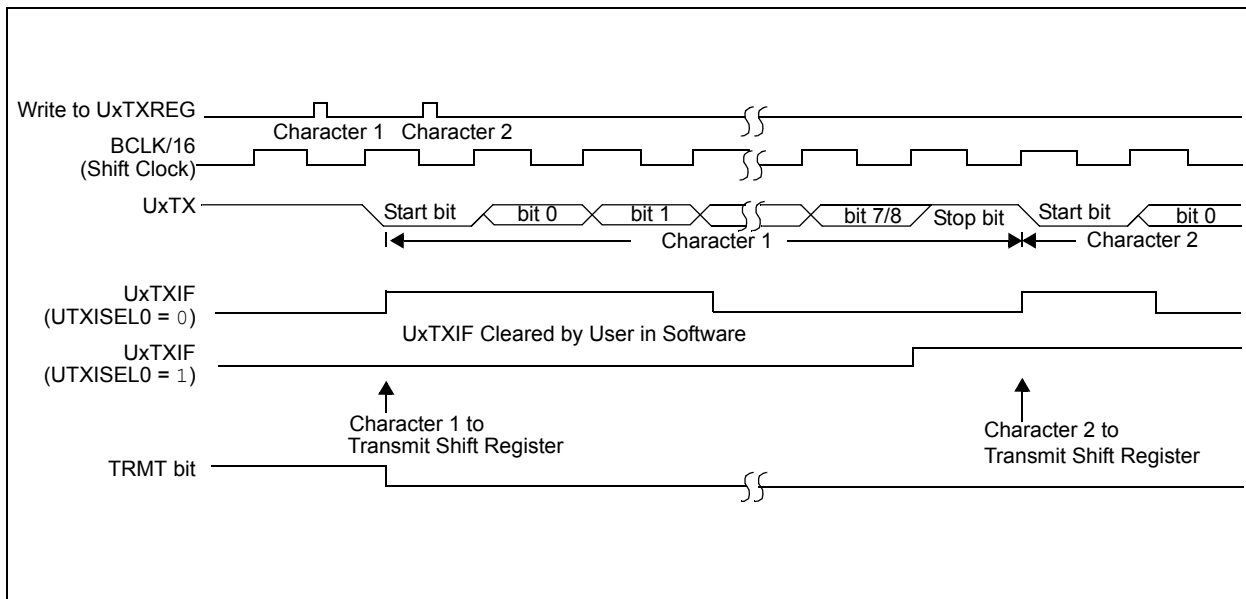


FIGURE 19-4: UART RECEPTION

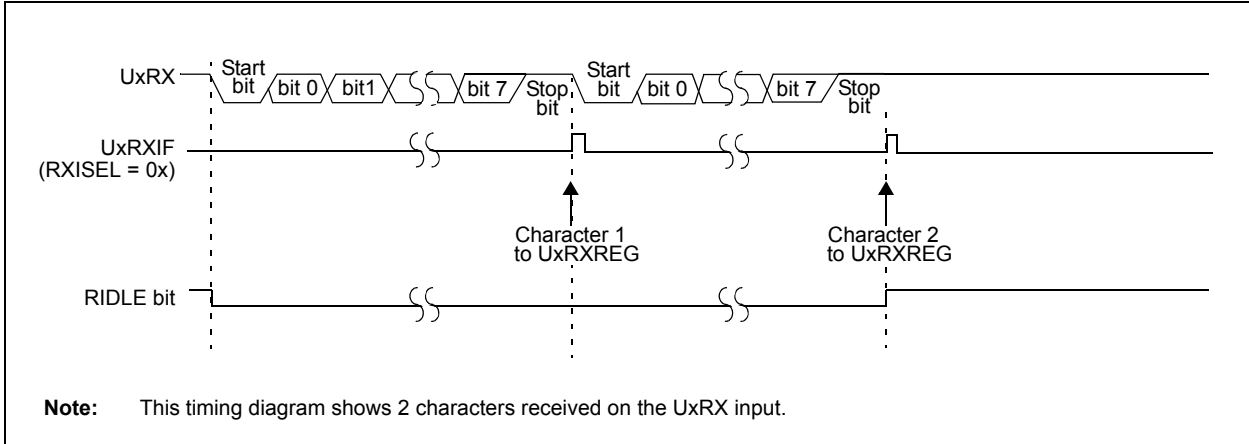
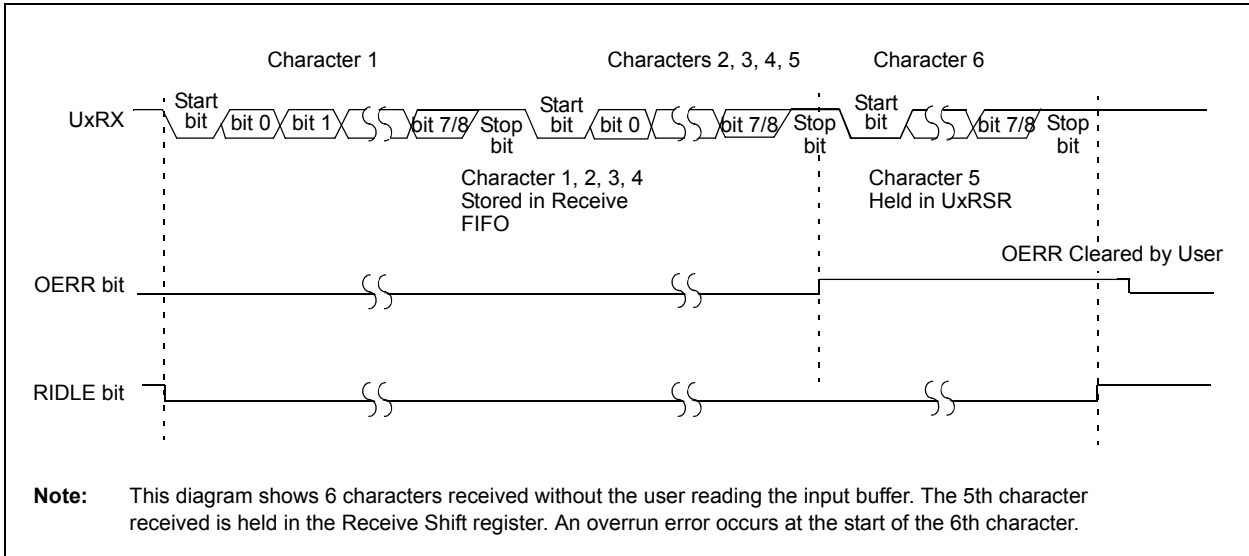


FIGURE 19-5: UART RECEPTION WITH RECEIVE OVERRUN



PIC32MX3XX/4XX

NOTES:

20.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 13. “Parallel Master Port (PMP)” (DS61128) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

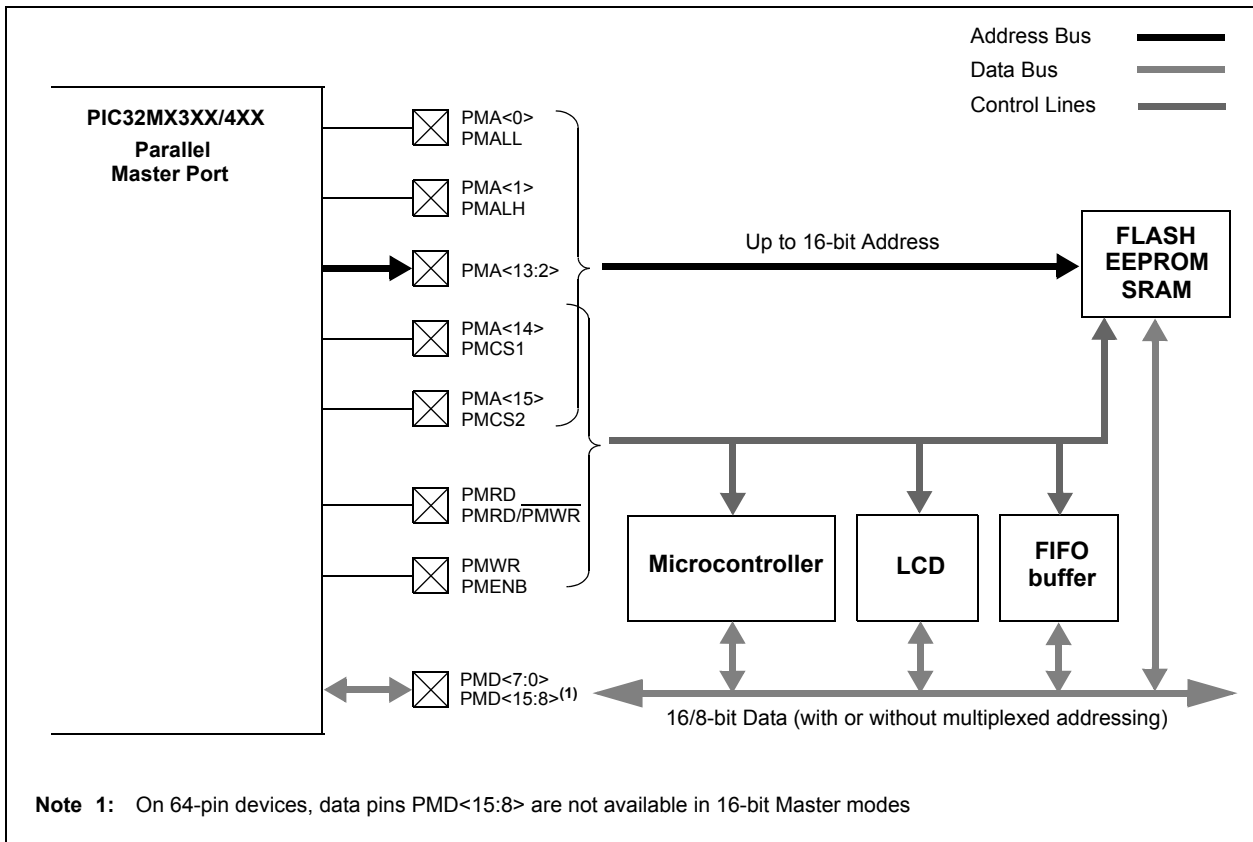
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices, and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- 8-bit, 16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options
 - Individual read and write strobes, or
 - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support
 - Legacy addressable
 - Address support
 - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Freeze option for in-circuit debugging

Note: On 64-pin devices, data pins PMD<15:8> are not available.

FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



PIC32MX3XX/4XX

NOTES:

21.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

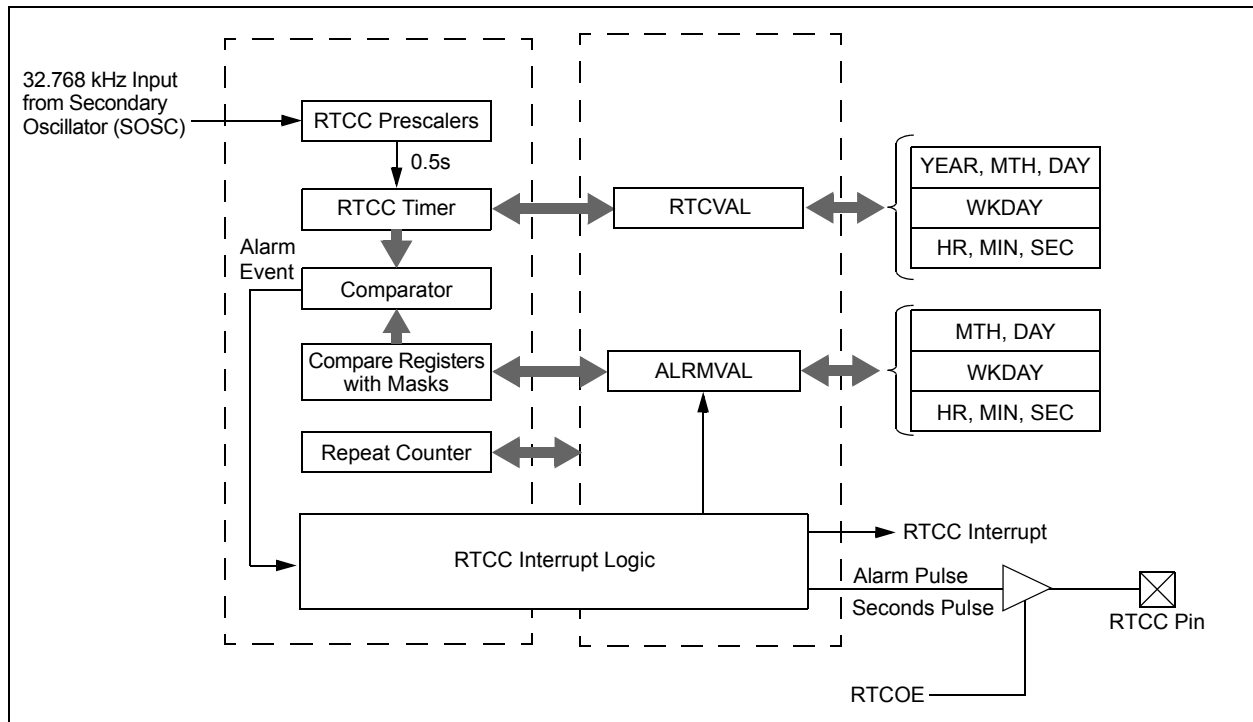
Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 29. “Real-Time Clock and Calendar (RTCC)” (DS61125) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

The PIC32MX RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

Following are some of the key features of this module:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (Military Time)
- Visibility of One-Half-Second Period
- Provides Calendar: Weekday, Date, Month and Year
- Alarm Intervals are configurable for Half of a Second, One Second, 10 Seconds, One Minute, 10 Minutes, One Hour, One Day, One Week, One Month and One Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat: Chime
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Smaller Firmware Overhead
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- User Calibration of the Clock Crystal Frequency with Auto-Adjust
- Calibration Range: ± 0.66 Seconds Error per Month
- Calibrates up to 260 ppm of Crystal Error
- Requirements: External 32.768 kHz Clock Crystal
- Alarm Pulse or Seconds Clock Output on RTCC pin

FIGURE 21-1: RTCC BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 17. “10-bit Analog-to-Digital Converter (ADC)” (DS61104) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

The PIC32MX3XX/4XX 10-bit Analog-to-Digital (A/D) converter (or ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1000 kilo samples per second (ksp/s) conversion speed
- Up to 16 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample-and-Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable Buffer Fill modes
- Eight conversion result format options
- Operation during CPU Sleep and Idle modes

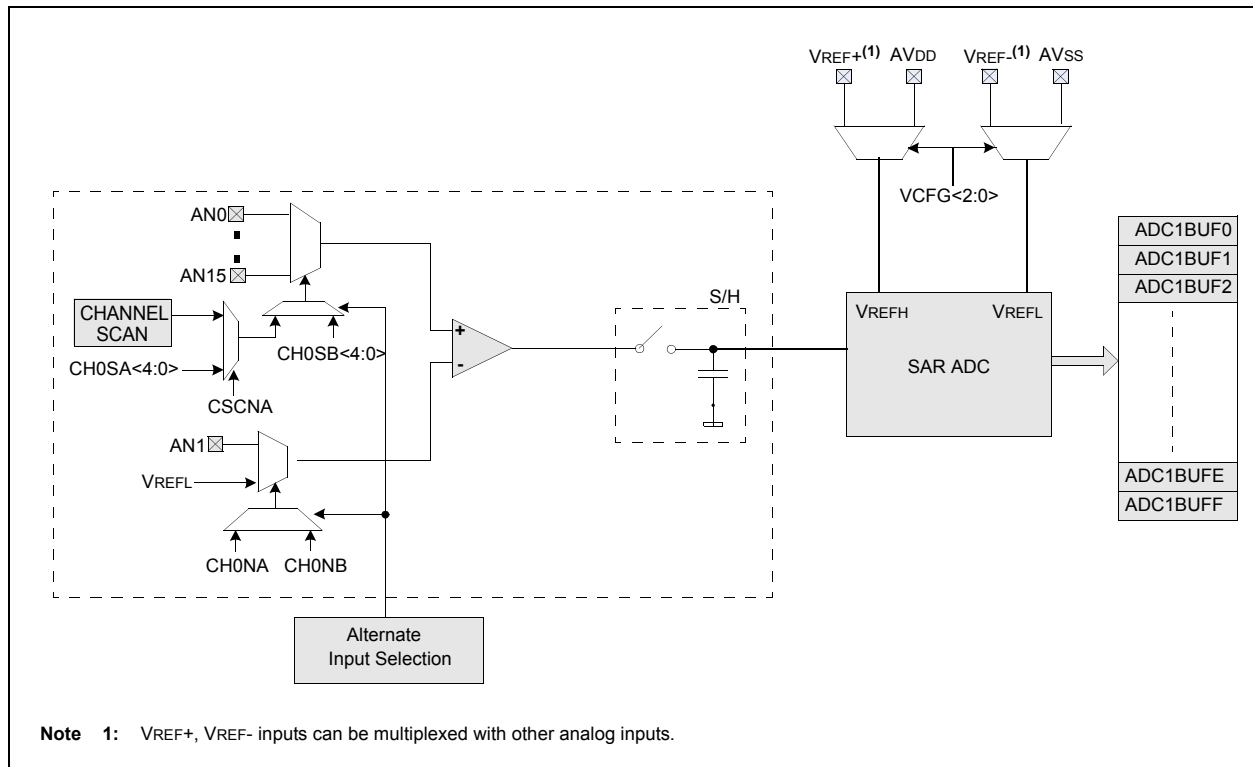
A block diagram of the 10-bit ADC is shown in Figure 22-1. The 10-bit ADC has 16 analog input pins, designated AN0-AN15. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

The analog inputs are connected through two multiplexers (MUXs) to one SHA. The analog input MUXs can be switched between two sets of analog inputs between conversions. Unipolar differential conversions are possible on all channels, other than the pin used as the reference, using a reference input pin (see Figure 22-1).

The Analog Input Scan mode sequentially converts user-specified channels. A control register specifies which analog input channels will be included in the scanning sequence.

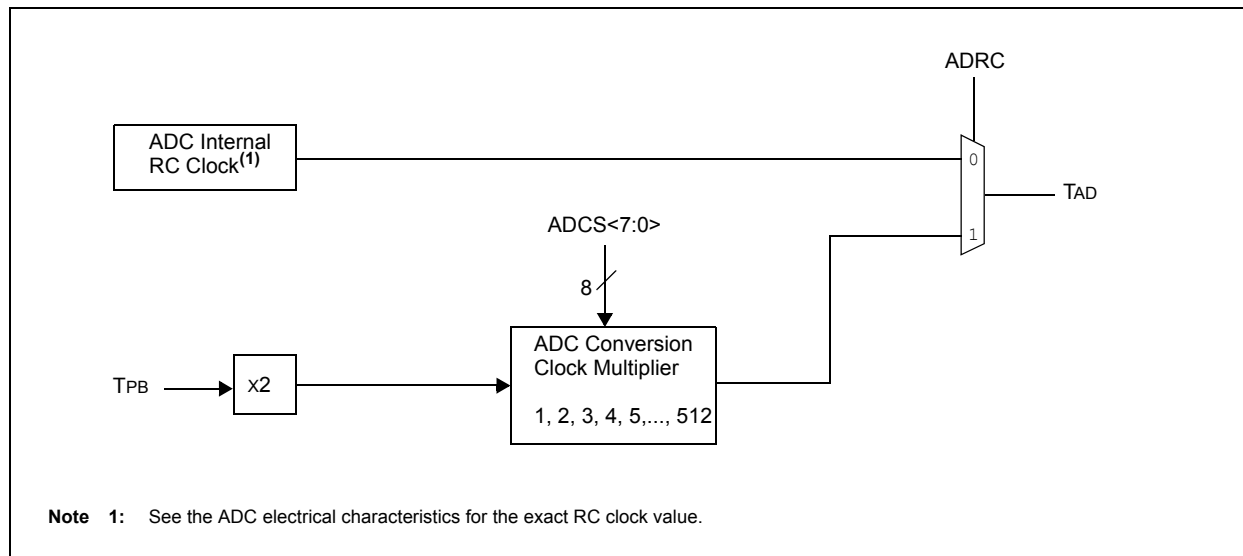
The 10-bit ADC is connected to a 16-word result buffer. Each 10-bit result is converted to one of eight, 32-bit output formats when it is read from the result buffer.

FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM



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FIGURE 22-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



23.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” **Section 19. “Comparator”** (DS61110) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

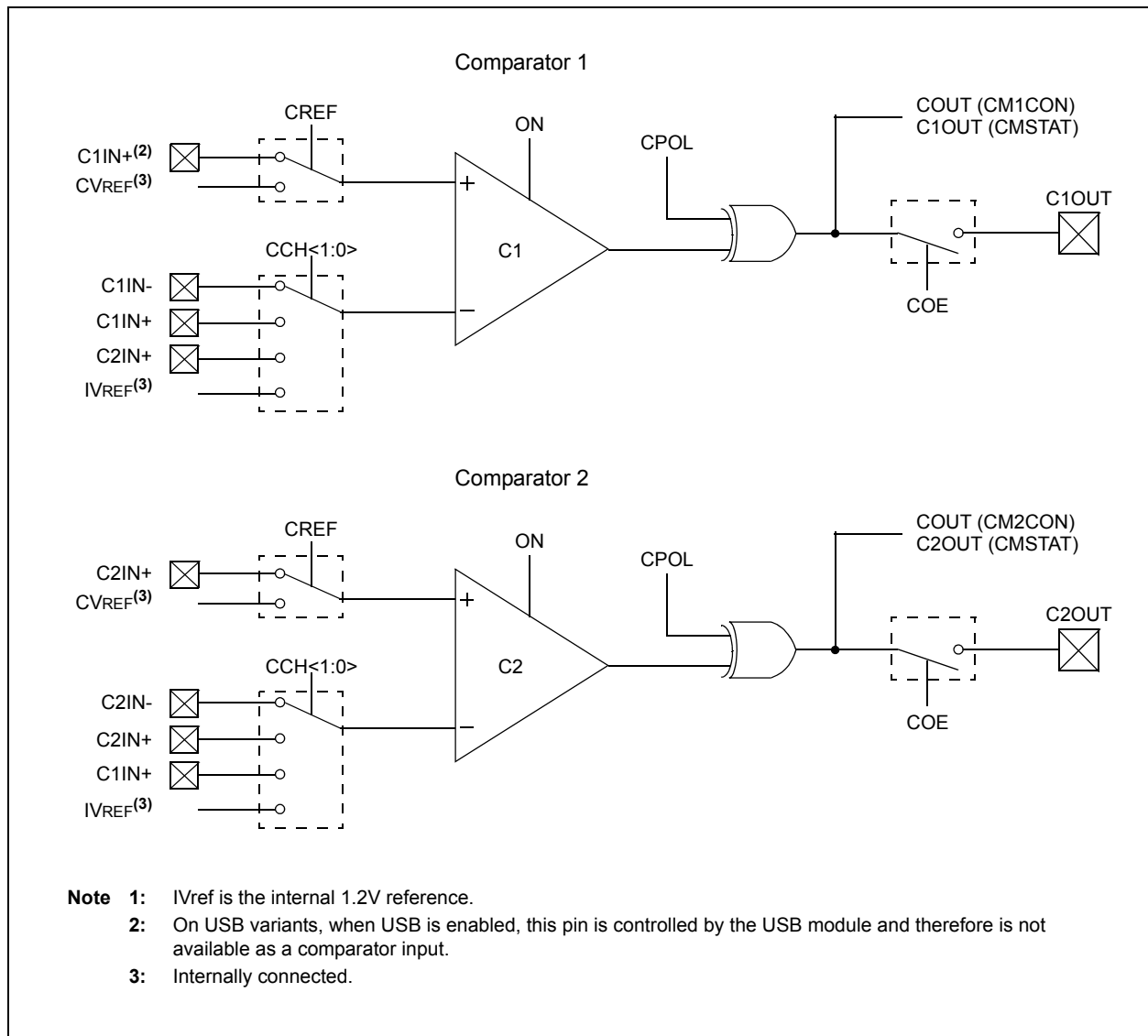
The PIC32MX3XX/4XX Analog Comparator module contains one or more comparator(s) that can be configured in a variety of ways.

Following are some of the key features of this module:

- Selectable inputs available include:
 - Analog inputs multiplexed with I/O pins
 - On-chip internal absolute voltage reference (IVREF)
 - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the comparator module is shown in Figure 23-1.

FIGURE 23-1: COMPARATOR BLOCK DIAGRAM



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NOTES:

24.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” Section 20. “Comparator Voltage Reference (CVREF)” (DS61109) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

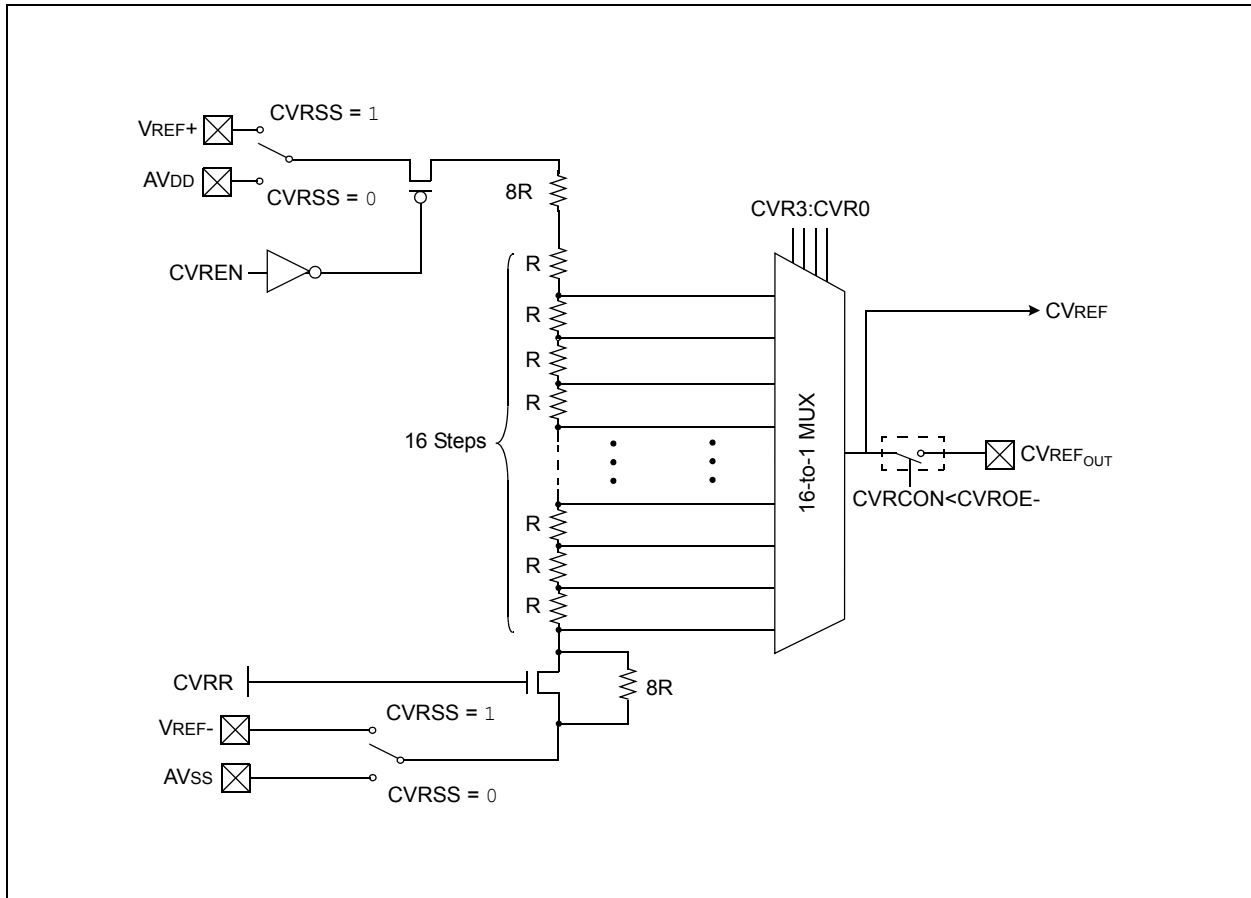
The CVREF is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is shown in Figure 24-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module’s supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

FIGURE 24-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

25.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” **Section 10. “Power-Saving Features”** (DS61130) for a detailed description of this peripheral. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

This section describes power saving for the PIC32MX3XX/4XX. The PIC32MX devices offer a total of nine methods and modes that are organized into two categories that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software.

25.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK, and by individually disabling modules. These methods are grouped into the following modes:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- SOSC Run mode: the CPU is clocked from the SOSC clock source.
- Peripheral Bus Scaling mode: peripherals are clocked at programmable fraction of the CPU clock (SYSCLK).

25.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- POSC Idle Mode: the system clock is derived from the POSC. The system clock source continues to operate.
Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle Mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- SOSC Idle Mode: the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- LPRC Idle Mode: the system clock is derived from the LPRC.
Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.

- Sleep Mode: the CPU, the system clock source, and any peripherals that operate from the system clock source, are halted.
Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

25.3 Power-Saving Operation

The purpose of all power saving is to reduce power consumption by reducing the device clock frequency. To achieve this, low-frequency clock sources can be selected. In addition, the peripherals and CPU can be halted or disabled to further reduce power consumption.

25.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device Power-Saving operating modes. The CPU and most peripherals are halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted.
- The system clock source is typically shut down. See **Section 25.4 “Peripheral Bus Scaling Method”** for specific information.
- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit, if enabled, remains operative during Sleep mode.
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode.
- Some peripherals can continue to operate in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART, and peripherals that use an external clock input or the internal LPRC oscillator, e.g., RTCC and Timer 1.
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The USB module can override the disabling of the POSC or FRC. Refer to the USB section for specific details.
- Some modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption.

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The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out. See **Section 26.2 "Watchdog Timer (WDT)"**.

If the interrupt priority is lower than or equal to current priority, the CPU will remain halted, but the PBCLK will start running and the device will enter into Idle mode.

Note: There is no FRZ mode for this module.

25.4 Peripheral Bus Scaling Method

Most of the peripherals on the device are clocked using the PBCLK. The peripheral bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK-to-PBCLK ratios of 1:1, 1:2, 1:4, and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the Interrupt Controller, DMA, Bus Matrix, and Prefetch Cache are clocked directly from SYSCLK, as a result, they are not affected by PBCLK divisor changes.

Most of the peripherals on the device are clocked using the PBCLK. The peripheral bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK-to-PBCLK ratios of 1:1, 1:2, 1:4, and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as USB, Interrupt Controller, DMA, Bus Matrix, and Prefetch Cache are clocked directly from SYSCLK, as a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements such as baud rate accuracy should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

25.5 Idle Mode

In the Idle mode, the CPU is halted but the System clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is halted. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency when exiting Idle mode is very low due to the CPU oscillator source remaining active.

Notes: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a POSC of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in PB divisor ratio.

Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from POSC to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to POSC, the appropriate PLL and or oscillator startup/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of CPU. If the priority of the interrupt event is lower than or equal to current priority of CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any source of device Reset.
- On a WDT time-out interrupt. See **Section 26.2 "Watchdog Timer (WDT)"**.

26.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to the “PIC32MX Family Reference Manual” (DS61132) for detailed descriptions of these features. The manual is available from the Microchip web site (www.Microchip.com/PIC32).

PIC32MX3XX/4XX devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Device Configuration
- Watchdog Timer
- JTAG Interface
- In-Circuit Serial Programming (ICSP)

26.1 Configuration Bits

The Configuration bits can be programmed to select various device configurations.

REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0

r-0	r-1	r-1	R/P-1	r-1	r-1	r-1	R/P-1
—	—	—	CP	—	—	—	BWP
bit 31							bit 24

r-1	r-1	r-1	r-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	PWP<7:4>			
bit 23							bit 16

R/P-1	R/P-1	R/P-1	R/P-1	r-1	r-1	r-1	r-1
PWP<3:0>				—	—	—	—
bit 15							bit 8

r-1	r-1	r-1	r-1	R/P-1	r-1	R/P-1	R/P-1
—	—	—	—	ICESEL	—	DEBUG<1:0>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
 U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

- bit 31 **Reserved:** Write '0'
- bit 30-29 **Reserved:** Write '1'
- bit 28 **CP:** Code-Protect bit
 Prevents boot and program Flash memory from being read or modified by an external programming device.
 1 = Protection disabled
 0 = Protection enabled
- bit 27-25 **Reserved:** Write '1'

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REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 24	BWP: Boot Flash Write-Protect bit Prevents boot Flash memory from being modified during code execution. 1 = Boot Flash is writable 0 = Boot Flash is not writable
bit 23-20	Reserved: Write '1'
bit 19-12	PWP<7:0>: Program Flash Write-Protect bits Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the one's compliment of the number of write protected program Flash memory pages. 11111111 = Disabled 11111110 = 0xBD00_0FFF 11111101 = 0xBD00_1FFF 11111100 = 0xBD00_2FFF 11111011 = 0xBD00_3FFF 11111010 = 0xBD00_4FFF 11111001 = 0xBD00_5FFF 11111000 = 0xBD00_6FFF 11110111 = 0xBD00_7FFF 11110110 = 0xBD00_8FFF 11110101 = 0xBD00_9FFF 11110100 = 0xBD00_AFFF 11110011 = 0xBD00_BFFF 11110010 = 0xBD00_CFFF 11110001 = 0xBD00_DFFF 11110000 = 0xBD00_EFFF 11101111 = 0xBD00_FFFF ... 01111111 = 0xBD07_FFFF
bit 11-4	Reserved: Write '1'
bit 3	ICESEL: In-Circuit Emulator/Debugger Communication Channel Select bit 1 = PGEC2/PGED2 pair is used 0 = PGEC1/PGED1 pair is used
bit 2	Reserved: Write '1'
bit 1-0	DEBUG<1:0>: Background Debugger Enable bits (forced to '11' if code-protect is enabled) 11 = Debugger disabled 10 = Debugger enabled 01 = Reserved (same as '11' setting) 00 = Reserved (same as '11' setting)

REGISTER 26-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 31						bit 24	

R/P-1	r-1	r-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FWDTEN	—	—	WDTPS<4:0>				
bit 23						bit 16	

R/P-1	R/P-1	R/P-1	R/P-1	r-1	R/P-1	R/P-1	R/P-1
FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMD<1:0>	
bit 15						bit 8	

R/P-1	r-1	R/P-1	r-1	r-1	R/P-1	R/P-1	R/P-1
IESO	—	FSOSCEN	—	—	FNOSC<2:0>		
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
 U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

- bit 31-24 **Reserved:** Write '1'
- bit 23 **FWDTEN:** Watchdog Timer Enable bit
 1 = The WDT is enabled and cannot be disabled by software
 0 = The WDT is not enabled; it can be enabled in software
- bit 22-21 **Reserved:** Write '1'
- bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits
 10100 = 1:1048576
 10011 = 1:524288
 10010 = 1:262144
 10001 = 1:131072
 10000 = 1:65536
 01111 = 1:32768
 01110 = 1:16384
 01101 = 1:8192
 01100 = 1:4096
 01011 = 1:2048
 01010 = 1:1024
 01001 = 1:512
 01000 = 1:256
 00111 = 1:128
 00110 = 1:64
 00101 = 1:32
 00100 = 1:16
 00011 = 1:8
 00010 = 1:4
 00001 = 1:2
 00000 = 1:1
 All other combinations not shown result in operation = '10100'

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REGISTER 26-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

- bit 15-14 **FCKSM<1:0>**: Clock Switching and Monitor Selection Configuration bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
- bit 13-12 **FPBDIV<1:0>**: Peripheral Bus Clock Divisor Default Value bits
11 = PBCLK is SYSCLK divided by 8
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1
- bit 11 **Reserved**: Write '1'
- bit 10 **OSCIOFNC**: CLKO Enable Configuration bit
1 = CLKO output signal active on the OSCO pin; primary oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMD<1:0> = 11 OR 00)
0 = CLKO output disabled
- bit 9-8 **POSCMD<1:0>**: Primary Oscillator Configuration bits
11 = Primary oscillator disabled
10 = HS oscillator mode selected
01 = XT oscillator mode selected
00 = External clock mode selected
- bit 7 **IESO**: Internal External Switchover bit
1 = Internal External Switchover mode enabled (Two-Speed Start-up enabled)
0 = Internal External Switchover mode disabled (Two-Speed Start-up disabled)
- bit 6 **Reserved**: Write '1'
- bit 5 **FSOSCEN**: Secondary Oscillator Enable bit
1 = Enable Secondary Oscillator
0 = Disable Secondary Oscillator
- bit 4-3 **Reserved**: Write '1'
- bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits
000 = Fast RC Oscillator (FRC)
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
010 = Primary Oscillator (XT, HS, EC)⁽¹⁾
011 = Primary Oscillator with PLL module (XT+PLL, HS+PLL, EC+PLL)
100 = Secondary Oscillator (SOSC)
101 = Low-Power RC Oscillator (LPRC)
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
111 = Fast RC Oscillator with divide-by-N (FRCDIV)
- Note 1:** Do not disable POSC (POSCMD = 00) when using this oscillator source.

REGISTER 26-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 31						bit 24	

r-1	r-1	r-1	r-1	r-1	R/P-1	R/P-1	R/P-1
—	—	—	—	—	FPLLODIV<2:0>		
bit 23					bit 16		

R/P-1	r-1	r-1	r-1	r-1	R/P-1	R/P-1	R/P-1
FUPLLEN	—	—	—	—	FUPLLDIV<2:0>		
bit 15						bit 8	

r-1	R/P-1	R/P-1	R/P-1	r-1	R/P-1	R/P-1	R/P-1
—	FPLLMULT<2:0>			—	FPLLDIV<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
 U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

- bit 31-19 **Reserved:** Write '1'
- bit 18-16 **FPLLODIV[2:0]:** Default Postscaler for PLL bits
 - 111 = PLL output divided by 256
 - 110 = PLL output divided by 64
 - 101 = PLL output divided by 32
 - 100 = PLL output divided by 16
 - 011 = PLL output divided by 8
 - 010 = PLL output divided by 4
 - 001 = PLL output divided by 2
 - 000 = PLL output divided by 1
- bit 15 **FUPLLEN:** USB PLL Enable bit
 - 1 = Enable USB PLL
 - 0 = Disable and bypass USB PLL
- bit 14-11 **Reserved:** Write '1'
- bit 10-8 **FUPLLDIV[2:0]:** PLL Input Divider bits
 - 111 = 12x divider
 - 110 = 10x divider
 - 101 = 6x divider
 - 100 = 5x divider
 - 011 = 4x divider
 - 010 = 3x divider
 - 010 = 3x divider
 - 001 = 2x divider
 - 000 = 1x divider
- bit 7 **Reserved:** Write '1'

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REGISTER 26-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

- bit 6-4 **FPLLMULT[2:0]:** PLL Multiplier bits
 111 = 24x multiplier
 110 = 21x multiplier
 101 = 20x multiplier
 100 = 19x multiplier
 011 = 18x multiplier
 010 = 17x multiplier
 001 = 16x multiplier
 000 = 15x multiplier
- bit 3 **Reserved:** Write '1'
- bit 2-0 **FPLLIDIV[2:0]:** PLL Input Divider bits
 111 = 12x divider
 110 = 10x divider
 101 = 6x divider
 100 = 5x divider
 011 = 4x divider
 010 = 3x divider
 001 = 2x divider
 000 = 1x divider

REGISTER 26-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 31				bit 24			

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 23				bit 16			

R/P-x	R/P-x	R/P-x	R/P-x	R/P-x	R/P-x	R/P-x	R/P-x
USERID<15:8>							
bit 15				bit 8			

R/P-x	R/P-x	R/P-x	R/P-x	R/P-x	R/P-x	R/P-x	R/P-x
USERID<7:0>							
bit 7				bit 0			

Legend:
 R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
 U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

- bit 31-16 **Reserved:** Write '1'
- bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user defined and is readable via ICSP™ and JTAG

REGISTER 26-5: DEVID: DEVICE AND REVISION ID REGISTER

R	R	R	R	R	R	R	R
VER<3:0>				DEVID<27:24>			
bit 31				bit 24			

R	R	R	R	R	R	R	R
DEVID<23:16>							
bit 23				bit 16			

R	R	R	R	R	R	R	R
DEVID<15:8>							
bit 15				bit 8			

R	R	R	R	R	R	R	R
DEVID<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
 U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-28 **VER<3:0>**: Revision Identifier bits⁽¹⁾

bit 27-0 **DEVID<27:0>**: Device ID⁽¹⁾

Note: See the PIC32MX Programming Specification for a list of Revision and Device ID values.

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26.2 Watchdog Timer (WDT)

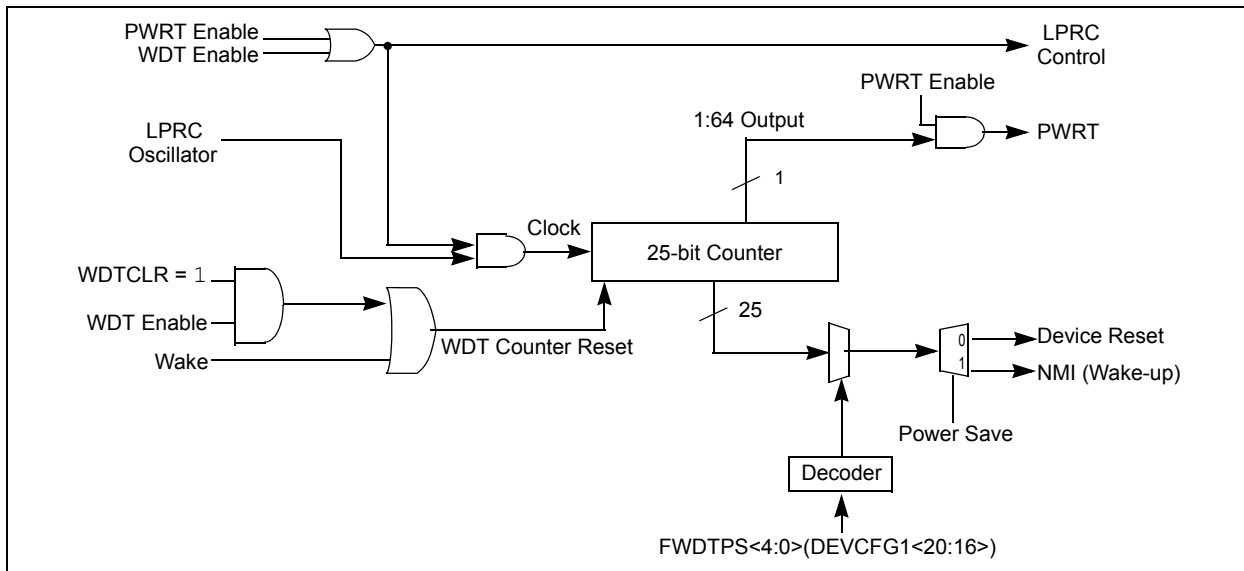
This section describes the operation of the WDT and Power-Up Timer of the PIC32MX3XX/4XX.

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 26-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM



26.3 On-Chip Voltage Regulator

All PIC32MX3XX/4XX device's core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX3XX/4XX incorporate an on-chip regulator providing the required core logic voltage from VDD.

The internal 1.8V regulator is controlled by the ENVREG pin. Tying this pin to VDD enables the regulator, which in turn provides power to the core. A low ESR capacitor (such as tantalum) must be connected to the VDDCORE/VCAP pin (Figure 26-2). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 28.1 "DC Characteristics"**.

Note: It is important that the low ESR capacitor is placed as close as possible to the VDDCORE/VCAP pin.

Tying the ENVREG pin to VSS disables the regulator. In this case, separate power for the core logic at a nominal 1.8V must be supplied to the device on the VDDCORE/VCAP pin.

Alternately, the VDDCORE/VCAP and VDD pins can be tied together to operate at a lower nominal voltage. Refer to Figure 26-2 for possible configurations.

26.3.1 ON-CHIP REGULATOR AND POR

When the voltage regulator is enabled, it takes fixed delay for it to generate output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

If the regulator is disabled, a separate Power-Up Timer (PWRT) is automatically enabled. The PWRT adds a fixed delay of TPWRT at device start-up. See **Section 28.0 "Electrical Characteristics"** for more information on TPU AND TPWRT.

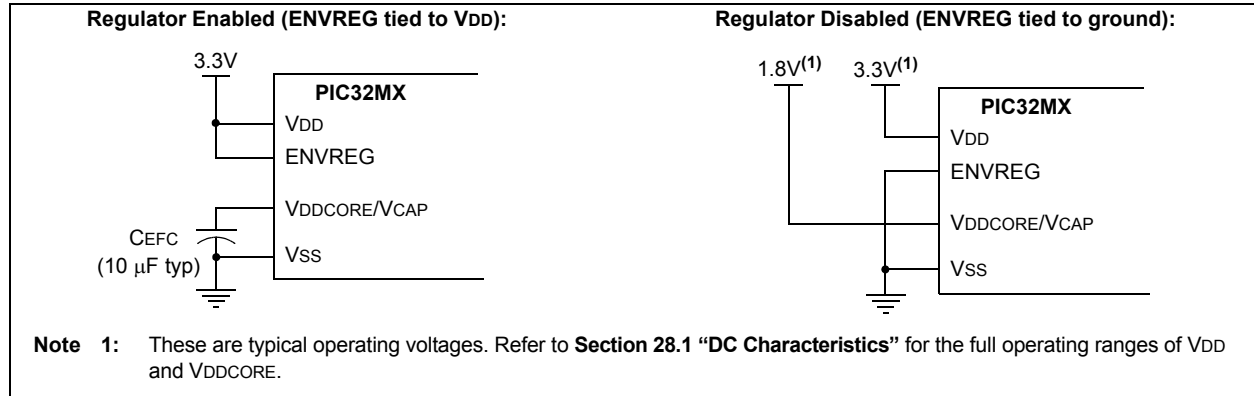
26.3.2 ON-CHIP REGULATOR AND BOR

When the on-chip regulator is enabled, PIC32MX3XX/4XX devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 28.1 “DC Characteristics”**.

26.3.3 POWER-UP REQUIREMENTS

The on-chip regulator is designed to meet the power-up requirements for the device. If the application does not use the regulator, then strict power-up conditions must be adhered to. While powering up, VDDCORE must never exceed VDD by 0.3 volts.

FIGURE 26-2: CONNECTIONS FOR THE ON-CHIP REGULATOR



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26.4 Programming and Diagnostics

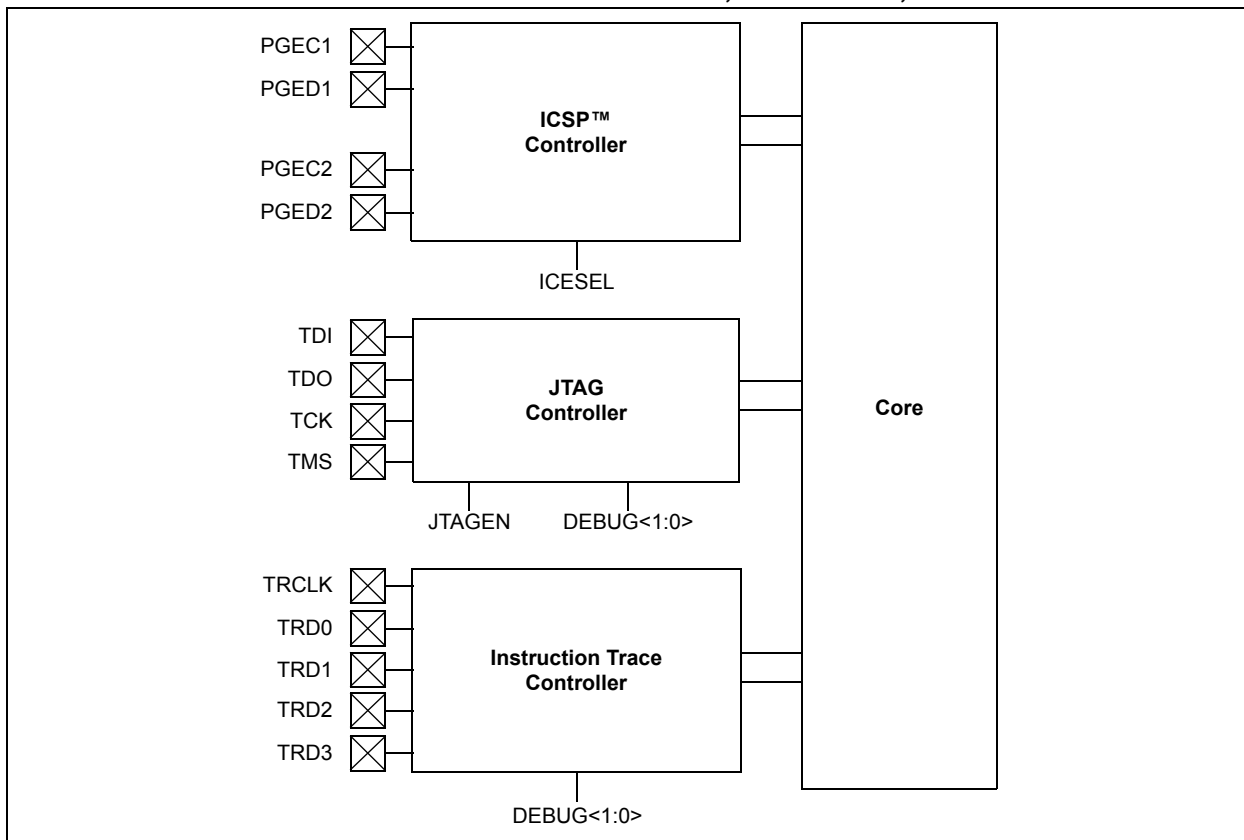
PIC32MX3XX/4XX devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them.

These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32MX devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 26-3: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING, AND TRACE PORTS



REGISTER 26-6: DDPCON: DEBUG DATA PORT CONTROL REGISTER

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31						bit 24	

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23						bit 16	

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	r-x	r-x
DDPUSB	DDPU1	DDPU2	DDPSPI1	JTAGEN	TROEN	—	—
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
 U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

- bit 31-8 **Reserved:** Write '0'; ignore read
- bit 7 **DDPUSB:** Debug Data Port Enable for USB bit
 1 = USB peripheral ignores USBFRZ (U1CNFG1<5>) setting
 0 = USB peripheral follows USBFRZ setting.
- bit 6 **DDPU1:** Debug Data Port Enable for UART1 bit
 1 = UART1 peripheral ignores FRZ (U1MODE<14>) setting
 0 = UART1 peripheral follows FRZ setting
- bit 5 **DDPU2:** Debug Data Port Enable for UART2 bit
 1 = UART2 peripheral ignores FRZ (U2MODE<14>) setting
 0 = UART2 peripheral follows FRZ setting
- bit 4 **DDPSPI1:** Debug Data Port Enable for SPI1 bit
 1 = SPI1 peripheral ignores FRZ (SPI1CON<14>) setting
 0 = SPI1 peripheral follows FRZ setting
- bit 3 **JTAGEN:** JTAG Port Enable bit
 1 = Enable JTAG Port
 0 = Disable JTAG Port
- bit 2 **TROEN:** Trace Output Enable bit
 1 = Enable Trace Port
 0 = Disable Trace Port
- bit 1-0 **Reserved:** Write '1'; ignore read

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NOTES:

27.0 INSTRUCTION SET

The PIC32MX3XX/4XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. PIC32MX does not support the following features:

- CoreExtend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Table 27-1 provides a summary of the instructions that are implemented by the PIC32MX3XX/4XX family core.

Note: Refer to “MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set” at www.mips.com for more information.

TABLE 27-1: MIPS32® INSTRUCTION SET

Instruction	Description	Function
ADD	Integer Add	$Rd = Rs + Rt$
ADDI	Integer Add Immediate	$Rt = Rs + Immed$
ADDIU	Unsigned Integer Add Immediate	$Rt = Rs +_U Immed$
ADDU	Unsigned Integer Add	$Rd = Rs +_U Rt$
AND	Logical AND	$Rd = Rs \& Rt$
ANDI	Logical AND Immediate	$Rt = Rs \& (0_{16} Immed)$
B	Unconditional Branch (Assembler idiom for: BEQ r0, r0, offset)	$PC += (int)offset$
BAL	Branch and Link (Assembler idiom for: BGEZAL r0, offset)	$GPR[31] = PC + 8$ $PC += (int)offset$
BEQ	Branch On Equal	if $Rs == Rt$ $PC += (int)offset$
BEQL	Branch On Equal Likely ⁽¹⁾	if $Rs == Rt$ $PC += (int)offset$ else Ignore Next Instruction
BGEZ	Branch on Greater Than or Equal To Zero	if $!Rs[31]$ $PC += (int)offset$
BGEZAL	Branch on Greater Than or Equal To Zero And Link	$GPR[31] = PC + 8$ if $!Rs[31]$ $PC += (int)offset$
BGEZALL	Branch on Greater Than or Equal To Zero And Link Likely ⁽¹⁾	$GPR[31] = PC + 8$ if $!Rs[31]$ $PC += (int)offset$ else Ignore Next Instruction
BGEZL	Branch on Greater Than or Equal To Zero Likely ⁽¹⁾	if $!Rs[31]$ $PC += (int)offset$ else Ignore Next Instruction
BGTZ	Branch on Greater Than Zero	if $!Rs[31] \&\& Rs != 0$ $PC += (int)offset$
BGTZL	Branch on Greater Than Zero Likely ⁽¹⁾	if $!Rs[31] \&\& Rs != 0$ $PC += (int)offset$ else Ignore Next Instruction
BLEZ	Branch on Less Than or Equal to Zero	if $Rs[31] Rs == 0$ $PC += (int)offset$

Note 1: This instruction is deprecated and should not be used.

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TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
BLEZL	Branch on Less Than or Equal to Zero Likely ⁽¹⁾	if Rs[31] Rs == 0 PC += (int)offset else Ignore Next Instruction
BLTZ	Branch on Less Than Zero	if Rs[31] PC += (int)offset
BLTZAL	Branch on Less Than Zero And Link	GPR[31] = PC + 8 if Rs[31] PC += (int)offset
BLTZALL	Branch on Less Than Zero And Link Likely ⁽¹⁾	GPR[31] = PC + 8 if Rs[31] PC += (int)offset else Ignore Next Instruction
BLTZL	Branch on Less Than Zero Likely ⁽¹⁾	if Rs[31] PC += (int)offset else Ignore Next Instruction
BNE	Branch on Not Equal	if Rs != Rt PC += (int)offset
BNEL	Branch on Not Equal Likely ⁽¹⁾	if Rs != Rt PC += (int)offset else Ignore Next Instruction
BREAK	Breakpoint	Break Exception
CLO	Count Leading Ones	Rd = NumLeadingOnes (Rs)
CLZ	Count Leading Zeroes	Rd = NumLeadingZeroes (Rs)
DERET	Return from Debug Exception	PC = DEPC Exit Debug Mode
DI	Atomically Disable Interrupts	Rt = Status; Status _{IE} = 0
DIV	Divide	LO = (int)Rs / (int)Rt HI = (int)Rs % (int)Rt
DIVU	Unsigned Divide	LO = (uns)Rs / (uns)Rt HI = (uns)Rs % (uns)Rt
EHB	Execution Hazard Barrier	Stop instruction execution until execution hazards are cleared
EI	Atomically Enable Interrupts	Rt = Status; Status _{IE} = 1
ERET	Return from Exception	if Status _{ERL} PC = ErrorEPC else PC = EPC Status _{EXL} = 0 Status _{ERL} = 0 LL = 0
EXT	Extract Bit Field	Rt = ExtractField(Rs, pos, size)
INS	Insert Bit Field	Rt = InsertField(Rs, Rt, pos, size)
J	Unconditional Jump	PC = PC[31:28] offset<<2

Note 1: This instruction is deprecated and should not be used.

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
JAL	Jump and Link	GPR[31] = PC + 8 PC = PC[31:28] offset<<2
JALR	Jump and Link Register	Rd = PC + 8 PC = Rs
JALR.HB	Jump and Link Register with Hazard Barrier	Like JALR, but also clears execution and instruction hazards
JR	Jump Register	PC = Rs
JR.HB	Jump Register with Hazard Barrier	Like JR, but also clears execution and instruction hazards
LB	Load Byte	Rt = (byte)Mem[Rs+offset]
LBU	Unsigned Load Byte	Rt = (ubyte)Mem[Rs+offset]
LH	Load Halfword	Rt = (half)Mem[Rs+offset]
LHU	Unsigned Load Halfword	Rt = (uhalf)Mem[Rs+offset]
LL	Load Linked Word	Rt = Mem[Rs+offset] LL _{bit} = 1 LLAdr = Rs + offset
LUI	Load Upper Immediate	Rt = immediate << 16
LW	Load Word	Rt = Mem[Rs+offset]
LWPC	Load Word, PC relative	Rt = Mem[PC+offset]
LWL	Load Word Left	Re = Re MERGE Mem[Rs+offset]
LWR	Load Word Right	Re = Re MERGE Mem[Rs+offset]
MADD	Multiply-Add	HI LO += (int)Rs * (int)Rt
MADDU	Multiply-Add Unsigned	HI LO += (uns)Rs * (uns)Rt
MFC0	Move From Coprocessor 0	Rt = CPR[0, Rd, sel]
MFHI	Move From HI	Rd = HI
MFLO	Move From LO	Rd = LO
MOVN	Move Conditional on Not Zero	if Rt ≠ 0 then Rd = Rs
MOVZ	Move Conditional on Zero	if Rt = 0 then Rd = Rs
MSUB	Multiply-Subtract	HI LO -= (int)Rs * (int)Rt
MSUBU	Multiply-Subtract Unsigned	HI LO -= (uns)Rs * (uns)Rt
MTC0	Move To Coprocessor 0	CPR[0, n, Sel] = Rt
MTHI	Move To HI	HI = Rs
MTLO	Move To LO	LO = Rs
MUL	Multiply with register write	HI LO = Unpredictable Rd = ((int)Rs * (int)Rt) _{31..0}
MULT	Integer Multiply	HI LO = (int)Rs * (int)Rd
MULTU	Unsigned Multiply	HI LO = (uns)Rs * (uns)Rd
NOP	No Operation (Assembler idiom for: SLL r0, r0, r0)	
NOR	Logical NOR	Rd = ~(Rs Rt)
OR	Logical OR	Rd = Rs Rt
ORI	Logical OR Immediate	Rt = Rs Immed
RDHWR	Read Hardware Register (if enabled by HWRE _{na} Register)	Re = HWR[Rd]

Note 1: This instruction is deprecated and should not be used.

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TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
RDPGPR	Read GPR from Previous Shadow Set	$Rt = SGPR[SRSCtl_{PSS}, Rd]$
ROTR	Rotate Word Right	$Rd = Rt_{sa-1..0} Rt_{31..sa}$
ROTRV	Rotate Word Right Variable	$Rd = Rt_{Rs-1..0} Rt_{31..Rs}$
SB	Store Byte	$(byte)Mem[Rs+offset] = Rt$
SC	Store Conditional Word	if $LL_{bit} = 1$ $mem[Rs+offset] = Rt$ $Rt = LL_{bit}$
SDBBP	Software Debug Break Point	Trap to SW Debug Handler
SEB	Sign-Extend Byte	$Rd = SignExtend (Rs-7..0)$
SEH	Sign-Extend Half	$Rd = SignExtend (Rs-15..0)$
SH	Store Half	$(half)Mem[Rs+offset] = Rt$
SLL	Shift Left Logical	$Rd = Rt \ll sa$
SLLV	Shift Left Logical Variable	$Rd = Rt \ll Rs[4:0]$
SLT	Set on Less Than	if $(int)Rs < (int)Rt$ $Rd = 1$ else $Rd = 0$
SLTI	Set on Less Than Immediate	if $(int)Rs < (int)Immed$ $Rt = 1$ else $Rt = 0$
SLTIU	Set on Less Than Immediate Unsigned	if $(uns)Rs < (uns)Immed$ $Rt = 1$ else $Rt = 0$
SLTU	Set on Less Than Unsigned	if $(uns)Rs < (uns)Immed$ $Rd = 1$ else $Rd = 0$
SRA	Shift Right Arithmetic	$Rd = (int)Rt \gg sa$
SRAV	Shift Right Arithmetic Variable	$Rd = (int)Rt \gg Rs[4:0]$
SRL	Shift Right Logical	$Rd = (uns)Rt \gg sa$
SRLV	Shift Right Logical Variable	$Rd = (uns)Rt \gg Rs[4:0]$
SSNOP	Superscalar Inhibit No Operation	NOP
SUB	Integer Subtract	$Rt = (int)Rs - (int)Rd$
SUBU	Unsigned Subtract	$Rt = (uns)Rs - (uns)Rd$
SW	Store Word	$Mem[Rs+offset] = Rt$
SWL	Store Word Left	$Mem[Rs+offset] = Rt$
SWR	Store Word Right	$Mem[Rs+offset] = Rt$
SYNC	Synchronize	Orders the cached coherent and uncached loads and stores for access to the shared memory
SYSCALL	System Call	SystemCallException
TEQ	Trap if Equal	if $Rs == Rt$ TrapException
TEQI	Trap if Equal Immediate	if $Rs == (int)Immed$ TrapException

Note 1: This instruction is deprecated and should not be used.

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
TGE	Trap if Greater Than or Equal	if (int)Rs >= (int)Rt TrapException
TGEI	Trap if Greater Than or Equal Immediate	if (int)Rs >= (int)Immed TrapException
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	if (uns)Rs >= (uns)Immed TrapException
TGEU	Trap if Greater Than or Equal Unsigned	if (uns)Rs >= (uns)Rt TrapException
TLT	Trap if Less Than	if (int)Rs < (int)Rt TrapException
TLTI	Trap if Less Than Immediate	if (int)Rs < (int)Immed TrapException
TLTIU	Trap if Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed TrapException
TLTU	Trap if Less Than Unsigned	if (uns)Rs < (uns)Rt TrapException
TNE	Trap if Not Equal	if Rs != Rt TrapException
TNEI	Trap if Not Equal Immediate	if Rs != (int)Immed TrapException
WAIT	Wait for Interrupt	Go to a low power mode and stall until interrupt occurs
WRPGPR	Write to GPR in Previous Shadow Set	SGPR[SRSCtl _{PSS} , Rd] = Rt
WSBH	Word Swap Bytes Within Halfwords	Rd = Rt _{23..16} Rt _{31..24} Rt _{7..0} Rt _{15..8}
XOR	Exclusive OR	Rd = Rs ^ Rt
XORI	Exclusive OR Immediate	Rt = Rs ^ (uns)Immed

Note 1: This instruction is deprecated and should not be used.

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NOTES:

28.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC32MX3XX/4XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX3XX/4XX are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings (Note 1)

Ambient temperature under bias	-40°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any combined analog and digital pin and MCLR, with respect to VSS	-0.3V to (VDD + 0.3V)
Voltage on any digital only pin with respect to VSS	-0.3V to +5.5V
Voltage on VDDCORE with respect to VSS	-0.3V to 2.0V
Maximum current out of VSS pin(s)	300 mA
Maximum current into VDD pin(s) (Note 2)	300 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2)	200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 28-2).

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28.1 DC Characteristics

TABLE 28-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp. Range (in °C)	Max. Frequency
			PIC32MX3XX/4XX
DC5	2.3-3.6V	-40°C to +85°C	80 MHz (Note 1)

Note 1: 40 MHz maximum for PIC32MX 40MHz family variants.

TABLE 28-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
PIC32MX3XX/4XX					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH) I/O Pin Power Dissipation: I/O = S ({VDD – VOH} x IOH) + S (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 28-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 100-Pin TQFP (12x12x1 mm)	θJA	43	—	°C/W	1
Package Thermal Resistance, 64-Pin TQFP (10x10x1 mm)	θJA	47	—	°C/W	1
Package Thermal Resistance, 64-Pin QFN (9x9x0,9 mm)	θJA	28	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 28-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Operating Voltage							
DC10	Supply Voltage						
	VDD		2.3	—	3.6	V	
DC12	VDR	RAM Data Retention Voltage (Note 1)	1.75	—	—	V	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	1.75	—	1.95	V	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

TABLE 28-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial			
Parameter No.	Typical ⁽³⁾	Max.	Units	Conditions		
Operating Current (IDD)						
DC20	8.5	13	mA	—	—	4 MHz
DC20c	4.0	—	mA	Code executing from SRAM	—	
DC21	23.5	32	mA	—	—	20 MHz (Note 4)
DC21c	16.4	—	mA	Code executing from SRAM	—	
DC22	48	61	mA	—	—	60 MHz (Note 4)
DC22c	45	—	mA	Code executing from SRAM	—	
DC23	55	75	mA	—	2.3V	80 MHz
DC23c	55	—	mA	Code executing from SRAM	—	
DC24	—	100	μA	-40°C	2.3V	LPRC (31 kHz) (Note 4)
DC24a	—	130	μA	+25°C		
DC24b	—	670	μA	+85°C		
DC25	94	—	μA	-40°C	3.3V	
DC25a	125	—	μA	+25°C		
DC25b	302	—	μA	+85°C		
DC25c	71	—	μA	Code executing from SRAM	—	
DC26	—	110	μA	-40°C	3.6V	
DC26a	—	180	μA	+25°C		
DC26b	—	700	μA	+85°C		

- Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type as well as temperature can have an impact on the current consumption.
- 2:** The test conditions for IDD measurements are as follows: Oscillator mode = EC+PLL with OSC1 driven by external square wave from rail to rail and PBCLK divisor = 1:8. CPU, Program Flash and SRAM data memory are operational, Program Flash memory Wait states = 7, program cache and prefetch are disabled and SRAM data memory Wait states = 1. All peripheral modules are disabled (ON bit = 0). WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to Vss. MCLR = VDD.
- 3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.
- 4:** This parameter is characterized, but not tested in manufacturing.

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TABLE 28-6: DC CHARACTERISTICS: IDLE CURRENT (IDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial		
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions	
Idle Current (IDLE): Core OFF, Clock ON Base Current (Note 1)					
DC30	—	5	mA	2.3V	4 MHz
DC30a	1.4	—	mA	—	
DC30b	—	5	mA	3.6V	
DC31	—	15	mA	2.3V	20 MHz, (Note 3)
DC31a	13	—	mA	—	
DC31b	—	17	mA	3.6V	
DC32	—	22	mA	2.3V	60 MHz (Note 3)
DC32a	20	—	mA	—	
DC32b	—	25	mA	3.6V	
DC33	—	29	mA	2.3V	80 MHz
DC33a	24	—	mA	—	
DC33b	—	32	mA	3.6V	
DC34	—	36	μA	-40°C	LPRC (31 kHz) (Note 3)
DC34a	—	62	μA	$+25^{\circ}\text{C}$	
DC34b	—	392	μA	$+85^{\circ}\text{C}$	
DC35	35	—	μA	-40°C	
DC35a	65	—	μA	$+25^{\circ}\text{C}$	
DC35b	242	—	μA	$+85^{\circ}\text{C}$	
DC36	—	43	μA	-40°C	
DC36a	—	106	μA	$+25^{\circ}\text{C}$	
DC36b	—	414	μA	$+85^{\circ}\text{C}$	

- Note 1:** The test conditions for base IDLE current measurements are as follows: System clock is enabled and PBCLK divisor = 1:8. CPU in Idle mode (CPU core halted). Only digital peripheral modules are enabled (ON bit = 1) and being clocked. WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to VSS. MCLR = VDD.
- 2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** This parameter is characterized, but not tested in manufacturing.

TABLE 28-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial		
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions	
Power-Down Current (IPD) (Note 1)					
DC40	7	30	μA	-40°C	2.3V Base Power-Down Current (Note 6)
DC40a	24	30	μA	$+25^{\circ}\text{C}$	
DC40b	205	300	μA	$+85^{\circ}\text{C}$	
DC40c	25	—	μA	$+25^{\circ}\text{C}$	3.3V Base Power-Down Current
DC40d	9	70	μA	-40°C	3.6V Base Power-Down Current
DC40e	25	70	μA	$+25^{\circ}\text{C}$	
DC40g	115	200 (Note 5)	μA	$+70^{\circ}\text{C}$	
DC40f	200	400	μA	$+85^{\circ}\text{C}$	
Module Differential Current					
DC41	—	10	μA	-40°C	2.3V Watchdog Timer Current: ΔIWDT (Notes 3, 6)
DC41a	—	10	μA	$+25^{\circ}\text{C}$	
DC41b	—	10	μA	$+85^{\circ}\text{C}$	
DC41c	5	—	μA	$+25^{\circ}\text{C}$	3.3V Watchdog Timer Current: ΔIWDT (Note 3)
DC41d	—	10	μA	-40°C	3.6V Watchdog Timer Current: ΔIWDT (Note 3)
DC41e	—	10	μA	$+25^{\circ}\text{C}$	
DC41f	—	12	μA	$+85^{\circ}\text{C}$	
DC42	—	10	μA	-40°C	2.3V RTCC + Timer1 w/32kHz Crystal: ΔIRTCC (Notes 3, 6)
DC42a	—	17	μA	$+25^{\circ}\text{C}$	
DC42b	—	37	μA	$+85^{\circ}\text{C}$	
DC42c	23	—	μA	$+25^{\circ}\text{C}$	3.3V RTCC + Timer1 w/32kHz Crystal: ΔIRTCC (Note 3)
DC42e	—	10	μA	-40°C	3.6V RTCC + Timer1 w/32kHz Crystal: ΔIRTCC (Note 3)
DC42f	—	30	μA	$+25^{\circ}\text{C}$	
DC42g	—	44	μA	$+85^{\circ}\text{C}$	
DC42	—	1100	μA	-40°C	2.5V ADC: ΔIADC (Notes 3, 4, 6)
DC42a	—	1100	μA	$+25^{\circ}\text{C}$	
DC42b	—	1000	μA	$+85^{\circ}\text{C}$	
DC42c	880	—	μA		ADC: ΔIADC (Notes 3, 4)
DC42e	—	1100	μA	-40°C	3.6V ADC: ΔIADC (Notes 3, 4)
DC42f	—	1100	μA	$+25^{\circ}\text{C}$	
DC42g	—	1000	μA	$+85^{\circ}\text{C}$	

Note 1: Base IPD is measured with all digital peripheral modules enabled (ON bit = 1) and being clocked, CPU clock is disabled. All I/Os are configured as outputs and pulled low. WDT and FSCM are disabled.

2: Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

5: Data is characterized at $+70^{\circ}\text{C}$ and not tested. Parameter is for design guidance only.

6: This parameter is characterized, but not tested in manufacturing.

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TABLE 28-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial						
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions		
DI10	V _{IL}	Input Low Voltage							
		I/O pins:							
		with TTL Buffer	V _{SS}	—	0.15 V _{DD}	V	(Note 4)		
		with Schmitt Trigger Buffer	V _{SS}	—	0.2 V _{DD}	V	(Note 4)		
		$\overline{\text{MCLR}}$	V _{SS}	—	0.2 V _{DD}	V	(Note 4)		
		OSC1 (XT mode)	V _{SS}	—	0.2 V _{DD}	V	(Note 4)		
		OSC1 (HS mode)	V _{SS}	—	0.2 V _{DD}	V	(Note 4)		
DI15		$\overline{\text{MCLR}}$	V _{SS}	—	0.2 V _{DD}	V	(Note 4)		
DI16		OSC1 (XT mode)	V _{SS}	—	0.2 V _{DD}	V	(Note 4)		
DI17		OSC1 (HS mode)	V _{SS}	—	0.2 V _{DD}	V	(Note 4)		
DI18		SDAx, SCLx	V _{SS}	—	0.3 V _{DD}	V	SMBus disabled (Note 4)		
DI19		SDAx, SCLx	V _{SS}	—	0.8	V	SMBus enabled (Note 4)		
DI20	V _{IH}	Input High Voltage							
		I/O pins:							
		with Analog Functions	0.8 V _{DD}	—	V _{DD}	V	(Note 4)		
		Digital Only	0.8 V _{DD}	—		V	(Note 4)		
		with TTL Buffer	0.25V _{DD} + 0.8v	—	5.5	V	(Note 4)		
		with Schmitt Trigger Buffer	0.8 V _{DD}	—	5.5	V	(Note 4)		
		DI25		$\overline{\text{MCLR}}$	0.8 V _{DD}	—	V _{DD}	V	(Note 4)
		DI26		OSC1 (XT mode)	0.7 V _{DD}	—	V _{DD}	V	(Note 4)
		DI27		OSC1 (HS mode)	0.7 V _{DD}	—	V _{DD}	V	(Note 4)
		DI28		SDAx, SCLx	0.7 V _{DD}	—	5.5	V	SMBus disabled (Note 4)
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ V _{PIN} ≤ 5.5 (Note 4)		
DI30	IC _{NPU}	CNxx Pull up Current	50	250	400	μA	V _{DD} = 3.3V, V _{PIN} = V _{SS}		
DI50	I _{IL}	Input Leakage Current (Note 3)							
		I/O Ports	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance		
		Analog Input Pins	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance		
		$\overline{\text{MCLR}}$	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}		
		OSC1	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT and HS modes		

- Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** This parameter is characterized, but not tested in manufacturing.

TABLE 28-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
DO10	VOL	Output Low Voltage I/O Ports	—	—	0.4	V	IOL = 7 mA, VDD = 3.6V
DO16		OSC2/CLKO	—	—	0.4	V	IOL = 6 mA, VDD = 2.3V
			—	—	0.4	V	IOL = 3.5 mA, VDD = 3.6V
			—	—	0.4	V	IOL = 2.5 mA, VDD = 2.3V
DO20	VOH	Output High Voltage I/O Ports	2.4	—	—	V	IOH = -12 mA, VDD = 3.6V
			1.4	—	—	V	IOH = -12 mA, VDD = 2.3V
DO26		OSC2/CLKO	2.4	—	—	V	IOH = -12 mA, VDD = 3.6V
			1.4	—	—	V	IOH = -12 mA, VDD = 2.3V

TABLE 28-10: DC CHARACTERISTICS: PROGRAM MEMORY⁽³⁾

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Programming temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (25°C recommended)				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
		Program Flash Memory					
D130	EP	Cell Endurance	1000	—	—	E/W	-40°C to $+85^{\circ}\text{C}$
D131	VPR	VDD for Read	V _{MIN}	—	3.6	V	V _{MIN} = Minimum operating voltage
D132	VPEW	VDD for Erase or Write	3.0	—	3.6	V	0°C to $+40^{\circ}\text{C}$
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	0°C to $+40^{\circ}\text{C}$
	TWW	Word Write Cycle Time	20	—	40	μs	0°C to $+40^{\circ}\text{C}$
D136	TRW	Row Write Cycle Time (Note 2) (128 words per row)	3	4.5	—	ms	0°C to $+40^{\circ}\text{C}$
D137	TPE	Page Erase Cycle Time	20	—	—	ms	0°C to $+40^{\circ}\text{C}$
	TCE	Chip Erase Cycle Time	80	—	—	ms	0°C to $+40^{\circ}\text{C}$

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to *PIC32MX Flash Programming Specification* (DS61145) for operating conditions during programming and erase cycles.

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TABLE 28-11: PROGRAM FLASH MEMORY WAIT STATE CHARACTERISTICS

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial		
Required Flash wait states	SYSCLK	Units	Comments	
0 Wait State	0 to 30	MHz		
1 Wait State	31 to 60			
2 Wait States	61 to 80			

Note 1: 40 MHz maximum for PIC32MX 40MHz family variants.

TABLE 28-12: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D300	VIOFF	Input Offset Voltage	—	± 7.5	± 25	mV	$AV_{DD} = V_{DD}$, $AV_{SS} = V_{SS}$
D301	VICM	Input Common Mode Voltage	0	—	V_{DD}	V	$AV_{DD} = V_{DD}$, $AV_{SS} = V_{SS}$ (Note 2)
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max $V_{ICM} = (V_{DD} - 1)V$ (Note 2)
D303	TRESP	Response Time	—	150	400	nsec	$AV_{DD} = V_{DD}$, $AV_{SS} = V_{SS}$ (Notes 1, 2)
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	μs	Comparator module is configured before setting the comparator ON bit. (Note 2)

Note 1: Response time measured with one comparator input at $(V_{DD} - 1.5)/2$, while the other input transitions from V_{SS} to V_{DD} .

2: These parameters are characterized but not tested.

TABLE 28-13: VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D310	VRES	Resolution	$V_{DD}/24$	—	$V_{DD}/32$	LSb	
D311	VRAA	Absolute Accuracy	—	—	1/2	LSb	
D312	TSET	Settling Time ⁽¹⁾	—	—	10	μs	

Note 1: Settling time measured while $CVRR = 1$ and $CVR3:CVR0$ transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

TABLE 28-14: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D320	VDDCORE	Regulator Output Voltage	1.62	1.80	1.98	V	
D321	CEFC	External Filter Capacitor Value	4.7	10	—	μF	Capacitor must be low series resistance (< 3 ohms)
D322	TPWRT		—	64	—	ms	ENVREG = 0

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28.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX3XX/4XX AC characteristics and timing parameters.

TABLE 28-15: AC CHARACTERISTICS

AC CHARACTERISTICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Operating voltage V_{DD} range.
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FIGURE 28-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

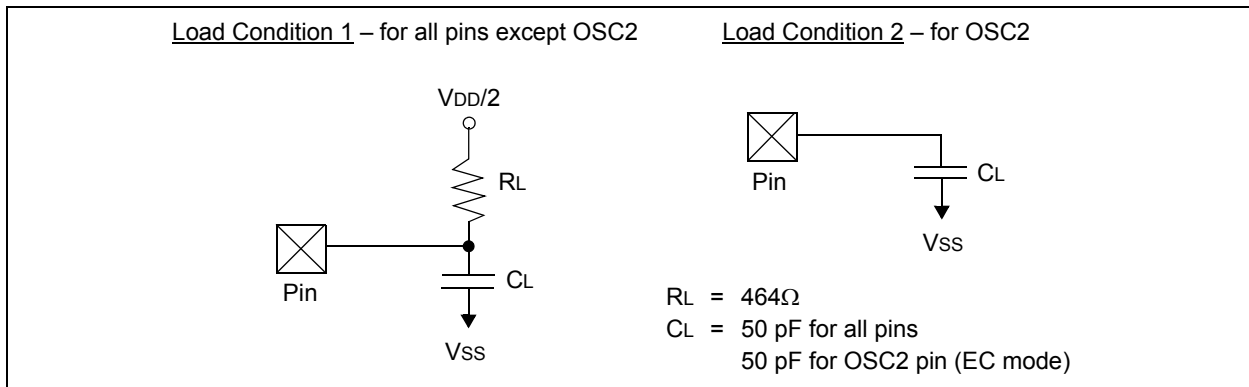


TABLE 28-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
DO56	C _{IO}	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	C _B	SCL _x , SDA _x	—	—	400	pF	In I ² C™ mode

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 28-2: EXTERNAL CLOCK TIMING

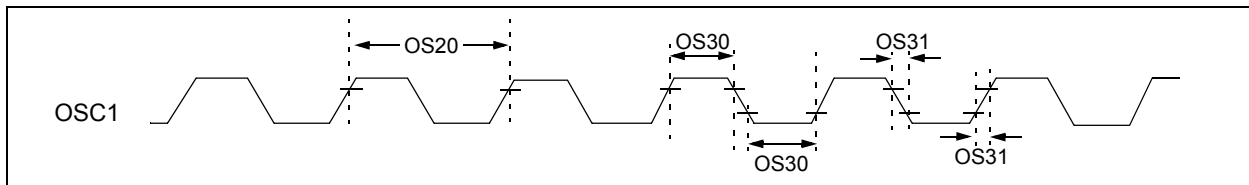


TABLE 28-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	50 (Note 3) 50 (Note 5)	MHz MHz	EC (Note 5) ECPLL (Note 4)
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT (Note 5)
OS12			4	—	10	MHz	XTPLL (Notes 4, 5)
OS13			10	—	25	MHz	HS (Note 5)
OS14			10	—	25	MHz	HSPLL (Notes 4, 5)
OS15			32	32.768	100	kHz	SOSC (Note 5)
OS20	Tosc	$T_{osc} = 1/F_{osc} = T_{CY}$ (Note 2)	—	—	—	—	See parameter OS10 for Fosc value
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	$0.45 \times T_{osc}$	—	—	nsec	EC (Note 5)
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	—	—	$0.05 \times T_{osc}$	nsec	EC (Note 5)
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and SOSC Clock Oscillator modes)	—	1024	—	Tosc	(Note 5)
OS41	TfSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 5)
OS42	GM	External Oscillator Transconductance	—	12	—	mA/V	$V_{DD} = 3.3V$ $T_A = +25^{\circ}\text{C}$ (Note 5)

- Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.
- 2:** Instruction cycle period (T_{CY}) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.
- 3:** 40 MHz maximum for PIC32MX 40 MHz family variants.
- 4:** PLL input requirements: $4 \text{ MHz} \leq F_{PLLIN} \leq 5 \text{ MHz}$ (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 5:** This parameter is characterized, but not tested in manufacturing.

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TABLE 28-18: PLL CLOCK TIMING SPECIFICATIONS (VDD = 2.3V TO 3.6V)

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	4	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes
OS51	FSYS	On-Chip VCO System Frequency	60	—	120	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	
OS53	DCLK	CLKO Stability (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period

Note 1: These parameters are characterized, but not tested in manufacturing.

Note 2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 28-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions	
Internal FRC Accuracy @ 8.00 MHz (Note 1)							
F20	FRC	-2	—	+2	%		

Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

TABLE 28-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial					
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions	
LPRC @ 31.25 kHz (Note 1)							
F21		-15	—	+15	%		

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 28-3: I/O TIMING CHARACTERISTICS

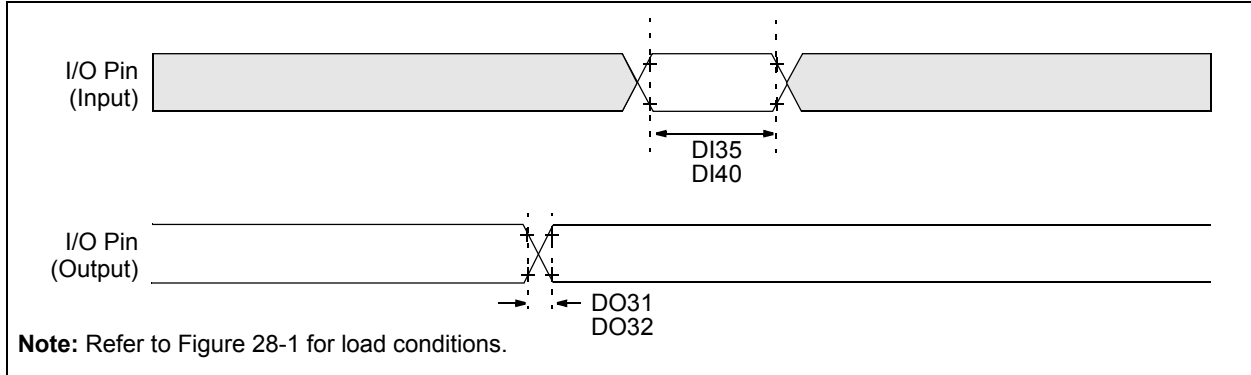


TABLE 28-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial					
Param. No.	Symbol	Characteristics ⁽²⁾	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time	—	5	10	nsec	
DO32	TioF	Port Output Fall Time	—	5	10	nsec	
DI35	TINP	INTx Pin High or Low Time	10	—	—	nsec	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TSYSCLK	

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

Note 2: This parameter is characterized, but not tested in manufacturing.

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FIGURE 28-4: POWER-ON RESET TIMING CHARACTERISTICS

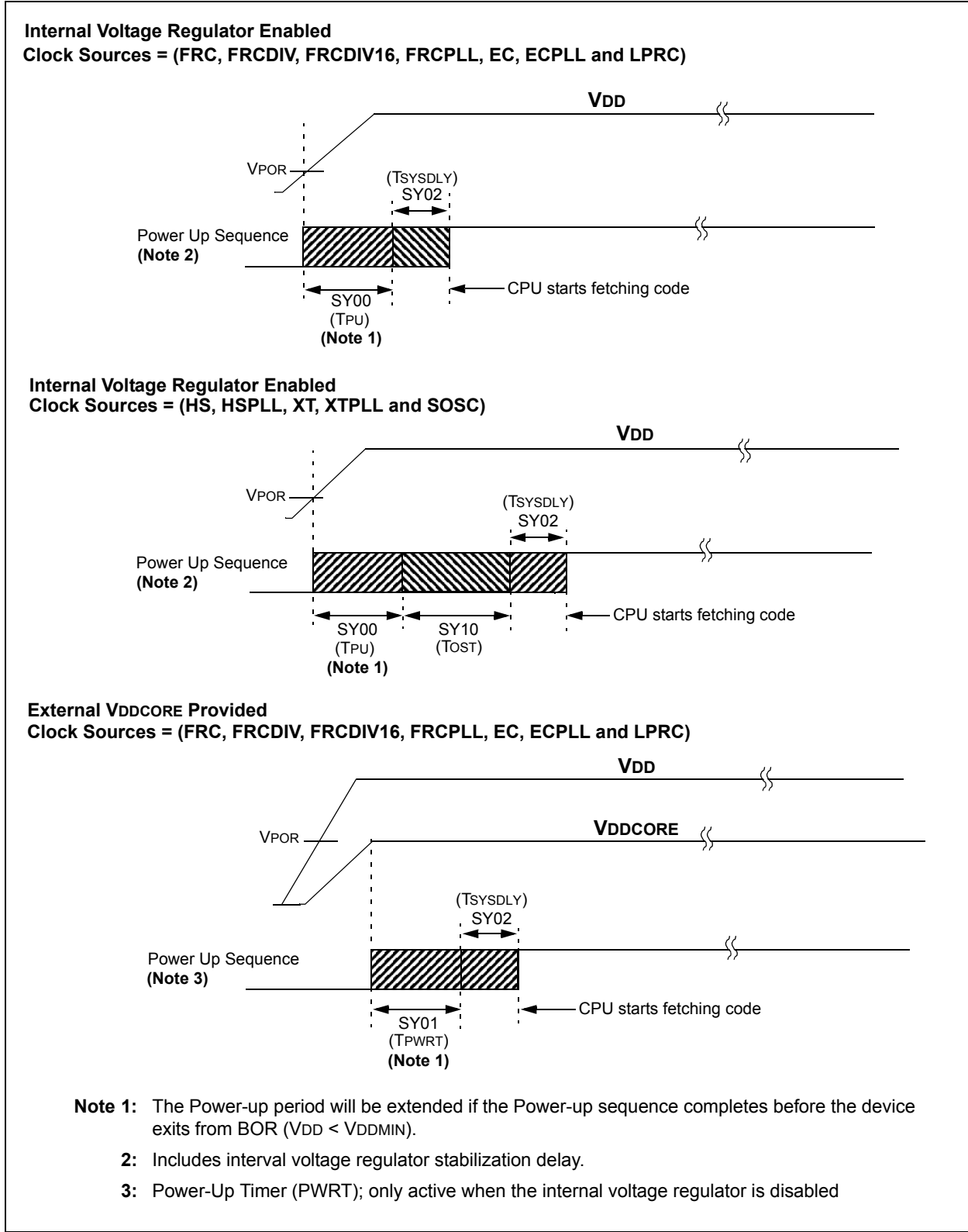


FIGURE 28-5: EXTERNAL RESET TIMING CHARACTERISTICS

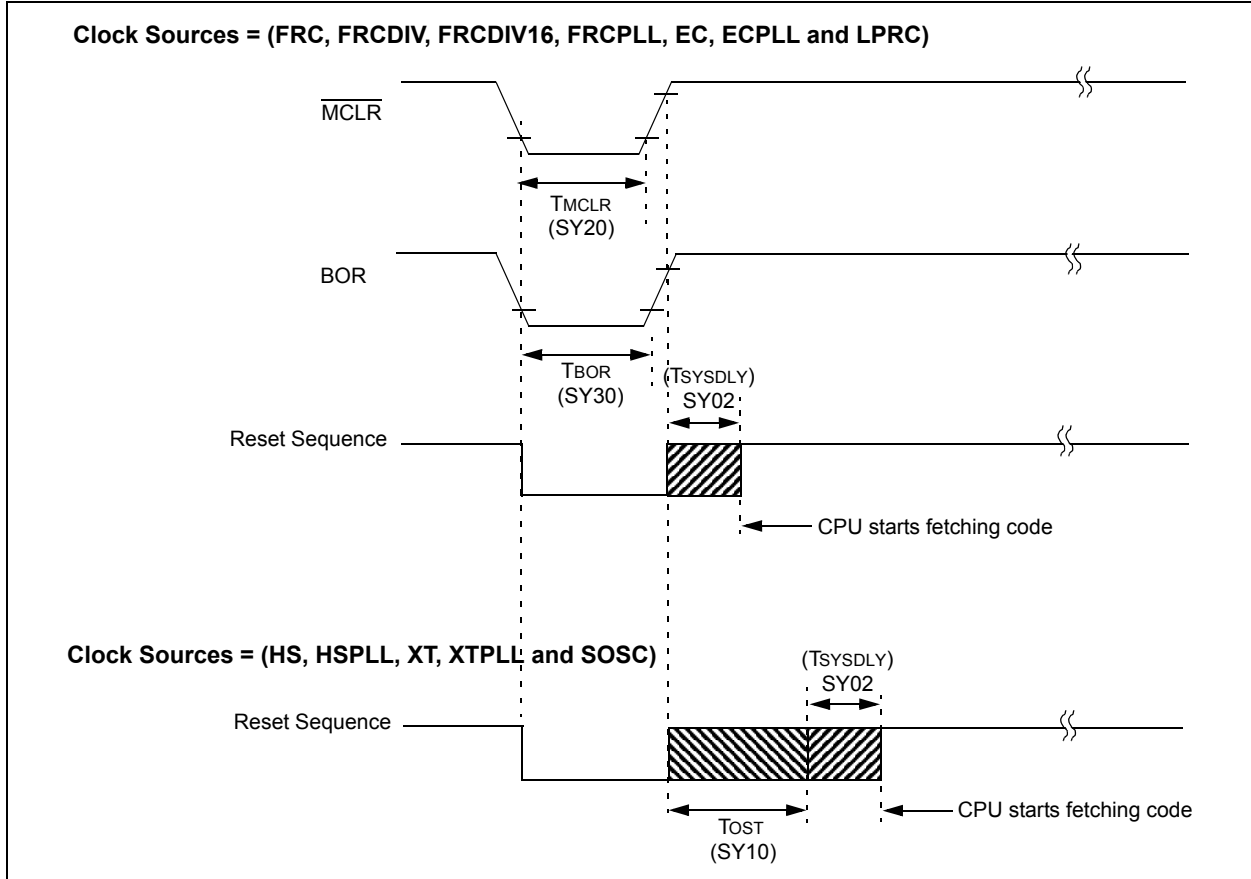


TABLE 28-22: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_a \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	-40°C to $+85^{\circ}\text{C}$
SY01	TPWRT	Power-up Period External VDDCORE Applied (Power-Up-Timer Active)	48	64	80	ms	-40°C to $+85^{\circ}\text{C}$
SY02	T_{SYSDLY}	System Delay Period: Time required to reload Device Configuration Fuses plus SY_{SCLK} delay before first instruction is fetched.	—	$1 \mu\text{s}$ + $8 \text{ } SY_{SCLK}$ cycles	—	—	-40°C to $+85^{\circ}\text{C}$
SY20	T_{MCLR}	\overline{MCLR} Pulse Width (low)	—	2	—	μs	-40°C to $+85^{\circ}\text{C}$
SY30	T_{BOR}	BOR Pulse Width (low)	—	1	—	μs	-40°C to $+85^{\circ}\text{C}$

Note 1: These parameters are characterized, but not tested in manufacturing.

Note 2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

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FIGURE 28-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS

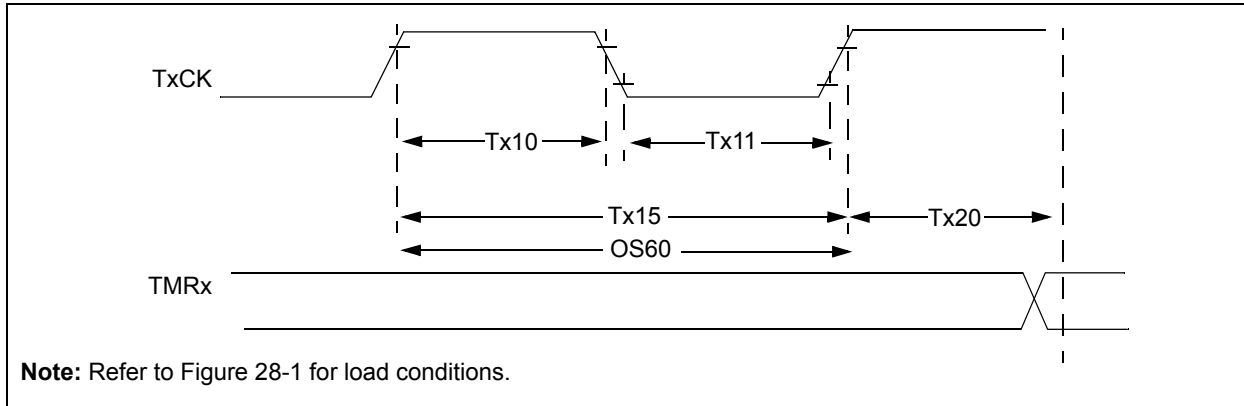


TABLE 28-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial						
Param. No.	Symbol	Characteristics ⁽²⁾		Min.	Typical	Max.	Units	Conditions
TA10	TTXH	TxCK High Time	Synchronous, with prescaler	$[(12.5\text{nsec or } 1\text{TPB}) / N] + 25\text{nsec}$	—	—	nsec	Must also meet parameter TA15.
			Asynchronous, with prescaler	10	—	—	nsec	
TA11	TTXL	TxCK Low Time	Synchronous, with prescaler	$[(12.5\text{nsec or } 1\text{TPB}) / N] + 25\text{nsec}$	—	—	nsec	Must also meet parameter TA15.
			Asynchronous, with prescaler	10	—	—	nsec	
TA15	TTXP	TxCK Input Period	Synchronous, with prescaler	$[(25\text{nsec or } 2\text{TPB}) / N] + 50\text{nsec}$	—	—	nsec	N = prescale value (1, 8, 64, 256)
			Asynchronous, with prescaler	20	—	—	nsec	
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	100	kHz	
TA20	TCKEXT-MRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPB	

Note 1: Timer1 is a Type A.

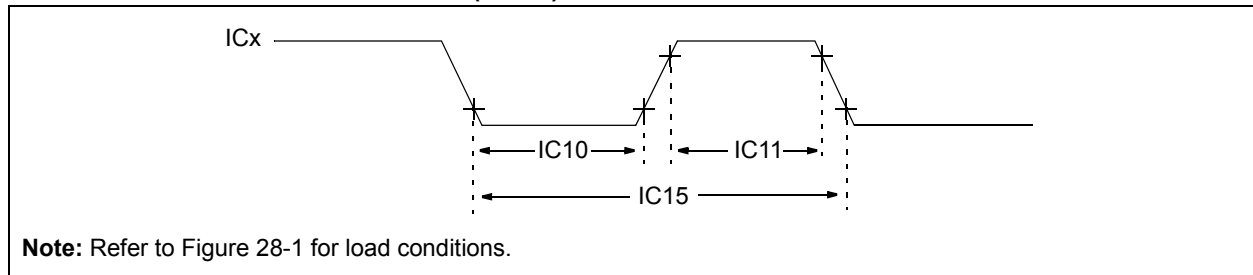
Note 2: This parameter is characterized, but not tested in manufacturing.

TABLE 28-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Max.	Units	Conditions
TB10	TTXH	TxCK High Time	Synchronous, with prescaler	$[(12.5\text{nsec or } 1\text{TPB}) / N] + 25\text{nsec}$	—	nsec	Must also meet parameter TB15. N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	TTXL	TxCK Low Time	Synchronous, with prescaler	$[(12.5\text{nsec or } 1\text{TPB}) / N] + 25\text{nsec}$	—	nsec	
TB15	TTXP	TxCK Input Period	Synchronous, with prescaler	$[(25\text{nsec or } 2\text{TPB}) / N] + 50\text{nsec}$	—	nsec	
TB20	TCKEXT-MRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPB	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 28-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



Note: Refer to Figure 28-1 for load conditions.

TABLE 28-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Max.	Units	Conditions
IC10	TcCL	ICx Input Low Time		$[(12.5\text{nsec or } 1\text{TPB}) / N] + 25\text{nsec}$	—	nsec	Must also meet parameter IC15. N = prescale value (1, 4, 16)
IC11	TcCH	ICx Input High Time		$[(12.5\text{nsec or } 1\text{TPB}) / N] + 25\text{nsec}$	—	nsec	
IC15	TcCP	ICx Input Period		$[(25\text{nsec or } 2\text{TPB}) / N] + 50\text{nsec}$	—	nsec	

Note 1: These parameters are characterized, but not tested in manufacturing.

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FIGURE 28-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS

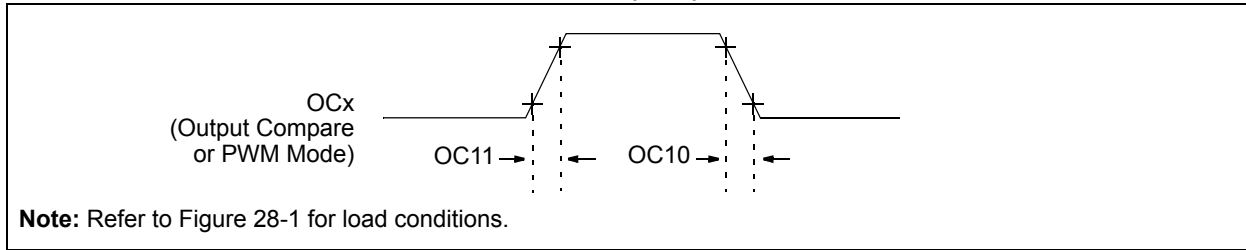


TABLE 28-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	nsec	See parameter DO32.
OC11	TccR	OCx Output Rise Time	—	—	—	nsec	See parameter DO31.

- Note 1:** These parameters are characterized, but not tested in manufacturing.
Note 2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 28-9: OC/PWM MODULE TIMING CHARACTERISTICS

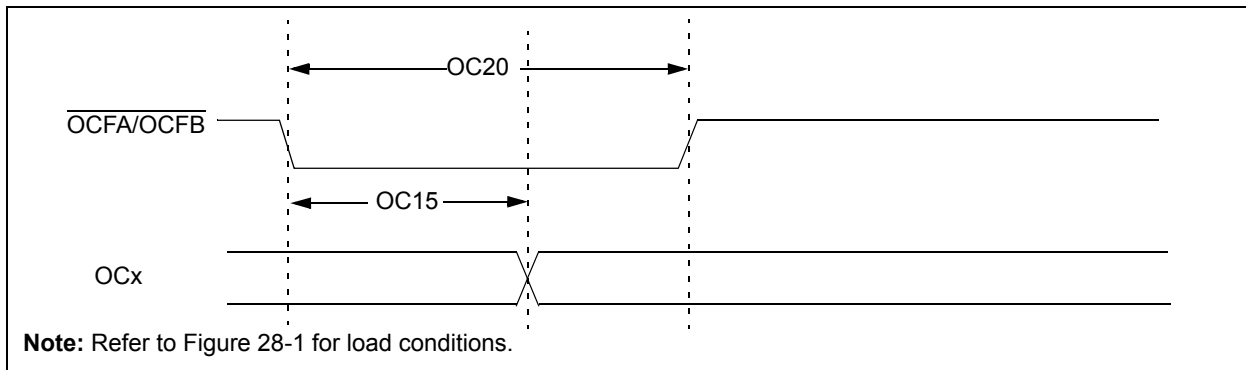


TABLE 28-27: SIMPLE OC/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristics ⁽¹⁾	Min	Typical ⁽²⁾	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	25	nsec	
OC20	TFLT	Fault Input Pulse Width	50	—	—	nsec	

- Note 1:** These parameters are characterized, but not tested in manufacturing.
Note 2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 28-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

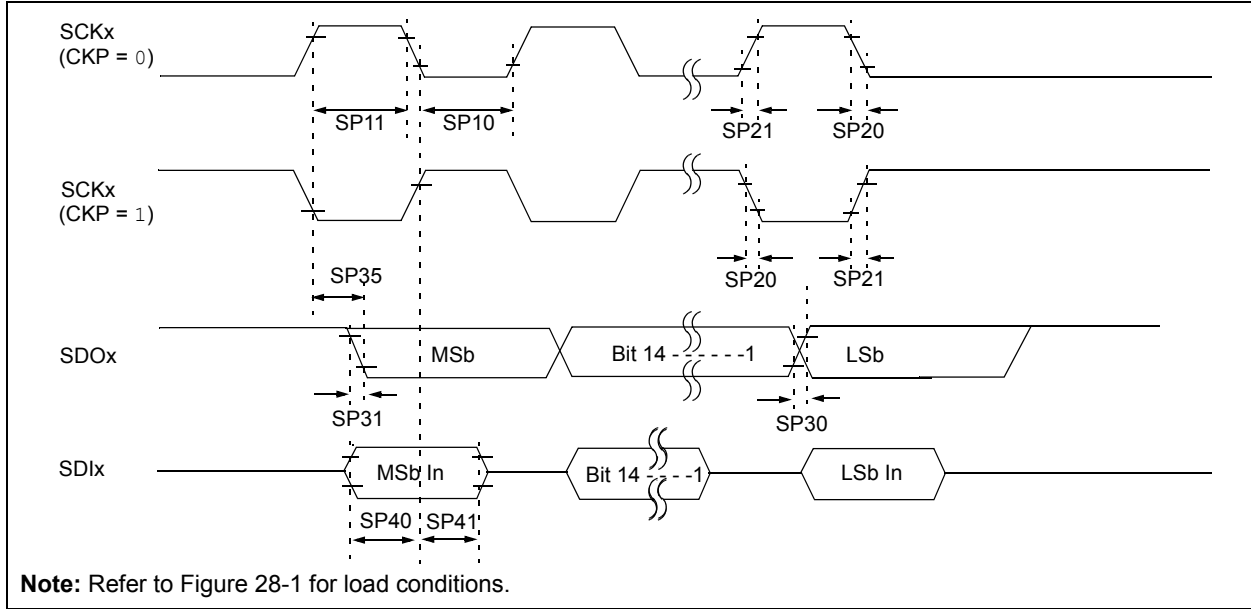


TABLE 28-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time (Note 3)	$T_{\text{SCK}}/2$	—	—	nsec	
SP11	Tsch	SCKx Output High Time (Note 3)	$T_{\text{SCK}}/2$	—	—	nsec	
SP20	TscF	SCKx Output Fall Time (Note 4)	—	—	—	nsec	See parameter DO32.
SP21	TscR	SCKx Output Rise Time (Note 4)	—	—	—	nsec	See parameter DO31.
SP30	TdOF	SDOx Data Output Fall Time (Note 4)	—	—	—	nsec	See parameter DO32.
SP31	TdOR	SDOx Data Output Rise Time (Note 4)	—	—	—	nsec	See parameter DO31.
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	nsec	
SP40	TdIV2sch, TdIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	
SP41	Tsch2dIL, TscL2dIL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 nsec. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

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FIGURE 28-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

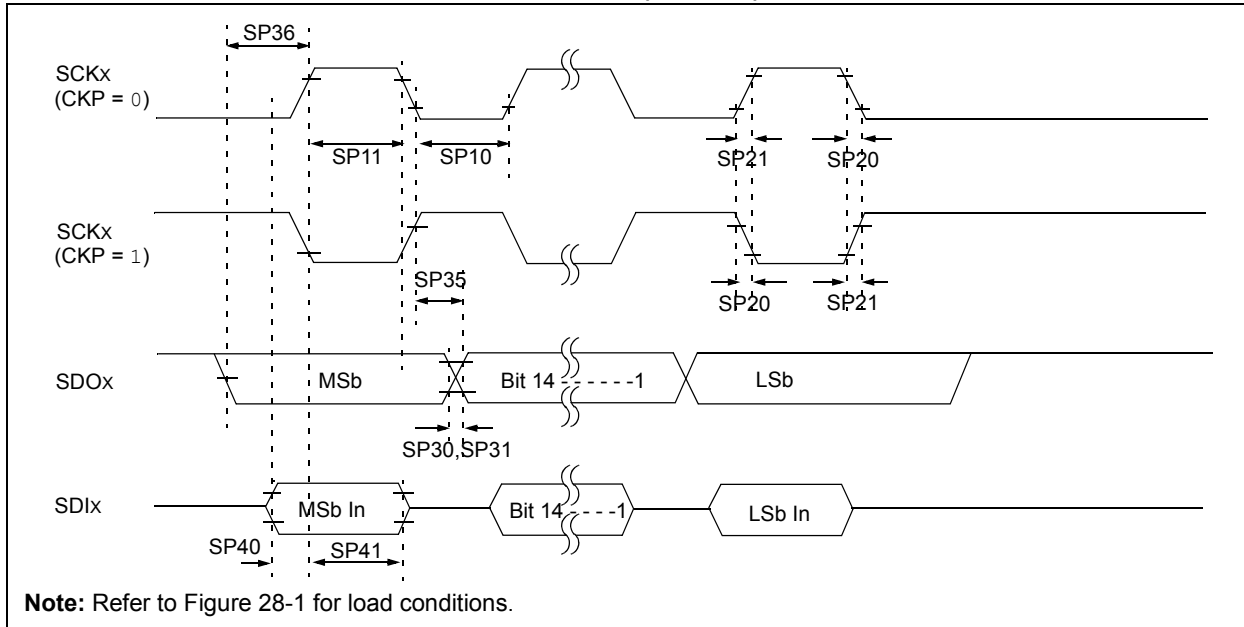


TABLE 28-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP10	TsCL	SCKx Output Low Time (Note 3)	$T_{\text{sck}}/2$	—	—	nsec	
SP11	TsCH	SCKx Output High Time (Note 3)	$T_{\text{sck}}/2$	—	—	nsec	
SP20	TsCF	SCKx Output Fall Time (Note 4)	—	—	—	nsec	See parameter DO32.
SP21	TsCR	SCKx Output Rise Time (Note 4)	—	—	—	nsec	See parameter DO31.
SP30	TdOF	SDOx Data Output Fall Time (Note 4)	—	—	—	nsec	See parameter DO32.
SP31	TdOR	SDOx Data Output Rise Time (Note 4)	—	—	—	nsec	See parameter DO31.
SP35	TsCH2dOV, TsCL2dOV	SDOx Data Output Valid after SCKx Edge	—	—	15	nsec	
SP36	TdOV2sc, TdOV2sCL	SDOx Data Output Setup to First SCKx Edge	15	—	—	nsec	
SP40	TdIV2sCH, TdIV2sCL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	

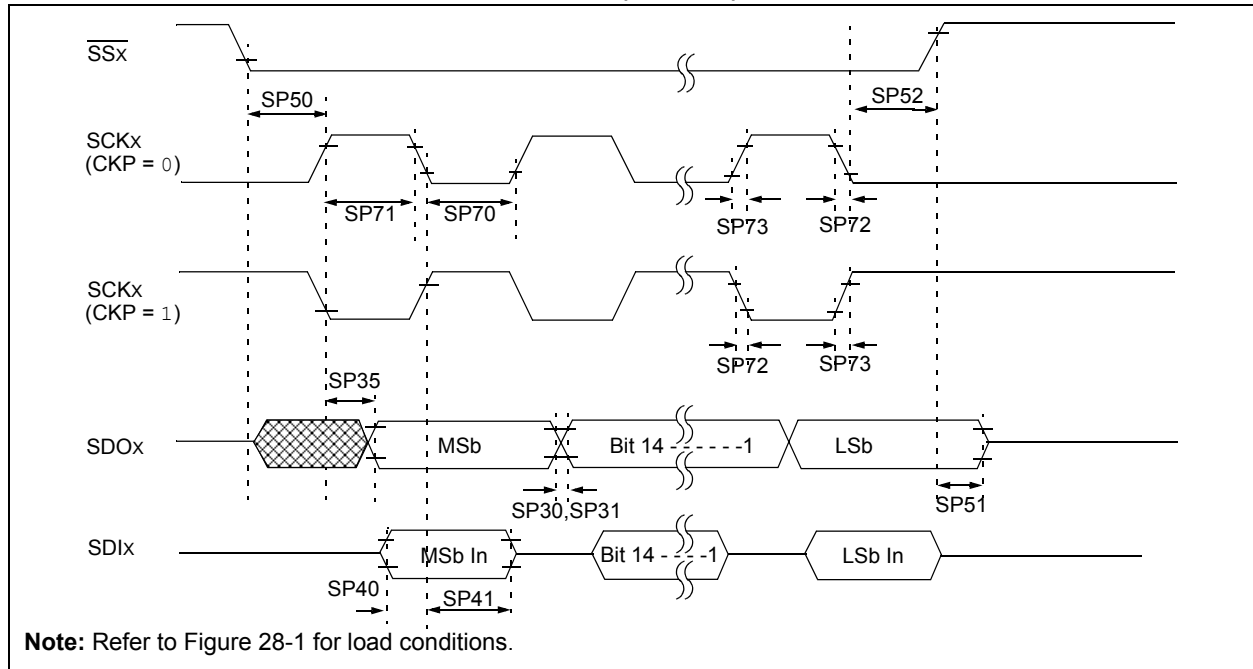
- Note 1:** These parameters are characterized, but not tested in manufacturing.
- Note 2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- Note 3:** The minimum clock period for SCKx is 40 nsec. Therefore, the clock generated in Master mode must not violate this specification.
- Note 4:** Assumes 50 pF load on all SPIx pins.

TABLE 28-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP41	TsCH2DiL, TsCL2DiL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	

- Note 1:** These parameters are characterized, but not tested in manufacturing.
- Note 2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- Note 3:** The minimum clock period for SCKx is 40 nsec. Therefore, the clock generated in Master mode must not violate this specification.
- Note 4:** Assumes 50 pF load on all SPIx pins.

FIGURE 28-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



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TABLE 28-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time (Note 3)	$T_{\text{SCK}}/2$	—	—	nsec	
SP71	TscH	SCKx Input High Time (Note 3)	$T_{\text{SCK}}/2$	—	—	nsec	
SP72	TscF	SCKx Input Fall Time	—	5	10	nsec	
SP73	TscR	SCKx Input Rise Time	—	5	10	nsec	
SP30	TdoF	SDOx Data Output Fall Time (Note 4)	—	—	—	nsec	See parameter DO32.
SP31	TdoR	SDOx Data Output Rise Time (Note 4)	—	—	—	nsec	See parameter DO31.
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	nsec	
SP40	TdIV2sch, TdIV2scl	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	
SP50	TssL2sch, TssL2scl	$\overline{\text{SS}}_x \downarrow$ to SCKx \uparrow or SCKx Input	60	—	—	nsec	
SP51	TssH2doZ	$\overline{\text{SS}}_x \uparrow$ to SDOx Output High-Impedance (Note 3)	5	—	25	nsec	
SP52	Tsch2ssH TscL2ssH	$\overline{\text{SS}}_x$ after SCKx Edge	$T_{\text{SCK}} + 20$	—	—	nsec	—

Note 1: These parameters are characterized, but not tested in manufacturing.

Note 2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Note 3: The minimum clock period for SCKx is 40 nsec.

Note 4: Assumes 50 pF load on all SPIx pins.

FIGURE 28-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

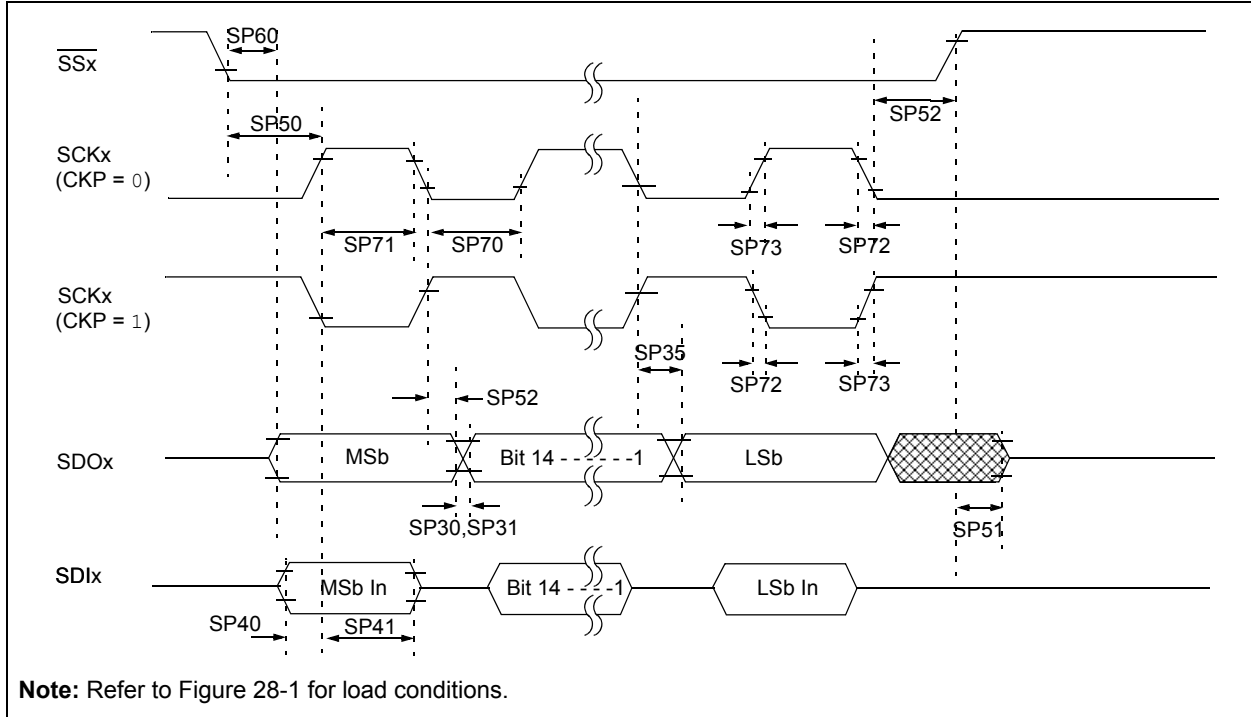


TABLE 28-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP70	TsCL	SCKx Input Low Time (Note 3)	$T_{\text{sck}}/2$	—	—	nsec	
SP71	TsCH	SCKx Input High Time (Note 3)	$T_{\text{sck}}/2$	—	—	nsec	
SP72	TscF	SCKx Input Fall Time	—	5	10	nsec	
SP73	TscR	SCKx Input Rise Time	—	5	10	nsec	
SP30	TdOF	SDOx Data Output Fall Time (Note 4)	—	—	—	nsec	See parameter DO32.
SP31	TdOR	SDOx Data Output Rise Time (Note 4)	—	—	—	nsec	See parameter DO31.
SP35	Tsch2DoV, Tscl2DoV	SDOx Data Output Valid after SCKx Edge	—	—	15	nsec	
SP40	TdIV2sCH, TdIV2sCL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	
SP41	Tsch2dIL, Tscl2dIL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	

Note 1: These parameters are characterized, but not tested in manufacturing.

Note 2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Note 3: The minimum clock period for SCKx is 40 nsec.

Note 4: Assumes 50 pF load on all SPIx pins.

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TABLE 28-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP50	TssL2sch, TssL2scl	$\overline{\text{SS}}_x \downarrow$ to SCKx \downarrow or SCKx \uparrow Input	60	—	—	nsec	
SP51	TssH2doZ	$\overline{\text{SS}}_x \uparrow$ to SDOx Output High-Impedance (Note 4)	5	—	25	nsec	
SP52	Tsch2ssH TscL2ssH	$\overline{\text{SS}}_x \uparrow$ after SCKx Edge	Tsck + 20	—	—	nsec	
SP60	TssL2doV	SDOx Data Output Valid after $\overline{\text{SS}}_x$ Edge	—	—	25	nsec	

- Note 1:** These parameters are characterized, but not tested in manufacturing.
Note 2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
Note 3: The minimum clock period for SCKx is 40 nsec.
Note 4: Assumes 50 pF load on all SPIx pins.

FIGURE 28-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

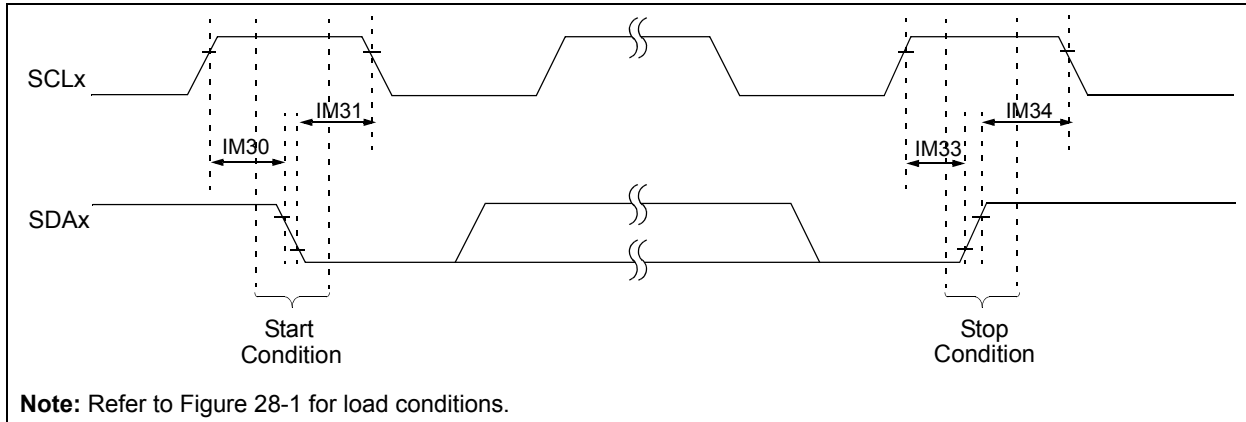


FIGURE 28-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

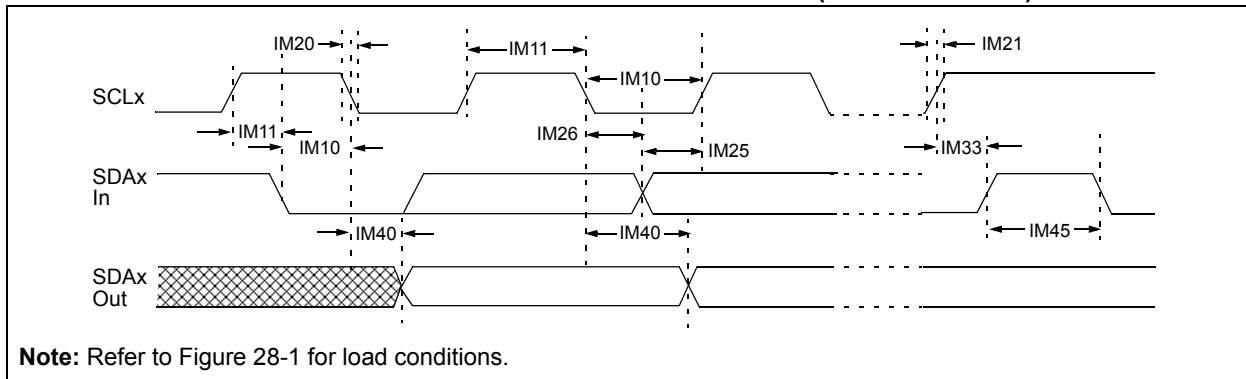


TABLE 28-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	—
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$T_{PB} * (BRG + 2)$	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	—
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$T_{PB} * (BRG + 2)$	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	nsec	Cb is specified to be from 10 to 400 pF.
			400 kHz mode	$20 + 0.1 C_b$	300	nsec	
			1 MHz mode (Note 2)	—	100	nsec	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	nsec	Cb is specified to be from 10 to 400 pF.
			400 kHz mode	$20 + 0.1 C_b$	300	nsec	
			1 MHz mode (Note 2)	—	300	nsec	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	nsec	—
			400 kHz mode	100	—	nsec	
			1 MHz mode (Note 2)	100	—	nsec	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 2)	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	Only relevant for Repeated Start condition.
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$T_{PB} * (BRG + 2)$	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	After this period, the first clock pulse is generated.
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$T_{PB} * (BRG + 2)$	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	—
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$T_{PB} * (BRG + 2)$	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	nsec	—
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	nsec	
			1 MHz mode (Note 2)	$T_{PB} * (BRG + 2)$	—	nsec	

Note 1: BRG is the value of the I²C™ Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

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TABLE 28-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min. ⁽¹⁾	Max.	Units	Conditions	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	nsec	—
			400 kHz mode	—	1000	nsec	
			1 MHz mode (Note 2)	—	350	nsec	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start.
			400 kHz mode	1.3	—	μs	
			1 MHz mode (Note 2)	0.5	—	μs	
IM50	CB	Bus Capacitive Loading	—	400	pF		

Note 1: BRG is the value of the I²C™ Baud Rate Generator.

Note 2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

FIGURE 28-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

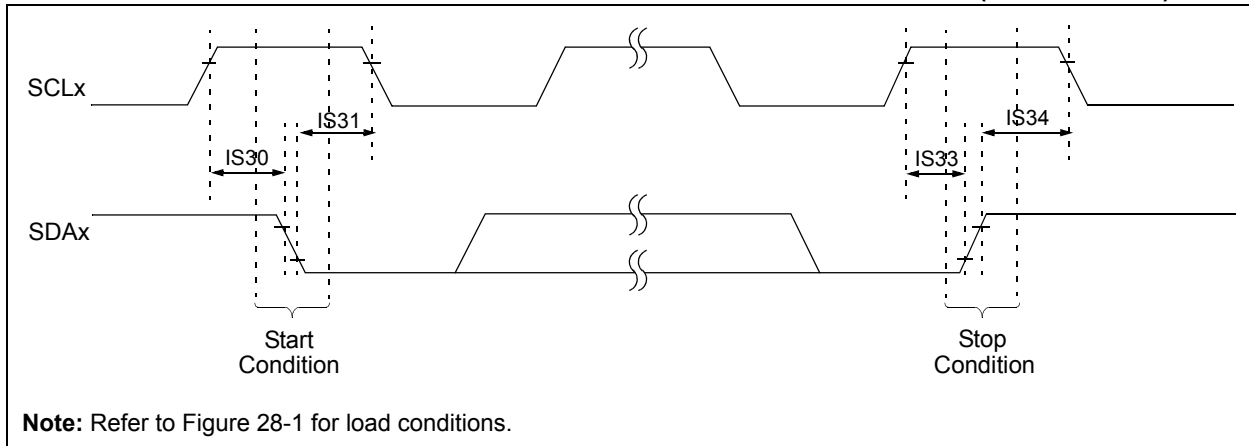


FIGURE 28-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

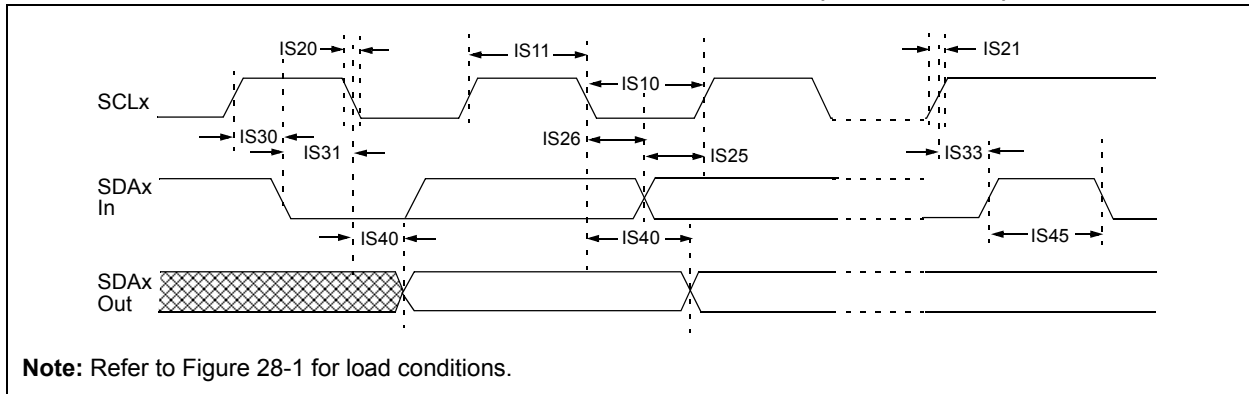


TABLE 28-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions	
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 KHz.	
			400 kHz mode	1.3	—	μs		PBCLK must operate at a minimum of 3.2 MHz.
			1 MHz mode (Note 1)	0.5	—	μs		
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 KHz.	
			400 kHz mode	0.6	—	μs		PBCLK must operate at a minimum of 3.2 MHz.
			1 MHz mode (Note 1)	0.5	—	μs		
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	nsec	Cb is specified to be from 10 to 400 pF.	
			400 kHz mode	$20 + 0.1 C_B$	300	nsec		
			1 MHz mode (Note 1)	—	100	nsec		
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	nsec	Cb is specified to be from 10 to 400 pF.	
			400 kHz mode	$20 + 0.1 C_B$	300	nsec		
			1 MHz mode (Note 1)	—	300	nsec		
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	nsec		
			400 kHz mode	100	—	nsec		
			1 MHz mode (Note 1)	100	—	nsec		
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	nsec		
			400 kHz mode	0	0.9	μs		
			1 MHz mode (Note 1)	0	0.3	μs		
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	μs	Only relevant for Repeated Start condition.	
			400 kHz mode	600	—	μs		
			1 MHz mode (Note 1)	250	—	μs		
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	μs	After this period, the first clock pulse is generated.	
			400 kHz mode	600	—	μs		
			1 MHz mode (Note 1)	250	—	μs		
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	μs		
			400 kHz mode	600	—	μs		
			1 MHz mode (Note 1)	600	—	μs		

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

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TABLE 28-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Max.	Units	Conditions	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	nsec	
			400 kHz mode	600	—	nsec	
			1 MHz mode (Note 1)	250	—	nsec	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	nsec	
			400 kHz mode	0	1000	nsec	
			1 MHz mode (Note 1)	0	350	nsec	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start.
			400 kHz mode	1.3	—	μs	
			1 MHz mode (Note 1)	0.5	—	μs	
IS50	CB	Bus Capacitive Loading	—	400	pF		

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 28-34: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	
AD02	AVSS	Module Vss Supply	Vss	—	Vss + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.0	—	AVDD	V	(Note 1)
AD05a			2.5	—	3.6	V	VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08	IREF	Current Drain	—	250	400	μA	ADC operating
				—	3	μA	ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	
	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

TABLE 28-34: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
	VIN	Absolute Input Voltage	AVSS – 0.3		AVDD + 0.3	V	
		Leakage Current	—	+/- 0.001	+/-0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10KΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5K	Ω	(Note 1)
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	
AD21c	INL	Integral Nonlinearity	—	—	<+/-1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	—	<+/-1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	—	—	<+/-1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24n	E _{OFF}	Offset Error	—	—	<+/-1	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed
ADC Accuracy – Measurements with Internal VREF+/VREF-							
AD20d	Nr	Resolution	10 data bits			bits	(Note 3)
AD21d	INL	Integral Nonlinearity	—	—	<+/-1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD22d	DNL	Differential Nonlinearity	—	—	<+/-1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Notes 2, 3)
AD23d	GERR	Gain Error	—	—	<+/-4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD24d	E _{OFF}	Offset Error	—	—	<+/-2	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD25d	—	Monotonicity	—	—	—	—	Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

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TABLE 28-35: 10-BIT CONVERSION RATE PARAMETERS

PIC32MX 10-bit A/D Converter Conversion Rates (Note 2)						
ADC Speed	TAD Minimum	Sampling Time Min	Rs Max	VDD	Temperature	ADC Channels Configuration
1 MIPS to 400 ksp/s (Note 1)	65 ns	132 ns	500Ω	3.0V to 3.6V	-40°C to +85°C	
Up to 400 ksp/s	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	-40°C to +85°C	
Up to 300 ksp/s	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	-40°C to +85°C	

Note 1: External VREF- and VREF+ pins must be used for correct operation.

Note 2: These parameters are characterized, but not tested in manufacturing.

TABLE 28-36: A/D CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	A/D Clock Period (Note 2)	65	—	—	nsec	See Table 28-35.
AD51	TRC	A/D Internal RC Oscillator Period	—	250	—	nsec	(Note 3)
Conversion Rate							
AD55	TCNV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	KSPS	AVDD = 3.0V to 3.6V
			—	—	400	KSPS	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1	—	31	TAD	TSAMP must be ≥ 132 nsec.
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected.
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1) (Note 3)	—	0.5 TAD	—	—	—
AD63	TDFU	Time to Stabilize Analog Stage from A/D OFF to A/D ON (Note 3)	—	—	2	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

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FIGURE 28-18: A/D CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS
 (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000)

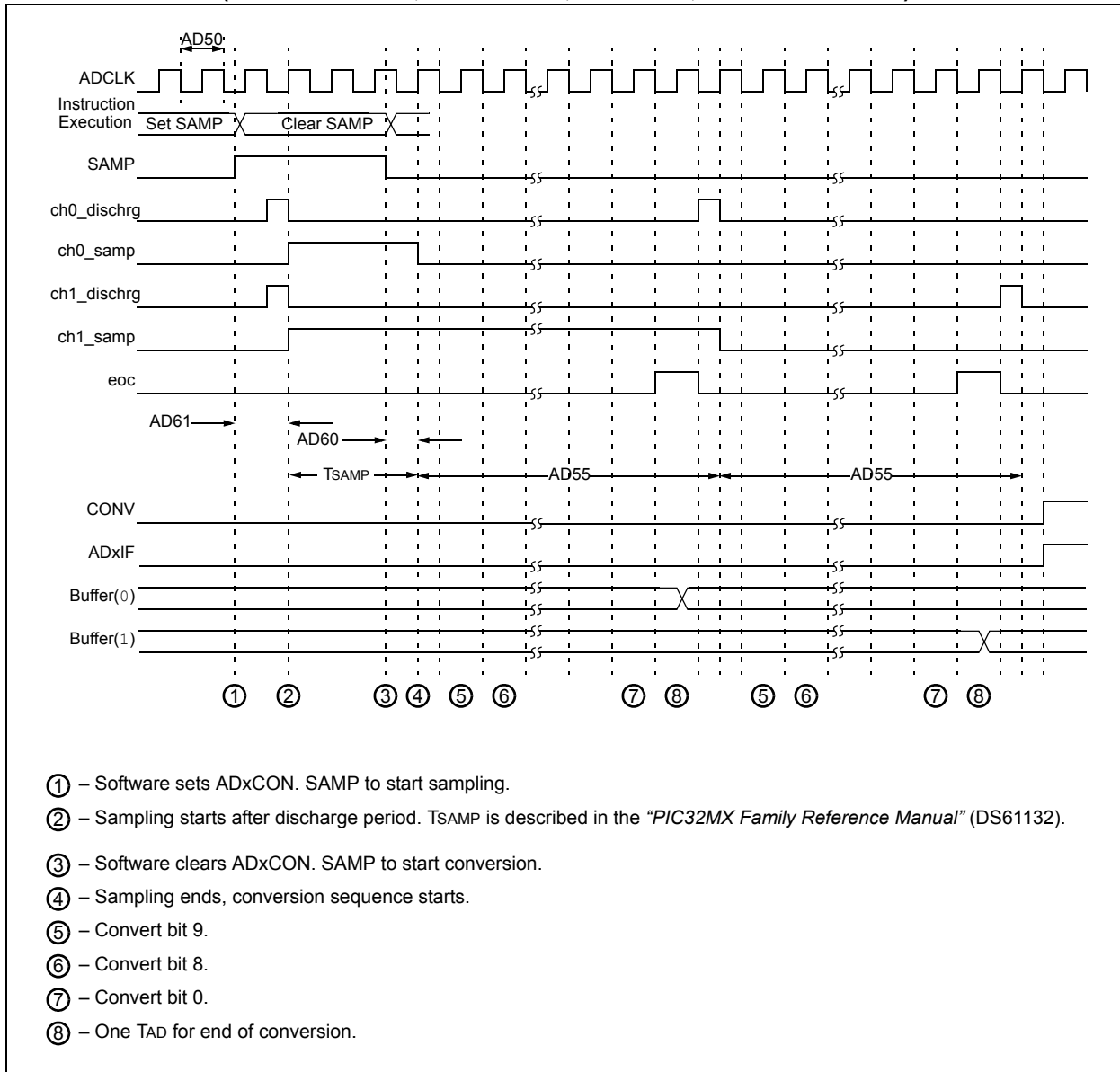
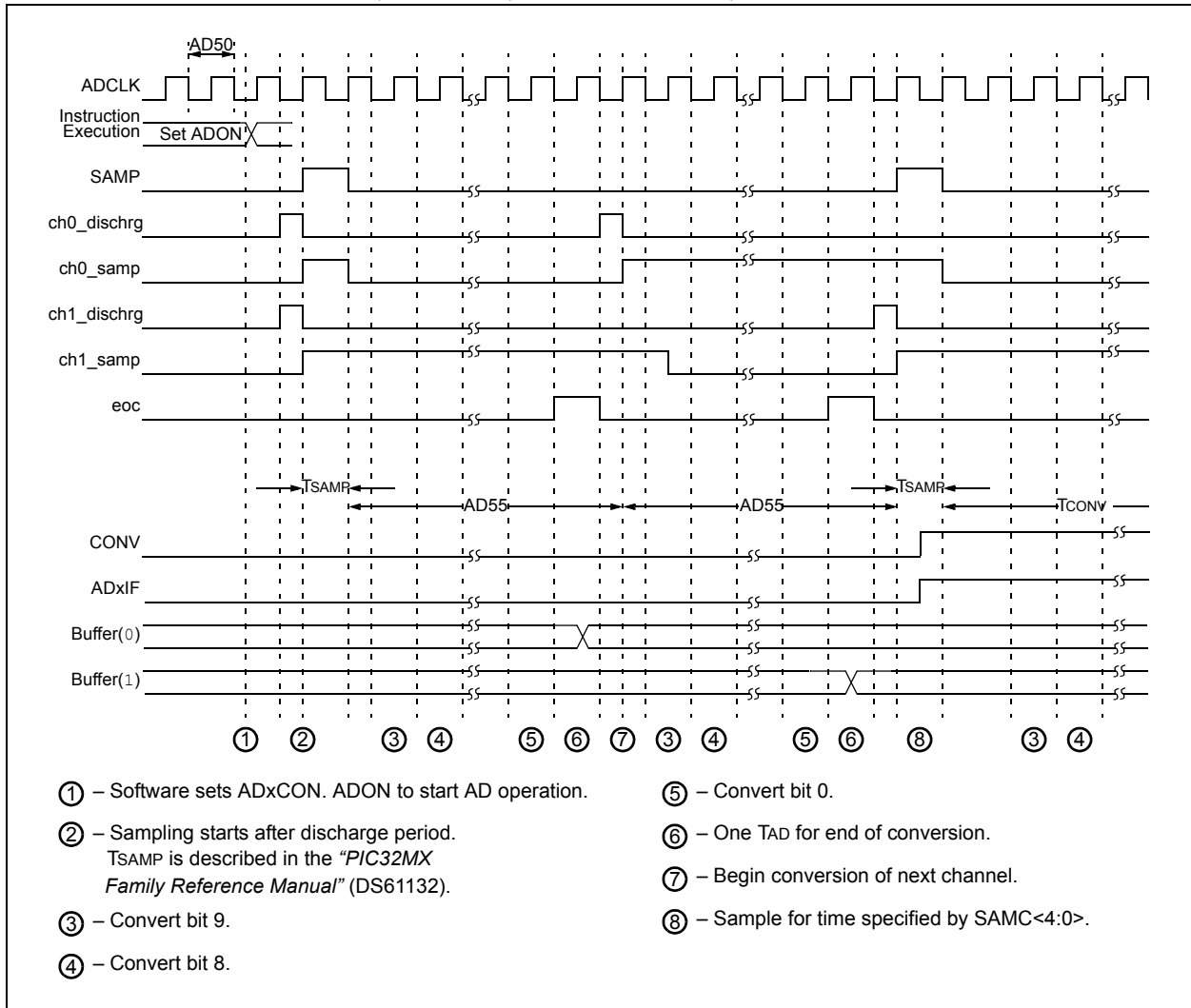


FIGURE 28-19: A/D CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001



PIC32MX3XX/4XX

FIGURE 28-20: PARALLEL SLAVE PORT TIMING

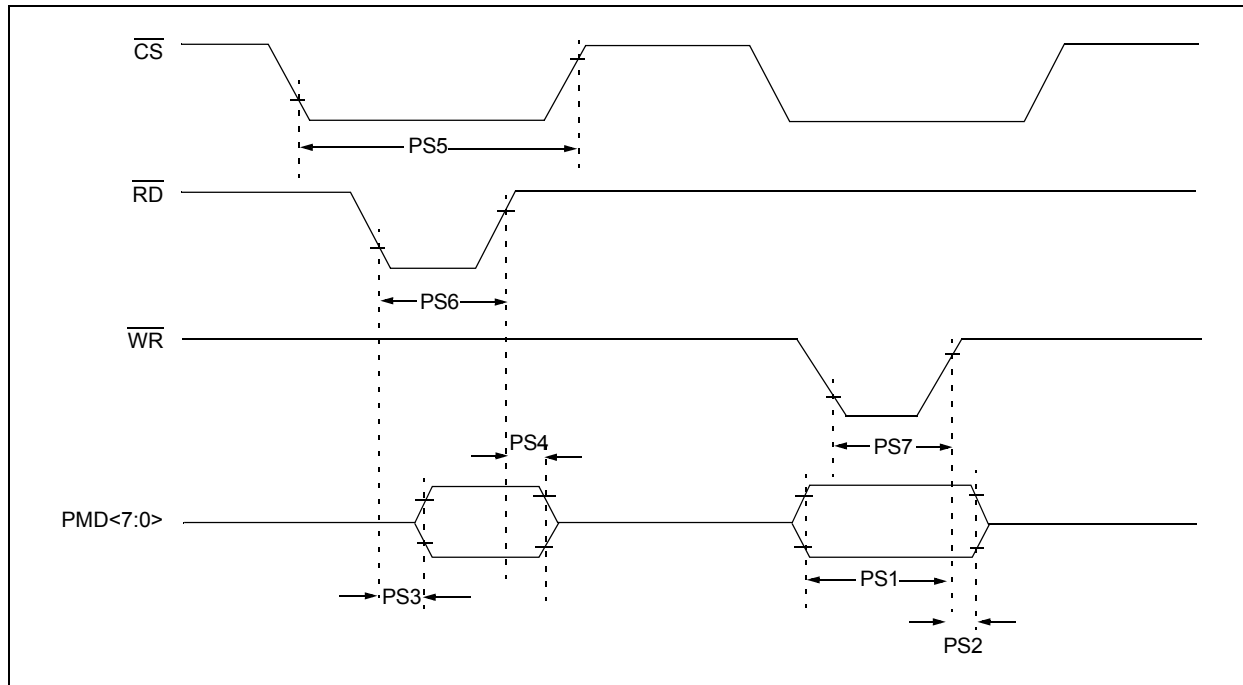


TABLE 28-37: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PS1	TdtV2wrH	Data In Valid before \overline{WR} or \overline{CS} Inactive (setup time)	20	—	—	nsec	
PS2	TwrH2dtl	\overline{WR} or \overline{CS} Inactive to Data-In Invalid (hold time)	20	—	—	nsec	
PS3	TrdL2dtV	\overline{RD} and \overline{CS} Active to Data-Out Valid	—	—	60	nsec	
PS4	TrdH2dtl	\overline{RD} Active or \overline{CS} Inactive to Data-Out Invalid	0	—	10	nsec	
PS5	Tcs	\overline{CS} Active Time	25	—	—	nsec	
PS6	TWR	\overline{WR} Active Time	25	—	—	nsec	
PS7	TRD	\overline{RD} Active Time	25	—	—	nsec	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 28-21: PARALLEL MASTER PORT READ TIMING DIAGRAM

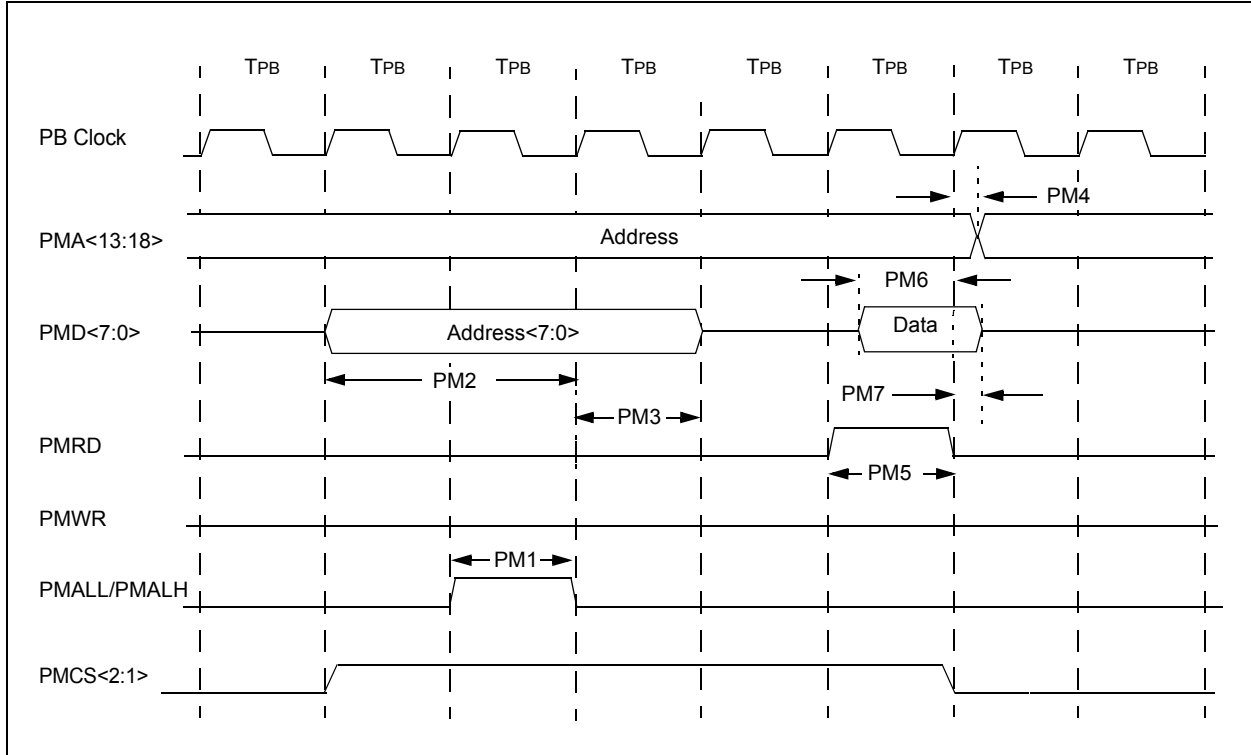


TABLE 28-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	
PM2	TADSU	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 TPB	—	—	
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	1	—	—	nsec	
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	5	—	—	nsec	
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	0	—	nsec	

Note 1: These parameters are characterized, but not tested in manufacturing.

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FIGURE 28-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

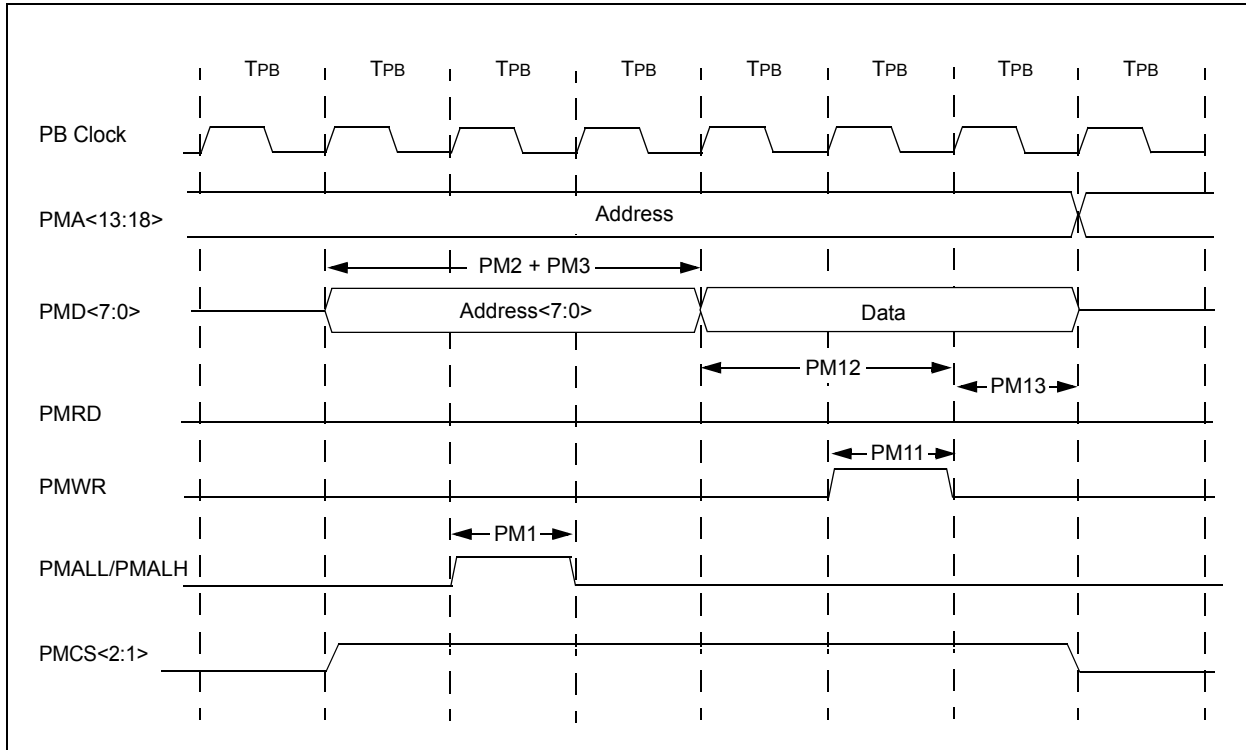


TABLE 28-39: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PM11	TWR	PMWR Pulse Width	—	1 TPB	—	—	
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPB	—	—	
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPB	—	—	

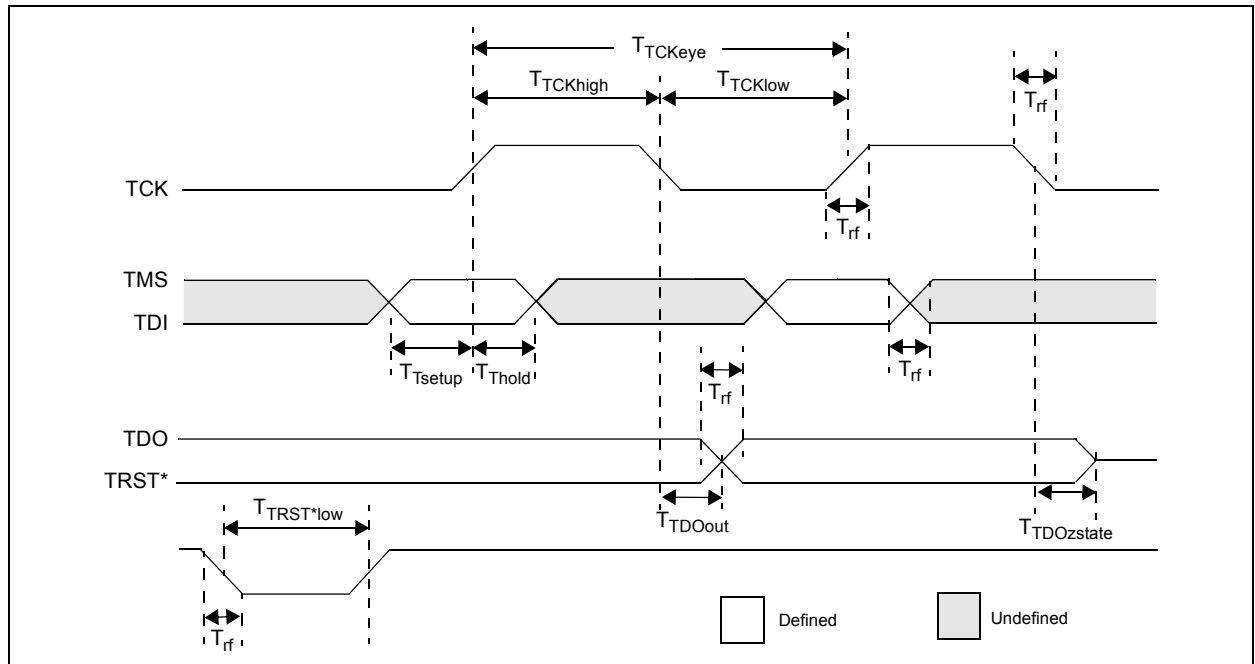
Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 28-40: OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ	Max.	Units	Conditions
USB313	VUSB	USB Voltage	3.0	—	3.6	V	Voltage on bus must be in this range for proper USB operation.
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	The difference between D+ and D- must exceed this value while VCM is met.
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	1.5 k Ω load connected to 3.6V
USB322	VOH	Voltage Output High	2.8	—	3.6	V	1.5 k Ω load connected to ground

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 28-23: EJTAG TIMING CHARACTERISTICS



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TABLE 28-41: EJTAG TIMING REQUIREMENTS

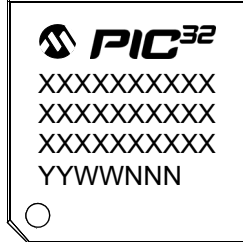
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial			
Param. No.	Symbol	Description ⁽¹⁾	Min.	Max.	Units	Conditions
EJ1	TTCKCYC	TCK Cycle Time	25	—	nsec	
EJ2	TTCKHIGH	TCK High Time	10	—	nsec	
EJ3	TTCKLOW	TCK Low Time	10	—	nsec	
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	nsec	
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	nsec	
EJ6	TTDOOUT	TDO Output Delay Time From Falling TCK	—	5	nsec	
EJ7	TTDOZSTATE	TDO 3-State Delay Time From Falling TCK	—	5	nsec	
EJ8	TTRSTLOW	TRST Low Time	25	—	nsec	
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	nsec	

Note 1: These parameters are characterized, but not tested in manufacturing.

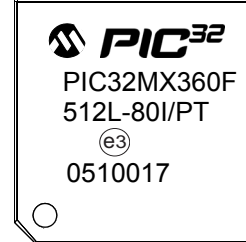
29.0 PACKAGING INFORMATION

29.1 Package Marking Information

64-Lead TQFP (10x10x1 mm)



Example



100-Lead TQFP (12x12x1 mm)



Example



64-Lead QFN (9x9x0.9 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	*	Pb-free JEDEC designator for Matte Tin (Sn)
		This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

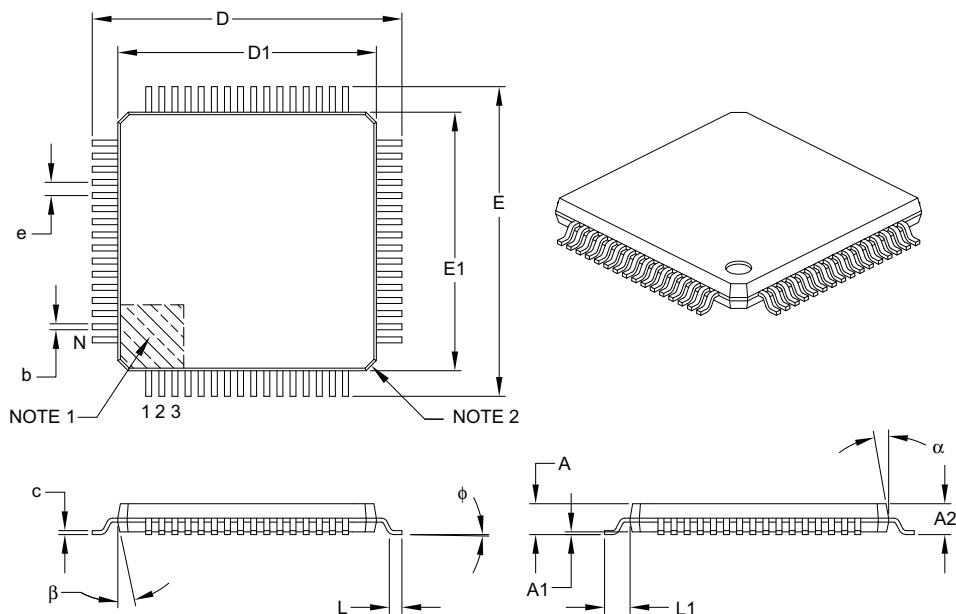
PIC32MX3XX/4XX

29.2 Package Details

The following sections give the technical details of the packages.

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	64		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

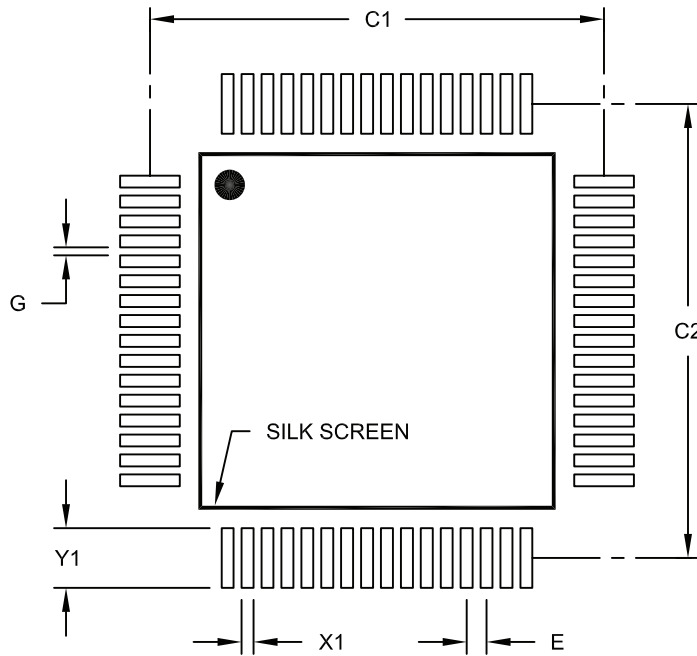
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

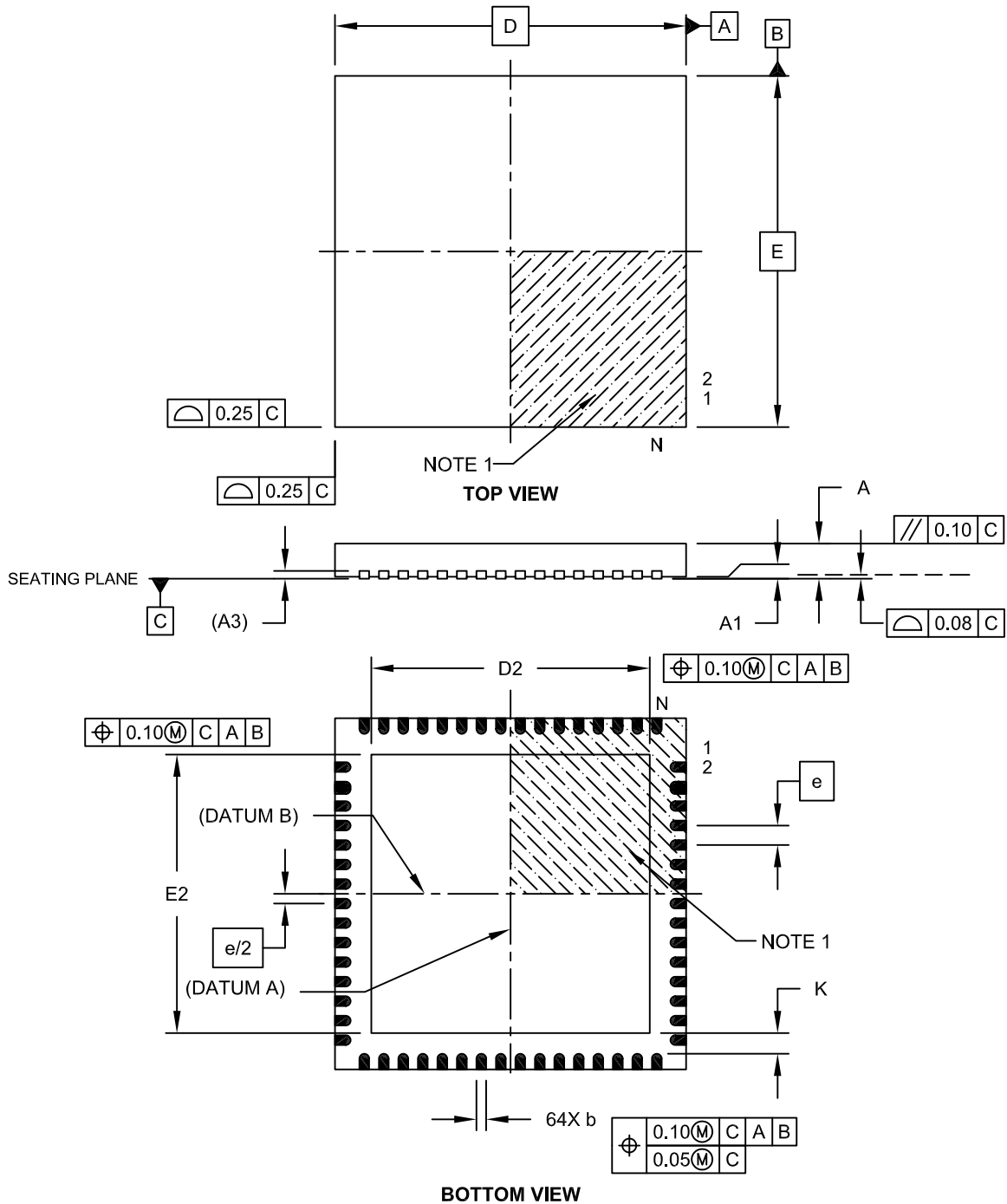
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085A

PIC32MX3XX/4XX

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

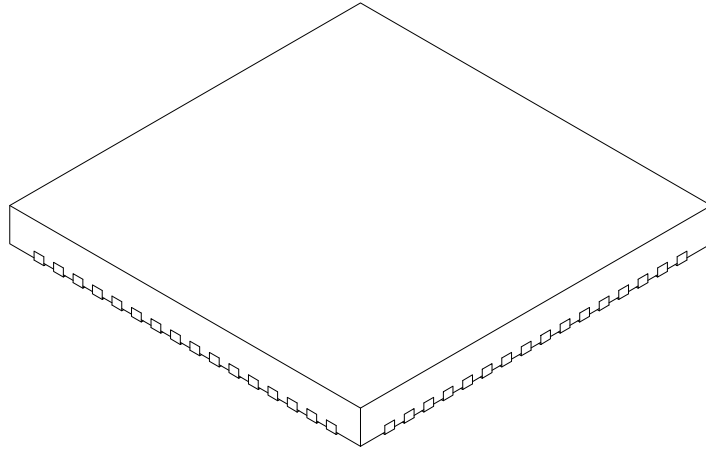


Microchip Technology Drawing C04-149B Sheet 1 of 2

PIC32MX3XX/4XX

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

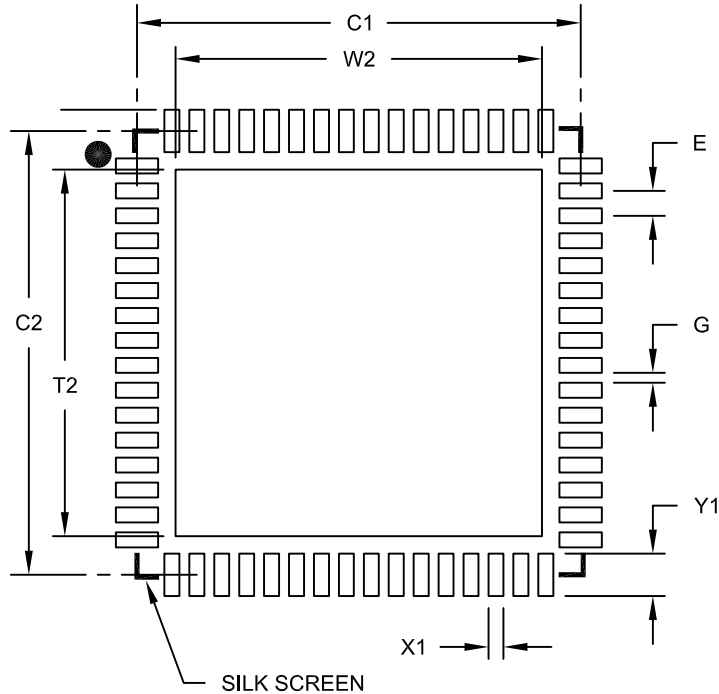
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149B Sheet 2 of 2

PIC32MX3XX/4XX

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
 With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

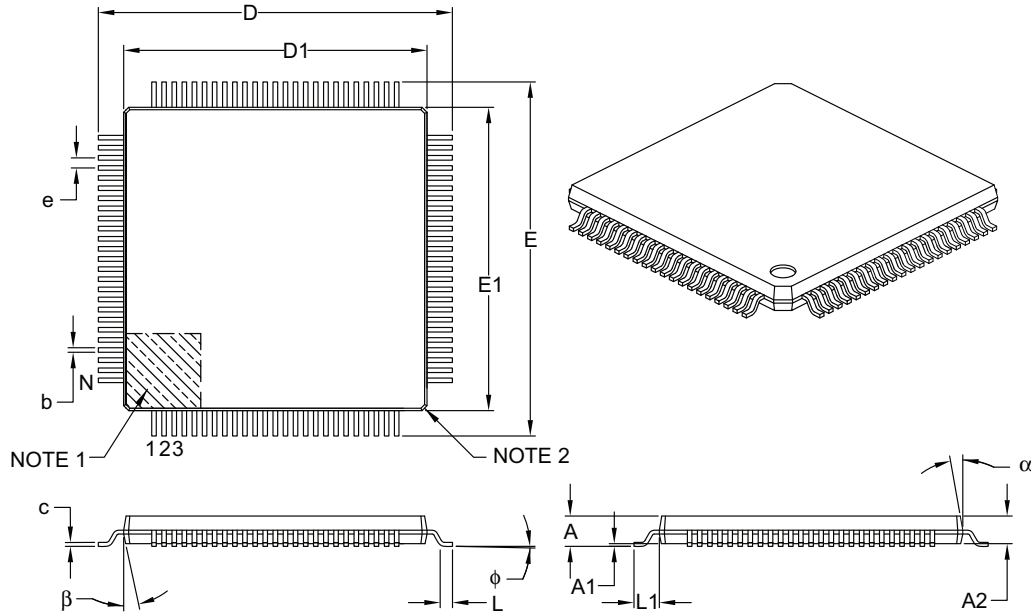
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	100		
Lead Pitch	e	0.40 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	14.00 BSC		
Overall Length	D	14.00 BSC		
Molded Package Width	E1	12.00 BSC		
Molded Package Length	D1	12.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

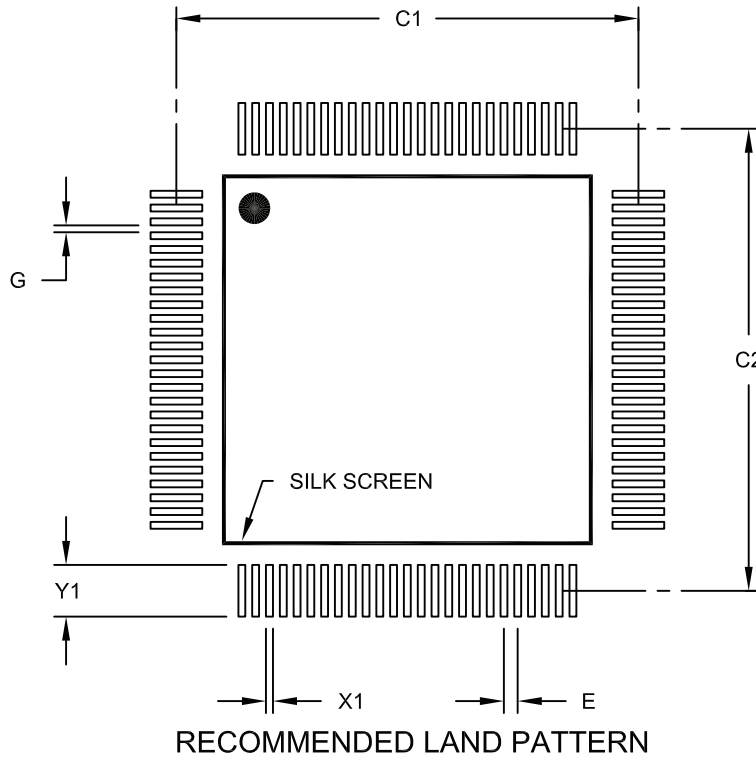
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

PIC32MX3XX/4XX

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100A

APPENDIX A: REVISION HISTORY

Revision E (July 2008)

- Updated the PIC32MX340F128H features in Table 1 to include 4 programmable DMA channels.

Revision F (June 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

- Changed all instances of OSC1 to OSC1 and OSC0 to OSC2
- Changed all instances of VDDCORE and VDDCORE/VCAP to VCAP/VDDCORE
- Deleted registers in most sections, refer to the related section of the *PIC32MX3XX/4XX Family Reference Manual* (DS61132).

The other changes are referenced by their respective section in the following table.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
“High-Performance 80 MHz MIPS-Based 32-bit Flash Microcontroller 64/100-Pin General Purpose and USB”	Added a “Packages” column to Table 1 and Table 2. Corrected all pin diagrams to update the following pin names. Previous: Current: PGC1/EMUC1 PGEC1 PGD1/EMUD1 PGED1 PGC2/EMUC2 PGEC2 PGD2/EMUD2 PGED2 Shaded appropriate pins in each diagram to indicate which pins are 5V tolerant. Added 64-Lead QFN package pin diagrams, one for General Purpose and one for USB.
Section 1.0 “Device Overview”	Reconstructed Figure 1-1 to include Timers, ADC, and RTCC in the block diagram.
Section 2.0 “Guidelines for Getting Started with 32-bit Microcontrollers”	Added a new section to the data sheet that provides the following information: <ul style="list-style-type: none"> Basic Connection Requirements Capacitors Master Clear PIN ICSP Pins External Oscillator Pins Configuration of Analog and Digital Pins Unused I/Os
Section 4.0 “Memory Organization”	Updated the memory maps, Figure 4-1 through Figure 4-6. All summary peripheral register maps were relocated to Section 4.0 “Memory Organization” .
Section 7.0 “Interrupt Controller”	Removed the “Address” column from Table 7-1.
Section 12.0 “I/O Ports”	Added a second paragraph to Section 12.1.3 “Analog Inputs” to clarify that all pins that share ANx functions are analog by default, because the AD1PCFG register has a default value of 0x0000.
Section 26.0 “Special Features”	Modified bit names and locations in Register 26-5 “DEVID: Device and Revision ID Register” . Replaced “TSTARTUP” with “TPU”, and “64-ms nominal delay” with “TPWRT”, in Section 26.3.1 “On-Chip Regulator and POR” . The information that appeared in the Watchdog Timer and the Programming and Diagnostics sections of 61143E version of this data sheet has been incorporated into the Special Features section: Section 26.2 “Watchdog Timer (WDT)” Section 26.4 “Programming and Diagnostics”

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TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 28.0 “Electrical Characteristics”	<p>In Section 28.1 “DC Characteristics”:</p> <p>Added the 64-Lead QFN package to Table 28-3.</p> <p>Updated data in Table 28-5.</p> <p>Updated data in Table 28-7.</p> <p>Updated data in Section 28.2 “AC Characteristics and Timing Parameters”, Table 28-4, Table 28-5, Table 28-7 and Table 28-8.</p> <p>Updated data in Table 28-10.</p> <p>Added OS42 parameter to Table 28-17.</p> <p>Replaced Table 28-23.</p> <p>Replaced Table 28-24.</p> <p>Replaced Table 28-25.</p> <p>Updated Table 28-36.</p>
Section 29.0 “Packaging Information”	<p>Added 64-Lead QFN package marking information to Section 29.1 “Package Marking Information”.</p> <p>Added the 64-Lead QFN (MR) package drawing and land pattern to Section 29.2 “Package Details”.</p>
“Product Identification System”	Added the MR package designator for the 64-Lead (9x9x0.9) QFN.

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NOTES:

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

	PIC32	MX	3XX	F	512	H	I	- 80	I / PT	- XXX	Examples:
Microchip Brand	_____										PIC32MX320F032H-40I/PT:
Architecture	_____										General purpose PIC32MX, 32 KB program memory, 64-pin, Industrial temp., TQFP package.
Product Groups	_____										PIC32MX360F256L-80I/PT:
Flash Memory Family	_____										General purpose PIC32MX, 256 KB program memory, 100-pin, Industrial temp., TQFP package.
Program Memory Size (KB)	_____										
Pin Count	_____										
Tape and Reel Flag (if applicable)	_____										
Speed	_____										
Temperature Range	_____										
Package	_____										
Pattern	_____										

Flash Memory Family

Architecture	MX = 32-bit RISC MCU core
Product Groups	3xx = General purpose microcontroller family 4xx = USB
Flash Memory Family	F = Flash program memory
Program Memory Size	32 = 32K 64 = 64K 128 = 128K 256 = 256K 512 = 512K
Pin Count	H = 64-pin L = 100-pin
Temperature Range	I = -40°C to +85°C (Industrial)
Package	PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample



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