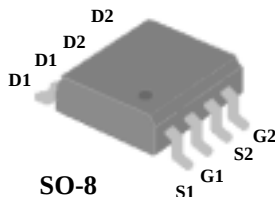


N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

PRODUCT SUMMARY

Simple Drive Requirement
Low On-resistance
Fast Switching



N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	28m Ω
	I_D	7A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	50m Ω
	I_D	-5.3A

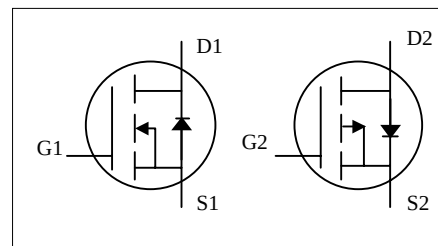
DESCRIPTION

The advanced power MOSFETs from Silicon Standard Corp. provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Pb-free; RoHS-compliant



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current ³	7	-5.3	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current ³	5.8	-4.7	A
I_{DM}	Pulsed Drain Current ¹	20	-20	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	2		W
	Linear Derating Factor	0.016		W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient ³ Max.	62.5	$^\circ\text{C}/\text{W}$

N-CH ELECTRICAL CHARACTERISTICS

@T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.02	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =7A	-	-	28	mΩ
		V _{GS} =4.5V, I _D =5A	-	-	42	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =7A	-	13	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C)	V _{DS} =30V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =24V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =7A	-	8.4	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =24V	-	2.1	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	4.7	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =15V	-	6	-	ns
t _r	Rise Time	I _D =1A	-	5.2	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	18.8	-	ns
t _f	Fall Time	R _D =15Ω	-	4.4	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	645	-	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	150	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	95	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V, V _S =1.2V	-	-	1.7	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =7A, V _{GS} =0V	-	-	1.2	V

P-CH ELECTRICAL CHARACTERISTICS

@T_J=25°C (unless otherwise specified)

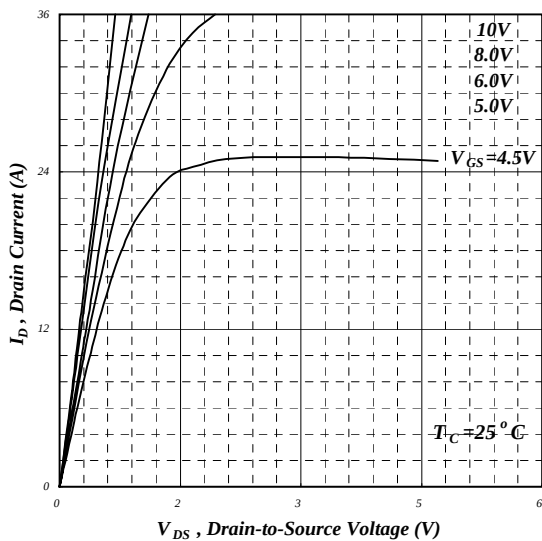
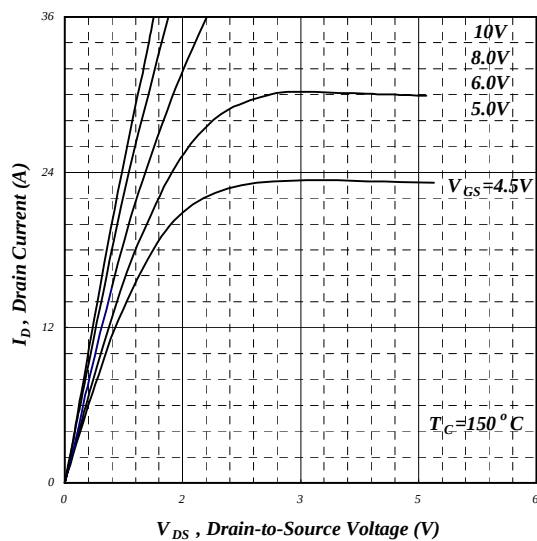
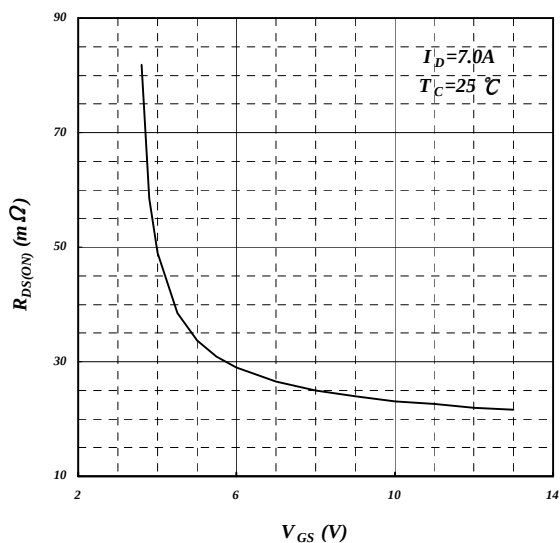
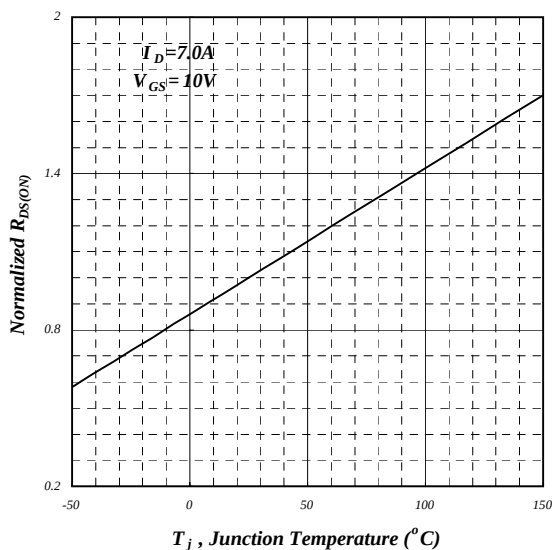
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.03	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-5.3A	-	-	50	mΩ
		V _{GS} =-4.5V, I _D =-4.2A	-	-	90	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-5.3A	-	8.5	-	S
I _{DSS}	Drain-Source Leakage Current (T=25°C)	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T=70°C)	V _{DS} =-24V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ± 20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-5.3A	-	20	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-15V	-	3.5	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-10V	-	2	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-15V	-	12	-	ns
t _r	Rise Time	I _D =-1A	-	20	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =-10V	-	45	-	ns
t _f	Fall Time	R _D =15Ω	-	27	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	790	-	pF
C _{oss}	Output Capacitance	V _{DS} =-15V	-	440	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	120	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V, V _S =-1.2V	-	-	-1.7	A
V _{SD}	Forward On Voltage ²	T _J =25°C, I _S =-2.6A, V _{GS} =0V	-	-	-1.2	V

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse width ≤300us, duty cycle ≤2%.
- 3.Surface mounted on 1 in² copper pad of FR4 board; 135°C/W when mounted on Min. copper pad.

N-Channel

Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. On-Resistance v.s. Gate Voltage

**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**

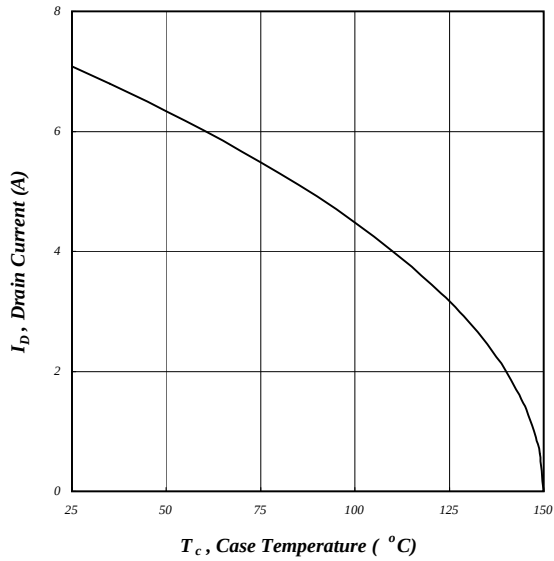
N-Channel


Fig 5. Maximum Drain Current v.s. Case Temperature

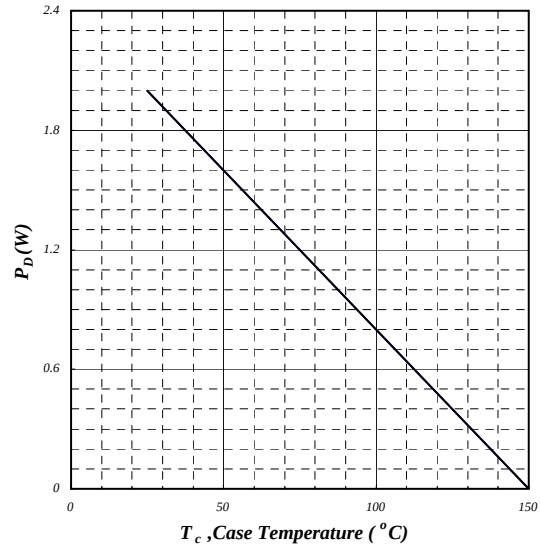


Fig 6. Typical Power Dissipation

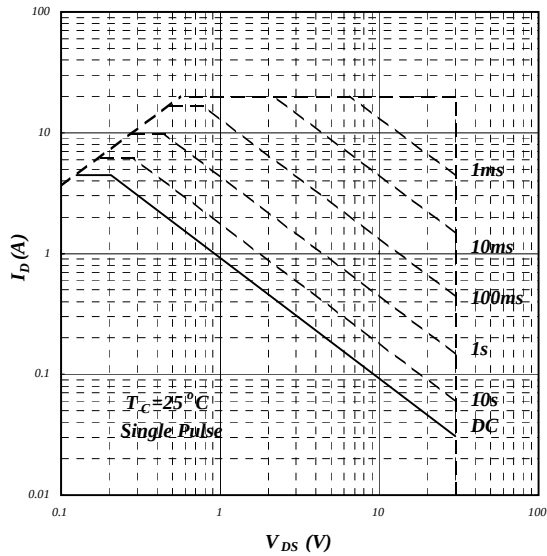


Fig 7. Maximum Safe Operating Area

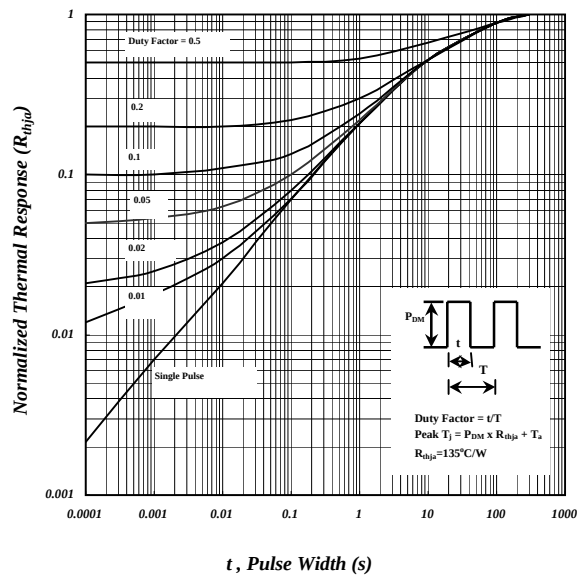
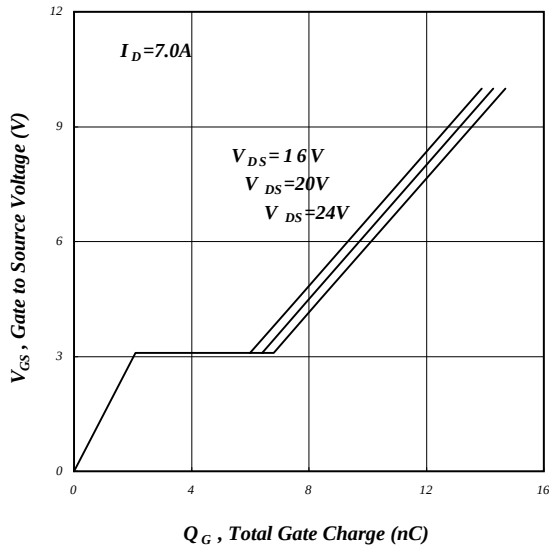
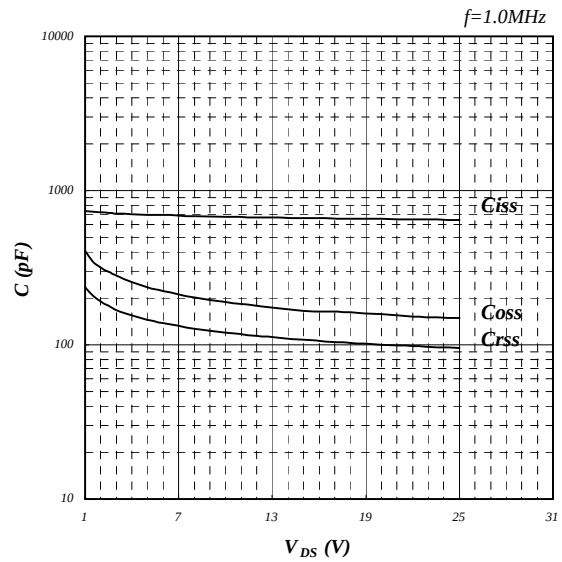
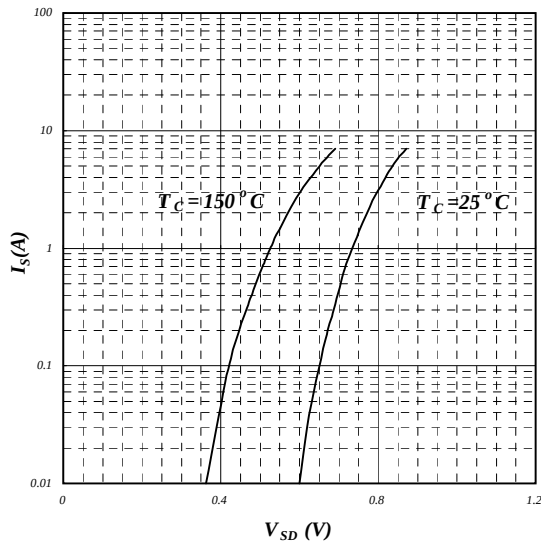
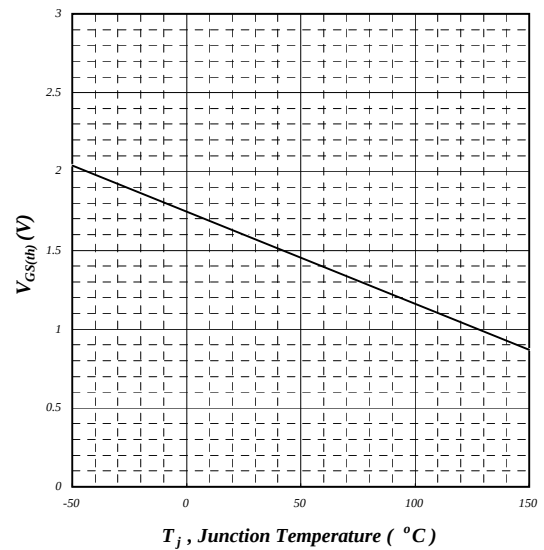


Fig 8. Effective Transient Thermal Impedance

N-Channel

Fig 9. Gate Charge Characteristics

Fig 10. Typical Capacitance Characteristics

Fig 11. Forward Characteristic of Reverse Diode

Fig 12. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

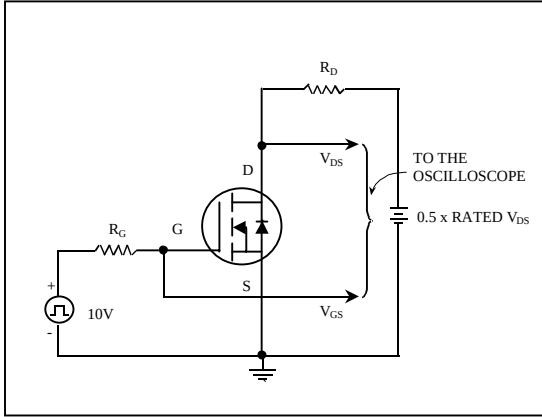


Fig 13. Switching Time Circuit

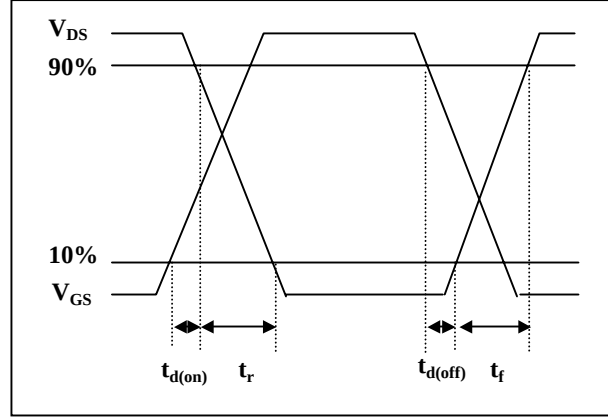


Fig 14. Switching Time Waveform

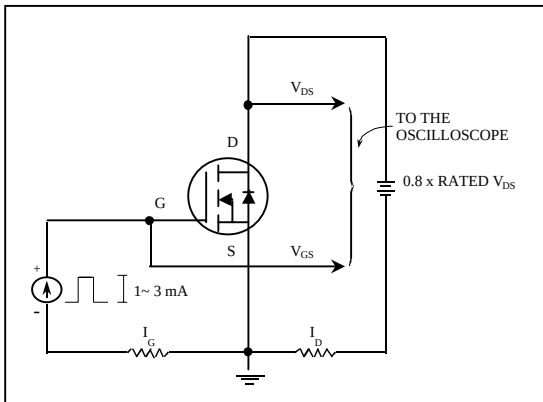


Fig 15. Gate Charge Circuit

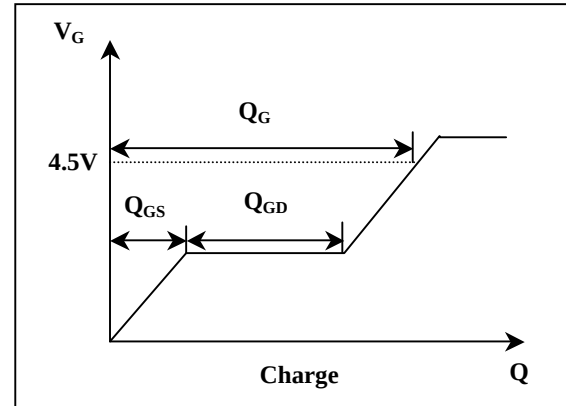
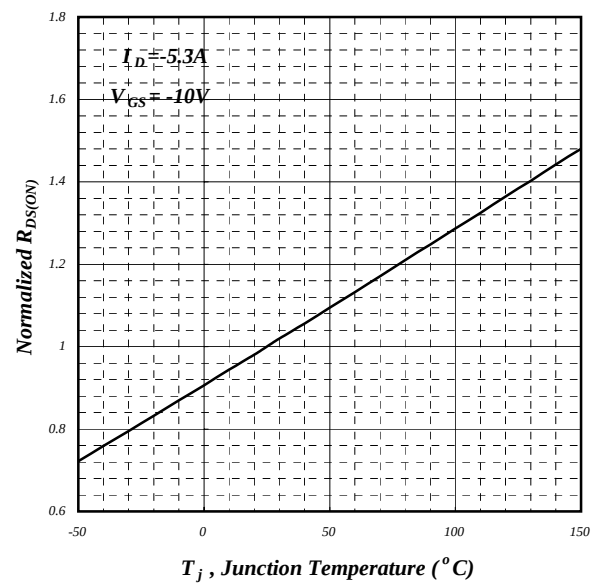
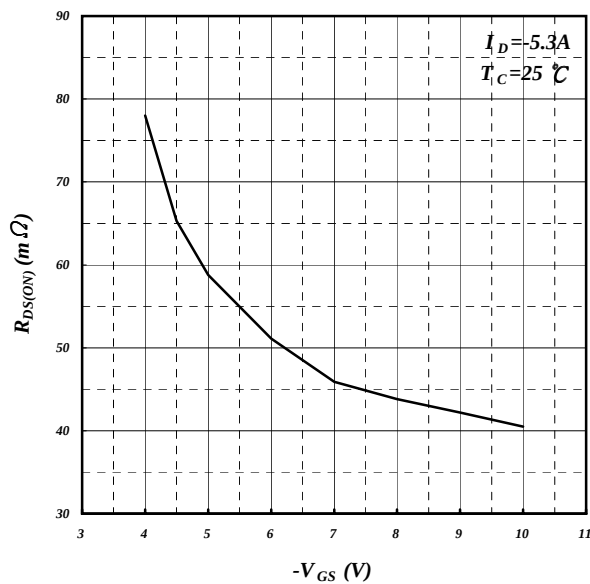
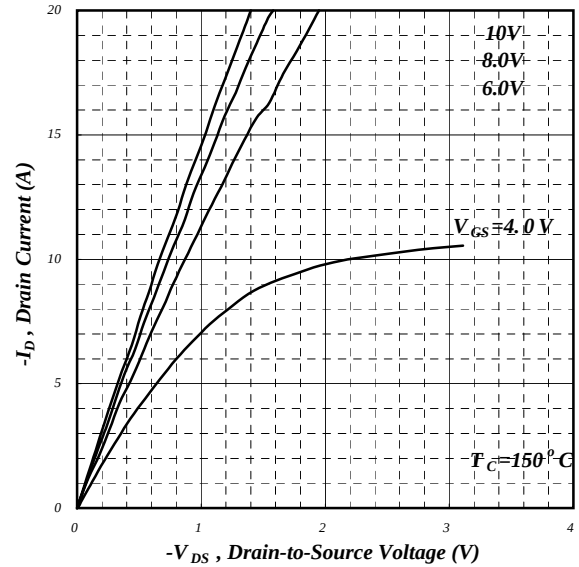
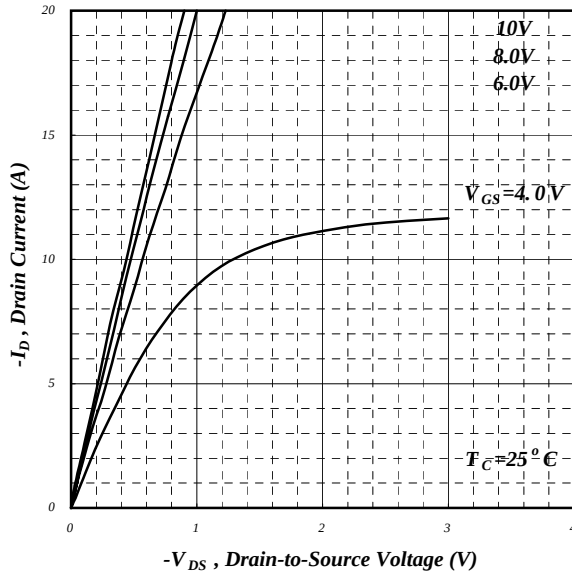


Fig 16. Gate Charge Waveform

P-Channel


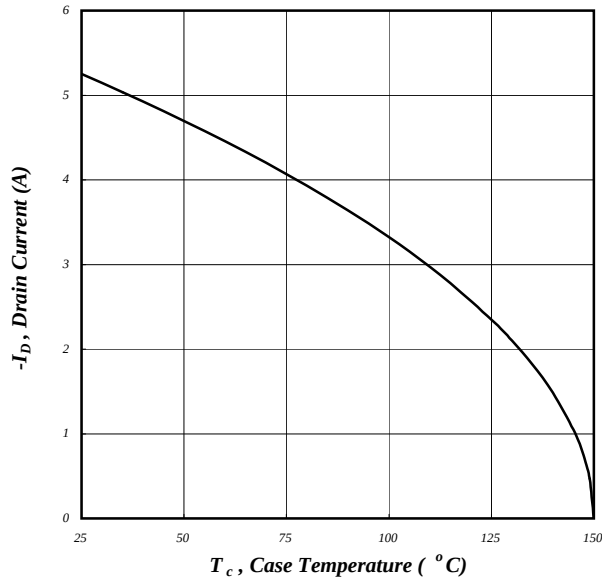
P-Channel


Fig 5. Maximum Drain Current v.s. Case Temperature

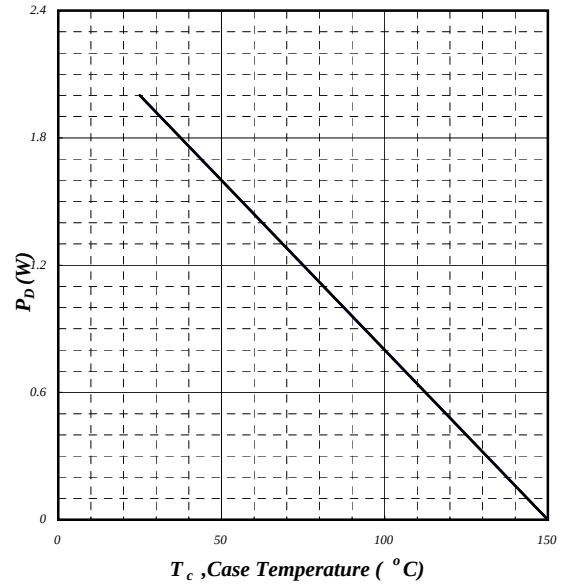


Fig 6. Typical Power Dissipation

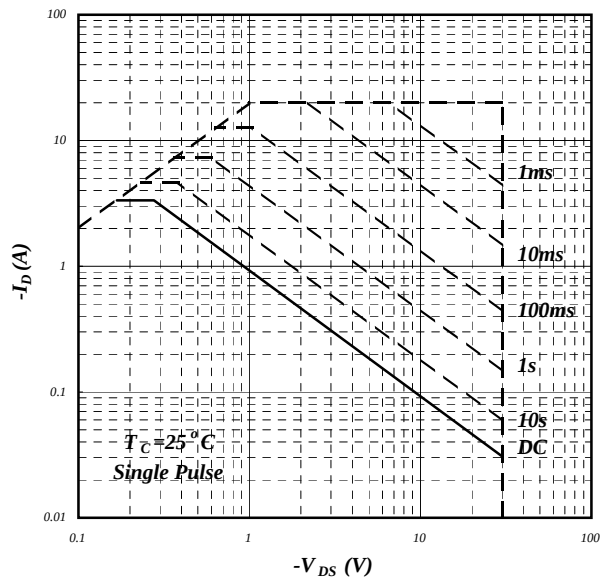


Fig 7. Maximum Safe Operating Area

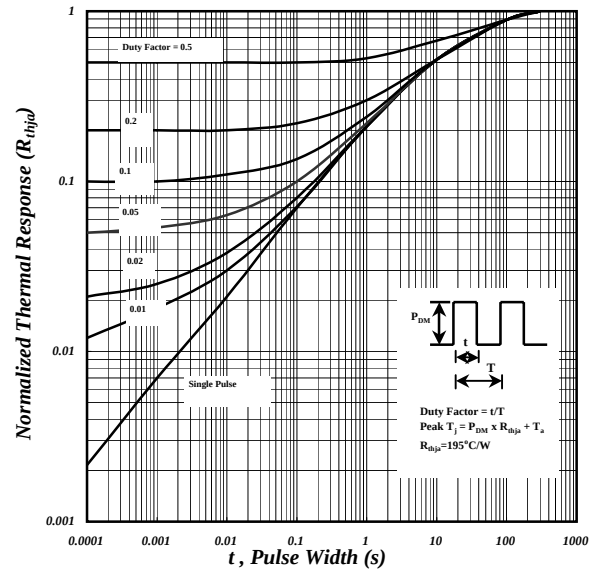
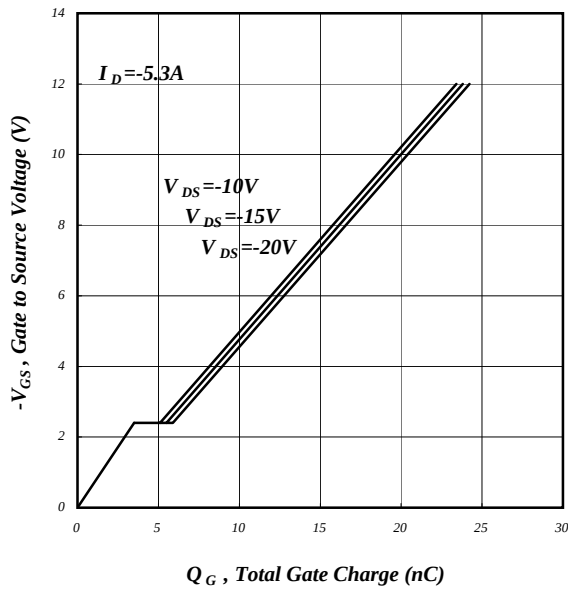
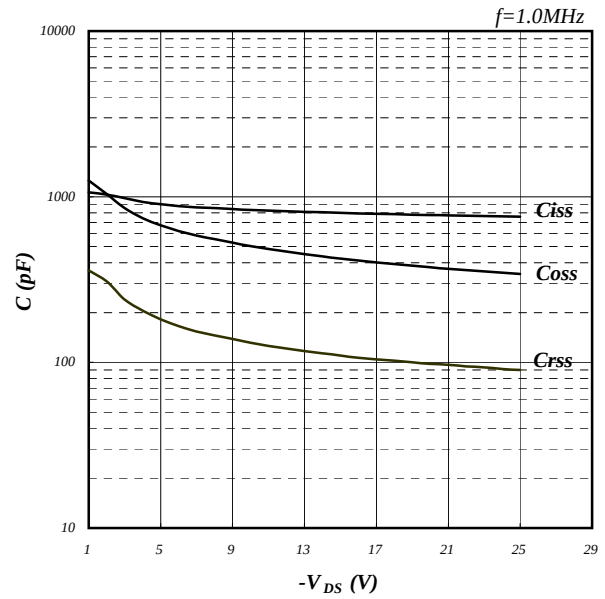
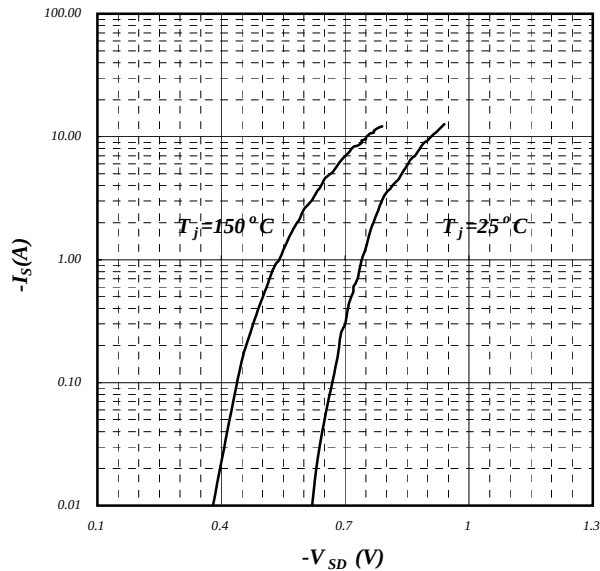
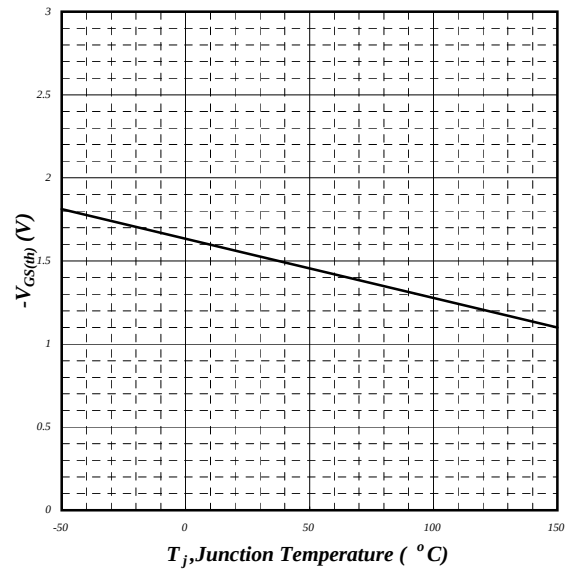


Fig 8. Effective Transient Thermal Impedance

P-Channel

Fig 9. Gate Charge Characteristics

Fig 10. Typical Capacitance Characteristics

Fig 11. Forward Characteristic of Reverse Diode

Fig 12. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

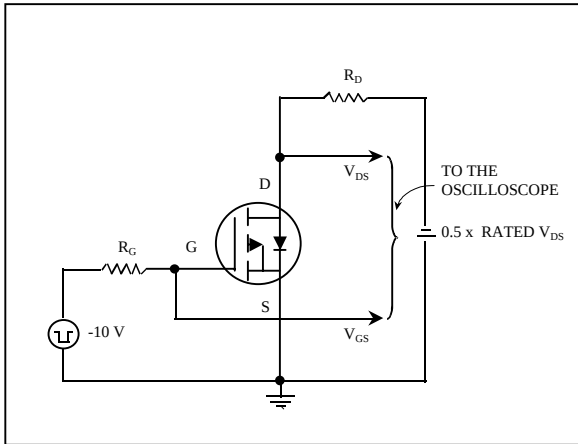


Fig 13. Switching Time Circuit

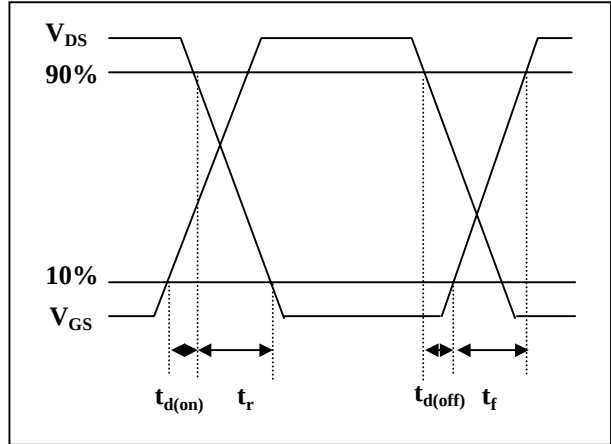


Fig 14. Switching Time Waveform

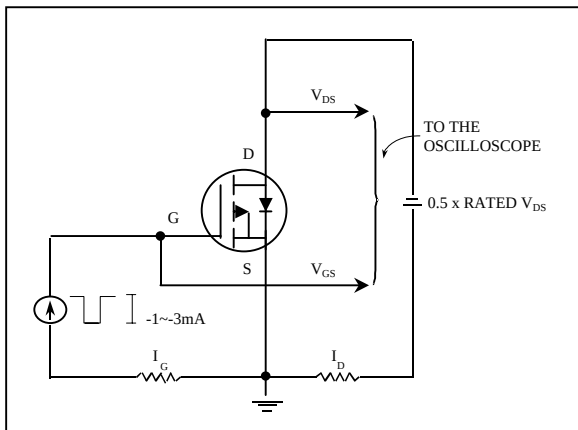


Fig 15. Gate Charge Circuit

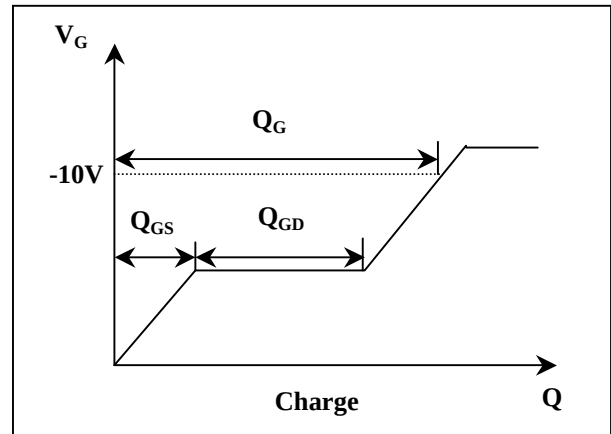


Fig 16. Gate Charge Waveform

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, expressed or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.