

### XPM-4100WG / XPM-4100BWG / XPM-4100AWG

(RoHS Compliant)

### 8.5Gb/s 850 nm XFP Multi-Mode Optical Transceiver for 8G FC Applications

#### FEATURES

- | Up to 8.5 Gb/s Bi-directional Data Link
- | Complaint to XFP MSA
- | Compliant with 8G FC 800-M5/M6/M5E-LC-I
- | Multirate for 8G / 4G / 2G FC
- | Link Distance at 8.5 Gbd
  - 150 m links with OM3 MMF Cables
  - 50 m links with OM2 MMF Cables
  - 21 m links with OM1 MMF Cables
- | 850 nm VCSEL Transmitter
- | 2-Wire Interface for Integrated Digital Diagnostic Monitoring
- | XFI Loopback Mode
- | No reference clock required
- | Low Power Dissipation < 1.2W
- | Only Required +3.3 V Power Supply
- | RoHS Compliant
- | 0 to 70°C Operating: XPM-4100WG
- | -10 to 85°C Operating: XPM-4100BWG
- | -40 to 85°C Operating: XPM-4100AWG
- | Duplex LC Connector

#### DESCRIPTION

XPM-4100WG series multi-rate 8G XFP transceiver is designed for serial optical data communications such as 8G Fiber Channel. It supports the 8.5Gbps transmission on both 50/125 μm and 62.5/125 μm MMF.

The transceiver consists of two sections: The transmitter section consists of a directly modulated 850 nm VCSEL, driver and signal conditioner. The receiver section incorporates a PIN photodiode integrated with a trans-impedance preamplifier (TIA) and signal conditioner.

The module is with the XFP 30-pin connector to allow hot plug capability. Integrated Tx and Rx signal conditioners provide high jitter-tolerance for full XFI compliance and no external reference clock required. The internally ac coupled high speed serial I/O simplifies interfacing to external circuitry. Only single 3.3V power supply is needed. The optical output can be disabled by LVTTTL logic high-level input of TX\_DIS. Loss of signal (RX\_LOS) output is provided to indicate the loss of an input optical signal of receiver.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specific data is held in a series of tables in the high memory area.

#### APPLICATIONS

- | Multi-rate 8x/4x/2x Fiber Channel

#### STANDARD

- | Compliant with XFP MSA
- | Compliant with 8G FC

#### LASER SAFETY

This transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

#### ORDER INFORMATION

P/No.	Bit Rate (Gb/s)	Distance (m)	Wavelength (nm)	Package	Connector	Temp (°C)	RoHS Compliant
XPM-4100WG	8 / 4 / 2	150/50/21*	850	XFP with DMI	LC	0 to 70	Yes
XPM-4100BWG	8 / 4 / 2	150/50/21*	850	XFP with DMI	LC	-10 to 85	Yes
XPM-4100AWG	8 / 4 / 2	150/50/21*	850	XFP with DMI	LC	-40 to 85	Yes

#### \*LINK LENGTH

Data Rate / Standard	Fiber Type	Model Bandwidth @ 850nm (MHz-km)	Distance Range (m)
8.5 Gbd	62.5/125 μm MMF (OM1)	200	0.5 to 21
	50 / 125 μm MMF (OM2)	500	0.5 to 50
	50 / 125 μm MMF	900	0.5 to 90
	50 / 125 μm MMF	1500	0.5 to 120
	50 / 125 μm MMF (OM3)	2000	0.5 to 150

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Absolute Maximum Ratings					
Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Tstg	-40	85	°C	
Operating Case Temperature	Topr	0	70	°C	XPM-4100WG
		-10	85	°C	XPM-4100BWG
		-40	85	°C	XPM-4100AWG
Relative Humidity	RH	0	85	%	Non condensing
Power Supply Voltage	V <sub>CC3</sub>	0	3.6	V	
Input Voltage	---	GND	V <sub>cc3</sub>	V	

Recommended Operating Conditions					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Power Supply Voltage	V <sub>CC3</sub>	3.13	3.3	3.47	V
Power Supply Current (@3.3V)	I <sub>CC3</sub>		240	400	mA
Power Dissipation	P <sub>D</sub>			1.2	W
Operating Case Temperature	Topr	0		70	°C / XPM-4100WG
		-10		85	°C / XPM-4100BWG
		-40		85	°C / XPM-4100AWG
Data Rate			8.5		Gb/s

Transmitter Optical Specifications (Topr= 0 to 70°C, Vcc3 = 3.3V ±5%)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Average Launch Power	P <sub>O, AVE</sub>	-8.2	-3.3	-1	dBm	1
Launch Power in OMA	P <sub>O, OMA</sub>	302			μW	1
Output Center Wavelength	λ <sub>c</sub>	840	850	860	nm	
Output Spectrum Width	σ <sub>λ</sub>			0.60	nm	RMS (σ)
Relative Intensity Noise	RIN			-128	dB/Hz	
Average Launch Power of OFF Transmitter				-30	dBm	

1. Output power is power coupled into a 50/125 μm MMF.

Receiver Optical Specifications (Topr= 0 to 70°C, Vcc3 = 3.3V ±5%)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Unstressed Sensitivity at 8.5 Gb/s	Sen			0.076	mWp-p	2, OMA
				-12.5	dBm	3, Average Power
Stress Sensitivity at 8.5 Gb/s	Sens		---	0.155	mWp-p	2, OMA
Receiver Overload	P <sub>MAX</sub>	0.5	---		dBm	
LOS -- Deasserted	LOS <sub>D</sub>	---	---	-15	dBm	Transition: low to high
LOS -- Asserted	LOS <sub>A</sub>	-25	---	---	dBm	Transition: high to low
LOS -- Hysteresis		1	---		dB	
Wavelength of Operation	λ <sub>c</sub>	840		860	nm	
Optical Return Loss	ORL			-12	dB	

1. Measured with worst ER; BER=1E-12 and PRBS 2<sup>7</sup>-1s.

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Electrical Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
<b>High-Speed Signal (CML) Interface Specification</b>						
Input Data Rate			8.5		Gps	1
TX Clock Tolerance				±100	ppm	1
Differential Input Impedance	R <sub>in</sub>		100		Ω	
Differential Data Input Amplitude		120		820	mV <sub>pp</sub>	2, Internally AC coupled
Output Data Rate			8.5		Gps	1
RX Clock Tolerance				±100	ppm	1
Differential Output Impedance	R <sub>out</sub>		100		Ω	
Differential Data Output Amplitude		340		850	mV <sub>pp</sub>	2, Internally AC coupled
<b>Low-Speed Signal (LVTTTL) Interface Specification</b>						
Input High Voltage		2.0		V <sub>cc</sub>	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		V <sub>cc</sub>	V	
Output Low Voltage		GND		0.5	V	
<b>Reference Clock (LVPECL) Interface Specification</b>						
No reference clock						

1. Clock tolerance for 8.5Gb/s, 4.25Gb/s, 2.12Gb/s, 1.063Gb/s and 1.25 Gb/s.
2. The differential input and output amplitudes are per XFP MSA mask at points B' and C'.

Transceiver Timing Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
TX_DIS Assert Time	t <sub>off</sub>			10	μs	
TX_DIS Negate Time	t <sub>on</sub>			2	ms	
Time to Initialize	t <sub>init</sub>			300	ms	
Interrupt Assert Delay	interrupt <sub>on</sub>			200	ms	
Interrupt Negate Delay	interrupt <sub>off</sub>			500	μs	
P_Down/PST Assert Delay	P_Down/RST <sub>on</sub>			100	μs	
P_Down Negate Delay	P_Down/RST <sub>off</sub>			300	ms	
Mod_NR Assert Delay	Mod_nr <sub>on</sub>			1	ms	
Mod_NR Negate Delay	Mod_nr <sub>off</sub>			1	ms	
Mod_Desel Assert Time	T_Mod_Desel			2	ms	
Mod_Desel De-Assert Time	T_Mod_Sel			2	ms	
P_Down Reset Time	T <sub>reset</sub>	10			μs	
RX_LOS Assert Delay	T_Los <sub>on</sub>			100	μs	
RX_LOS Negate Delay	T_Los <sub>off</sub>			100	μs	
Serial ID Clock Rate	f <sub>SCL</sub>	0		400	kHz	

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## Management Interface

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128\*256 = 32 Kbytes in this upper memory space. The contents of Table 01h are listed in Table 1 below. Please refer SFF INF-8077i (Revision 4.5) for detailed information.

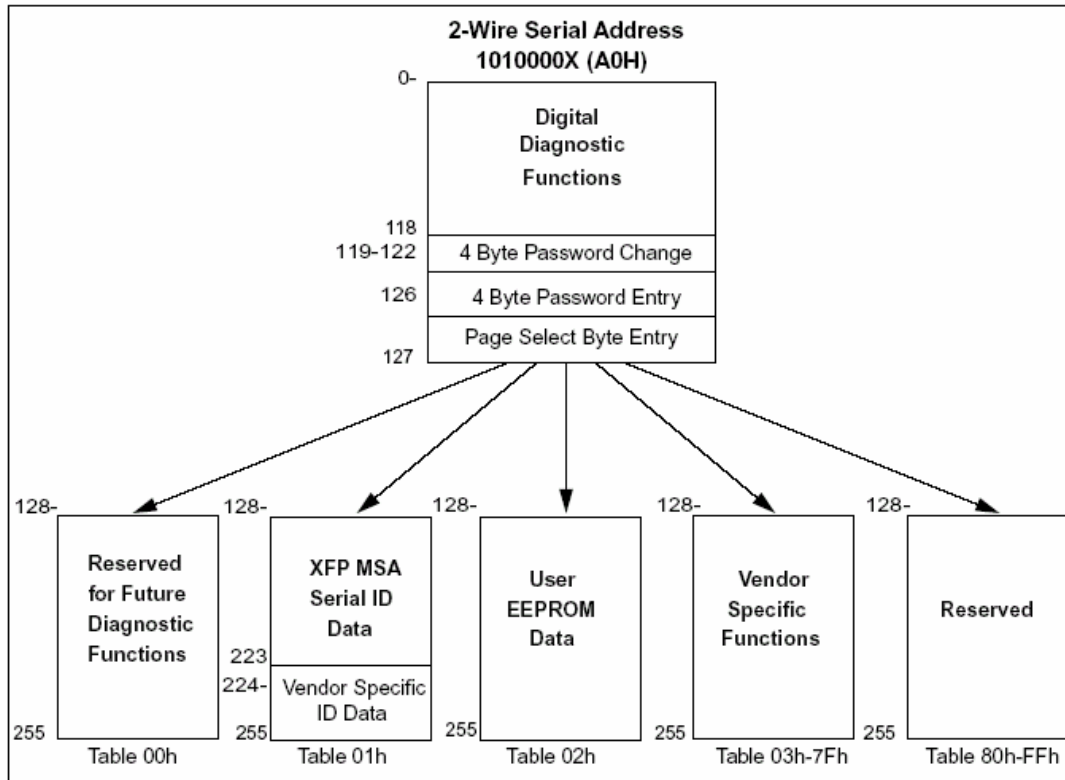
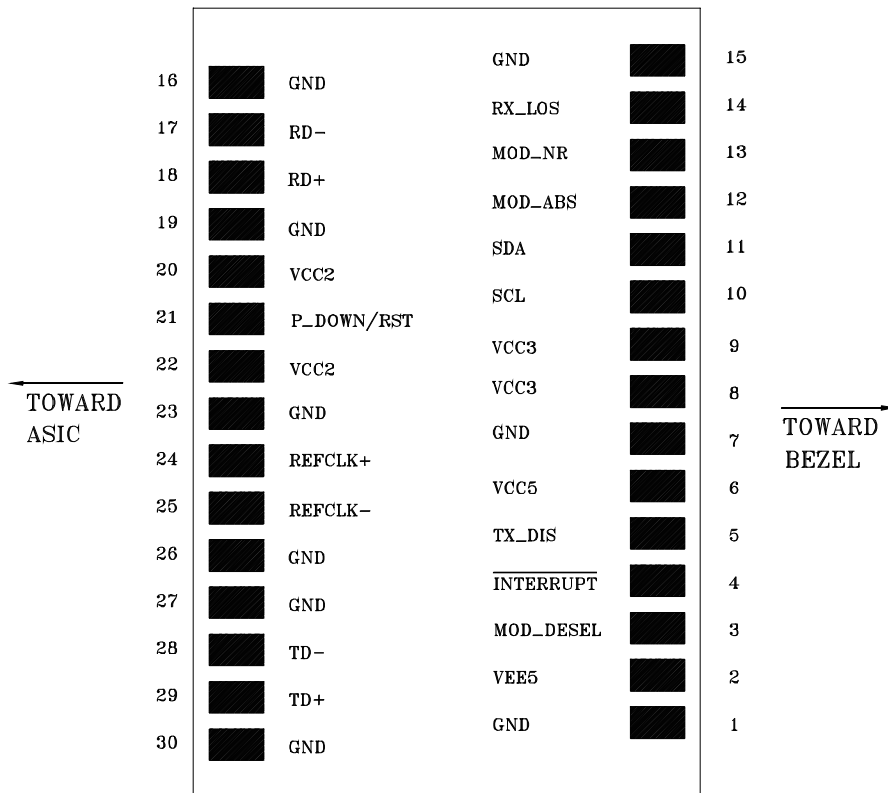


Figure 1. 2-wire Serial Digital Diagnostic Memory Map

**Table 1 Monitoring Specification**

Data Address	Parameter	Accuracy
96 ~ 97	Temperature	± 3°C
98 ~ 99	Reserved	
100 ~ 101	Tx Bias	± 10%
102 ~ 103	Tx Power	± 2dB
104 ~ 105	Rx Power	± 2dB
106 ~ 107	Vcc3	± 3%

## CONNECTION DIAGRAM



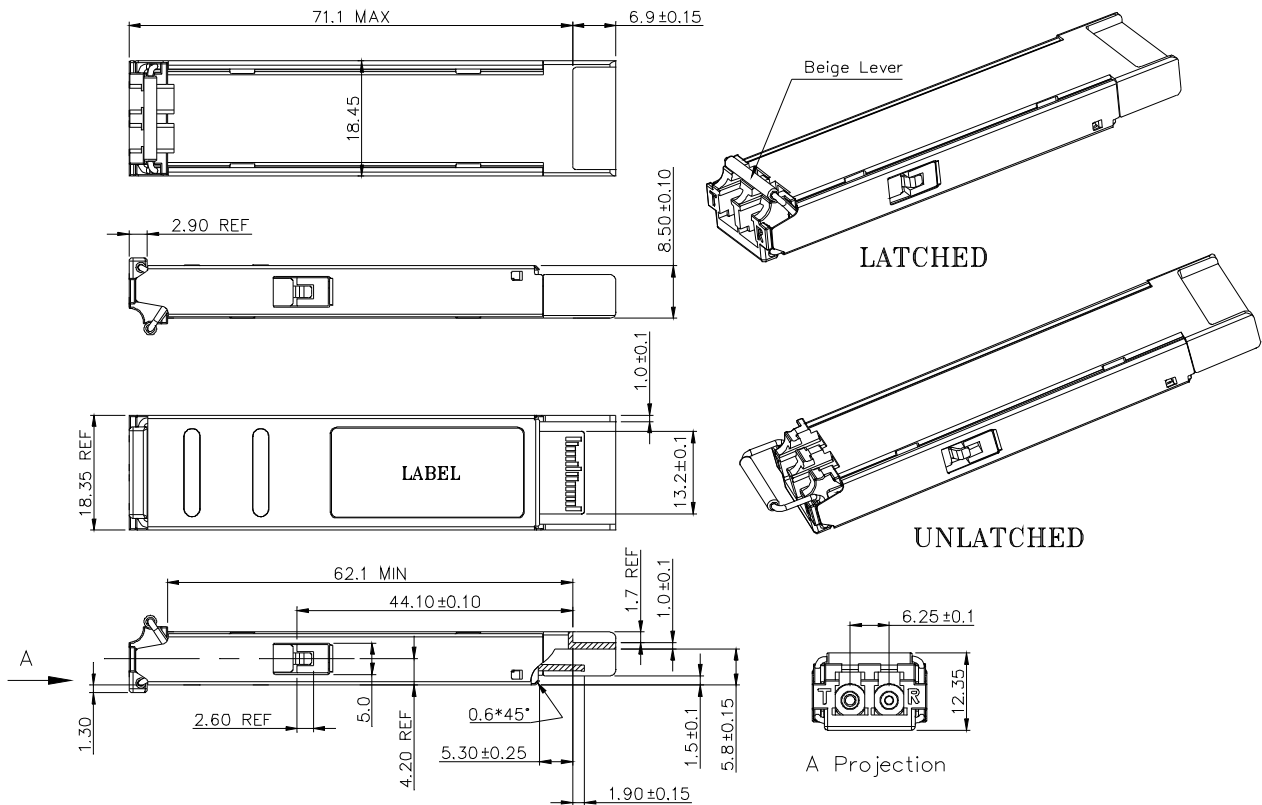
**Table 3 PIN Description**

PIN	Logic	Signal Name	Description	Note
1		GND	Module Ground	1
2		VEE5	-5.2V Power Supply <b>(Not required)</b>	3
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	Interrupt	Interrupt; Indicates presence of an important condition which can be read over the 2-wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply <b>(Not required)</b>	3
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply <b>(Not required)</b>	3

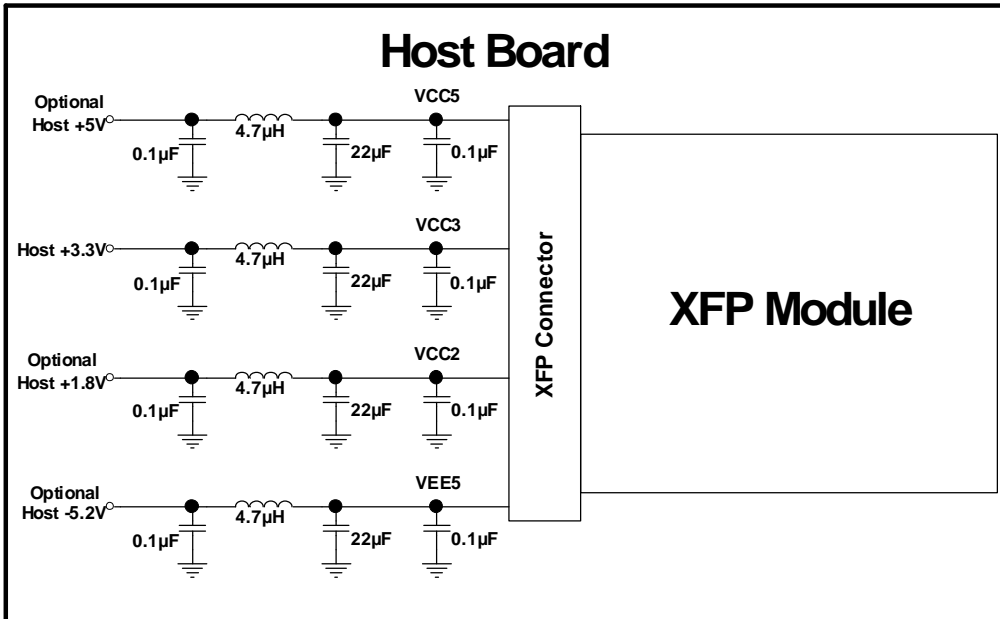
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode. Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply ( <b>Not required</b> )	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board. ( <b>Not used. Internally terminated to 50 ohm (100 ohm diff.)</b> )	4
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board. ( <b>Not used. Internally terminated to 50 ohm (100 ohm diff.)</b> )	4
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. These PINs are open within module.
4. A Reference Clock input is not required. If present, it will be ignored.

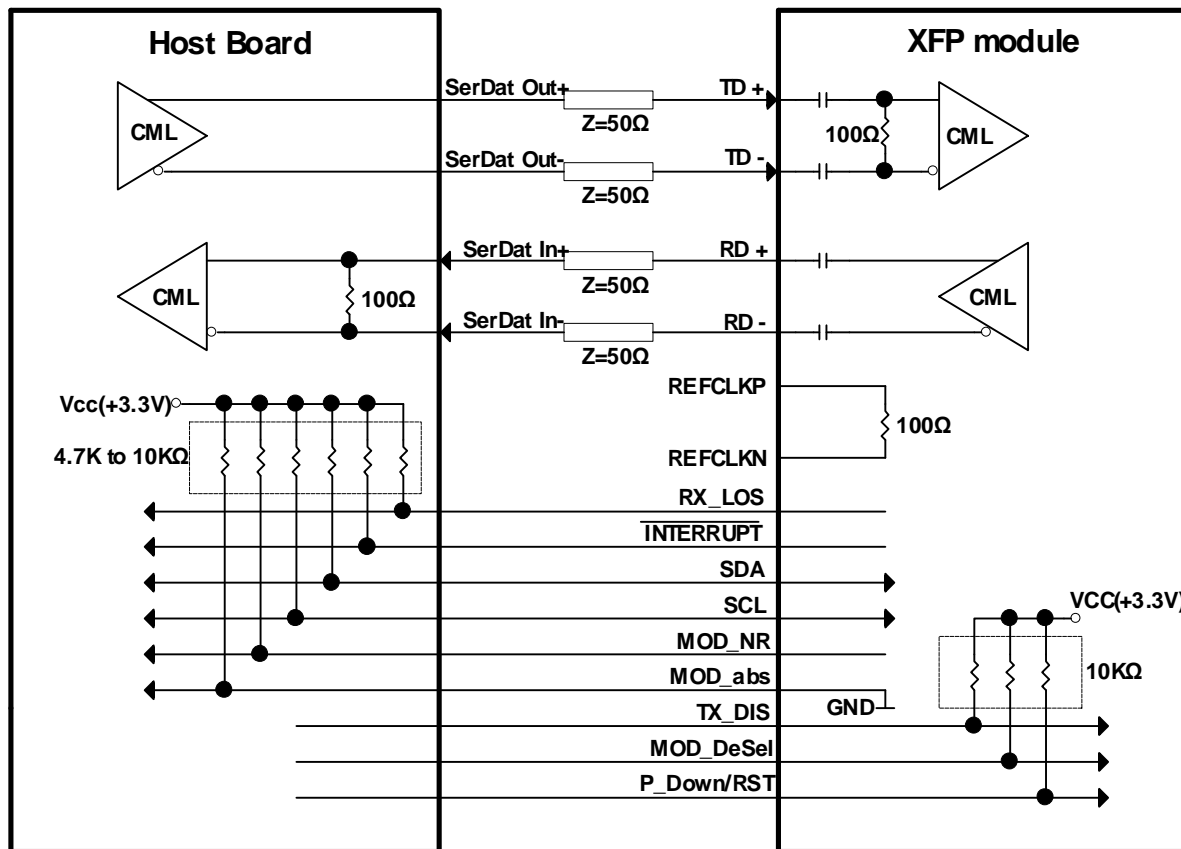
## MECHANICAL SPECIFICATION (UNITS IN MM)



RECOMMENDED POWER CIRCUIT SCHEMATIC



RECOMMENDED INTERFACE CIRCUIT



**Table 2 Serial ID Memory Contents (Table 01h)**

Address	Field Size (Byte)	Name of Filed	Description	Hex
128	1	Identifier	XFP	06
129	1	Ext. Identifier	power consumption <1.5W, no Ref Clock required	10
130	1	Connector type	LC connector	07
131~138	8	Transceiver	800-MX-SN-I	00 00 00 00 00 00 00 00
139	1	Encoding	8B/10B, NRZ	50
140	1	BR-Min	1.063Gbps	0A
141	1	BR-Max	8.5Gbps	55
142	1	length (SMF)-Km	0	00
143	1	Length (E-50μm)	150m	4B
144	1	Length (50 μm)	50m	32
145	1	Length (62.5 μm)	21m	15
146	1	Length (Copper)	0 m	00
147	1	Device Tech	850 nm VCSEL, PIN detector	00
148~163	16	Vendor name	OPTOWAY	4F 50 54 4F 57 41 59 20 20 20 20 20 20 20 20 20
164	1	CDR Support	CDR supports 8.5G ~ 1.063G , XFI Loopback	01
165~167	3	Vendor OUI		00 0E FA
168~183	16	Vendor PN	XPM-4100WG	58 50 4D 2D 34 31 30 30 57 47 20 20 20 20 20 20
184~185	2	Vendor rev	ASCII (“31 61” means 1a revision)	xx xx
186~187	2	Wavelength	850 nm	42 68
188~189	2	Wavelength Tolerance	+/- 10nm	07 D0
190	1	Max Case Temp	70deg	46
191	1	CC_BASE	Check sum of Byte 128 -- 190	
192~195	4	Power Supply	1.2Wmax, 1.2W pd_max , 400mA 3.3V	3C 78 04 00
196~211	16	Vendor SN	ASCII	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx
212~219	8	Date code	ASCII Year (2 Byte), Month (2 Byte), Day (2 Byte)	xx xx xx xx xx xx 20 20
220	1	Diagnostic Monitoring Type	No BER Support, Average Power	08
221	1	Enhanced Options	Optional Soft TX_DISABLE implemented, Optional Soft P_down implemented	60
222	1	Aux Monitoring	AUX1 for Vcc3.	70
223	1	CC_EXT	Check sum of Byte 192 -- 222	
224~255	32	Vendor Specific		Reserved

Note: Specifications subject to change without notice.



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## REVISION HISTORY

Version	Subject	Release Date
1.0	Initial datasheet	2008/5/1
2.0	Add XPM-4100BWG and XPM-4100AWG	2008/12/1
3.0	Add XFI loopback mode	2009/11/1

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