

# Accutek Microcircuit Corporation

## AK62464Z 65,536 x 24 Bit CMOS/BiCMOS Static Random Access Memory

### DESCRIPTION

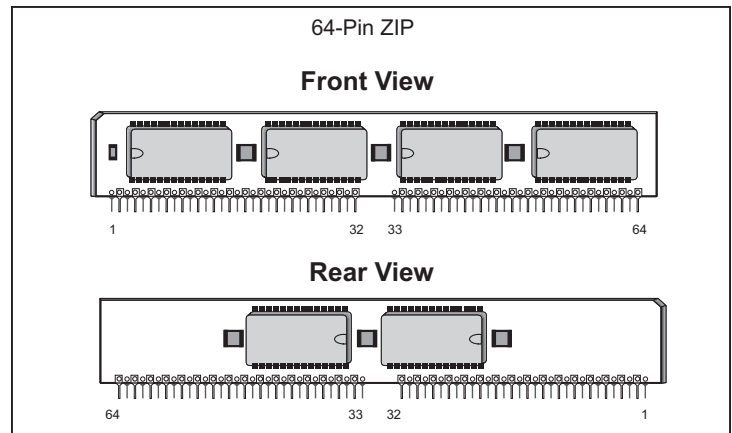
The Accutek AK62464 SRAM Module consists of fast high performance SRAMs mounted on a low profile, 64 pin ZIP Board. The module utilizes six 28 pin 64K x 4 SRAMs in 300 mil SOJ packages and three decoupling capacitors mounted on the top side and two 28 pin 64K x 4 SRAMs in 300 mil SOJ packages and three decoupling capacitors mounted on the bottom side of a printed circuit board.

The SRAMs used have common I/O functions and single output enable functions. Also, three separate chip select (CE) connections are used to independently enable the three bytes. The modules can be supplied in a variety of access time values from 8nSEC to 20nSEC in CMOS or BiCMOS technology.

The Accutek module is designed to have a maximum seated height of 0.500 inch to provide for the lowest height off the board. The modules conform to JEDEC - standard sizes and pin-out configurations. Using two pins for module memory density identification, PD<sub>0</sub> and PD<sub>1</sub>, minimizes interchangeability and design considerations when changing from one module size to the other in customer applications.

### FEATURES

- 65,536 x 24 bit organization
- JEDEC Standard 64 pin ZIP format
- Common I/O, single  $\overline{OE}$  functions with four separate chip selects (CE)
- Low height 0.500 inch maximum
- Upward compatible with



- Presence Detect, PD<sub>0</sub> and PD<sub>1</sub> for identifying module density
- Fast Access Times range from 8 nSEC BiCMOS to 20 nSEC CMOS
- TTL-compatible inputs and outputs
- Single 5 volt power supply - AK62464Z
- Single 3.3 volt power supply - AK62464Z/3.3
- Operating temperature range in free air, 0°C to 70°C
- Power
  - 900 mA Max Active (12 nS)
  - 840 mA Max Active (15 nS)
  - 780 mA Max Active (20 nS)
  - 240 mA Max Standby (Cycling)
  - 12 mA Max Standby (f=0MHZ)

### PIN NOMENCLATURE

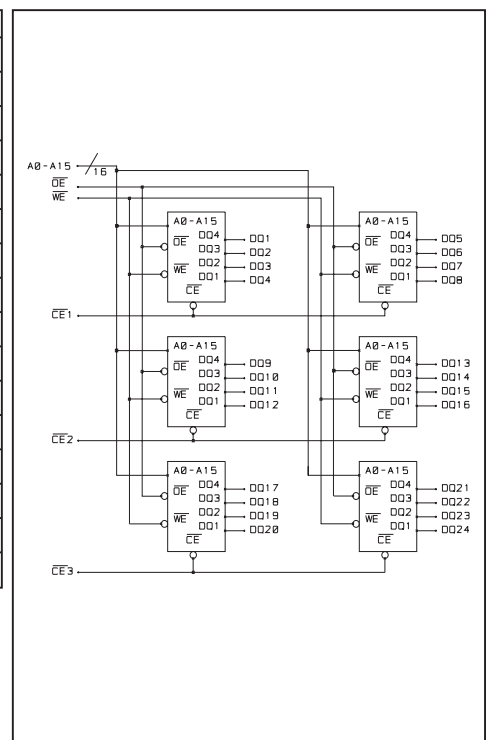
A <sub>0</sub> - A <sub>15</sub>	Address Inputs
$\overline{CE}_1$ - $\overline{CE}_3$	Chip Enable
DQ <sub>1</sub> - DQ <sub>24</sub>	Data In/Data Out
$\overline{OE}$	Output Enable
PD <sub>0</sub> - PD <sub>1</sub>	Presence Detect
V <sub>cc</sub>	Power Supply
V <sub>ss</sub>	Ground
$\overline{WE}$	Write Enable
NC	No Connect

### PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	V <sub>ss</sub>	17	A <sub>2</sub>	33	NC	49	A <sub>4</sub>
2	PD <sub>0</sub>	18	A <sub>9</sub>	34	$\overline{CE}_3$	50	A <sub>11</sub>
3	PD <sub>1</sub>	19	DQ <sub>9</sub>	35	NC	51	A <sub>5</sub>
4	DQ <sub>1</sub>	20	DQ <sub>5</sub>	36	NC	52	A <sub>12</sub>
5	NC	21	DQ <sub>10</sub>	37	$\overline{OE}$	53	V <sub>cc</sub>
6	DQ <sub>2</sub>	22	DQ <sub>6</sub>	38	V <sub>ss</sub>	54	A <sub>13</sub>
7	NC	23	DQ <sub>11</sub>	39	DQ <sub>13</sub>	55	A <sub>6</sub>
8	DQ <sub>3</sub>	24	DQ <sub>7</sub>	40	DQ <sub>17</sub>	56	DQ <sub>21</sub>
9	NC	25	DQ <sub>12</sub>	41	DQ <sub>14</sub>	57	NC
10	DQ <sub>4</sub>	26	DQ <sub>8</sub>	42	DQ <sub>18</sub>	58	DQ <sub>22</sub>
11	NC	27	V <sub>ss</sub>	43	DQ <sub>15</sub>	59	NC
12	V <sub>cc</sub>	28	$\overline{WE}$	44	DQ <sub>19</sub>	60	DQ <sub>23</sub>
13	A <sub>0</sub>	29	A <sub>15</sub>	45	DQ <sub>16</sub>	61	NC
14	A <sub>7</sub>	30	A <sub>14</sub>	46	DQ <sub>20</sub>	62	DQ <sub>24</sub>
15	A <sub>1</sub>	31	$\overline{CE}_2$	47	A <sub>3</sub>	63	NC
16	A <sub>8</sub>	32	$\overline{CE}_1$	48	A <sub>10</sub>	64	V <sub>ss</sub>

PD<sub>0</sub> = Open  
PD<sub>1</sub> = V<sub>ss</sub>

### FUNCTIONAL DIAGRAM



### MODULE OPTIONS

Leadless ZIP:	AK62464Z
---------------	----------

## ORDERING INFORMATION

### PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8										
<b>1 Product</b>	<b>AK = Accuthek Memory</b>																	
<b>2 Type</b>	4 = Dynamic RAM 5 = CMOS Dynamic RAM 6 = Static RAM																	
<b>3 Organization/Word Width</b>	1 = by 1    16 = by 16 4 = by 4    32 = by 32 8 = by 8    36 = by 36 9 = by 9																	
<b>4 Size/Bits Depth</b>	64 = 64K    4096 = 4 MEG 256 = 256K    8192 = 8 MEG 1024 = 1 MEG    16384 = 16 MEG																	
<b>5 Package Type</b>	G = Single In-Line Package (SIP) S = Single In-Line Module (SIM) D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP)																	
<b>6 Special Designation</b>	P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram																	
<b>7 Separator</b>	- = Commercial 0°C to +70°C M = Military Equivalent Screened (-55°C to +125°C) I = Industrial Temperature Tested (-45°C to +85°C) X = Burned In																	
<b>8 Speed (first two significant digits)</b>	<table border="0"> <tr> <td>DRAMS</td> <td>SRAMS</td> </tr> <tr> <td>50 = 50 nS</td> <td>12 = 12 nS</td> </tr> <tr> <td>60 = 60 nS</td> <td>15 = 15 nS</td> </tr> <tr> <td>70 = 70 nS</td> <td>20 = 20 nS</td> </tr> <tr> <td>80 = 80 nS</td> <td>25 = 25 nS</td> </tr> </table>								DRAMS	SRAMS	50 = 50 nS	12 = 12 nS	60 = 60 nS	15 = 15 nS	70 = 70 nS	20 = 20 nS	80 = 80 nS	25 = 25 nS
DRAMS	SRAMS																	
50 = 50 nS	12 = 12 nS																	
60 = 60 nS	15 = 15 nS																	
70 = 70 nS	20 = 20 nS																	
80 = 80 nS	25 = 25 nS																	

The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

### EXAMPLES:

#### AK62464Z-12

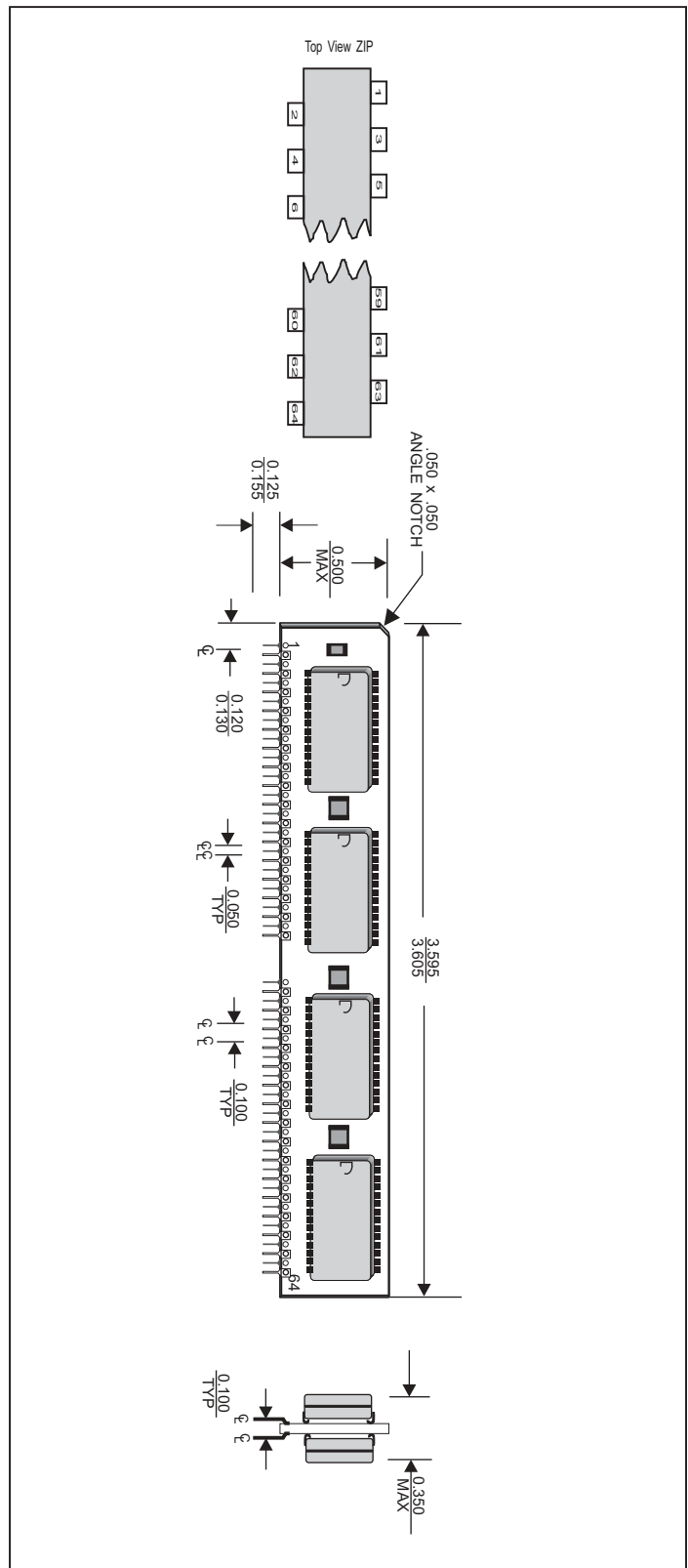
64K x 24, 12 nSEC SRAM Module, ZIP Configuration



**ACCUTEK MICROCIRCUIT CORPORATION**  
 BUSINESS CENTER at NEWBURYPORT  
 2 NEW PASTURE ROAD, SUITE 1  
 NEWBURYPORT, MA 01950-4054  
 PHONE: 978-465-6200 FAX: 978-462-3396  
 E-mail: sales@accutekmicro.com  
 Internet: www.accutekmicro.com

## MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.