Single N-channel MOSFET

ELM2N7002K-S

■General description

ELM2N7002K, a N-channel enhancement mode field effect transistor, is produced by using high cell density, DMOS technology; it is designed to minimize on-state resistance while providing rugged, reliable, and fast switching performance. It can be used in most applications requiring up to 200mA DC and deliver pulsed current up to 800mA. This product is particularly suitable for low voltage, low current applications, such as small servo motor controls, power MOSFET gate drivers, and other switching applications.

■Features

- Vds=60V
- Id=±200mA
- Rds(on) < 5.0Ω (Vgs=10V)
- Rds(on) < 5.0Ω (Vgs=5V)
- Rds(on) < 5.3Ω (Vgs=4.5V)
- ESD Rating : 2000V HBM

■Maximum absolute ratings

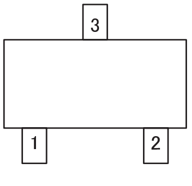
Parameter		Symbol	Limit	Unit
Drain-source voltage		Vds	60	V
Drain-gate voltage (Rgs=1.0MΩ)		Vdgr	60	V
Gate-source voltage		Vgs	±20	V
Continuous drain current	Ta=25℃	Id	±200	mA
Pulsed drain current		Idm	±800	mA
Repetitive avalanche energy (L=30mH)		Eav	9.6	mJ
Power dissipation	Ta=25℃	Pd	200	mW
	Ta>25℃		1.6	mW/℃
Junction and storage temperature range		Tj, Tstg	-55 to 150	℃

■Thermal characteristics

Parameter		Symbol	Value	Unit
Maximum junction-to-ambient	Steady-state	Rθja	625	℃/W

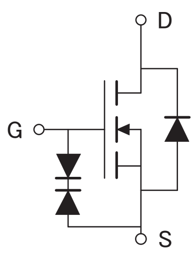
■Pin configuration

SOT-23 (TOP VIEW)



Pin No.	Pin name
1	GATE
2	SOURCE
3	DRAIN

■Circuit



■Electrical characteristics

Ta=25℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	BVdss	Id=10μA, Vgs=0V	60			V
Zero gate voltage drain current	Idss	Vds=48V, Vgs=0V			10	μA
Gate-body leakage current	Igss	Vgs=±20V			±5	μA
Gate threshold voltage *	Vgs(th)	Vds=Vgs, Id=250μA	1.0		2.0	V
On state drain current	Id(on)	Vgs=10V, Vds≥2V	500			mA
Static drain-source on-resistance *	Rds(on)	Vgs=10V, Id=0.5A		2.3	5.0	Ω
		Vgs=5V, Id=50mA		2.8	5.0	
		Vgs=4.5V, Id=75mA		3.3	5.3	
Drain-source on-voltage *	Vds(on)	Vgs=10V, Id=0.5A			3.750	V
		Vgs=5V, Id=50mA			0.375	
Forward transconductance	Gfs	Vds≥2V, Id=200mA *	80			S
DYNAMIC PARAMETERS						
Input capacitance	Ciss	Vgs=0V, Vds=25V, f=1MHz		50		pF
Output capacitance	Coss			25		pF
Reverse transfer capacitance	Crss			5		pF
SWITCHING PARAMETERS						
Turn-on delay time	td(on)	Vgs=10V, Vds=50V Rl=250Ω, Rgen=50Ω *			20	ns
Turn-off delay time	td(off)				40	ns

* : 1.The Power Dissipation of the package may result in a continuous drain current.
2.Pulse Width≤300us, Duty Cycle≤2%.

■Typical electrical and thermal characteristics

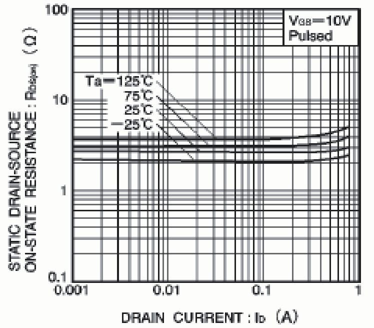


Fig.1 Static drain-source on-state resistance vs. drain current (I)

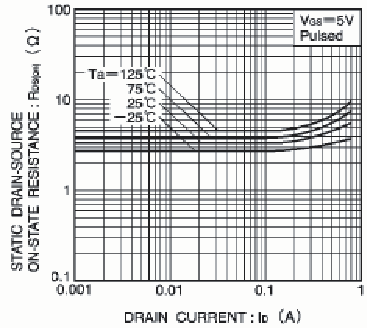


Fig.2 Static drain-source on-state resistance vs. drain current (II)

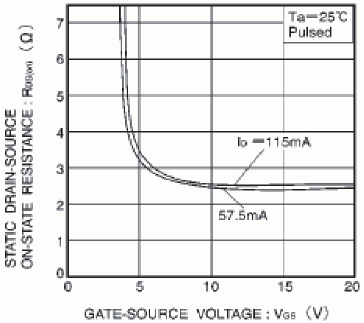


Fig.3 Static drain-source on-state resistance vs. gate-source voltage

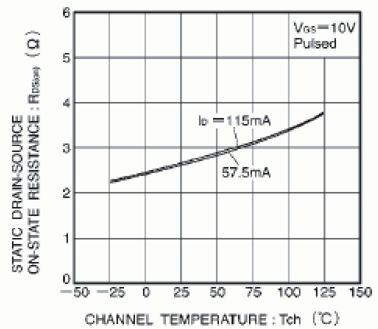


Fig.4 Static drain-source on-state resistance vs. channel temperature

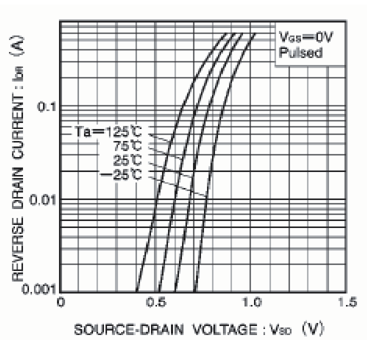


Fig.5 Reverse drain current vs. source-drain voltage (I)

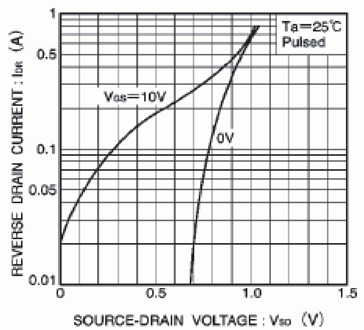


Fig.6 Reverse drain current vs. source-drain voltage (II)

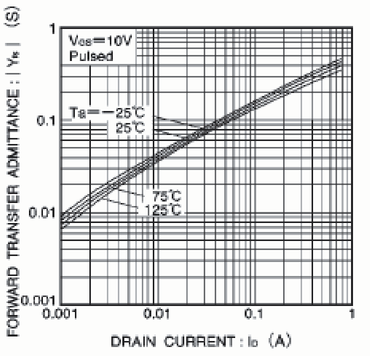


Fig. 7 Forward transfer admittance vs. drain current

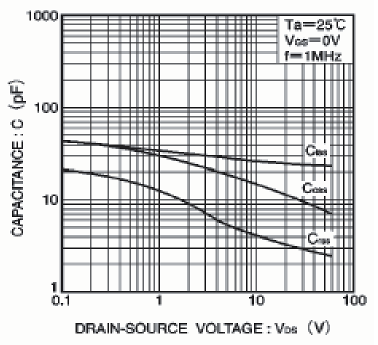


Fig. 8 Typical capacitance vs. drain-source voltage

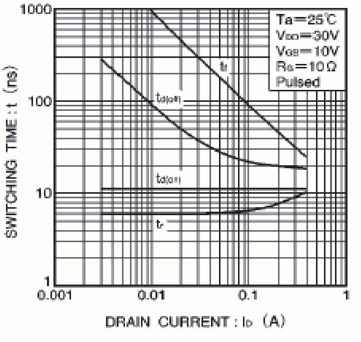


Fig. 9 Switching characteristics (See Figures 13 and 14 for the measurement circuit and resultant waveforms)