Product Family Specification

VTI Automotive Digital Accelerometer Platform

SCA8X0 / 21X0 / 31X0 Accelerometers

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General Description

1.1 Introduction

VTI Automotive Digital Accelerometer Platform is an accelerometer product concept based on VTI capacitive 3D-MEMS technology. The VTI ADP platform integrates high accuracy micromechanical acceleration sensing together with a flexible SPI digital interface. The products within the platform range from single axis accelerometers into two or three axis accelerometers. Dual Flat Lead (DFL) housing of the component guarantees robust operation over the product lifetime.

The products are designed, manufactured and tested for high stability, reliability and quality requirements of automotive applications. The accelerometers have extremely stable output over wide range of temperature, humidity and mechanical noise. The components are qualified against AEC-Q100 standard and have several advanced self diagnostics features. The DFL housing is suitable for SMD mounting and the component is compatible with RoHS and ELV directives.

This Product Family Specification describes the VTI Automotive Digital Accelerometer Platform common characteristics and how to operate with the products. Detail product specification is described in individual data sheets of each product.

1.2 Features

Standard features of the VTI Automotive Digital Accelerometer Platform

- Single, dual or three axis acceleration measurement
- SPI digital interface
- 3.3V supply voltage
- Enhanced self diagnostics features
- Internal temperature sensor
- Size 7.6 x 3.3 x 8.6 mm (w x h x l)
- RoHS compliant Dual Flat Lead (DFL) plastic package suitable for lead free soldering process and SMD mounting
- Package, pin-out and SPI protocol compatible within the product family
- Proven capacitive 3D-MEMS technology
- Qualified according to AEC-Q100 standard

Main characteristics of each product within the product family are listed in Table 1 below.

Table 1: Digital platform summary

Type	Measuring directions	
SCA810	X	Single axis Accelerometer
SCA820	Z	Single axis Accelerometer
SCA830	Y	Single axis Accelerometer
SCA2100	X, Y	Dual axis Accelerometer
SCA2110	X, Z	Dual axis Accelerometer
SCA2120	Y, Z	Dual axis Accelerometer
SCA3100	X, Y, Z	Three axis Accelerometer

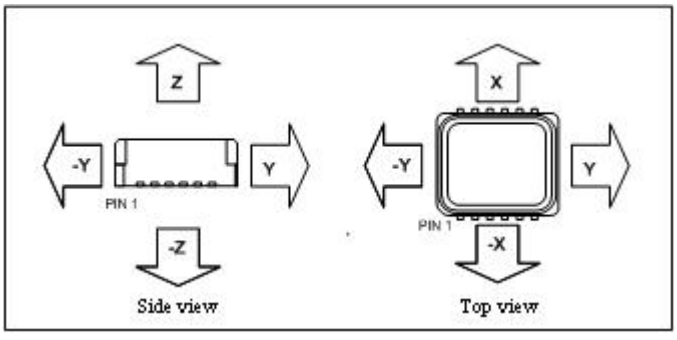


Figure 1: Measurement directions

1.3 Typical applications

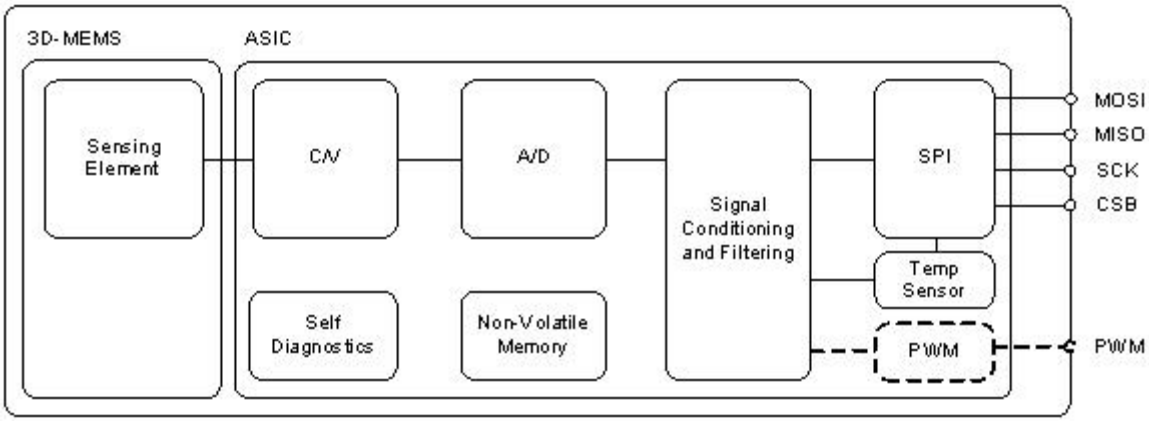
VTI Automotive Digital Accelerometer Platform is targeted to automotive applications with high stability requirements. Typical applications include but are not limited to

- Electronic Stability Control (ESC)
- Hill Start Assist (HSA)
- Electronic Parking Brake (EPB)
- Roll Over
- Active Suspension
- Inclination
- Industrial applications

1.4 Functional Description

Basic product concept of the VTI Automotive Digital Accelerometer Platform is a two chip solution consisting of a single sensing element and one ASIC inside a pre-molded 12-pin housing. The interface to the application is a four wire digital SPI interface. In single axis products there is also Pulse Width Modulation output available. In addition to the supply voltage filtering the component does not require any other components to be connected to the device.

Block diagram of SCA8X0/SCA21X0/31X0



1.4.1 Sensing element

The sensing element of the product is manufactured by using VTI Technologies proprietary bulk 3D-mems process enabling a robust, stable and low noise capacitive sensor. Depending on the product type and measurement direction the sensing element type and orientation inside the housing can vary. Single axis products are equipped with single axis sensing elements and multi axis products are equipped with multi axis sensing elements.

1.4.2 Interface IC

The main functional blocks of the interface ASIC are the following:

1.4.3 Capacitance to voltage conversion

The acceleration is causing a capacitance change inside the sensing element. The capacitance change can be detected by the ASIC analog interface. The capacitance information is converted into an analog voltage that can be further processed easily inside the ASIC.

1.4.4 Analog to digital conversion

Analog voltage information is amplified and filtered and converted into digital information for signal processing inside the ASIC.

1.4.5 Signal conditioning and filtering

The block filters and conditions the measurement information needed for the application

1.4.6 Temperature measurement

The accelerometers contain a temperature sensor for temperature compensation purposes and for use in the application.

1.4.7 Memory

Factory programmed calibration values are stored in a non-volatile memory

1.4.8 SPI

SPI interface is a simple four wire interface for communication between the component and the application micro controller.

1.4.9 Self diagnostics

The VTI Automotive Digital Platform contains several enhanced diagnostics features to allow timely and robust failure detection.

1.4.10 Power supply interface

The products are equipped with separate power and ground pins for analog and digital functionality to allow high accuracy measurement.

1.4.11 Factory calibration

VTI Automotive Digital Platform accelerometers are factory calibrated. No separate calibration is required in the application. Trimmed parameters during production include sensitivity, offset and frequency response. Calibration parameters are stored during the manufacturing of the part inside a non-volatile memory. The parameters are read automatically from the internal non-volatile memory during the startup of the sensor after power on.

2 Operation Modes

2.1 Measurement mode

After the startup the acceleration data is immediately available through the SPI registers. There is no need to initialize the accelerometer before starting to use of it. If the application is requiring monitoring of the correctness of the operation there are several options available to monitor the operation status.

2.2 Temperature output

The devices include a temperature measurement function. Temperature data can be read through the SPI interface. Temperature measurement is not calibrated for absolute accuracy. If absolute accuracy is needed, it can be achieved through measuring the temperature value in two temperature points in final application and storing them as a calibration value and calculating the absolute temperature value by using the two points.

2.3 Self-diagnostic functions

VTI Automotive Digital Accelerometer Platform has a set of built-in self-diagnostic functions to support the application fail safety. The diagnostic functions cover the accelerometer sensing element functionality, accelerometer internal operation and signal path functionality

2.3.1 Memory self-diagnostic

Factory calibrated values of the accelerometer are stored in a non-volatile memory. The calibrated values are read during the device power on into volatile registers that control the operation of the device. During the startup of the device the calculated sum of non-volatile registers is compared to the factory calibrated value. The test is done automatically after supplies are set on, after any reset state of component and after return from power-down mode. Test can also be started by a CTRL-register command.

2.3.2 Signal path self-diagnostic

2.3.2.1 SCA8X0 – single axis accelerometers

Sensor element and signal path is tested by deflecting the proof mass of the sensing element to both directions over a predefined dynamic range. The test is done automatically during start-up and it can be repeated by a CTRL-register command. The result of the test is a momentary mass deflection seen in the output of the device. During the test the accelerometer performs a comparison of the deflection result to a pre-defined threshold value. When the needed dynamics have been detected the device will return the result of a passed test in a register. By following the output of the device on SPI interface it is possible to detect failures through the signal path.

2.3.2.2 SCA21X0 and SCA31X0 – multi axis accelerometers

2.3.2.2.1 Start-up Self Test (STS)

During the application start up or when the accelerometer is affected by the gravity force only it is possible to detect possible sensing element anomalies by applying a start up self test. The test is done in a following way: a digitally calculated resultant acceleration of x, y and z-axis is compared to predefined threshold value. Test is started by CTRL-register command and it is done once when requested.

2.3.2.2.2 Continuous Self Test (STC)

During device operation the continuous self test is monitoring the sensing element performance. Digitally calculated self-diagnostic function is compared to predefined threshold value. Test is started by CTRL-register command and it is calculated continuously on background until disabled. Possible errors are indicated in an error status register and in SPI frame.

2.4 Power Down mode

For low power applications it is possible to set the accelerometer into power down mode. During the power down mode the power consumption is minimized inside the device. This is achieved by stopping the internal clocks and resetting the control registers of the device. Please refer to the individual device data sheets for detail power consumption figures.

2.5 Recommended start-up sequence

For correct device operation there are no specific configuration needed for the device before starting of measuring the acceleration. However if the device detail features are being used the following operations could be made after the powering on the device.

Table 2: SCA8X0 start up sequence

Item	Procedure	Functions	Check
1	Set Vdd=3.0...3.6V	• Set the power on to release part from reset and to start the operation	-
2	Wait 95ms	• During the first 95ms the part is performing the memory read and self-diagnostics. • Possible signal path self-diagnostic test is carried out. • Settling of signal path	-
3	Read CTRL-register	• Check the self-test pass status	• CTRL.ST=0 • SPI fixed bits • dPAR, data parity
4	Read STATUS-register	• Check the memory checksum pass status	• STATUS.CSMERR=0 • SPI fixed bits • SPI FRME=0 • dPAR, data parity
5	Write CTRL=0000 0000	• After device power on set PORST=0 to be able to detect any future occurring power failures	• SPI fixed bits • SPI FRME=0
6	Read X_MSB, X_LSB – registers	• Start reading the acceleration data	• SPI fixed bits • SPI FRME=0 • SPI PORST=0 • dPAR, data parity

Table 3: SCA21X0 and SCA31X0 start up sequence

Item	Procedure	Functions	Check
1	Set Vdd=3.0...3.6V	• Release part from reset	-
2	Wait 35ms	• Memory reading and self-diagnostic • Settling of signal path	-
3	Read INT_STATUS	• Acknowledge for possible saturation (SAT-bit) • Checksum pass detected from SPI frame	• SPI fixed bits • SPI ST=0
4	Write CTRL=00001010 (a) or CTRL=00001000 (b) or CTRL=00000000 (c)	• Set PORST=0 (abc) • Start STC (ab) • Start STS (a)	• SPI fixed bits • SPI FRME=0 • SPI ST=0 • SPI SAT=0
5	Wait 10ms	STS calculation	-
6	Read CTRL	• Check that STC is on, if enabled • Check that STS is over if enabled	• CTRL.ST=1 • CTRL.ST_CFG=0 • SPI fixed bits • SPI FRME=0 • SPI PORST=0 • SPI ST=0 • SPI SAT=0 • dPAR, data parity
7	Read Z_MSB, Z_LSB, Y_MSB, Y_LSB, X_MSB, X_LSB	Read acceleration data	• SPI fixed bits • SPI FRME=0 • SPI PORST=0 • SPI ST=0 • SPI SAT=0 • dPAR, data parity

2.6 Recommended operation sequence

Table 4: Reading of the acceleration data

Item	Procedure	Functions	Check
1	Read acceleration data	Desired x, y, or/and z-data	• SPI fixed bits • SPI FRME=0 • SPI PORST=0 • SPI ST=0 • SPI SAT=0 • dPAR, data parity
2	Repeat item 1 (N-1) times	Noise averaging	-
3	Calculate average (AVE) of N-samples	Noise averaging	-
4	Read acceleration data	Desired x, y, or/and z-data (one read before sending	• SPI fixed bits • SPI FRME=0 • SPI PORST=0

Item	Procedure	Functions	Check
		AVE forward to check SPI failure bits)	• SPI ST=0 • SPI SAT=0 • dPAR, data parity
5	Send calculated AVE forward	-	-
6	Jump back to item 2	-	-

For detailed SPI failure bit information see chapter 4.2 Error Conditioning

2.7 Recommended procedures or optional features

Product family components have different features, which are not required during normal operation. However, they are recommended in some cases if they are seen important from system perspective.

2.7.1 SCA8x0/SCA21x0/SCA31x0

2.7.1.1 Read back procedure

It is recommended to read back every write command to compare read data to the write command. This way it is detected very unlikely failures in MCU, in SPI wiring, in SPI interface, in system clock or inside state machine.

2.7.1.2 Checksum during operation

Checksum is calculated for component register values that control the operation of product. Data is read from non-volatile memory to these registers during start-up and checksum is calculated automatically. It is possible to repeat checksum calculation during normal operation by CTRL register command and test result can be seen from STATUS register (see more info in 3.2.1 and 3.1.6). In multi-axis products test result can be seen also from SPI frame. By repeating checksum during normal operation, it is possible to detect very unlikely intermittent or static bit failures in register map.

2.7.1.3 Saturated data

Output data saturates to predefined value if product dynamic range is exceeded. If output data has been saturated it should be considered invalid and it should not be used for system controlling. Output data saturation can also be indication of some very unlike component failure.

2.7.1.4 Noiseless output

Valid acceleration output includes always some noise. If output data is constant, it can be indication of system error and data is not valid anymore. Therefore it is useful to monitor noise or deviation of output data.

2.7.1.5 Component ID

Each product family component type has unique identification number, which is stored to non-volatile memory (see 3.3.2). This number can be used for example in production line to check that correct component is mounted to the system. In some cases it may be used for MCU software controlling.

2.7.2 SCA8x0

2.7.2.1 Mass deflection during operation

Mass deflection self-test is performed automatically to both direction in start-up. Mass deflection can be performed during operation if requested by user. Test is started and direction is controlled

by CTRL register (see more info in 3.2.1). Note that acceleration output data is not valid during test and after test is started to one direction there has to be 50ms wait time before output data is used.

2.7.2.2 Monitor acceleration data during mass deflection

Acceleration data can be read out from acceleration output registers during mass deflection self-test in start-up or during operation, in case that test is repeated by the request. Monitoring this data it is possible to determine product frequency response and check product timing properties.

3 Addressing Space

Table 5 presents the registers of SCA8X0, SCA21X0 and SCA31X0 products.

Table 5: Register address space

Addr hex	Name	Description	Mode (R/RW)
00	REVID	ASIC revision ID number	R
01	CTRL	Control	RW
02	STATUS	Status	R
03	RESET	Reset component	RW
04	X_LSB	X-axis (or Y- or Z-axis in SCA8X0) LSB frame	R
05	X_MSB	X-axis (or Y- or Z-axis in SCA8X0) MSB frame	R
06	Y_LSB	Y-axis LSB frame in multi-axis components	R
07	Y_MSB	Y-axis MSB frame in multi-axis components	R
08	Z_LSB	Z-axis LSB frame in multi-axis components	R
09	Z_MSB	Z-axis MSB frame in multi-axis components	R
0A		Reserved	-
...		Reserved	-
11		Reserved	-
12	TEMP_LSB	Temperature LSB frame	R
13	TEMP_MSB	Temperature MSB frame	R
14		Reserved	-
15		Reserved	-
16	INT_STATUS	Interrupt status register in multi-axis components	R
17		Reserved	-
...		Reserved	-
26		Reserved	-
27	ID	Component ID	RW
28		Reserved	-
...		Reserved	-
3F		Reserved	-

3.1 Output registers

3.1.1 X axis acceleration output

3.1.1.1 X_LSB

Address: 4h

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	X-axis LSB frame (or Y-axis or Z-axis in SCA8X0) Read always X_MSB prior to X_LSB.

3.1.1.2 X_MSB

Address: 5h

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	X-axis MSB frame (or Y-axis or Z-axis in SCA8X0) Reading of this register latches X_LSB.

3.1.2 Y axis acceleration output

3.1.2.1 Y_LSB

Address: 6h

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Y-axis LSB frame Read always Y_MSB prior to Y_LSB.

3.1.2.2 Y_MSB

Address: 7h

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Y-axis MSB frame Reading of this register latches Y_LSB.

3.1.3 Z axis acceleration output

3.1.3.1 Z_LSB

Address: 8h

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Z-axis LSB frame Read always Z_MSB prior to Z_LSB.

3.1.3.2 Z_MSB

Address: 9h

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Z-axis MSB frame Reading of this register latches Z_LSB.

The bit level description of acceleration data from X_LSB ... Z_MSB registers is presented below (Note that the available axis combination of xyz depends on product type). The acceleration data is presented in 2's complement format. At 0 g acceleration the output is ideally 0000h.

3.1.4 Output data conversion

3.1.4.1 2g products

+/-2g product	DOUT MSB bits(7:0)								DOUT LSB bits(7:0)									12b	12b
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	[-]	Bits (15:4)	Bits (15:4)
SCA8x0	s	1137.8	568.9	284.4	142.2	71.1	35.6	17.8	8.89	4.44	2.22	1.11	x	x	x	x	[mg]	[Dec]	[Hex]
+1g position	0	0	1	1	1	0	0	0	0	1	0	0	x	x	x	x	1000	900	384
-1g position	1	1	0	0	0	1	1	1	1	1	0	0	x	x	x	x	-1000	-900	C7C
+Full-scale	0	1	1	1	1	1	1	1	1	1	1	1	x	x	x	x	2274	2047	7FF
-Full-scale	1	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	-2275	-2048	800

+/-2g product	DOUT MSB bits(7:0)								DOUT LSB bits(7:0)										
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	[-]	Bits (15:2)	Bits (15:2)
SCA31x0/SCA21x0	s	4551.1	2275.6	1137.8	568.9	284.4	142.2	71.1	35.56	17.78	8.89	4.44	2.22	1.11	x	x	[mg]	[Dec]	[Hex]
+1g position	0	0	0	0	1	1	1	0	0	0	0	1	0	0	x	x	1000	900	384
-1g position	1	1	1	1	0	0	0	1	1	1	1	1	0	0	x	x	-1000	-900	3C7C
+Full-scale *)	0	0	0	1	1	1	1	1	1	1	1	1	1	1	x	x	2274	2047	7FF
-Full-scale *)	1	1	1	0	0	0	0	0	0	0	0	0	0	0	x	x	-2275	-2048	3800

s = sign bit
x = not used/defined bit
*) = positive/negative full-scale or saturation limit of ±2 g product is 2.27 g.

In SCA8X0 acceleration bits can be converted to mg acceleration (Acc) using following equation

$$Acc[mg] = \frac{10}{9}\left[-s\cdot 2^{11} + b14\cdot 2^{10} + b13\cdot 2^{9} + b12\cdot 2^{8} + b11\cdot 2^{7} + b10\cdot 2^{6} + b9\cdot 2^{5} + b8\cdot 2^{4} + b7\cdot 2^{3} + b6\cdot 2^{2} + b5\cdot 2 + b4\right]$$

and in SCA21X0/SCA31X0

$$Acc[mg] = \frac{10}{9}\left[\begin{array}{l} -s\cdot 2^{13} + b14\cdot 2^{12} + b13\cdot 2^{11} + b12\cdot 2^{10} + b11\cdot 2^{9} + b10\cdot 2^{8} \\ + b9\cdot 2^{7} + b8\cdot 2^{6} + b7\cdot 2^{5} + b6\cdot 2^{4} + b5\cdot 2^{3} + b4\cdot 2^{2} + b3\cdot 2 + b2 \end{array}\right],$$

where bits are defined according to following table.

Acceleration MSB-register: Address 5'hex / 7'hex / 9'hex								Acceleration LSB-register: Address 4'hex / 6'hex / 8'hex							
DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

In data output registers of SCA21X0/SCA31X0 there is reserved room for different g-ranges. To make sure that same software works with different product types it is recommended to use bits(15:2) for data conversion. If dynamic output range of product does not require bits b14 or b13 they include copy of sign bit b15.
If self-test (checksum, STC, STS) alarms it sets ST bit in SPI frame and forces output data to value 7FFF'hex (checksum fail) or to value FFFF'hex (STC/STS alarm).

In SCA21X0/SCA31X0 there is also possible to use 1-extra lsb bit (b1) for calculation to improve resolution. In that case acceleration bits can be converted to mg acceleration (Acc) using following equation

$$Acc[mg] = \frac{10}{18}\left[\begin{array}{l} -s\cdot 2^{14} + b14\cdot 2^{13} + b13\cdot 2^{12} + b12\cdot 2^{11} + b11\cdot 2^{10} + b10\cdot 2^{9} + b9\cdot 2^{8} \\ + b8\cdot 2^{7} + b7\cdot 2^{6} + b6\cdot 2^{5} + b5\cdot 2^{4} + b4\cdot 2^{3} + b3\cdot 2^{2} + b2\cdot 2 + b1 \end{array}\right].$$

3.1.4.2 6 g products

+/-6g product	DOUT MSB bits(7:0)								DOUT LSB bits(7:0)									12b	12b
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	[-]	Bits (15:4)	Bits (15:4)
SCA8x0	s	3150.8	1575.4	787.7	393.8	196.9	98.5	49.2	24.6	12.31	6.15	3.08	x	x	x	x	[mg]	[Dec]	[Hex]
+1g position	0	0	0	1	0	1	0	0	0	1	0	1	x	x	x	x	1000	325	145
-1g position	1	1	1	0	1	0	1	1	1	0	1	1	x	x	x	x	-1000	-325	EBB
+Full-scale	0	1	1	1	1	1	1	1	1	1	1	1	x	x	x	x	6300	2047	7FF
-Full-scale	1	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	-6302	-2048	800

+/-6g product	DOUT MSB bits(7:0)								DOUT LSB bits(7:0)										
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	[-]	Bits (15:2)	Bits (15:2)
SCA31x0/SCA21x0	s	6301.5	3150.8	1575.4	787.7	393.8	196.9	98.5	49.2	24.6	12.3	6.15	3.08	1.54	x	x	[mg]	[Dec]	[Hex]
+1g position	0	0	0	0	1	0	1	0	0	0	1	0	1	0	x	x	1000	650	28A
-1g position	1	1	1	1	0	1	0	1	1	1	0	1	1	0	x	x	-1000	-650	3D76
+Full-scale *)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	x	x	6300	4095	FFF
-Full-scale *)	1	1	0	0	0	0	0	0	0	0	0	0	0	0	x	x	-6302	-4096	3000

s = sign bit
x = not used/defined bit
*) = positive/negative full-scale or saturation limit of ±6 g product is 6.3 g.

In SCA8X0 acceleration bits can be converted to mg acceleration (Acc) using following equation

$$Acc[mg] = \frac{1000}{325}\left[-s\cdot 2^{11} + b14\cdot 2^{10} + b13\cdot 2^{9} + b12\cdot 2^{8} + b11\cdot 2^{7} + b10\cdot 2^{6} + b9\cdot 2^{5} + b8\cdot 2^{4} + b7\cdot 2^{3} + b6\cdot 2^{2} + b5\cdot 2 + b4\right]$$

and in SCA21X0/SCA31X0

$$Acc[mg] = \frac{1000}{650}\left[\begin{array}{l} -s\cdot 2^{13} + b14\cdot 2^{12} + b13\cdot 2^{11} + b12\cdot 2^{10} + b11\cdot 2^{9} + b10\cdot 2^{8} \\ + b9\cdot 2^{7} + b8\cdot 2^{6} + b7\cdot 2^{5} + b6\cdot 2^{4} + b5\cdot 2^{3} + b4\cdot 2^{2} + b3\cdot 2 + b2 \end{array}\right],$$

3.1.4.3 1 g products

+/-1g product	DOUT MSB bits(7:0)								DOUT LSB bits(7:0)									16b
Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	[-]	Bits (15:0)
SCA8xx	s	512,0	256,0	128,0	64,0	32,0	16,0	8,0	4,00	2,00	1,00	0,50	0,25	0,13	0,06	0,03	[mg]	[Dec]
+1g position	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1000	32000
-1g position	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	-1000	-32000
+Full-scale	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1023	32767
-Full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1024	-32768

s = sign bit

Acceleration bits can be converted to mg acceleration (Acc) using following equation

$$Acc[mg] = \frac{1}{32}\left[\begin{array}{l} -s\cdot 2^{15} + b14\cdot 2^{14} + b13\cdot 2^{13} + b12\cdot 2^{12} + b11\cdot 2^{11} + b10\cdot 2^{10} + b9\cdot 2^{9} + b8\cdot 2^{8} + b7\cdot 2^{7} + b6\cdot 2^{6} + b5\cdot 2^{5} + b4\cdot 2^{4} + b3\cdot 2^{4} \\ + b2\cdot 2^{3} + b1\cdot 2^{1} + b0 \end{array}\right]$$

3.1.5 Temperature output

3.1.5.1 Temperature Register Low (TEMP_LSB)

Address: 12h

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Data bits [7:0] of temperature sensor. Read always TEMP_MSB prior to TEMP_LSB.

3.1.5.2 Temperature Register High (TEMP_MSB)

Address: 13h

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Data bits [15:8] of temperature sensor. Reading of this register latches TEMP_LSB.

The bit level description of temperature data:

In SCA8X0 temperature data is not factory calibrated and hence sensitivity and offset of temperature data varies from part to part. Temperature data is in 2's complement format and 14 bits (13:0) of TEMP_MSB/TEMP_LSB are used for temperature. Here is presented temperature calculation using 10bit but 4-extra LSB bit can be used to improve resolution in noise sense if needed.

Table 6 Bit level description for SCA8X0 temperature registers

Register	TEMP_MSB							TEMP_LSB				
Bit number	B7:B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3:B0
Bit temperature weight [°C]	xx	sign	~82	~41	~21	~10	~5.1	~2.6	~1.3	~0.6	~0.3	rrrr
Bit in temperature register	xx	t9	t8	t7	t6	T5	t4	t3	t2	t1	t0	rrrr

x = not used bit
r=reserved

$$Temp[°C] = (45 \pm 32)°C + \frac{Temp_{dec}}{k\frac{LSB}{°C}},$$

where Temp[°C] is temperature in Celsius and $Temp_{dec}$ is temperature from TEMP_MSB and TEMP_LSB registers in decimal format, bits(t9:0). k is temperature slope factor specified as

	Min	Typ	Max	Unit
k	2.8	3.1	3.5	LSB/ °C

In SCA21X0 and SCA31X0 offset of temperature data is factory calibrated but sensitivity of the temperature data varies from part to part. Temperature data is in unsigned format and 13 bits (13:1) of TEMP_MSB/TEMP_LSB are used for temperature. Here is presented temperature calculation using 10bit but 3-extra LSB bit can be used to improve resolution in noise sense if needed.

Table 7 Bit level description for SCA21X0/31X0 temperature registers

Register	TEMP_MSB							TEMP_LSB				
Bit number	B7:B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3:B0
Bit temperature weight [°C]	xx	~162	~81	~41	~20	~10	~5.1	~2.5	~1.3	~0.6	~0.3	rrrx
Bit in temperature register	xx	t9	t8	t7	T6	T5	t4	t3	t2	t1	t0	rrrx

x = not used bit
r=reserved

Temperature registers' typical output at +23 °C is 512 counts and 1 °C change in temperature typically corresponds to 3.2 LSB change in temperature output. Temperature information is converted to [°C] as follows

$$Temp[°C] = (23 \pm 10)°C + \frac{Temp_{dec} - 512LSB}{k\,\frac{LSB}{°C}},$$

where Temp[°C] is temperature in Celsius and $Temp_{dec}$ is temperature from TEMP_MSB and TEMP_LSB registers in decimal format, bits(t9:0). k is temperature slope factor specified as

	Min	Typ	Max	Unit
k	2.8	3.2	3.6	LSB/°C

3.1.6 Status Register (STATUS)

Address: 2h

Bits	Mode	Initial Value	Name	Description
7:3	-	-		Reserved
2	R	0	ATEST	Analog test mode status 1 – Test mode is active 0 – Test mode is not active
1	R	0	CSMERR	EEPROM Checksum Error. In SCA21X0/SCA31X0 ST bit of SPI frame is also set if CSMERR is set.
0	R	0	FRME	SPI frame error. Bit is reset, when next correct SPI frame is received. Bit is also visible in SPI frame.

3.1.7 Interrupt Status Register (INT_STATUS)

Address: 16h

Bits	Mode	Initial Value	Name	Description
7	R	0		Reserved
6	R	0	SAT	Saturation status of output data 1 – Over range detected, one or 2-3 of xyz axis is saturated and output data is not valid. 0 – Data in range SAT bit is also visible in SPI frame. This bit can be active after start-up or reset stage before signal path settles to final value and it has to be acknowledged in start-up sequence (see **Table 3**) or after SW reset or after PORST stage.
5	R	0	STS	Status of gravitation based start-up self test 1 – Failure 0 – No failure STS sets also ST bit in SPI frame.
4	R	0	STC	Status of continuous self test 1 – Failure 0 – No failure STC sets also ST bit in SPI frame.
3:0	R	0000		Reserved

The bits in this interrupt status register and corresponding SPI frame bits are cleared after register has been read. Register reading is treated as interrupt acknowledgement signal. These bits are kept active even failure condition is over if they are not acknowledged.

This register is not defined in SCA8X0.

3.2 Operation control registers

3.2.1 Control Register (CTRL)

Address: 1h

Bits	Mode	Initial Value	Name	Description
7	RW	0		Reserved
6	RW	0	PORST	1 means reset state. Bit gets set to 1 when the digital gets reset by supply off control or under voltage control. Bit is set after supply off/on transition or startup. This bit can not be set by SPI but it can be reset to 0 by writing a 0 over the SPI. This bit is also sent as Bit3 of SPI output data frame on MISO.
5	RW	0	PDOW	Set chip to power down mode
4	RW	0	SLEEP	Set chip to sleep mode. This bit can not be set to 1 if PDOW is already 1 or if PDOW is being set by the current SPI command. (bit is not used in SCA8X0)
3	RW	0	ST	Set chip to self-test mode. SCA8X0: This bit starts mass deflection self-test (see also ST_CFG bit). This bit is set to 0, when test is passed. This bit can not be set to 1 if PDOW is already 1 or if PDOW is being set by the current SPI command. Test is done automatically during start-up and acceleration output data can be read during test. SCA21X0 and SCA31X0: Start continuous self-test calculation (STC). This bit can not be set to 1 if PDOW or SLEEP or MTST is already 1 or if PDOW or SLEEP or MTST is being set by the current SPI command. Use INT_STATUS.STC and ST bit of SPI frame for test result monitoring.
2	RW	0	MST	Memory self-test function is activated, when user sets bit to '1'. This bit is reset to 0 when test is over. During memory self test, SPI access is prevented for 85us. This bit can not be set to 1 if PDOW or SLEEP is already 1 or if PDOW or SLEEP is being set by the current SPI command. Test is done automatically during start-up. Set other bits to zero in CTRL register by previous SPI command before starting memory self-test by CTRL.MST command. Use STATUS.CSMERR for test result monitoring and in SCA21X0/SCA31X0 ST bit in SPI frame.
1	RW	0	ST_CFG	Self-test configuration. SCA8X0: Select direction of mass deflection. SCA21X0 and SCA31X0: Start gravitation based start-up self-test calculation (STS). This bit can not be set to 1 if PDOW or SLEEP or MTST is already 1 or if PDOW or SLEEP or MTST is being set by the current SPI command. STC and

Bits	Mode	Initial Value	Name	Description
				STS have same priority and they can be set and used simultaneously. This bit is set to 0 when test is over. Use INT_STATUS.STS and ST bit of SPI frame for test result monitoring.
0	RW	0	MISO	0 = Set MISO line to normal state (= High impedance state between SPI transfers, data out state during transfers) 1 = Set MISO like to a continuous high impedance state (same write command to multiple slaves, which share MISO line).

3.2.2 Reset Register (RESET)

Address: 3h

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	RST	Writing 0C'hex, 05'hex, 0F'hex in this order resets component.

3.3 Identification registers

3.3.1 Revision ID (REVID)

Address: 0h

Bits	Mode	Initial Value	Name	Description
7:0	R	23h [1] 22h [2]	REVID	ASIC revision identification number, each ASIC version has different REVID-number.

1) SCA8X0
2) SCA21X0/SCA31X0

3.3.2 Component ID (ID)

Address: 27h

Bits	Mode	Initial Value	Name	Description
7:0	RW		ID	Component identification number (write operation by user is possible to this register but not to non-volatile memory)

The ID register contains information about the product version and value is loaded from non-volatile memory. Each VTI Automotive Digital Accelerometer Platform product will have a unique identification number. Single axis products can be differentiated from multi axis products through this register.

SCA8X0: MSB = 0
SCA21X0: MSB = 1
SCA31X0: MSB = 1

Please refer to the product data sheet for correct ID number.

4 SPI Interface

Serial peripheral interface (SPI) is a 4-wire synchronous serial interface. Data communication is enabled with active low Slave Select or Chip Select wire (CSB). Data is transmitted via 3-wire interface consisting of serial data input (MOSI), serial data output (MISO) and serial clock (SCK). Every SPI system consists of one master and one or more slaves, where the master is defined as the microcomputer that provides the SPI clock, and the slave is any integrated circuit that receives the SPI clock from the master.

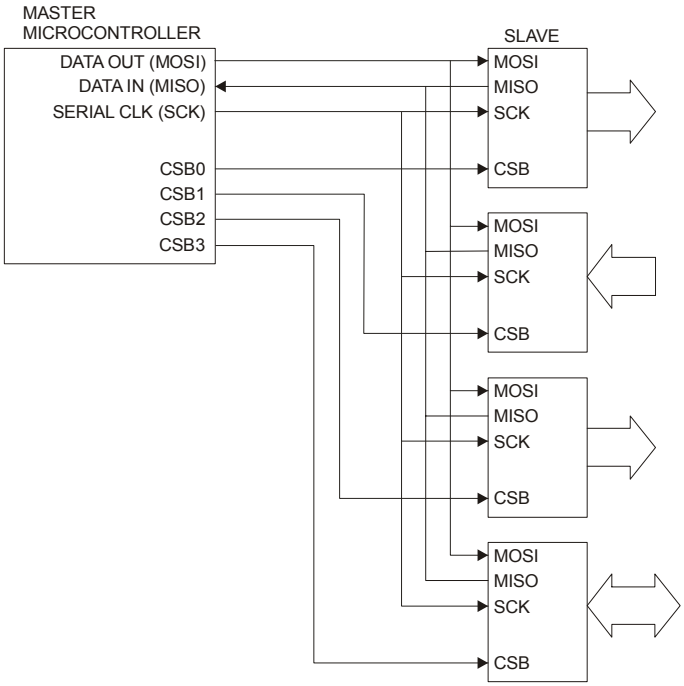


Figure 2: Typical SPI connection

The SPI interface of VTI automotive series is designed to support almost any micro controller that uses software implemented SPI. However it is not designed to support any particular hardware implemented SPI found in many commercial micro controllers. SCA8X0/SCA21X0/SCA31X0 accelerometer operates always as a slave device in the master-slave operation mode. The data transfer between the master (µP test machine etc.) and accelerometer is performed serially with four wire system.

MOSI	master out slave in	µP → ASIC
MISO	master in slave out	ASIC → µP
SCK	serial clock	µP → ASIC
CSB	chip select (low active)	µP → ASIC

Each transmission starts with a falling edge on CSB and ends with the rising edge. During the transmission, commands and data are controlled by SCK and CSB according to the following rules:

- commands and data are shifted MSB first LSB last
- each output data/status-bits are shifted out on the falling edge of SCK (MISO line)
- each bit is sampled on the rising edge of SCK (MOSI line)

SPI communication transfers data between SPI master and registers of the SCA8X0/SCA21X0/SCA31X0. Registers can be read and write.

SPI communication is full duplex communication. Data is send and received simultaneously.

SPI frame format and transfer protocol is presented in Figure 3.

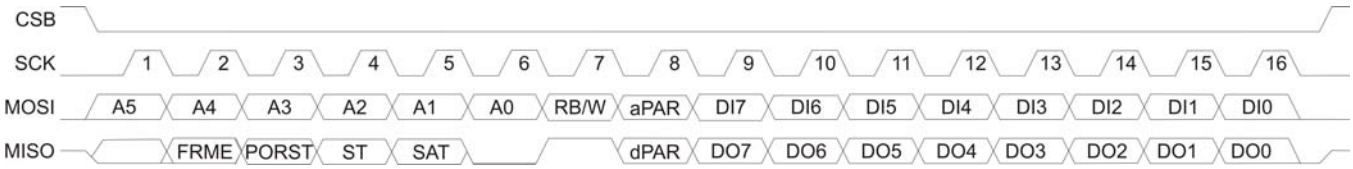


Figure 3: SPI frame format

- MOSI
  - A5:A0 Register address
  - RB/W Read/Write selection, '0'=read
  - aPAR Odd parity for bits A5:A0, RB/W
  - DI7:DI0 Input data for data write
- MISO
  - Bit 1 not defined bit
  - FRME Frame error indication (previous frame)
  - Bit 3-5 status bits
    - PORST Power On Reset Status
    - ST Self Test error, not defined in SCA8X0
    - SAT Output SATuration indicator, not defined in SCA8X0
  - Bit 6 always ‘0’, fixed bit
  - Bit 7 always ‘1’, fixed bit
  - dPAR Odd parity for output data (DO7:DO0)
  - DO7:DO0 Output data

Each communication frame contains 16 bits. Please see Figure 3 for SPI bit definition. The first 8 bits in MOSI line contains info about the operation (read/write) and the register address being accessed. First 6 bits define 6 bit address for selected operation, which is defined by bit 7 (‘0’ = read ‘1’ = write), which is followed by odd parity bit (aPAR) for 8 bit pattern. The later 8 bits in MOSI line contain data for a write operation and are ignored in case of read operation.
The first bits in MISO line are frame error bit (FRME, bit2) of previous frame, reset status bit (PORST, bit3), self-test status bit (ST, bit4), saturation status (SAT, bit5), fixed zero bit (bit6), fixed one bit (bit7) and odd parity bit of output data (dPAR, bit8)). Parity is calculated from data, which is currently sent. The later 8 bits contain data for a read operation. During the write operation, these data bits are previous data bits of addressed register.

For write commands, data is written into the addressed register on the rising edge of CSB. If the command frame is invalid, data will not be written into the register.

The output register is shifted out MSB first over MISO output. Attempt to read a reserved register outputs data of 00h.

When CSB is high state between data transfers, MISO line is in high-impedance state. If bit CTRL.SDODIS is set to ‘1’, MISO line is always in high-impedance state. In multi-chip SPI bus master can send data to all slave chips simultaneously.

4.1 Output of Acceleration Data

16-bit data is sent in 8-bit data bytes during two frames. Each frame contains odd parity bit of data bits. Number format of acceleration data is two’s complement number.

4.1.1 Register read operation

An example of X-axis acceleration read command is presented in Figure 4. Master gives the register address to be read via MOSI line: '05' in hex format and '000101' in binary format, register name is X_MSB (X-axis MSB frame). 7th bit is set to '0' to indicate the read operation and 8th bit is 1 for odd parity.
The sensor replies to asked operation by transferring the register content via MISO line. After transferring the asked X_MSB register content, master gives next register address to be read: '04' in hex format and '000100' in binary format, register name is X_LSB (X-axis LSB frame). The sensor replies to asked operation by transferring the register content MSB first.

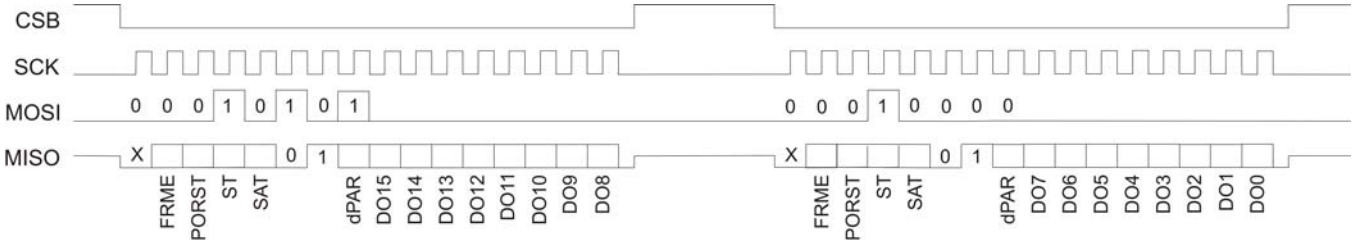


Figure 4: Example of 16 bit acceleration data transfer from registers DOUT2-1 (05h,04h). DO15…DO0 bits are acceleration data bits (DO15=MSB) and parity (dPAR) is odd parity of register of 8 data bits. FRME is possible frame error bit of previous frame, PORST is reset bit, ST is self-test status bit and SAT is output saturation status bit.

4.1.2 Decremented register read operation

In Figure 5 is presented a decremented read operation where the content of four output registers is read by one SPI frame. After normal register addressing and one register content reading the µC keeps CSB line low and continues supplying the SCK pulses. After every 8 SCK pulses the output data address is decremented by one and the previous DOUT register's content is shifted out without parity bits. Parity bit is calculated and transferred only for the first data frame. From X_LSB register address the SCA21X0/SCA31X0 jumps to Z_MSB. Decremented reading is possible only for registers X_LSB ... Z_MSB in SCA21X0 and SCA31X0 series.
Decremented read is not recommended in fail-safe critical applications because output data parity is only available for first 8bit data.

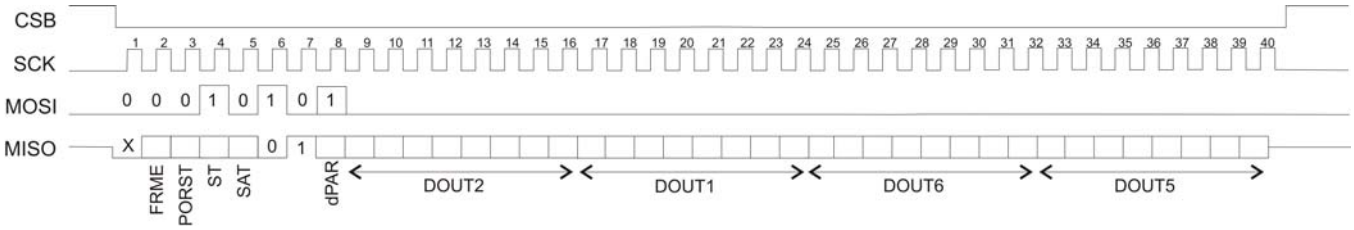


Figure 5: An example of decremented read operation.

4.1.3 MOSI data of SPI commands

Table 8: MOSI data during SPI read command

Register to be read	Function	MOSI (15:0) [bits]	MOSI [hex]
REVID	Read ASIC revision ID	000000 01 xxxxxxxx	01xx
CTRL	Read CTRL register	000001 00 xxxxxxxx	04xx
STATUS	Read Status register	000010 00 xxxxxxxx	08xx
X_LSB	Read acceleration on X-axis, LSB	000100 00 xxxxxxxx	10xx
X_MSB	Read acceleration on X-axis, MSB	000101 01 xxxxxxxx	15xx
Y_LSB	Read acceleration on Y-axis, LSB	000110 01 xxxxxxxx	19xx
Y_MSB	Read acceleration on Y-axis, MSB	000111 00 xxxxxxxx	1Cxx
Z_LSB	Read acceleration on Z-axis, LSB	001000 00 xxxxxxxx	20xx
Z_MSB	Read acceleration on Z-axis, MSB	001001 01 xxxxxxxx	25xx
TEMP_LSB	Read temperature, LSB	010010 01 xxxxxxxx	49xx
TEMP_MSB	Read temperature, MSB	010011 00 xxxxxxxx	4Cxx
INT_STATUS	Read INT_STATUS register	010110 00 xxxxxxxx	58xx
ID	Read product ID number	100111 01 xxxxxxxx	9Dxx

Table 9: MOSI data during write command

Register to be written	Function	MOSI (15:0) [bits]	MOSI [hex]
RESET	Reset component (data C'hex)	000011 10 00001100	0E0C
RESET	Reset component (data 5'hex)	000011 10 00000101	0E05
RESET	Reset component (data F'hex)	000011 10 00001111	0E0F
CTRL	Set PORST to zero	000001 11 00000000	0700
CTRL	Set chip to power down mode	000001 11 00100000	0720
CTRL	Start self-diagnostic	000001 11 00001000	0708
CTRL	Start memory self-test	000001 11 00000100	0704

4.2 Error Conditioning

4.2.1 FRME-bit

While sending a frame, if CSB is raised to 1 before sending 16 SCKs, the frame is considered invalid. In SCA8X0 the frame error is raised if number of SCK pulses is not 16. In SCA21X0/3100 the frame error is raised only if number of SCK pulses is not divisible by 8 to support decremented mode reading. When an invalid frame is received, the last command is simply ignored and the register contents are left unchanged. Status bit STATUS.FRME is set to indicate this error condition. During next SPI frame error bit send out as bit number 2. Bit STATUS.FRME will be reseted, if correct frame is received.

4.2.2 PORST-bit

PORST length is 1bit in SPI frame. PORST bit is set if chip is reseted (HW reset by POR or supply on/off) or under-voltage is detected. PORST bit is also set after power-up because chip has been in reset state. PORST can be set to zero (reseted) by writing CTRL.PORST =0. Software (SW) reset does not set PORST.
When CTRL.PORST bit is written to 0 via SPI, there is 300ns delay before register value is set to zero.

4.2.3 ST-bit (SCA21X0 / 3100)

Self-test frame status (ST) is set if STC or STS is alarmed or checksum is not passed.

- CASE 1: Checksum fails and ST-frame bit is set 1. ST is set back to zero when (and only if) new checksum calculation is passed.
- CASE 2: ST-frame bit is set because STC or STS is alarmed. In this case ST-frame bit can be cleared by INT_STATUS register reading.

ST bit is not defined in SCA8X0 series.

4.2.4 SAT-bit (SCA21X0 / 3100)

Saturation status (SAT) is set if any of axis xyz is saturated and it can be cleared by INT_STATUS register reading. This bit is kept active even failure condition is over if it is not acknowledged.

Saturation limit varies between different product types. For example:

- SCA2100 2 g product: x and y channel saturates to 2.27 g and SAT bit in SPI frame and in INT_STATUS register is set, if 2.27 g is exceeded. Additional to this, if acceleration to z-direction exceeds 4.54 g, SAT bit in SPI frame and in INT_STATUS register is set. In all cases INT_STATUS register reading is needed for acknowledgement and acceleration output data of any channel is not valid, when bit is active.
- SCA2110 2 g product: x and z channel saturates to 2.27 g and SAT bit in SPI frame and in INT_STATUS register is set, if 2.27 g is exceeded. Additional to this, if acceleration to y-direction exceeds 4.54 g, SAT bit in SPI frame and in INT_STATUS register is set. In all cases INT_STATUS register reading is needed for acknowledgement and acceleration output data of any channel is not valid, when bit is active.
- SCA2120 2 g product: y and z channel saturates to 2.27 g and SAT bit in SPI frame and in INT_STATUS register is set, if 2.27 g is exceeded. Additional to this, if acceleration to x-direction exceeds 4.54 g, SAT bit in SPI frame and in INT_STATUS register is set. In all cases INT_STATUS register reading is needed for acknowledgement and acceleration output data of any channel is not valid, when bit is active.

SAT bit is not defined in SCA8X0 series, but output saturates to the calibrated level. For example acceleration output data of SCA8x0 2 g products saturates to 2.27 g.

4.2.5 aPAR-bit (SCA21X0 / 3100)

aPAR is odd parity bit of input address+RB/W-bit. Master write it and slave check that bit.

- If there is parity error and RB/W='1', write command is ignored and frame error bit is set to STATUS-register and to SPI frame. Next correct SPI frame will zero this bit.
- If there is parity error and RB/W='0', read command is performed normally and frame error bit is set to STATUS-register and to SPI frame. Next correct SPI frame will zero this bit.

aPAR bit is not checked in SCA8X0 series.

Table 10: Address parity

Address								Notes
A5	A4	A3	A2	A1	A0	RB/W	aPAR	
0	0	0	0	0	0	0	**1**	correct frame
1	1	1	1	1	1	1	**0**	correct frame
1	0	1	0	1	0	1	**1**	correct frame
0	1	0	1	0	1	0	**0**	correct frame

4.2.6 dPAR-bit

dPAR bit is odd parity bit of 8bit data that is currently sent in the frame. Master checks this bit and compares to received data. Using dPAR at least one bit errors in data transmission can be detected.

4.2.7 Fixed bits

Bits 6 and 7 are always fixed in MISO line. Bit 6 should always be '0' and bit 7 always '1'

4.2.8 Output data

1. Reset stage: When component is in reset or under voltage state, PORST bit in SPI frame and CTRL.PORST bit is set. Furthermore, all register values are set to 00'hex.
2. Saturation: When acceleration exceeds measurement range, the output data is saturated to specified positive or negative full-scale.
3. Self-diagnostic failure: In SCA21X0 and 31X0 the ST bit in SPI frame is set when memory diagnostic or signal path diagnostic functions fail. Furthermore acceleration output data is forced to 7FFF'hex if memory diagnostic fails or to FFFF'hex if signal path diagnostic functions (STC/STS) fail.

5 Electrical Characteristics

All voltages are referenced to ground. Currents flowing into the circuit have positive values.

5.1 Absolute maximum ratings

The absolute maximum ratings of Digital Family are presented in Table 11 below.

Table 11: Absolute maximum ratings

Parameter	Value	Unit
Supply voltage (V_{dd})	-0.3 to +3.6	V
Voltage at input / output pins	-0.3 to (V_{dd} + 0.3)	V
ESD (Human body model)	±2	kV
Storage temperature	-40 ... +125	°C
Operating temperature	-40 ... +125	°C
Ultrasonic cleaning	Not allowed	

5.2 Power Supply

5.3 Digital I/O Specification

5.3.1 DC Characteristics

Supply voltage is 3.3 V unless otherwise noted. Current flowing into the circuit has positive values.

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
	Input terminal CSB						
1	Pull up current	V_{IN} = 0 V	I_{PU}	10		50	µA
2	Input high voltage	DVDD = 3.3 V	V_{IH}	2		DVDD	V
3	Input low voltage	DVDD = 3.3 V	V_{IL}			0.8	V
4	Hysteresis	DVDD = 3.3 V	V_{HYST}	0.18			V
	Input terminal MOSI, SCK						
5	Pull down current	V_{IN} = 3.3 V	I_{PD}	10		50	µA
6	Input high voltage	DVDD = 3.3 V	V_{IH}	2		DVDD	V
7	Input low voltage	DVDD = 3.3 V	V_{IL}			0.8	V
8	Hysteresis	DVDD = 3.3 V	V_{HYST}	0.18			V
	Output terminal MISO						
9	Output high voltage	I > -1mA DVDD = 3.3 V	V_{OH}	DVDD – 0.5			V
10	Output low voltage	I < 1 mA	V_{OL}			0.5	V
11	Tri-state leakage	0 < V_{MISO} < 3.3 V	I_{LEAK}	-3		3	uA

5.3.2 AC Characteristics

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
	Terminal CSB, SCK						
1	Time from CSB (10%) to SCK (90%)[1]		T_{LS1}	$T_{per}/2$			ns
2	Time from SCK (10%) to CSB (90%)[1]		T_{LS2}	$T_{per}/2$			ns
	Terminal SCK						
3	SCK low time	Load capacitance at MISO < 50 pF t_r=rise time t_f=fall time	T_{CL}	60	$T_{per}/2 – (t_r+t_f)/2$		ns
4	SCK high time	Load capacitance at MISO < 50 pF	T_{CH}	60	$T_{per}/2 – (t_r+t_f)/2$		ns

5	SCK Frequency		fsck = $1/T_{per}$		8	MHz
	Terminal MOSI, SCK					
6	Time from changing MOSI (10%, 90%) to SCK (90%)[1]. Data setup time		T_{SET}	$T_{per}/4$		ns
7	Time from SCK (90%) to changing MOSI (10%, 90%)[1]. Data hold time		T_{HOL}	$T_{per}/4$		ns
	Terminal MISO, CSB					
8	Time from CSB (10%) to stable MISO (10%, 90%)	Load capacitance at MISO < 50 pF	T_{VAL1}		$T_{per}/4$	ns
9	Time from CSB (90%) to high impedance state of MISO[1].	Load capacitance at MISO < 50 pF	T_{LZ}		$T_{per}/4$	ns
	Terminal MISO, SCK					
10	Time from SCK (10%) to stable MISO (10%, 90%)[1].	Load capacitance at MISO < 50 pF	T_{VAL2}		1.3 x $T_{per}/4$	ns
	Terminal CSB					
11	Time between SPI cycles, CSB at high level (90%)		T_{LH}	T_{per}		ns

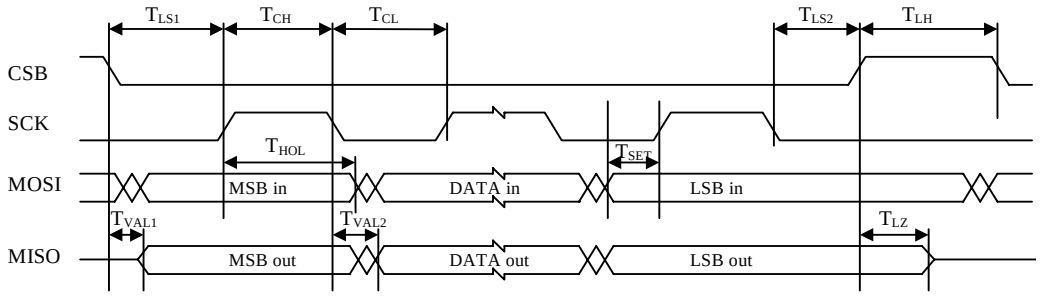


Figure 6: Timing diagram of SPI communication

6 Application information

6.1 Package dimensions

The package dimensions are presented in the Figure 7 below (measures in mm with ±0.1 mm tolerance). The part weights < 0.35 g.

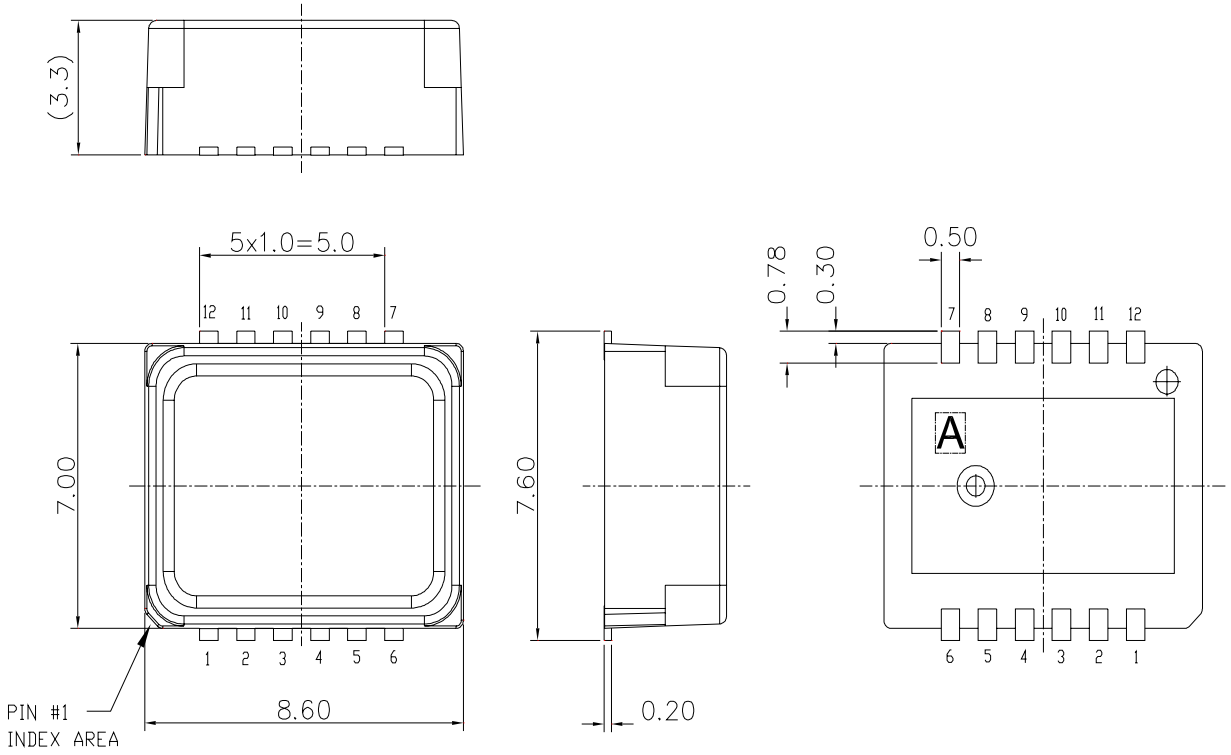


Figure 7: Package dimensions

6.2 Output to Angle Conversion

Product output is function of sin and it can be transferred to angle using the following equation for conversion:

$$\alpha = \arcsin\left(\frac{Output_{LSB} - Offset_{0g}}{Sensitivity}\right),$$

Where $Output_{LSB}$ is output in g, $Offset_{0g}$ is offset at 0 g position and sensitivity is sensitivity of product. Nominal sensitivity is determined at datasheet of product and 0 g can be used in $Offset_{0g}$ if not measured after installation. To read output of product refer chapter Output Data Conversion.

Angles close to 0° inclination can be estimated quite accurately with straight line conversion but for the best possible accuracy, arcsine conversion is recommended to be used. The following table shows the angle measurement error if straight line conversion is used.

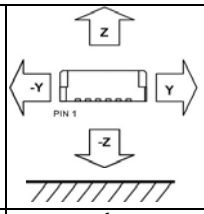
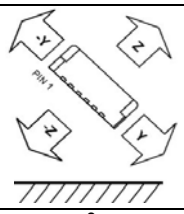
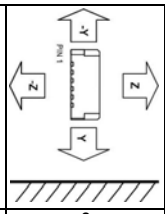
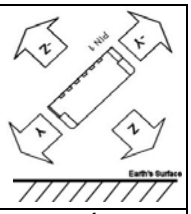
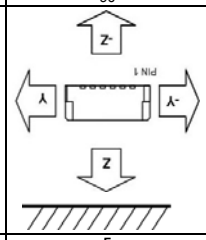
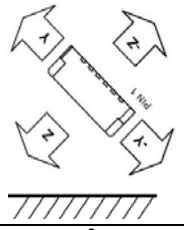
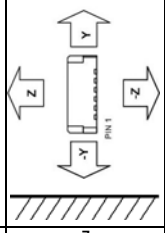
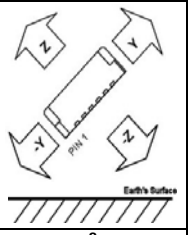
Straight line conversion equation:

$$\alpha = \left(\frac{Output_{LSB} - Offset_{0g}}{Sensitivity}\right),$$

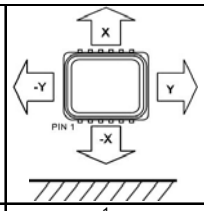
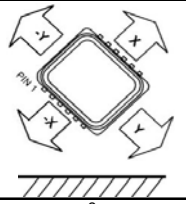
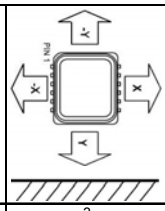
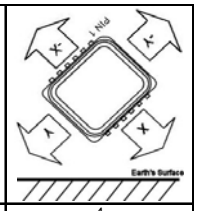
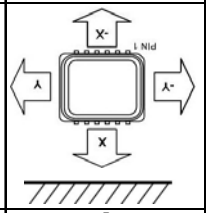
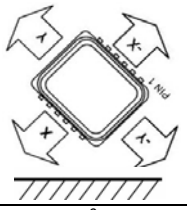
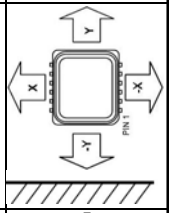
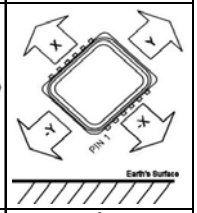
Where $Output_{LSB}$ is output in g, $Offset_{0g}$ is offset at 0 g position and sensitivity is sensitivity of product.

Tilt angle [°]	Straight line conversion error [°]
0	0
1	0.0027
2	0.0058
3	0.0094
4	0.0140
5	0.0198
10	0.0787
15	0.2185
30	1.668

6.3 Measuring Directions

				
	1	**2**	**3**	**4**
X [mg]	0	0	0	0
ARCSIN(X) [°]	0	0	0	0
Y [mg]	0	-707	-1000	-707
ARCSIN(Y) [°]	0	-45	-90	-45
Z [mg]	1000	707	0	-707
ARCSIN(Z) [°]	90	45	0	-45
				
	5	**6**	**7**	**8**
X [mg]	0	0	0	0
ARCSIN(X) [°]	0	0	0	0
Y [mg]	0	707	1000	707
ARCSIN(Y) [°]	0	45	90	45
Z [mg]	-1000	-707	0	707
ARCSIN(Z) [°]	-90	-45	0	45

Measuring direction of Z and Y axis of ADP-product and output in mg and degree

				
	1	2	3	4
X [mg]	1000	707	0	-707
ARCSIN(X) [°]	90	45	0	-45
Y [mg]	0	-707	-1000	-707
ARCSIN(Y) [°]	0	-45	-90	-45
Z [mg]	0	0	0	0
ARCSIN(Z) [°]	0	0	0	0
				
	5	6	7	8
X [mg]	-1000	-707	0	707
ARCSIN(X) [°]	-90	-45	0	45
Y [mg]	0	707	1000	707
ARCSIN(Y) [°]	0	45	90	45
Z [mg]	0	0	0	0
ARCSIN(Z) [°]	0	0	0	0

Measuring direction of Z and Y axis of ADP-product and output in mg and degree

6.4 Pin Description

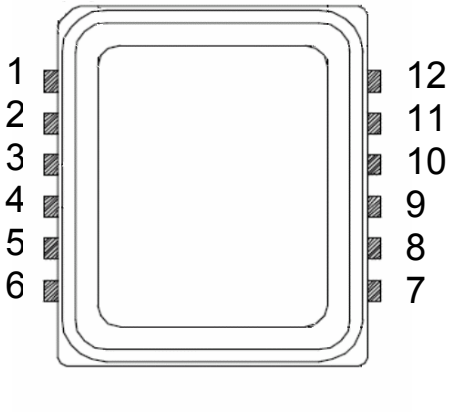


Figure 8: Component pinout

Table 12: Component pinout

No.	Name	Type [1]	PD/PU [2]	Function	Connect
1	Reserved			Not used	Gnd
2	Reserved		PD	Factory use	Gnd
3	AVSS	AI		Negative power supply (analog)	Gnd
4	AVDD	AI		Positive power supply (analog)	Vdd
5	CSB	DI	PU	Chip select	CSB
6	MISO	ZO		Data output	MISO
7	SCK	DI	PD	Serial clock	SCK
8	MOSI	DI	PD	Data input	MOSI
9	PWM	ADO	PD	Pulse Width Modulation output	N.C. or PWM [3]
10	DVDD	AI		Positive power supply (digital)	Vdd
11	DVSS	AI		Negative power supply (digital)	Gnd
12	EGnd	AI		EMC ground	Gnd

Notes:
1) A=Analog, D=Digital, I=Input, O=Output, Z=Tristate Output
2) PU=internal pullup, PD=internal pulldown
3) PWM output in some SCA8X0 products, N.C.= Not Connected

6.5 Recommended circuit diagram

Recommended circuit diagram for all product family components with SPI interface is shown in Figure 9. Following design rules and recommendations should be considered to achieve maximum performance:

Required:
1 Connect (C4) 100 nF (ESR < 1) capacitor between AVDD and AVSS
2 Connect (C5) 100 nF (ESR < 1) capacitor between DVDD and DVSS
3 Use one power supply VDD for AVDD and DVDD (AVDD voltage level has to be raised always same time or after DVDD during power up sequence)

Recommended for improved PSRR (Note 1 in Figure 9):
4 Connect (C6) 10 µF capacitor between AVDD and AVSS
5 Connect serial resistance (R1) 10 Ω between VDD and AVDD/DVDD

- Specified operation voltage (VDD) range 3.05...3.6 V

6 To achieve high EMC DPI performance, add serial inductance (L1) to VDD line before serial resistance (for example Murata: BLM18HG102S)

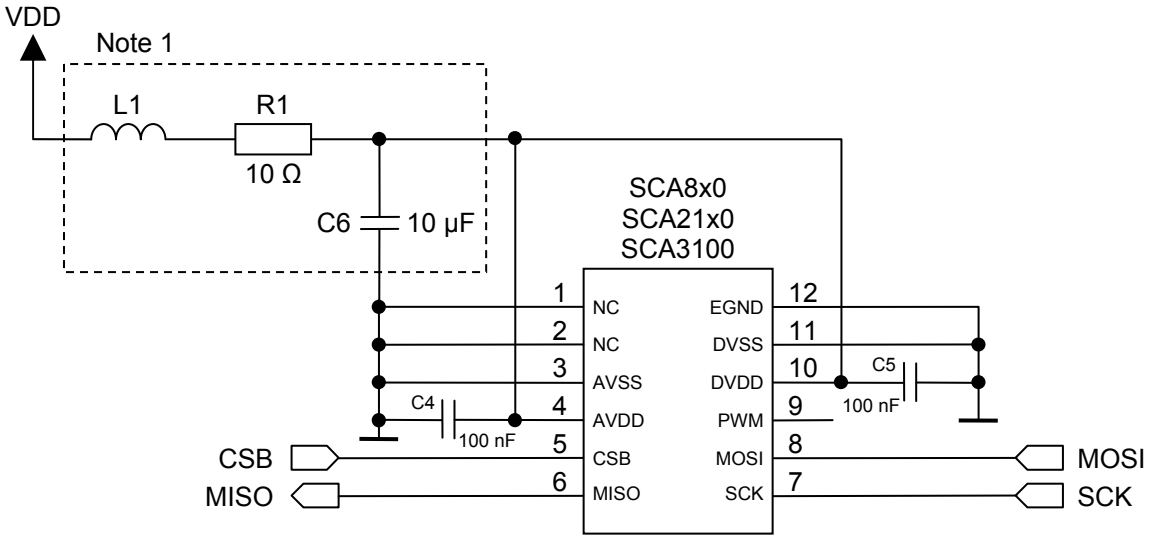


Figure 9: Recommended circuit diagram

6.6 Recommended PWB layout

Recommended PWB layout for all product family components with SPI interface is shown in Figure 10 and Figure 11. Following design rules and recommendations should be considered:

Required:

1 Connect (C4) 100 nF SMD capacitor between AVDD and AVSS right next to component pins AVDD and AVSS
2 Connect (C5) 100 nF SMD capacitor between DVDD and DVSS right next to component pins DVDD and DVSS
3 Use separate ground levels AVSS and DVSS under and near the component but connect them together on the PCB, see Figure 10
4 Locate ground plate under component
5 Do not route signals or power supplies under the component on top layer
6 Ensure good ground connection of Egnd (pin12) to AVSS

Recommended:

7 Locate digital ground under digital signal lines
8 Do not route digital signals one upon the other for long distance
9 Avoid crossing of AVDD path with digital signal especially between serial resistance R1 and AVDD pin
10 Do not route digital signals under the component on 2nd layer

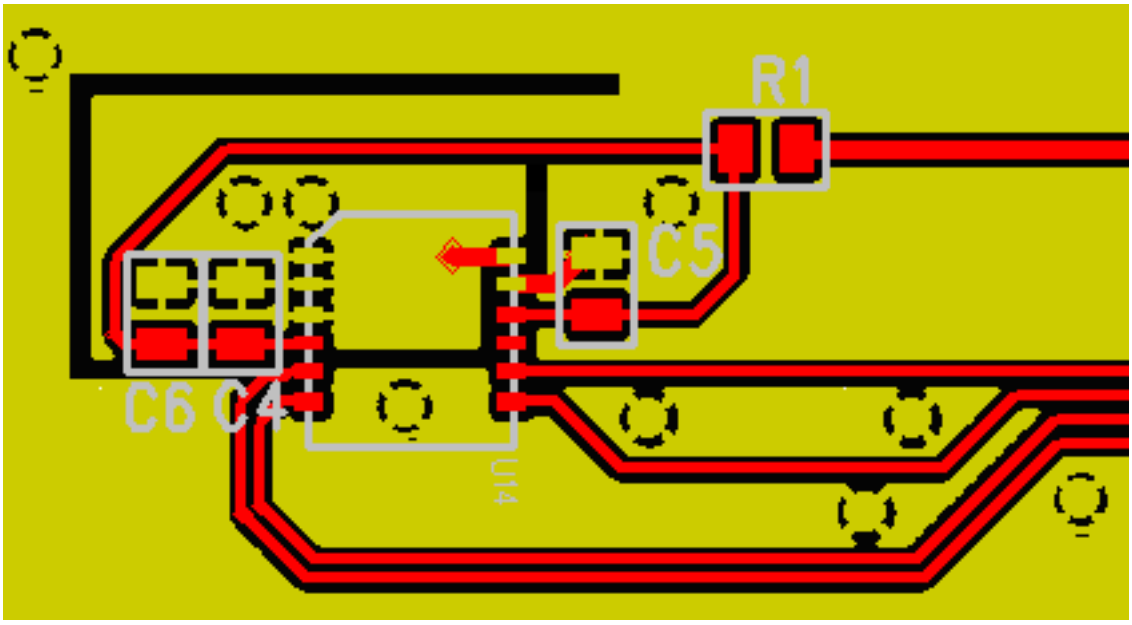


Figure 10: Recommended PWB layout for product family components with SPI interface (Top layer, Not actual size, for reference only)

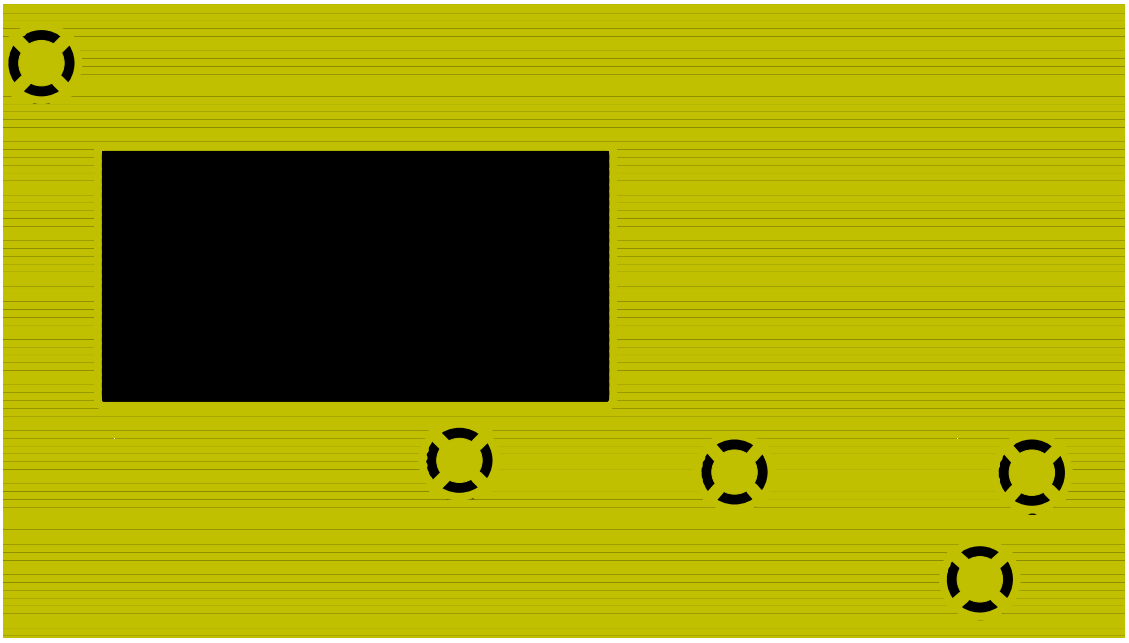


Figure 11: Recommended PWB layout for product family components with SPI interface (2nd layer, Not actual size, for reference only)

Recommended PWB pad layout is presented in the Figure 12 below (dimensions in mm).

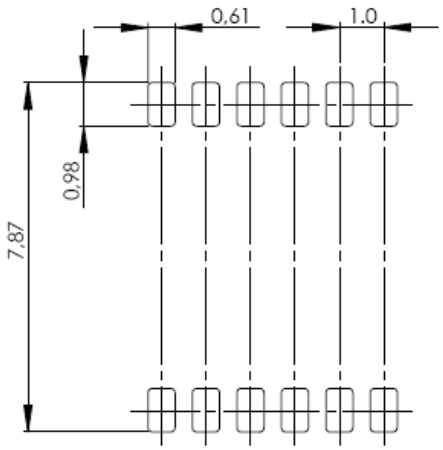


Figure 12: Component pad layout

6.7 Assembly instructions

The Moisture Sensitivity Level (MSL) of the component is 3 according to the IPC/JEDEC J-STD-020C. Please refer to the document "TN53 Assembly Instructions for Dual Flat Lead Package" for more detailed information of the assembly.

6.8 Tape and reel specifications

Please refer to the document "TN53 Assembly Instructions for Dual Flat Lead Package" for tape and reel specifications.

7 Contact Information

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