

N- AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

MTC4503Q8

Description

The MTC4503Q8 consists of a N-channel and a P-channel enhancement-mode MOSFET in a single SOP-8 package, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOP-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

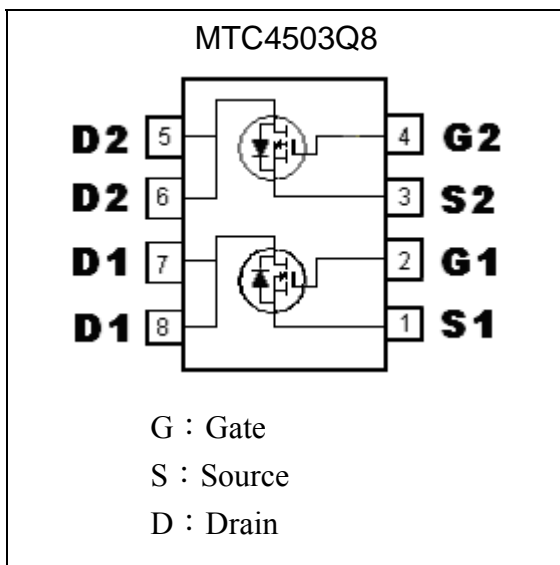
Features

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free package

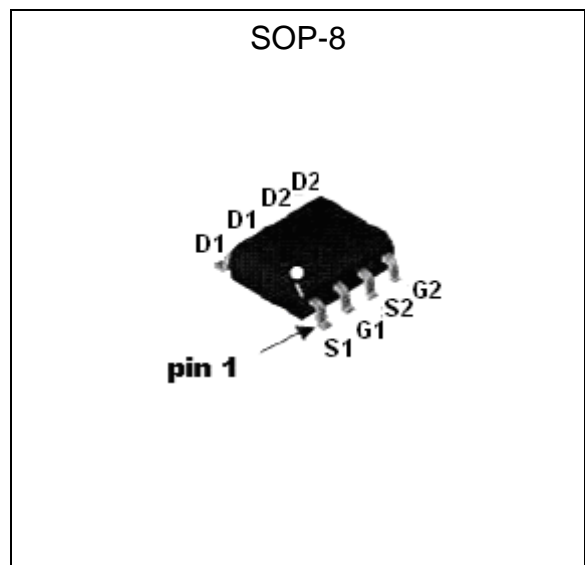
Applications

- Power management in notebook computer, portable equipment and battery powered systems.

Equivalent Circuit



Outline





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		N-channel	P-channel	
Drain-Source Breakdown Voltage	BV _{DSS}	30	-30	V
Gate-Source Voltage	V _{GS}	±20	±20	V
Continuous Drain Current @T _A =25 °C (Note 1)	I _D	6.9	-6.3	A
Continuous Drain Current @T _A =70 °C (Note 1)	I _D	5.5	-5.0	A
Pulsed Drain Current (Note 2)	I _{DM}	30	-30	A
Total Power Dissipation (Note 1)	P _d	2		W
Linear Derating Factor		0.016		W / °C
Operating Junction Temperature	T _j	-55~+150		°C
Storage Temperature	T _{stg}	-55~+150		°C
Thermal Resistance, Junction-to-Ambient (Note 1)	R _{th,ja}	62.5		°C/W

Note : 1.Surface mounted on 1 in² copper pad of FR-4 board, 135°C/W when mounted on minimum copper pad
 2.Pulse width limited by maximum junction temperature

N-Channel Electrical Characteristics (T_j=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	0.005	-	V/°C	Reference to 25°C, I _D =1mA
V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0
I _{DSS}	-	-	1	μA	V _{DS} =30V, V _{GS} =0
I _{DSS}	-	-	25	μA	V _{DS} =24V, V _{GS} =0, T _j =70°C
*R _{DS(ON)}	-	-	28	mΩ	I _D =6A, V _{GS} =10V
	-	-	42		I _D =4A, V _{GS} =4.5V
*G _{FS}	-	5.7	-	S	V _{DS} =10V, I _D =6A
Dynamic					
C _{iss}	-	610	970	pF	V _{DS} =25V, V _{GS} =0, f=1MHz
C _{oss}	-	160	-		
C _{rss}	-	120	-		
*t _{d(ON)}	-	8	-	ns	V _{DS} =15V, I _D =1A, V _{GS} =10V, R _G =3.3Ω, R _D =15Ω
*t _r	-	7	-		
*t _{d(OFF)}	-	19	-		
*t _f	-	6	-		
*Q _g	-	9	15	nC	V _{DS} =24V, I _D =6A, V _{GS} =4.5V
*Q _{gs}	-	2	-		
*Q _{gd}	-	6	-		
Source-Drain Diode					
*V _{SD}	-	-	1.2	V	V _{GS} =0V, I _S =6A
*t _{rr}	-	18	-	ns	I _S =6A, V _{GS} =0V, dI/dt=100A/μs
*Q _{rr}	-	11	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%



P-Channel Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-30	-	-	V	V _{GS} =0, I _D =-250μA
ΔBV _{DSS} /ΔT _j	-	-0.004	-	V/°C	Reference to 25°C, I _D =-1mA
V _{GS(th)}	-1.0	-	-3.0	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0
I _{DSS}	-	-	-1	μA	V _{DS} =-30V, V _{GS} =0
I _{DSS}	-	-	-25	μA	V _{DS} =-24V, V _{GS} =0, T _j =70°C
*R _{DS(ON)}	-	-	36	mΩ	I _D =-6A, V _{GS} =-10V
	-	-	55		I _D =-4A, V _{GS} =-4.5V
*G _{FS}	-	5.8	-	S	V _{DS} =-10V, I _D =-6A
Dynamic					
C _{iss}	-	960	1540	pF	V _{DS} =-25V, V _{GS} =0, f=1MHz
C _{oss}	-	300	-		
C _{rss}	-	220	-		
*t _{d(ON)}	-	12	-	ns	V _{DS} =-15V, I _D =-1A, V _{GS} =-10V, R _G =3.3Ω, R _D =15Ω
*t _r	-	8	-	ns	
*t _{d(OFF)}	-	42	-	ns	
*t _f	-	34	-	ns	
*Q _g	-	15	24	nC	V _{DS} =-24V, I _D =-6A, V _{GS} =-4.5V
*Q _{gs}	-	3	-	nC	
*Q _{gd}	-	9	-	nC	
Source-Drain Diode					
*V _{SD}	-	-	-1.2	V	V _{GS} =0V, I _S =-6A
*t _{rr}	-	24	-	ns	I _S =-6A, V _{GS} =0V, dI/dt=100A/μs
*Q _{rr}	-	18	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%

N-channel Characteristic Curves

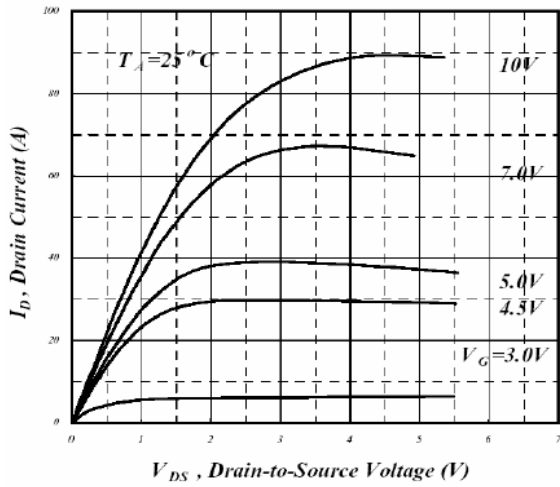


Fig 1. Typical Output Characteristics

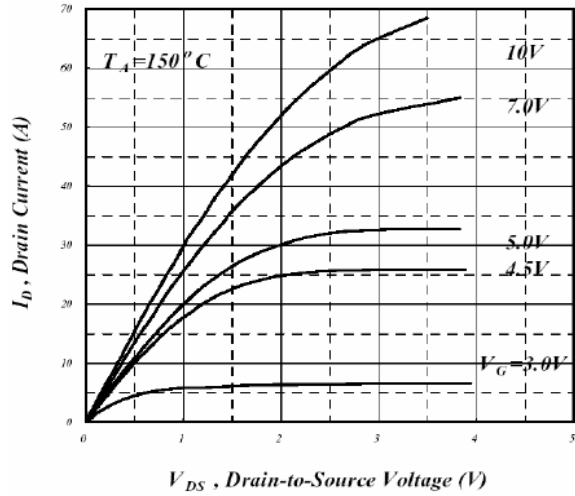


Fig 2. Typical Output Characteristics

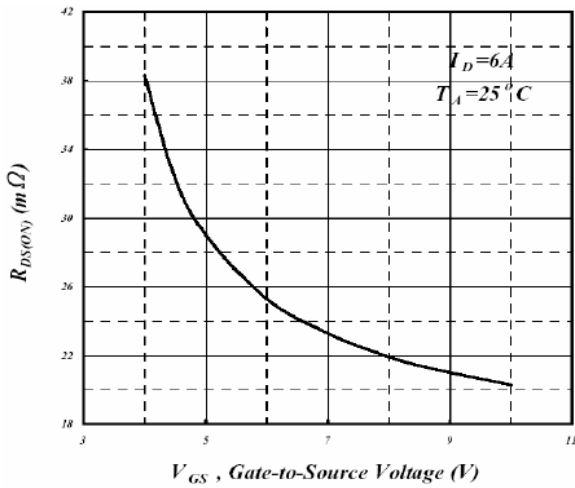


Fig 3. On-Resistance v.s. Gate Voltage

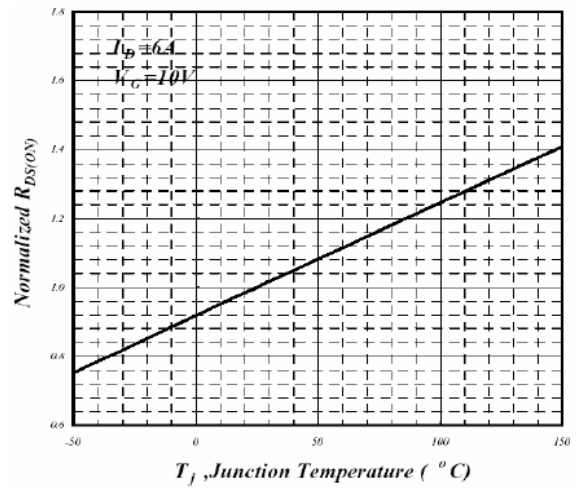


Fig 4. Normalized On-Resistance v.s. Junction Temperature

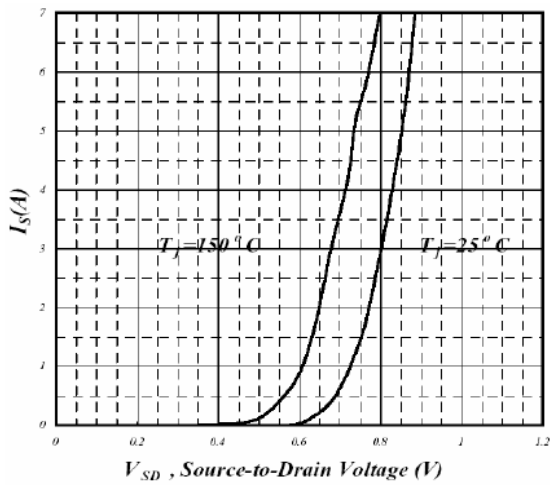


Fig 5. Forward Characteristics of Reverse Diode

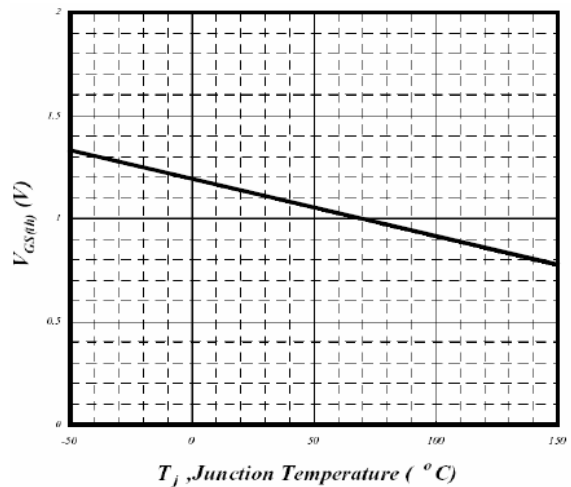


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-channel Characteristic Curves(Cont.)

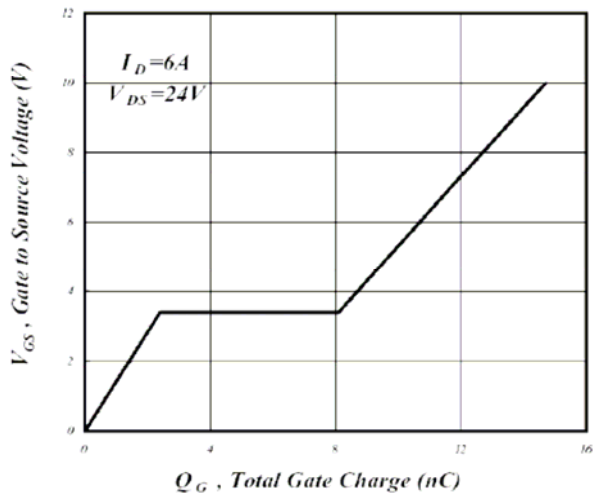


Fig 7. Gate Charge Characteristics

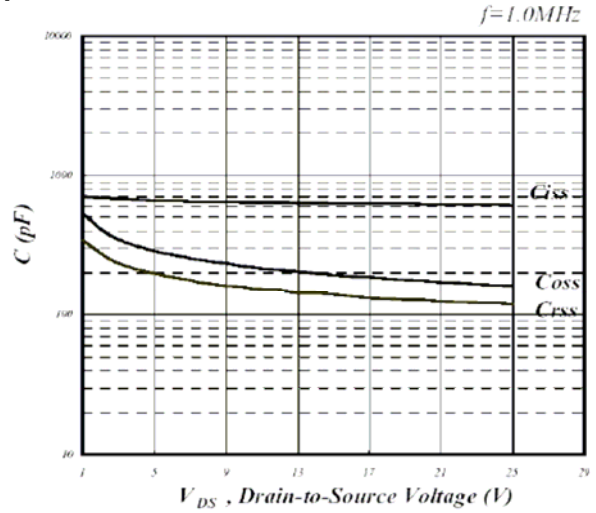


Fig 8. Typical Capacitance Characteristics

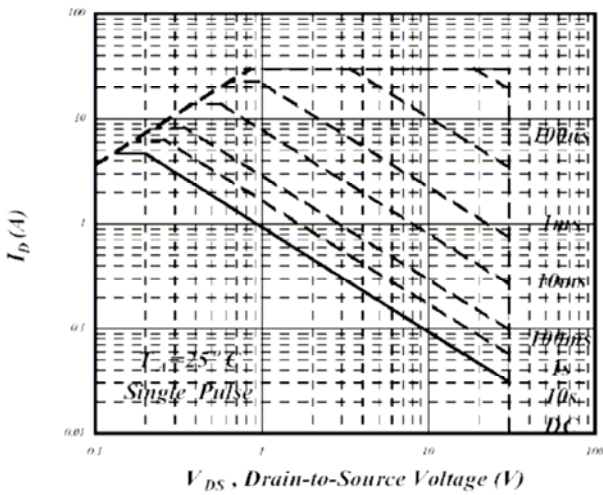


Fig 9. Maximum Safe Operating Area

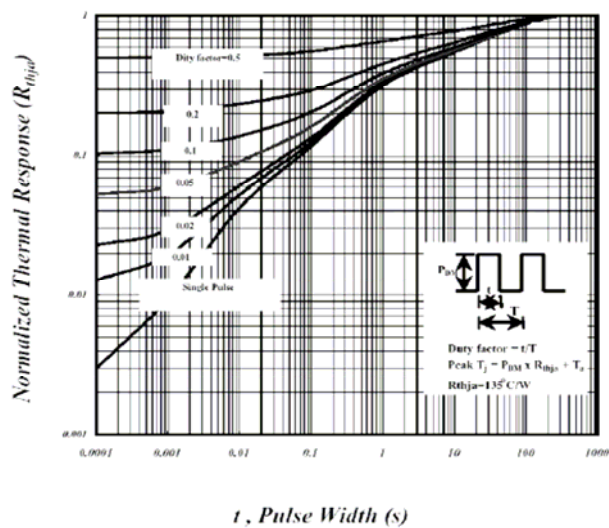


Fig 10. Effective Transient Thermal Impedance

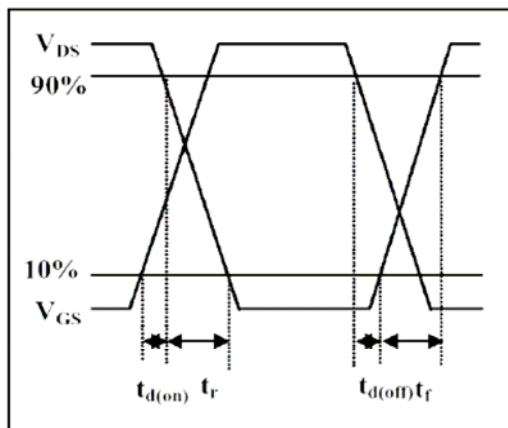


Fig 11. Switching Time Waveform

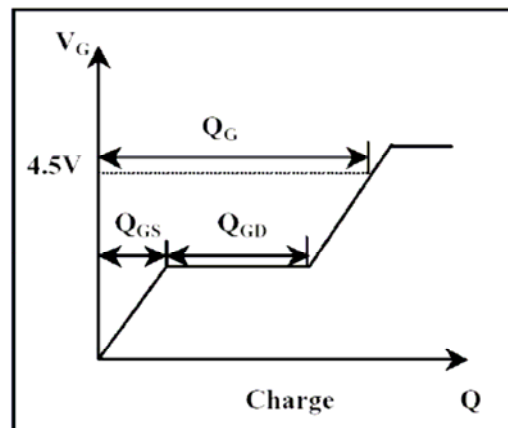


Fig 12. Gate Charge Waveform

P-channel Characteristic Curves

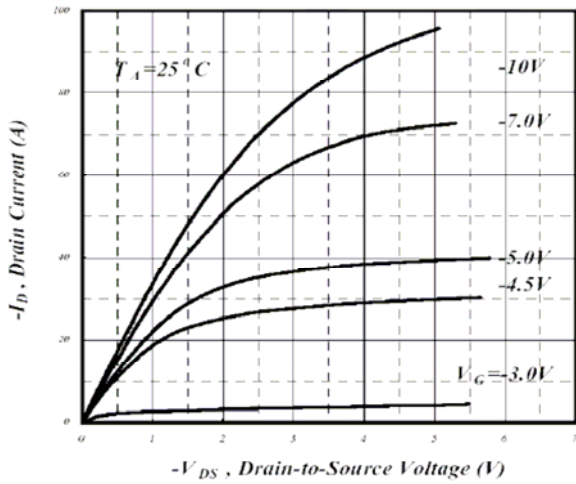


Fig 1. Typical Output Characteristics

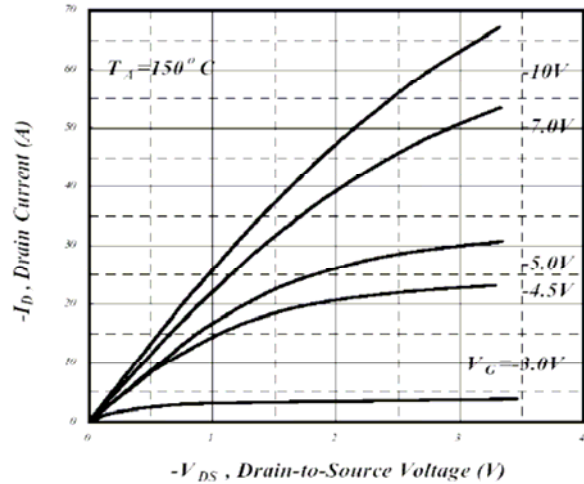


Fig 2. Typical Output Characteristics

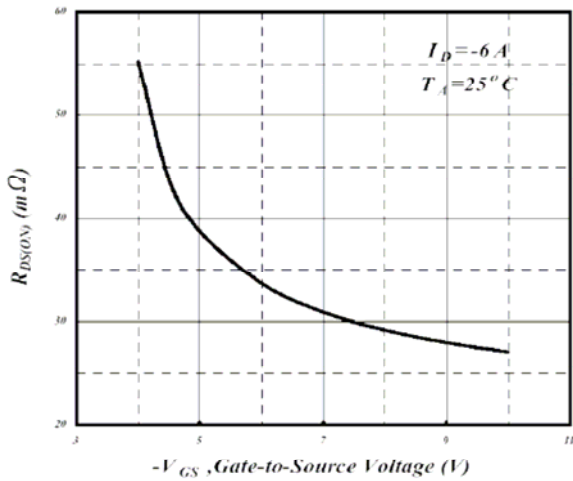


Fig 3. On-Resistance v.s. Gate Voltage

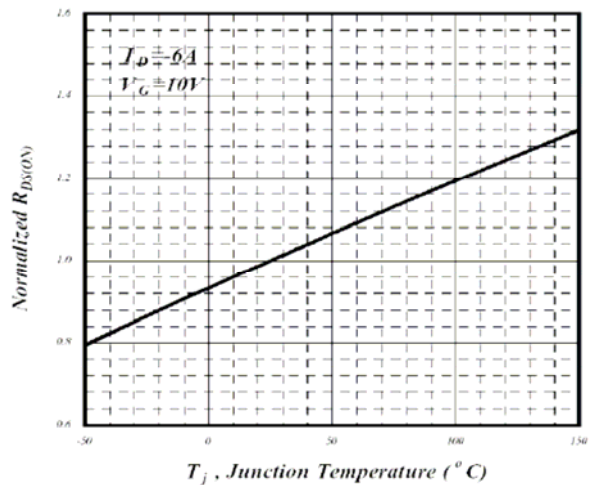


Fig 4. Normalized On-Resistance v.s. Junction Temperature

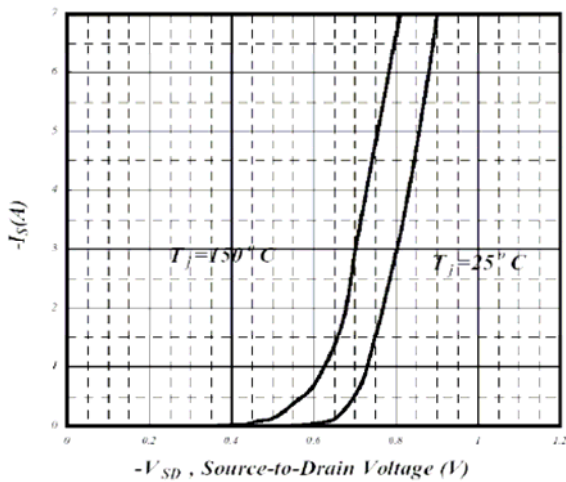


Fig 5. Forward Characteristics of Reverse Diode

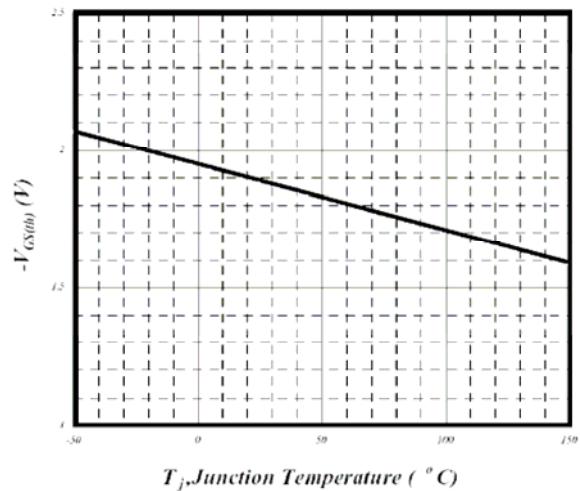


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-channel Characteristic Curves(Cont.)

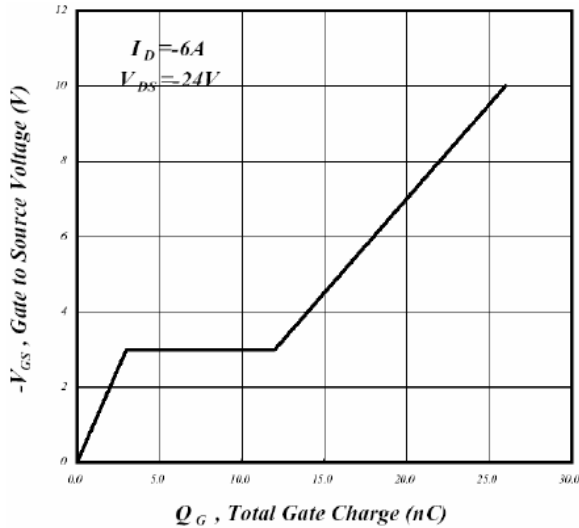


Fig 7. Gate Charge Characteristics

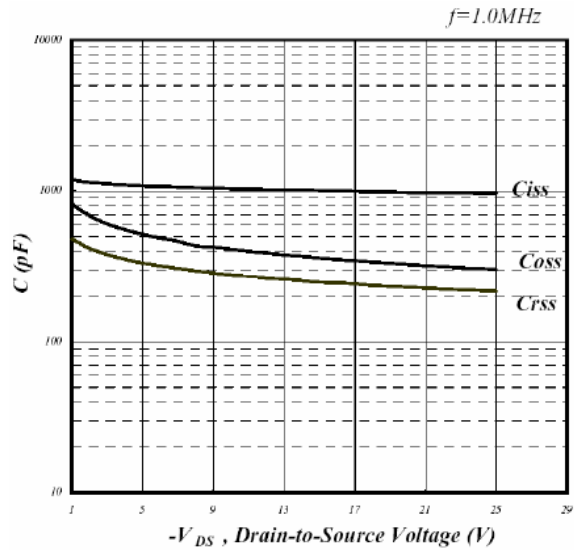


Fig 8. Typical Capacitance Characteristics

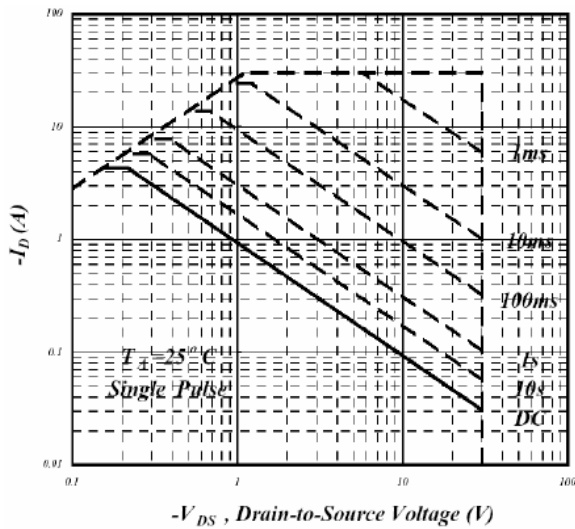


Fig 9. Maximum Safe Operating Area

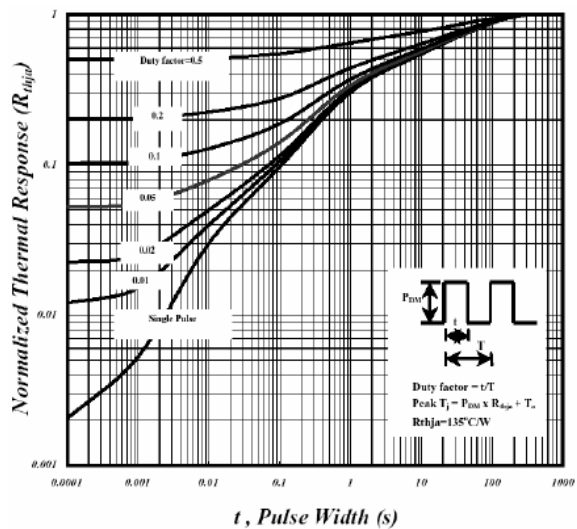


Fig 10. Effective Transient Thermal Impedance

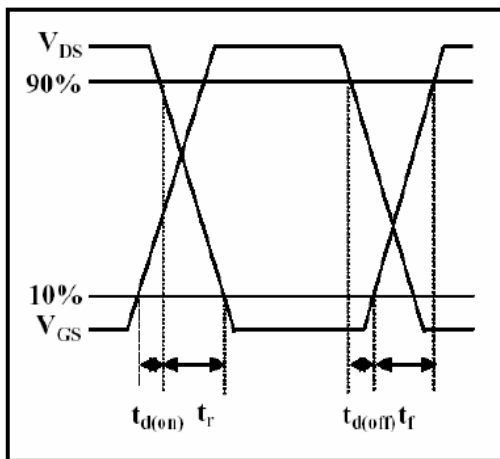


Fig 11. Switching Time Waveform

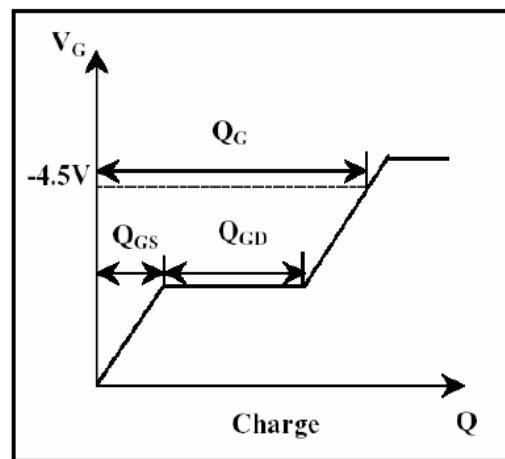
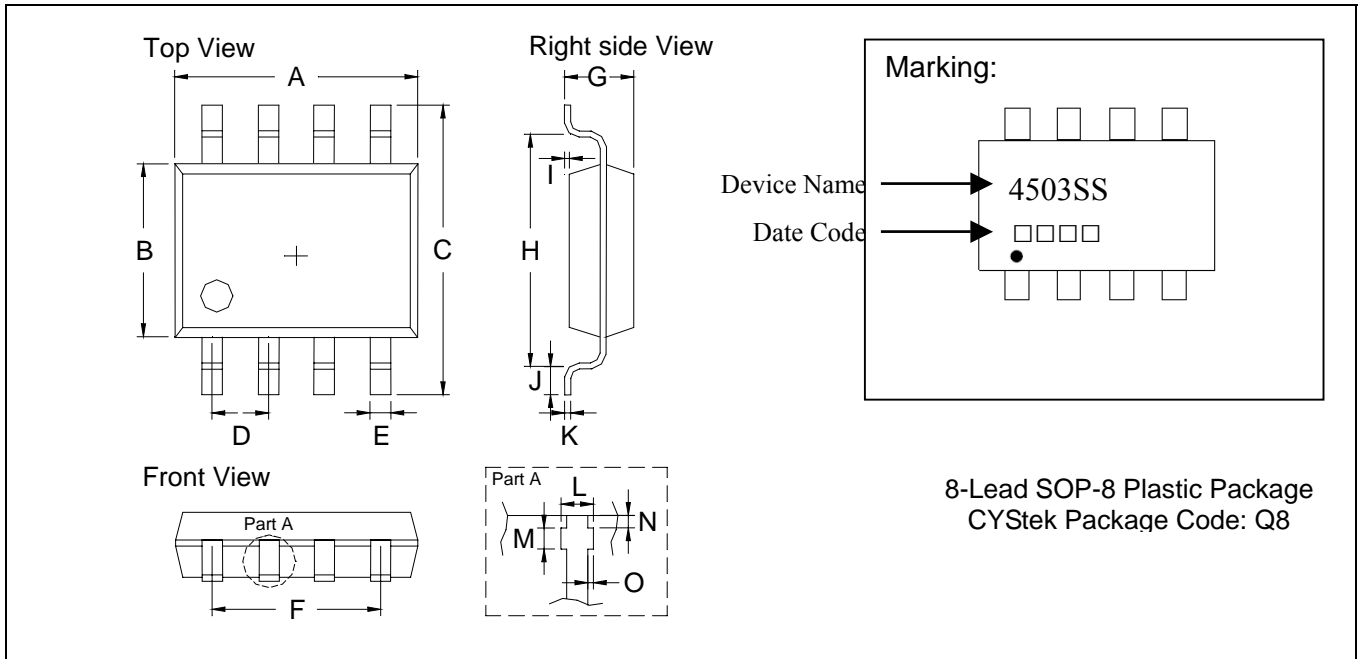


Fig 12. Gate Charge Waveform

SOP-8 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

- Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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