

Preliminary DATASHEET

Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group RENESAS MCU

REJ03B0317-0010 Rev.0.10 May 31, 2010

1. Overview

1.1 Features

The R8C/38W Group, R8C/38X Group, R8C/38Y Group, and R8C/38Z Group of single-chip MCUs incorporate the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

The R8C/38W Group and R8C/38X Group have a single channel CAN module and are suitable for LAN systems in vehicles and for FA.

The R8C/38Y Group and R8C/38Z Group do not have CAN modules.

The R8C/38W Group and R8C/38Y Group have data flash (1 KB \times 4 blocks) with the background operation (BGO) function.

1.1.1 Applications

Automobiles and others

1.1.2 Specifications

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

Tables 1.1 and 1.2 outline the Specifications for R8C/38W Group, tables 1.3 and 1.4 outline the Specifications for R8C/38X Group, tables 1.5 and 1.6 outline the Specifications for R8C/38Y Group, and tables 1.7 and 1.8 outline the Specifications for R8C/38Z Group.

Table 1.1 Specifications for R8C/38W Group (1)

Item	Function	Specification			
CPU	Central processing	R8C CPU core			
	unit	Number of fundamental instructions: 89			
		Minimum instruction execution time:			
		50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)			
		 Multiplier: 16 bits x 16 bits → 32 bits 			
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits 			
		Operating mode: Single-chip mode (address space: 1 Mbyte)			
Memory	ROM, RAM, Data	Refer to Table 1.9 Product List for R8C/38W Group.			
	flash				
Power Supply	Voltage detection	Power-on reset			
Voltage	circuit	Voltage detection 3 (detection level of voltage detection 1 selectable)			
Detection					
I/O Ports	Programmable I/O	Input-only: 1 pin			
	ports	CMOS I/O ports: 75, selectable pull-up resistor			
Clock Clock generation		3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),			
	circuits	High-speed on-chip oscillator (with frequency adjustment function),			
		Low-speed on-chip oscillator			
		Oscillation stop detection: XIN clock oscillation stop detection function			
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16			
		Low power consumption modes:			
		Standard operating mode (high-speed clock, high-speed on-chip oscillator,			
		low-speed on-chip oscillator), wait mode, stop mode			
Interrupts		Interrupt vectors: 69			
		• External: 9 sources (INT x 5, key input x 4)			
		Priority levels: 7 levels			
Watchdog Timer		14 bits x 1 (with prescaler)			
		Reset start selectable			
		Low-speed on-chip oscillator for watchdog timer selectable			
DTC (Data Tra	insfer Controller)	• 1 channel			
		Activation sources: 40			
		Transfer modes: 2 (normal mode, repeat mode)			

Table 1.2 Specifications for R8C/38W Group (2)

Table 1.2		Charification			
Item	Function	Specification			
Timer	Timer RA0	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period			
		measurement mode			
	Timer RA1	8 bits (with 8-bit prescaler) × 1			
	Timer NAT	Timer mode (period timer), pulse output mode (output level inverted every			
		period), event counter mode, pulse width measurement mode, pulse period measurement mode			
	Timer RB	8 bits (with 8-bit prescaler) x 1 Timer mode (period timer), programmable waveform generation mode (PWM			
		output), programmable one-shot generation mode, programmable wait one-			
	T: D0	shot generation mode			
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode			
	Timer DD	(output 3 pins), PWM2 mode (PWM output pin)			
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms			
		(6 pins), sawtooth wave modulation), complementary PWM mode (output			
		three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)			
	Timer RE	8 bits x 1 Output compare mode			
	Timer RF	16 bits x 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)			
	Timer RG	16 bits x 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)			
Serial Interface	UART0, 1	2 channels Clock synchronous serial I/O, UART			
	UART2	1 channel Clock synchronous serial I/O, UART, I ² C mode (I ² C-bus), IE mode (IEbus), multiprocessor communication function			
Synchronous Communicati	Serial on Unit (SSU)	1 channel			
LIN Module	· /	Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)			
CAN Module		1 channel, 16 Mailboxes (conforms to the ISO 11898-1)			
A/D Converte	er	10-bit resolution × 20 channels, includes sample and hold function, with sweep mode			
Flash Memor	у	Programming and erasure voltage: VCC = 2.7 to 5.5 V			
		Programming and erasure endurance: 10,000 times (data flash)			
		1,000 times (program ROM)			
		Program security: ROM code protect, ID code check			
		Debug functions: On-chip debug, on-board flash rewrite function			
		Background operation (BGO) function (data flash)			
Operating Free Voltage	equency/Supply	f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)			
Current Cons		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)			
Operating An	nbient Temperature	-40 to 85°C (J version) -40 to 125°C (K version) (1)			
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)			
		1 . 25.25 5555.1 24. 5555.12 / (provided 6566. 661 64 /)			



Table 1.3 Specifications for R8C/38X Group (1)

Item				
CPU	Central processing	R8C CPU core		
	unit	Number of fundamental instructions: 89		
		Minimum instruction execution time:		
		50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)		
		Multiplier: 16 bits × 16 bits → 32 bits		
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits 		
		Operating mode: Single-chip mode (address space: 1 Mbyte)		
Memory	ROM, RAM, Data	Refer to Table 1.10 Product List for R8C/38X Group.		
-	flash	·		
Power Supply	Voltage detection	Power-on reset		
Voltage	circuit	Voltage detection 3 (detection level of voltage detection 1 selectable)		
Detection				
I/O Ports	Programmable I/O	Input-only: 1 pin		
	ports	CMOS I/O ports: 75, selectable pull-up resistor		
Clock Clock generation circuits		3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),		
		High-speed on-chip oscillator (with frequency adjustment function),		
		Low-speed on-chip oscillator		
		Oscillation stop detection: XIN clock oscillation stop detection function		
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16		
		Low power consumption modes:		
		Standard operating mode (high-speed clock, high-speed on-chip oscillator,		
		low-speed on-chip oscillator), wait mode, stop mode		
Interrupts		Interrupt vectors: 69		
		• External: 9 sources (INT × 5, key input × 4)		
		Priority levels: 7 levels		
Watchdog Timer		• 14 bits x 1 (with prescaler)		
		Reset start selectable		
		Low-speed on-chip oscillator for watchdog timer selectable		
DTC (Data Tra	insfer Controller)	• 1 channel		
		Activation sources: 40		
		Transfer modes: 2 (normal mode, repeat mode)		

Table 1.4 Specifications for R8C/38X Group (2)

Item	
Timer RA1 Timer RA3 Timer RA3 Timer RA4 Timer RA4 Timer RA5 Timer RB Timer RC Timer RC Timer RC Timer RC Timer RC Timer RD Timer RD	
period), event counter mode, pulse width measurement mode, pulse measurement mode Timer RA1 8 bits (with 8-bit prescaler) x 1 Timer mode (period timer), pulse output mode (output level inverted period), event counter mode, pulse width measurement mode, pulse measurement mode Timer RB 8 bits (with 8-bit prescaler) x 1 Timer mode (period timer), programmable waveform generation mootput), programmable one-shot generation mode, programmable via shot generation mode Timer RC 16 bits (with 4 capture/compare registers) x 1 Timer mode (input capture function, output compare function), PWM (output 3 pins), PWM2 mode (PWM output pin) Timer RD 16 bits (with 4 capture/compare registers) x 2 Timer mode (input capture function, output compare function), PWM (output 6 pins), reset synchronous PWM mode (output three-phase (6 pins), sawtooth wave modulation), complementary PWM mode (very my mode) (PWM output 2 pins with fixed period) Timer RE 8 bits x 1 Output compare mode Timer RF 16 bits x 1 Output compare mode Timer RF 16 bits x 1 Timer mode (input capture circuit), output compare mode (or compare circuit) Timer RG 16 bits x 1 Output capture function, output compare function), PWM (output 1 pin), phase counting mode (available automatic measurem counts of 2-phase encoder) Serial Interface UARTO, 1 2 channels Clock synchronous serial I/O, UART UART2 1 channel Clock synchronous serial I/O, UART, I2C mode (I2C-bus), IE mode multiprocessor communication function Synchronous Serial Communication Unit (SSU)	everv
Timer RA1 Timer RA1 8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted period), event counter mode, pulse width measurement mode, pulse measurement mode 1 Timer RB 8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable with shot generation mode 16 bits (with 4 capture/compare registers) × 1 Timer RD 16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM (PWM output 2 pins with fixed period) Timer RE	
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(6 pins), sawtooth wave modulation), complementary PWM mode (contraction) three-phase waveforms (6 pins), triangular wave modulation), PWM (PWM output 2 pins with fixed period) Timer RE 8 bits × 1 Output compare mode Timer RF 16 bits × 1 Input capture mode (input capture circuit), output compare mode (or compare circuit) Timer RG 16 bits × 1 Timer mode (input capture function, output compare function), PWM (output 1 pin), phase counting mode (available automatic measurem counts of 2-phase encoder) Serial Interface UARTO, 1 2 channels Clock synchronous serial I/O, UART UART2 1 channel Clock synchronous serial I/O, UART, I2C mode (I2C-bus), IE mode multiprocessor communication function Synchronous Serial Communication Unit (SSU)	
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Timer RE 8 bits x 1	3 mode
Output compare mode Timer RF 16 bits × 1	
Input capture mode (input capture circuit), output compare mode (or compare circuit) Timer RG 16 bits × 1 Timer mode (input capture function, output compare function), PWN (output 1 pin), phase counting mode (available automatic measurem counts of 2-phase encoder) Serial Interface UARTO, 1 2 channels Clock synchronous serial I/O, UART UART2 1 channel Clock synchronous serial I/O, UART, I²C mode (I²C-bus), IE mode multiprocessor communication function Synchronous Serial Communication Unit (SSU)	
Compare circuit	
Timer mode (input capture function, output compare function), PWM (output 1 pin), phase counting mode (available automatic measurem counts of 2-phase encoder) Serial Interface UARTO, 1 2 channels Clock synchronous serial I/O, UART UART2 1 channel Clock synchronous serial I/O, UART, I²C mode (I²C-bus), IE mode multiprocessor communication function Synchronous Serial Communication Unit (SSU)	ıtput
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Synchronous Serial 1 channel Communication Unit (SSU)	
Communication Unit (SSU)	IEbus),
LIN Module Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)	
CAN Module 1 channel, 16 Mailboxes (conforms to the ISO 11898-1)	
A/D Converter 10-bit resolution × 20 channels, includes sample and hold function, wi	th sweep
mode	
Flash Memory • Programming and erasure voltage: VCC = 2.7 to 5.5 V	
Programming and erasure endurance: 100 times (program ROM)	
Program security: ROM code protect, ID code check Pateur functions: On a big delayer and fleet requires functions.	
Debug functions: On-chip debug, on-board flash rewrite function (V(N)) 20 MHz (VOC) 2.745.5.3000 (V(N	
Operating Frequency/Supply f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) Voltage	
Current Consumption Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)	
Operating Ambient Temperature -40 to 85°C (J version)	
-40 to 125°C (K version) (1)	
Package 80-pin LQFP	
Package code: PLQP0080KB-A (previous code: 80P6Q-A)	



Table 1.5 Specifications for R8C/38Y Group (1)

Item Function		Specification				
CPU	Central processing	R8C CPU core				
	unit	Number of fundamental instructions: 89				
		Minimum instruction execution time:				
		50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)				
		Multiplier: 16 bits × 16 bits → 32 bits				
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits 				
		Operating mode: Single-chip mode (address space: 1 Mbyte)				
Memory	ROM, RAM, Data	Refer to Table 1.11 Product List for R8C/38Y Group.				
-	flash	·				
Power Supply	Voltage detection	Power-on reset				
Voltage	circuit	Voltage detection 3 (detection level of voltage detection 1 selectable)				
Detection						
I/O Ports	Programmable I/O	Input-only: 1 pin				
	ports	CMOS I/O ports: 75, selectable pull-up resistor				
Clock Clock generation		3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),				
	circuits	High-speed on-chip oscillator (with frequency adjustment function),				
		Low-speed on-chip oscillator				
		Oscillation stop detection: XIN clock oscillation stop detection function				
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16				
		Low power consumption modes:				
		Standard operating mode (high-speed clock, high-speed on-chip oscillator,				
		low-speed on-chip oscillator), wait mode, stop mode				
Interrupts		Interrupt vectors: 69				
		• External: 9 sources (INT x 5, key input x 4)				
		Priority levels: 7 levels				
Watchdog Timer		• 14 bits x 1 (with prescaler)				
		Reset start selectable				
		Low-speed on-chip oscillator for watchdog timer selectable				
DTC (Data Tra	ansfer Controller)	• 1 channel				
	•	Activation sources: 40				
		Transfer modes: 2 (normal mode, repeat mode)				

Table 1.6 Specifications for R8C/38Y Group (2)

Item	Function	Specification
Timer	Timer RA0	8 bits (with 8-bit prescaler) x 1
		Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period
		measurement mode
	Timer RA1	8 bits (with 8-bit prescaler) × 1
		Timer mode (period timer), pulse output mode (output level inverted every
		period), event counter mode, pulse width measurement mode, pulse period
		measurement mode
	Timer RB	8 bits (with 8-bit prescaler) x 1 Timer mode (period timer), programmable waveform generation mode (PWM
		output), programmable one-shot generation mode, programmable wait one- shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode
		(output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchropous PWM mode (output three-phase wayeforms
		(output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output
		three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode
		(PWM output 2 pins with fixed period)
	Timer RE	8 bits x 1 Output compare mode
	Timer RF	16 bits x 1
		Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits x 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UARTO, 1	2 channels Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I ² C mode (I ² C-bus), IE mode (IEbus), multiprocessor communication function
Synchronous		1 channel
Communication	on Unit (SSU)	Herdware LINE O (Alexandre DAO) Cont. DAA (LADTO LADTO)
LIN Module	r	Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
A/D Converte	I	10-bit resolution × 20 channels, includes sample and hold function, with sweep mode
Flash Memory	/	Programming and erasure voltage: VCC = 2.7 to 5.5 V
·		Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM)
		Program security: ROM code protect, ID code check
		Debug functions: On-chip debug, on-board flash rewrite function
		Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consi	umption	Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
	bient Temperature	-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		80-pin LQFP
		Package code: PLQP0080KB-A (previous code: 80P6Q-A)



Table 1.7 Specifications for R8C/38Z Group (1)

Item Function		Specification			
CPU	Central processing	R8C CPU core			
	unit	Number of fundamental instructions: 89			
		Minimum instruction execution time:			
		50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)			
		Multiplier: 16 bits × 16 bits → 32 bits			
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits 			
		Operating mode: Single-chip mode (address space: 1 Mbyte)			
Memory	ROM, RAM, Data	Refer to Table 1.12 Product List for R8C/38Z Group.			
-	flash	·			
Power Supply	Voltage detection	Power-on reset			
Voltage	circuit	Voltage detection 3 (detection level of voltage detection 1 selectable)			
Detection					
I/O Ports	Programmable I/O	Input-only: 1 pin			
	ports	CMOS I/O ports: 75, selectable pull-up resistor			
Clock Clock generation		3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),			
	circuits	High-speed on-chip oscillator (with frequency adjustment function),			
		Low-speed on-chip oscillator			
		Oscillation stop detection: XIN clock oscillation stop detection function			
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16			
		Low power consumption modes:			
		Standard operating mode (high-speed clock, high-speed on-chip oscillator,			
		low-speed on-chip oscillator), wait mode, stop mode			
Interrupts		Interrupt vectors: 69			
		• External: 9 sources (INT x 5, key input x 4)			
		Priority levels: 7 levels			
Watchdog Timer		• 14 bits x 1 (with prescaler)			
		Reset start selectable			
		Low-speed on-chip oscillator for watchdog timer selectable			
DTC (Data Tra	ansfer Controller)	• 1 channel			
	•	Activation sources: 40			
		Transfer modes: 2 (normal mode, repeat mode)			

Table 1.8 Specifications for R8C/38Z Group (2)

Item Function		Specification	
Timer	Timer RA0	8 bits (with 8-bit prescaler) x 1	
		Timer mode (period timer), pulse output mode (output level inverted every	
		period), event counter mode, pulse width measurement mode, pulse period	
		measurement mode	
	Timer RA1	8 bits (with 8-bit prescaler) × 1	
		Timer mode (period timer), pulse output mode (output level inverted every	
		period), event counter mode, pulse width measurement mode, pulse period	
	T: 00	measurement mode	
	Timer RB	8 bits (with 8-bit prescaler) x 1 Timer mode (period timer), programmable waveform generation mode (PWM	
		output), programmable one-shot generation mode, programmable wait one-	
		shot generation mode	
	Timer RC		
	Timer RC	16 bits (with 4 capture/compare registers) x 1 Timer mode (input capture function, output compare function), PWM mode	
		(output 3 pins), PWM2 mode (PWM output pin)	
	Timer RD	16 bits (with 4 capture/compare registers) × 2	
	Timerito	Timer mode (input capture function, output compare function), PWM mode	
		(output 6 pins), reset synchronous PWM mode (output three-phase waveforms	
		(6 pins), sawtooth wave modulation), complementary PWM mode (output	
		three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode	
		(PWM output 2 pins with fixed period)	
	Timer RE	8 bits × 1	
	Timor RE	Output compare mode	
	Timer RF	16 bits × 1	
		Input capture mode (input capture circuit), output compare mode (output compare circuit)	
	Timer RG	16 bits x 1	
		Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)	
Serial Interface	UARTO, 1	2 channels Clock synchronous serial I/O, UART	
monaco	UART2	1 channel	
		Clock synchronous serial I/O, UART, I ² C mode (I ² C-bus), IE mode (IEbus), multiprocessor communication function	
Synchronous	Serial	1 channel	
Communicat	ion Unit (SSU)		
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)	
A/D Converter		10-bit resolution × 20 channels, includes sample and hold function, with sweep mode	
Flash Memory		 Programming and erasure voltage: VCC = 2.7 to 5.5 V 	
		Programming and erasure endurance: 100 times (program ROM)	
		Program security: ROM code protect, ID code check	
		Debug functions: On-chip debug, on-board flash rewrite function	
Operating Frequency/Supply		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)	
Voltage			
Current Cons	sumption	Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)	
	mbient Temperature	-40 to 85°C (J version)	
	F	-40 to 125°C (K version) (1)	
Package		80-pin LQFP	
Package			



1.2 Product List

Table 1.9 lists Product List for R8C/38W Group, Table 1.10 lists Product List for R8C/38X Group, Table 1.11 lists Product List for R8C/38Y Group, and Table 1.12 lists Product List for R8C/38Z Group.

Table 1.9 Product List for R8C/38W Group

Current of May 2010

Part No.	ROM Capacity		RAM	Package Type	Remarks
Fait No.	Program ROM	Data flash	Capacity	rackage Type	Remarks
R5F21388WJFP (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	J version
R5F2138AWJFP (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CWJFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F21388WKFP (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	K version
R5F2138AWKFP (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CWKFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	

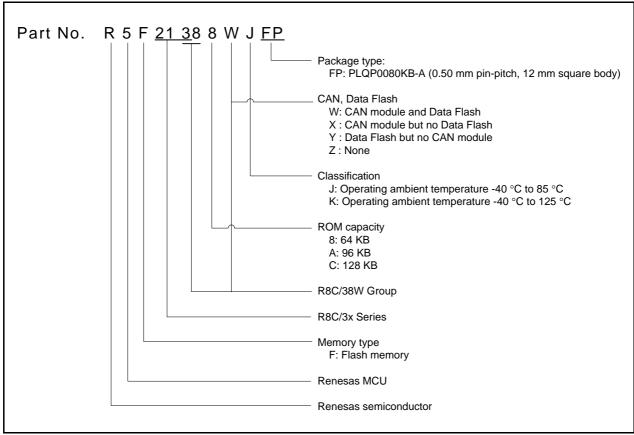


Figure 1.1 Part Number, Memory Size, and Package of R8C/38W Group

Table 1.10 Product List for R8C/38X Group

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

Current of May 2010

Part No.	ROM Capacity Program ROM	RAM Capacity	Package Type	Remarks
R5F21388XJFP (D)	64 Kbytes	6 Kbytes	PLQP0080KB-A	J version
R5F2138AXJFP (D)	96 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2138CXJFP (D)	128 Kbytes	10 Kbytes	PLQP0080KB-A	
R5F21388XKFP (D)	64 Kbytes	6 Kbytes	PLQP0080KB-A	K version
R5F2138AXKFP (D)	96 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2138CXKFP (D)	128 Kbytes	10 Kbytes	PLQP0080KB-A	

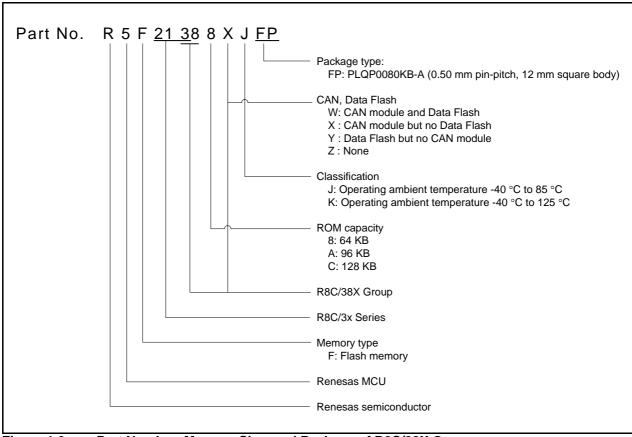


Figure 1.2 Part Number, Memory Size, and Package of R8C/38X Group

Table 1.11 Product List for R8C/38Y Group

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

Current of May 2010

Part No.	ROM Capacity		RAM	Dookogo Typo	Remarks
Pail No.	Program ROM	Data flash	Capacity	Package Type	Remarks
R5F21388YJFP (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	J version
R5F2138AYJFP (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CYJFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F21388YKFP (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	K version
R5F2138AYKFP (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CYKFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	

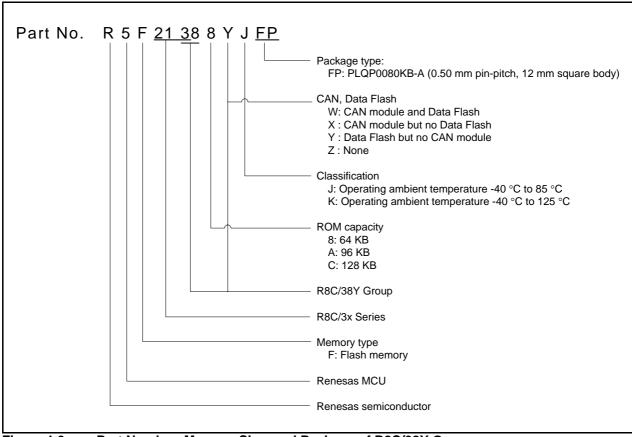


Figure 1.3 Part Number, Memory Size, and Package of R8C/38Y Group

Table 1.12 Product List for R8C/38Z Group

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

Current of May 2010

Part No.	ROM Capacity Program ROM	RAM Capacity	Package Type	Remarks
R5F21388ZJFP (D)	64 Kbytes	6 Kbytes	PLQP0080KB-A	J version
R5F2138AZJFP (D)	96 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2138CZJFP (D)	128 Kbytes	10 Kbytes	PLQP0080KB-A	
R5F21388ZKFP (D)	64 Kbytes	6 Kbytes	PLQP0080KB-A	K version
R5F2138AZKFP (D)	96 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2138CZKFP (D)	128 Kbytes	10 Kbytes	PLQP0080KB-A	

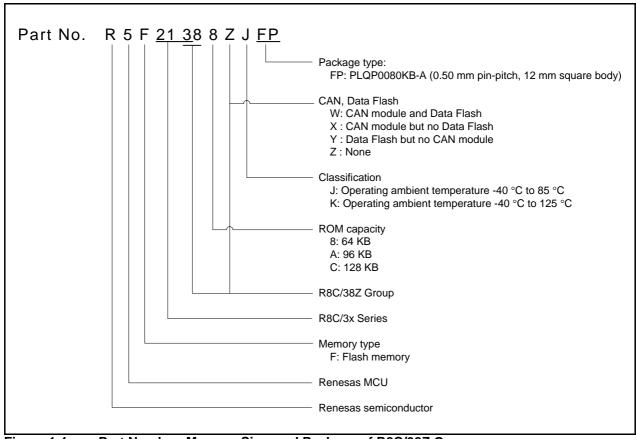


Figure 1.4 Part Number, Memory Size, and Package of R8C/38Z Group

1.3 Block Diagram

Figure 1.5 shows a Block Diagram.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

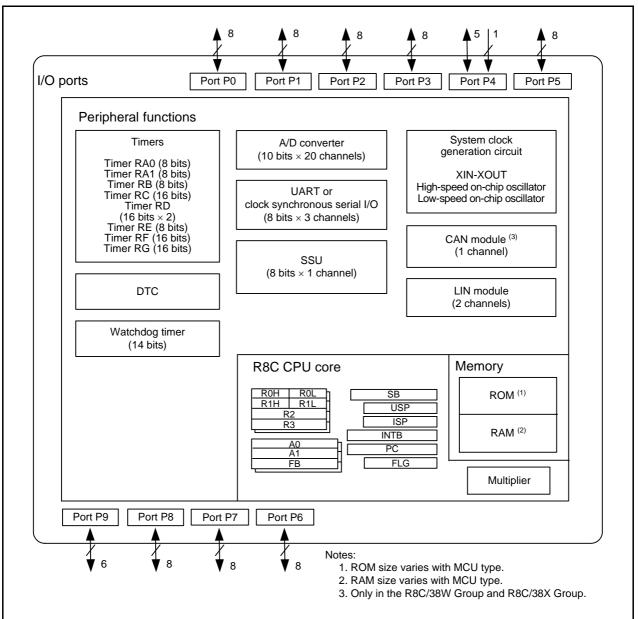


Figure 1.5 Block Diagram

1.4 Pin Assignment

Figure 1.6 shows Pin Assignment (Top View). Tables 1.13 and 1.14 outline the Pin Name Information by Pin Number.

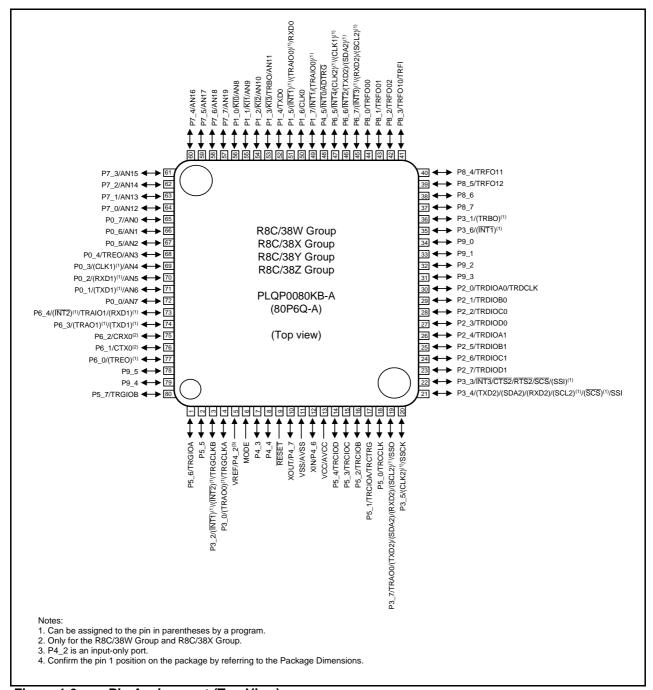


Figure 1.6 Pin Assignment (Top View)

Table 1.13 Pin Name Information by Pin Number (1)

					I/O Pin Functions for	Peripheral Modules	3	
Pin Number	Control Pin	Port	Interrupt	Timer	Serial Interface	SSU	CAN Module	A/D Converter, Voltage Detection Circuit
1		P5_6		TRGIOA				
2		P5_5						
3		P3_2	(INT1) ⁽¹⁾ / (INT2) ⁽¹⁾	TRGCLKB				
4		P3_0		(TRAO0) (1)/ TRGCLKA				
5		P4_2						VREF
6	MODE							
7		P4_3						
8		P4_4						
9	RESET							
10	XOUT	P4_7						
11	VSS/AVSS							
12	XIN	P4_6						
13	VCC/ AVCC							
14		P5_4		TRCIOD				
15		P5_3		TRCIOC				
16		P5_2		TRCIOB				
17		P5_1		TRCIOA/ TRCTRG				
18		P5_0		TRCCLK				
19		P3_7		TRAO0	(TXD2)/(SDA2)/ (RXD2)/(SCL2) (1)	SSO		
20		P3_5			(CLK2) (1)	SSCK		
21		P3_4			(TXD2)/(SDA2)/ (RXD2)/(SCL2) (1)	(SCS) (1)/SSI		
22		P3_3	INT3		CTS2/RTS2	SCS/(SSI) (1)		
23		P2_7		TRDIOD1				
24		P2_6		TRDIOC1				
25		P2_5		TRDIOB1				
26		P2_4		TRDIOA1				
27		P2_3		TRDIOD0				
28		P2_2		TRDIOC0				
29		P2_1	·	TRDIOB0				
30		P2_0		TRDIOA0/ TRDCLK				
31		P9_3			_			
32		P9_2						
33		P9_1						
34		P9_0						
35		P3_6	(INT1) (1)					
36		P3_1		(TRBO) (1)				
37		P8_7						
38		P8_6						
39		P8_5		TRFO12				
40		P8_4		TRFO11				

Notes:

- 1. This can be assigned to the pin in parentheses by a program.
- 2. Only for the R8C/38W Group and R8C/38X Group.

Table 1.14 Pin Name Information by Pin Number (2)

					I/O Pin Functions f	or Perinheral Modu	les	
Pin Number	Control Pin	Port	Interrupt	Timer	Serial Interface	SSU	CAN Module	A/D Converter, Voltage Detection Circuit
41		P8_3		TRFO10/TRFI				
42		P8_2		TRFO02				
43		P8_1		TRFO01				
44		P8_0		TRFO00				
45		P6_7	(INT3) (1)		(RXD2)/ (SCL2) (1)			
46		P6_6	ĪNT2		(TXD2)/ (SDA2) ⁽¹⁾			
47		P6_5	ĪNT4		(CLK2) (1)/ (CLK1) (1)			
48		P4_5	ĪNT0		(OLIVI)			ADTRG
49		P1_7	INT1	(TRAIO0) (1)				
50		P1_6		(CLK0			
51		P1_5	(INT1) (1)	(TRAIO0) (1)	RXD0			
52		P1_4	()	(110.00)	TXD0			
53		P1_3	KI3	TRBO				AN11
54		P1_2	KI2					AN10
55		P1_1	KI1					AN9
56		P1_0	KI0					AN8
57		P7_7						AN19
58		P7_6						AN18
59		P7_5						AN17
60		P7_4						AN16
61		P7_3						AN15
62		P7_2						AN14
63		P7_1						AN13
64		P7_0						AN12
65		P0_7						AN0
66		P0_6						AN1
67		P0_5						AN2
68		P0_4		TREO				AN3
69		P0_3			(CLK1) (1)			AN4
70		P0_2			(RXD1) ⁽¹⁾			AN5
71		P0_1			(TXD1) ⁽¹⁾			AN6
72		P0_0						AN7
73		P6_4	(INT2) (1)	TRAIO1	(RXD1) ⁽¹⁾			
74		P6_3		(TRAO1) (1)	(TXD1) ⁽¹⁾			
75		P6_2					CRX0 (2)	
76		P6_1					CTX0 (2)	
77		P6_0		(TREO) (1)				
78		P9_5						
79		P9_4						
80		P5_7		TRGIOB				

Notes:

- 1. This can be assigned to the pin in parentheses by a program.
- 2. Only for the R8C/38W Group and R8C/38X Group.

1.5 Pin Functions

Tables 1.15 and 1.16 list Pin Functions.

Table 1.15 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input		- -	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power	AVCC, AVSS		Power supply for the A/D converter.
supply input	AVOO, AVOO		Connect a capacitor between AVCC and AVSS.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between
XIN clock output	XOUT	I/O	the XIN and XOUT pins (1). To use an external clock, input it to the XOUT pin and leave the XIN pin open.
INT interrupt input	INT0 to INT4	I	INT interrupt input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer RA0	TRAIO0, TRAIO1	I/O	Timer RA I/O pin
Timer RA1	TRAO0, TRAO1	0	Timer RA output pin
Timer RB	TRBO	0	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK		External clock input pin
Timer RE	TREO	0	Divided clock output pin
Timer RF	TRFO00, TRFO10, TRFO01, TRFO11, TRFO02, TRFO12	0	Timer RF output pins.
	TRFI	I	Timer RF input pin.
Timer RG	TRGIOA, TRGIOB	I/O	Timer RG I/O ports.
	TRGCLKA, TRGCLKB	I	External clock input pins.
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	0	Serial data output pins
	CTS2	I	Transmission control input pin
	RTS2	0	Reception control output pin
	SCL2	I/O	I ² C mode clock I/O pin
	SDA2	I/O	I ² C mode data I/O pin
SSU	SSI	I/O	Data I/O pin
	SCS	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
i l	SSO	I/O	Data I/O pin

I: Input O: Output

I/O: Input and output

Note:

^{1.} Refer to the oscillator manufacturer for oscillation characteristics.



Table 1.16 Pin Functions (2)

Item	Pin Name	I/O Type	Description
CAN module	CRX0 (1)	I	CAN data input pin
	CTX0 (1)	0	CAN data output pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN19	I	Analog input pins to A/D converter
	ADTRG	I	AD external trigger input pin
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only ports

I: Input

O: Output

I/O: Input and output

Note:

1. Only in the R8C/38W Group and R8C/38X Group.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

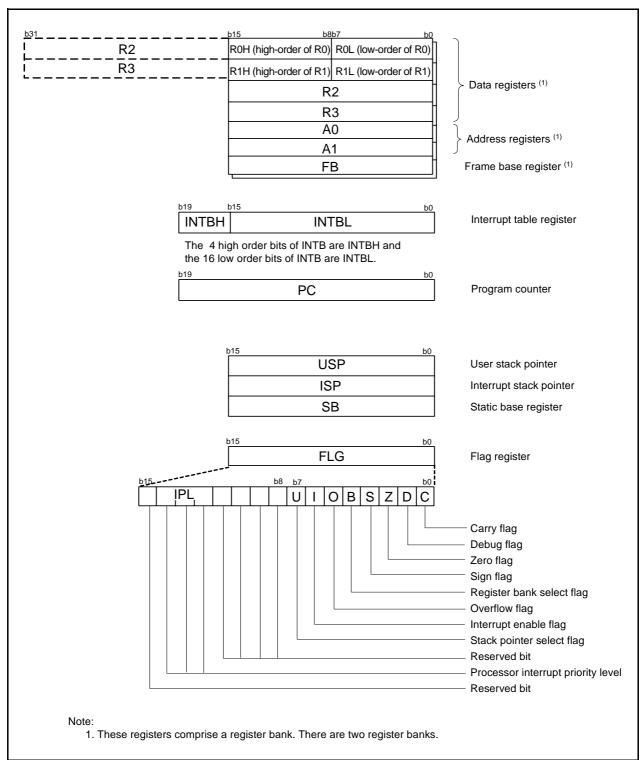


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 **Zero Flag (Z)**

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.



3. Memory

3.1 **R8C/38W Group**

Figure 3.1 is a Memory Map of R8C/38W Group. The R8C/38W Group has a 1-Mbyte address space from addresses 00000h to FFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

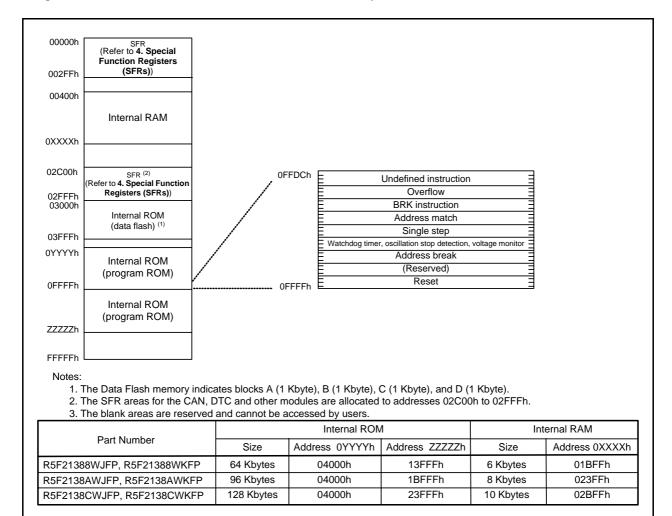


Figure 3.1 Memory Map of R8C/38W Group

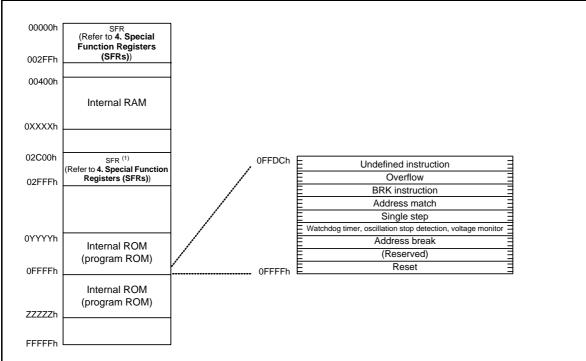
3.2 **R8C/38X Group**

Figure 3.2 is a Memory Map of R8C/38X Group. The R8C/38X Group has a 1-Mbyte address space from addresses 00000h to FFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:

- 1. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
- 2. The blank areas are reserved and cannot be accessed by users.

5		Internal ROM	Internal RAM		
Part Number	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388XJFP, R5F21388XKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AXJFP, R5F2138AXKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CXJFP, R5F2138CXKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.2 Memory Map of R8C/38X Group

3.3 **R8C/38Y Group**

Figure 3.3 is a Memory Map of R8C/38Y Group. The R8C/38Y Group has a 1-Mbyte address space from addresses 00000h to FFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

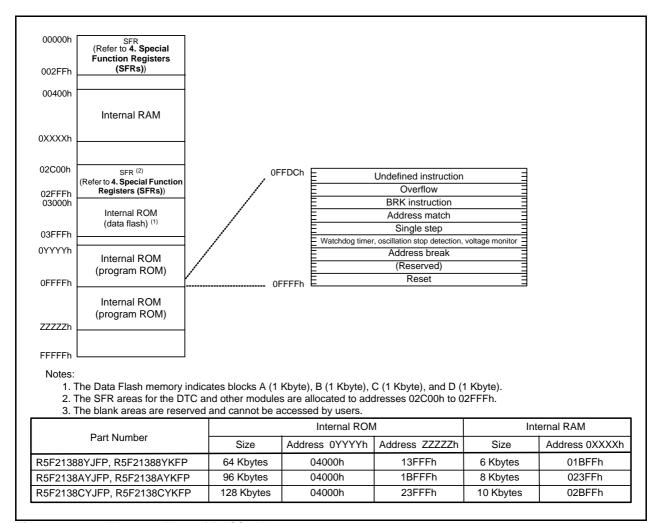


Figure 3.3 Memory Map of R8C/38Y Group

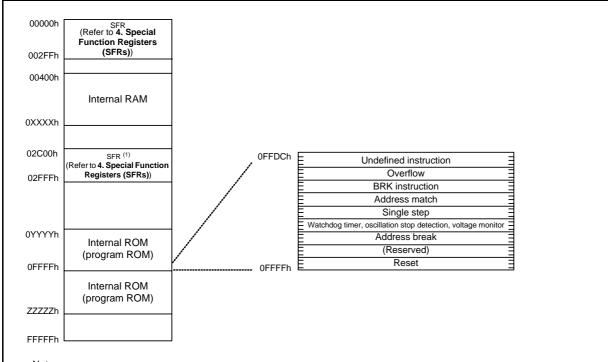
3.4 R8C/38Z Group

Figure 3.4 is a Memory Map of R8C/38Z Group. The R8C/38Z Group has a 1-Mbyte address space from addresses 00000h to FFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:

- 1. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
- 2. The blank areas are reserved and cannot be accessed by users.

Dard Normals and		Internal ROM	Internal RAM		
Part Number	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388ZJFP, R5F21388ZKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AZJFP, R5F2138AZKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CZJFP, R5F2138CZKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.4 Memory Map of R8C/38Z Group

Special Function Registers (SFRs) 4.

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.17 list the special function registers and Table 4.18 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Eh	Watchdog Timer Control Register	WDTC	00111111b
0010h	Waterlady Timer Control Register	WB10	001111115
0010h			
0011h			+
0012II 0013h			
0013h			
0014h	High-Speed On-Chip Oscillator Control Pogistor 7	FRA7	When shipping
0015h	High-Speed On-Chip Oscillator Control Register 7	FRAI	when shipping
0016h			
0017H			
0018h			
0019h			
001Bh		0000	001
001Ch	Count Source Protection Mode Register	CSPR	00h
			10000000b ⁽³⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch	5 , ,	1	
002Dh		<u> </u>	<u> </u>
002Eh		<u> </u>	
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁴⁾
000-111	- Stage Dollor Region L	V 5/12	001 (4) 00100000b (5)
0025			(S) @00001 00
0035h	Voltage Detection 1.1 aval Calcat Desister	1/041.0	000001115
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			7.5
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b ⁽⁴⁾
			1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X : Undefined Notes: 1. The b

- The blank areas are reserved and cannot be accessed by users.

 The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset or watchdog timer reset does not affect this bit.
- The CSPROINI bit in the OFS register is set to 0. 3.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.



SFR Information (2) (1) Table 4.2

Address	Register	Symbol	After reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h	Timer RA1 Interrupt Control Register	TRA1IC	XXXXX000b
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register	SSUIC	XXXXX000b
0050h	Timer RF Compare1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UARTO Transmit Interrupt Control Register	SOTIC	XXXXX000b
0052h	UARTO Receive Interrupt Control Register	SORIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA0 Interrupt Control Register	TRAOIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Timer RF Compare0 Interrupt Control Register	CMPOIC	XXXXX000b
005Dh	INTO Interrupt Control Register	INTOIC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh	Timer RF Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	Timer RG Interrupt Control Register	TRGIC	XXXXX000b
006Ch	CANO Successful Reception Interrupt Control Register	CORIC	XXXXX000b XXXXX000b
006Dh	CANO Successful Transmission Interrupt Control Register	COTIC	XXXXX000b XXXXX000b
006Eh	CANO Successful Transmission interrupt Control Register CANO Receive FIFO Interrupt Control Register	COFRIC	XXXXX000b XXXXX000b
006En	CANO Transmit FIFO Interrupt Control Register	COFTIC	XXXXX000b XXXXX000b
0070h	CANO Fror Interrupt Control Register	COEIC	XXXXX000b XXXXX000b
0070H	CANO Wake-up Interrupt Control Register	COMIC	XXXXX000b
0071h	Voltage Monitor 1 Level Interrupt Control Register	VCMP1IC	XXXXX000b XXXXX000b
0072h	Voltage Monitor 2 Level Interrupt Control Register	VCMP2IC	XXXXX000b XXXXX000b
0073h	Voltago monitor 2 20voi interrupt control register	V OIVII ZIO	7777770000
0074H			
0075h		+	
0076h			
0077h 0078h			
		<u> </u>	
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X : Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (3) (1) Table 4.3

Address	Register	Symbol	After reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h		+	+
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h		DTCEN1	00h
	DTC Activation Enable Register 1	_	
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h	Timer RF Register	TRF	00h
0091h	_ ····· ··· · · · · · · · · · · · · ·	1	00h
0092h		+	
0092H			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	00h
009Bh	Timer RF Control Register 1	TRFCR1	00h
009Ch	Capture and Compare 0 Register	TRFM0	00h
009Dh	Oupture and Compare of Register	THE WIO	00h
	Common 4 Devictor	TDEM4	FFh
009Eh	Compare 1 Register	TRFM1	
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h		33.12	XXh
00A711	UART2 Transmit/Receive Mode Register	U2MR	00h
	UART2 Bit Rate Register	U2BRG	
00A9h			XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh	1		XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B0H	2 2 signar inter a matter colour regions	0.000	
00B1II		+	
00B2H			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh		+	
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 5 UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (4) (1) Table 4.4

Add=000	Donistor	Compt -1	Afterreact
Address	Register	Symbol	After reset
00C0h	A/D Register 0	AD0	XXh
00C1h	1475.5		000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh	1400		000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh	A/D Devistor 7	15-	000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h	A/D Mada Ragistar	ADMOD	100h
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Control Register	ADCONO	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h 00D9h			
00DAh			
00DBh			
00DCh 00DDh			
00DDh 00DEh			
00DEh 00DFh			
00DFh 00E0h	Port P0 Register	P0	XXh
00E0h 00E1h	Port P0 Register Port P1 Register	P0 P1	XXh
00E1h 00E2h	Port P1 Register Port P0 Direction Register	P1 PD0	00h
00E2h 00E3h	Port P0 Direction Register Port P1 Direction Register	PD0 PD1	00h 00h
00E3h	Port P1 Direction Register Port P2 Register	PD1	XXh
00E4h	Port P3 Register	P2	XXh
00E5h	Port P3 Register Port P2 Direction Register	PD2	00h
00E6f1	Port P3 Direction Register	PD3	00h
00E7h	Port P4 Register	P4	XXh
00E8h	Port P5 Register	P5	XXh
00E9h	Port P4 Direction Register	PD4	00h
00EAn	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00ECh	Port P7 Register	P6	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h	Port P8 Register	P8	XXh
00F0H	Port P9 Register	P9	XXh
00F1II	Port P8 Direction Register	PD8	00h
00F2H	Port P9 Direction Register	PD9	00h
00F4h		1.50	
00F5h			+
00F6h			+
00F7h		+	+
00F8h			+
00F9h		+	+
00FAh		+	+
00FBh			+
00FCh			+
00FDh		+	+
201 DII	i e	i	i
00FEh 00FFh			

X : Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (5) (1) Table 4.5

Address	Register	Symbol	After reset
	Timer RA0 Control Register	TRA0CR	00h
	Timer RA0 I/O Control Register	TRA0IOC	00h
	Timer RA0 Mode Register	TRAOMR	00h
	Timer RA0 Prescaler Register	TRA0PRE	FFh
	Timer RA0 Register	TRA0	FFh
0104n	LIN0 Control Register 2	LIN0CR2	00h
	LINO Control Register	LINOCR2	00h
	LINO Control Register	LINOST	00h
	Timer RB Control Register	TRBCR	
			00h
	Timer RB One-Shot Control Register	TRBOCR	00h
	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
	Timer RB Prescaler Register	TRBPRE	FFh
	Timer RB Secondary Register	TRBSC	FFh
	Timer RB Primary Register	TRBPR	FFh
010Fh			
	Timer RA1 Control Register	TRA1CR	00h
	Timer RA1 I/O Control Register	TRA1IOC	00h
	Timer RA1 Mode Register	TRA1MR	00h
	Timer RA1 Prescaler Register	TRA1PRE	FFh
0114h	Timer RA1 Register	TRA1	FFh
0115h l	LIN1 Control Register 2	LIN1CR2	00h
0116h l	LIN1 Control Register	LIN1CR	00h
	LIN1 Status Register	LIN1ST	00h
	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
	Timer RE Control Register 2	TRECR2	00h
	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh	· - · · · · · · · · · · · · · · · · · ·		
	Timer RC Mode Register	TRCMR	01001000b
	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
	Timer RC Status Register	TRCSR	01110000b
	Timer RC I/O Control Register 0	TRCIOR0	10001000b
	Timer RC I/O Control Register 1	TRCIOR1	10001000b
	Timer RC Counter	TRC	00h
0120H	Time INO Counter	11.0	00h
	Timer RC General Register A	TRCGRA	FFh
0128h 0129h	Times NO Selicial Negislei A	INOGRA	FFh
	Times PC Conoral Pagistar P	TDCCDD	
	Timer RC General Register B	TRCGRB	FFh
012Bh	Times DC Conord Decistor C	TDCCDC	FFh
	Timer RC General Register C	TRCGRC	FFh
012Dh	Times DO Commel Desistes D	TDOODD	FFh
	Timer RC General Register D	TRCGRD	FFh
012Fh	T' - DO O - 4 - ID - 14 - O	TDOODO	FFh
	Timer RC Control Register 2	TRCCR2	00011000b
	Timer RC Digital Filter Function Select Register	TRCDF	00h
	Timer RC Output Master Enable Register	TRCOER	01111111b
	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
	Timer RD Trigger Control Register	TRDADCR	00h
		TRDSTR	11111100b
	Timer RD Mode Register	TRDMR	00001110b
	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
	Timer RD Output Master Enable Register 1	TRDOER1	FFh
	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
	Timer RD Output Control Register	TRDOCR	00h
0135h 0136h 0137h 0138h 0139h 013Ah 013Bh 013Ch 013Dh 013Eh	Timer RD Start Register Timer RD Mode Register Timer RD PWM Mode Register Timer RD Function Control Register Timer RD Output Master Enable Register 1 Timer RD Output Master Enable Register 2	TRDSTR TRDMR TRDPMR TRDFCR TRDOER1 TRDOER2	11111100b 00001110b 10001000b 10000000b FFh 01111111b

Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (6) (1) Table 4.6

	, , , , , , , , , , , , , , , , , , ,	1 0 1 1	A.C
Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h	Timor No Countor o	11120	00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h	Tiller ND General Negister Au	TROGRAO	FFh
	T' DD 0 1D 11 D0	TDDODDO	
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0151h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	110001000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh		_	FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh	Timor NE Constant Cognition CT	THE CHO!	FFh
015Eh	Times DD Conesal Decistor D4	TRDGRD1	FFh
	Timer RD General Register D1	TRUGRUT	
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h	- Critical Reserve Bullet Register	02	XXh
0168h			AAII
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	01000000b
0171h	Timer RG Count Control Register	TRGCNTC	0000000b
017111 0172h	Timer RG Count Control Register	TRGCR	10000000b
0173h	Timer RG Interrupt Enable Register	TRGIER	11110000b
0174h	Timer RG Status Register	TRGSR	11100000b
0175h	Timer RG I/O Control Register	TRGIOR	0000000b
0176h	Timer RG Counter	TRG	00h
0177h			00h
0178h	Timer RG General Register A	TRGGRA	FFh
0179h	1		FFh
017Ah	Timer RG General Register B	TRGGRB	FFh
	Limbi NO Ocholal Register D	11.001.0	
	1		
017Bh	Times BC Coneral Pagister C	TDCCDC	FFh
017Bh 017Ch	Timer RG General Register C	TRGGRC	FFh
017Bh 017Ch 017Dh			FFh FFh
017Bh 017Ch	Timer RG General Register C Timer RG General Register D	TRGGRC	FFh

X : Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (7) (1) Table 4.7

Addross	Register	Symbol	After reset
Address	Timer RA Pin Select Register		After reset 00h
0180h	5	TRASR	
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h	Timer RF Output Control Register	TRFOUT	00h
0188h	UARTO Pin Select Register	UOSR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0191h			
	CC Dit Counter Degister	CCDD	11111000h
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register	SSTDR	FFh
0195h			FFh
0196h	SS Receive Data Register	SSRDR	FFh
0197h			FFh
0198h	SS Control Register H	SSCRH	00h
0199h	SS Control Register L	SSCRL	01111101b
019Ah	SS Mode Register	SSMR	00010000b
019Bh	SS Enable Register	SSER	00h
019Ch	SS Status Register	SSSR	00h
019Dh	SS Mode Register 2	SSMR2	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B0II			
	Flook Mamon, Ctatus Donistar	гот	10000V00h
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
V . I ladafiaad			

X : Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (8) (1) Table 4.8

	, , , , , , , , , , , , , , , , , , ,	1 0	
Address	Register	Symbol	After reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
	Address Match Interwent Enable Degister O	AIEDO	
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Motes Interrupt Cookle Degister 1	AIED4	
	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D3h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h	Pull-Up Control Register 2	PUR2	00h
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			1
01EBh			
01ECh			
01EDh			
01EEh			
04 E E E			
01EFh			
01F0h			
01F0h 01F1h			
01F0h 01F1h 01F2h			
01F0h 01F1h 01F2h 01F3h			
01F0h 01F1h 01F2h 01F3h 01F4h			
01F0h 01F1h 01F2h 01F3h 01F4h	Input Threshold Control Register 0	VLTO	00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h	Input Threshold Control Register 0	VLT0	00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h	Input Threshold Control Register 1	VLT1	00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h	Input Threshold Control Register 0 Input Threshold Control Register 1 Input Threshold Control Register 2		
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h 01F8h	Input Threshold Control Register 1	VLT1	00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h 01F8h	Input Threshold Control Register 1	VLT1	00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h 01F8h 01F9h	Input Threshold Control Register 1 Input Threshold Control Register 2	VLT1 VLT2	00h 00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h 01F8h 01F9h	Input Threshold Control Register 1 Input Threshold Control Register 2 External Input Enable Register 0	VLT1 VLT2 INTEN	00h 00h 00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h 01F8h 01F9h 01FAh 01FBh	Input Threshold Control Register 1 Input Threshold Control Register 2 External Input Enable Register 0 External Input Enable Register 1	VLT1 VLT2 INTEN INTEN1	00h 00h 00h 00h 00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h 01F8h 01F9h 01FAh 01FBh	Input Threshold Control Register 1 Input Threshold Control Register 2 External Input Enable Register 0 External Input Enable Register 1	VLT1 VLT2 INTEN INTEN1	00h 00h 00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h 01F8h 01F9h 01FAh 01FBh	Input Threshold Control Register 1 Input Threshold Control Register 2 External Input Enable Register 0 External Input Enable Register 1 INT Input Filter Select Register 0	VLT1 VLT2 INTEN INTEN1 INTF	00h 00h 00h 00h 00h 00h
01F0h 01F1h 01F2h 01F3h 01F3h 01F6h 01F6h 01F7h 01F8h 01F9h 01FBh 01FBh 01FCh 01FDh	Input Threshold Control Register 1 Input Threshold Control Register 2 External Input Enable Register 0 External Input Enable Register 1 INT Input Filter Select Register 0 INT Input Filter Select Register 1	VLT1 VLT2 INTEN INTEN1 INTF INTF1	00h 00h 00h 00h 00h 00h
01F0h 01F1h 01F2h 01F3h 01F4h 01F5h 01F6h 01F7h 01F8h 01F9h 01FAh 01FBh	Input Threshold Control Register 1 Input Threshold Control Register 2 External Input Enable Register 0 External Input Enable Register 1 INT Input Filter Select Register 0	VLT1 VLT2 INTEN INTEN1 INTF	00h 00h 00h 00h 00h 00h

X : Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (9) (1) Table 4.9

14510 4.5	or it information (3)		A.C
Address 2C00h	Register DTC Transfer Vector Area	Symbol	After reset XXh
	DTC Transfer Vector Area		XXh
	DTC Transfer Vector Area		XXh
	DTC Transfer Vector Area DTC Transfer Vector Area	+	XXh
	DTC Transfer Vector Area		XXh
2C05h	DTO Transier Vector Area		AAII
2C06h			
2C07h			
	DTC Transfer Vector Area		XXh
	DTC Transfer Vector Area		XXh
	DTC Transfer Vector Area		XXh
	DTC Transfer Vector Area		XXh
	DTC Transfer Vector Area		XXh
2C3Ah			
2C3Bh			
2C3Ch			
2C3Dh			
2C3Eh			
2C3Fh			
	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h	DTO O I D O	DTODO	XXh
	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh XXh
2C5Dh			
2C5Eh			XXh XXh
2C5Fh	DTC Control Data 4	DTCD4	
2C60h 2C61h	DTO CONIIO Dala 4	01004	XXh XXh
2C62h			XXh
2C62h			XXh
2C64h			XXh
2C64f1			XXh
2C66h			XXh
2C67h			XXh
	DTC Control Data 5	DTCD5	XXh
2C69h	DTO CONTROL Data 3	DICDS	XXh
2C69fi 2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6En 2C6Fh			XXh
ZOUFII			AVII

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

SFR Information (10) (1) **Table 4.10**

set

X : Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (11) (1) **Table 4.11**

Tubic 4.1	or it information (11)		
Address	Register	Symbol	After reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h	B TO COMMON BAILA TO	210210	XXh
2CC2h			XXh
2CC3h	†		XXh
2CC4h			XXh
2CC5h	1		XXh
2CC6h	1		XXh
2CC6H	1		XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h	DTC Control Data 17	DICDI/	XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			
2CCCh 2CCDh			XXh XXh
2CCEh			XXh
2CCFh	DTO 0 10	DTCD40	XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h	1		XXh
2CEAh	1		XXh
2CEBh	1		XXh
2CECh	†		XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh
Y : Undofined	<u>l</u>		.0.01

X : Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
2D01h			
:			
2E00h	CAN0 Mailbox 0 : Message ID	C0MB0	XXXX XXXXh
	Or Water Mainbox O . Micosage ID	CONIDO	AAAA AAAAII
2E01h			
2E02h			
2E03h			
2E04h			
2E05h	CAN0 Mailbox 0 : Data length		XXh
2E06h	CAN0 Mailbox 0 : Data field		XXXX XXXX
2E07h			XXXX XXXXh
2E08h			****
2E09h			
2E0Ah			
2E0Bh			
2E0Ch			
2E0Dh			
2E0Eh	CAN0 Mailbox 0 : Time stamp		XXXXh
2E0Fh	'		
2E10h	CAN0 Mailbox 1 : Message ID	C0MB1	XXXX XXXXh
2E11h	Or the mailbox 1: Modeago 15	COMBI	700007000011
2E12h			
2E13h			
2E14h			
2E15h	CAN0 Mailbox 1 : Data length		XXh
2E16h	CAN0 Mailbox 1 : Data field		XXXX XXXX
2E17h			XXXX XXXXh
2E18h	1		
2E19h	1		
2E1Ah			
2E1Bh			
2E1Ch			
2E1Dh			
2E1Eh	CAN0 Mailbox 1 : Time stamp		XXXXh
2E1Fh			
2E20h	CAN0 Mailbox 2 : Message ID	C0MB2	XXXX XXXXh
2E21h	1		
2E22h	1		
2E23h			
2E24h			
	LCANO Mailhay 2 - Data langth		VVb
2E25h	CANO Mailbox 2 : Data length		XXh
2E26h	CAN0 Mailbox 2 : Data field		XXXX XXXX
2E27h			XXXX XXXXh
2E28h			
2E29h			
2E2Ah	1		
2E2Bh			
2E2Ch			
2E2Dh			VA A A A
2E2Eh	CAN0 Mailbox 2 : Time stamp		XXXXh
2E2Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (13) ⁽¹⁾ **Table 4.13**

A d draga	Desigter	Cymahal	After react
Address	Register	Symbol	After reset
2E30h	CAN0 Mailbox 3 : Message ID	C0MB3	XXXX XXXXh
2E31h			
2E32h			
2E33h			
2E34h		1	
2E35h	CANO Mailbox 3 : Data longth	-	XXh
	CANO Mailbox 3 : Data length	4	
2E36h	CAN0 Mailbox 3 : Data field		XXXX XXXX
2E37h			XXXX XXXXh
2E38h			
2E39h			
2E3Ah			
2E3Bh			
2E3Ch			
2E3Dh			
	CANO M-illando Tima atama	4	VVVVI
2E3Eh	CAN0 Mailbox3 : Time stamp		XXXXh
2E3Fh			
2E40h	CAN0 Mailbox4 : Message ID	C0MB4	XXXX XXXXh
2E41h			
2E42h			
2E43h			
2E44h		1	
2E45h	CANO Mailboy4 : Data longth	4	VVh
	CANO Mailbox4 : Data length	4	XXh
2E46h	CAN0 Mailbox4 : Data field		XXXX XXXX
2E47h			XXXX XXXXh
2E48h			
2E49h			
2E4Ah			
2E4Bh	1		
2E4Ch			
2E4Dh			
	CANCAN-IIIA Ti	4	VVVVI
2E4Eh	CAN0 Mailbox4 : Time stamp		XXXXh
2E4Fh			
2E50h	CAN0 Mailbox5 : Message ID	C0MB5	XXXX XXXXh
2E51h			
2E52h	1		
2E53h	1		
2E54h		†	
	CANO MailbayE : Data longth	4	VVh
2E55h	CANO Mailbox5 : Data length	4	XXh
2E56h	CAN0 Mailbox5 : Data field		XXXX XXXX
2E57h			XXXX XXXXh
2E58h			
2E59h			
2E5Ah			
2E5Bh	1		
2E5Ch			
2E5Dh			
	CANCAN-III	4	VVVVI
2E5Eh	CAN0 Mailbox5 : Time stamp		XXXXh
2E5Fh			
2E60h	CAN0 Mailbox6 : Message ID	C0MB6	XXXX XXXXh
2E61h			
2E62h			
2E63h	1		
2E64h		†	
2E65h	CAN0 Mailbox6 : Data length	4	XXh
		4	
2E66h	CAN0 Mailbox6 : Data field		XXXX XXXX
2E67h			XXXX XXXXh
2E68h			
2E69h			
2E6Ah			
2E6Bh			
2E6Ch	1		
2E6Dh	LOANOM III. O. Ti.	4	20004
2E6Eh	CAN0 Mailbox6 : Time stamp		XXXXh
2E6Fh			
V : Undofined			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (14) (1) **Table 4.14**

Address Register Symbol After reset				
ZEF/In ZEF/An Z		Register		
ZEF/In ZEF/An Z	2E70h	CAN0 Mailbox7 : Message ID	C0MB7	XXXX XXXXh
The composition of the composi	2F71h			
ZE73h ZE73h ZE75h ZE75h ZE75h ZANO Mailbox7 : Data field XXX				
22F4h CANO Mailbox7 Data length XXX XXXX XXXX		4		
22F3h				
ZEF7h ZEF7	2E74h			
ZEF7h ZEF7	2E75h	CAN0 Mailbox7: Data length		XXh
ZET/R ZET/		CANO Mailbox7 : Data field	=	
ZE78h ZE88h ZE89h ZE89h ZE99h ZE98h ZE98		CANO IVIAIIDOX7 . Data field		
ZETAN ZETA				XXXX XXXXh
Page				
Page	2E79h			
Page	2F7Ah	1		
ZEF7Ch		4		
ZETPIN				
ZEFFh ZEFFh ZEFN ZEB0h ZEB1h ZEB1h ZEB2h ZEB3h ZEB3h				
ZEFFR ZE691	2E7Dh			
ZEFFR ZE691	2E7Eh	CAN0 Mailbox7: Time stamp		XXXXh
ZEB0h		The state of the s		
ZEB1h	2E00h	CANO Mailhays - Magazaga ID	COMPO	VVVV VVVVL
Page		OAINO IVIAIIDUXO . IVIESSAYE ID	CUIVIDO	^^^^ ^^^
ZE33h				1
ZE33h	2E82h			1
ZE36h		1		1
ZEBSh			1	
ZE88h		CANO Maille and a Data law oth	-	VVI
ZE87h		CAINU IVIAIIDOX8 : Data length	1	
ZE88h ZE88h ZE8Bh ZE9Bh ZE9Bh ZE9Bh ZE99h ZE9Bh ZEABh ZEAB		CAN0 Mailbox8 : Data field		XXXX XXXX
ZE88h ZE88h ZE8Bh ZE9Bh ZE9Bh ZE9Bh ZE99h ZE9Bh ZEABh ZEAB	2E87h			XXXX XXXXh
ZEB9h ZEBCh ZEBC		1		7,000,700,011
ZEBAh ZEBBh ZEBCh ZEBOH ZEBCh ZEBOH ZEBCh ZEBOH ZEBECh ZEBOH ZEBECh ZEBOH ZEBECh ZEBOH ZEBECh ZEBOH				
ZEBBCh ZEBCh ZEB				1
ZEBCh 2EBCh 2EBC				1
ZEBCh 2EBCh 2EBC				1
ZEBCh				1
ZEBEh CAN0 Mailbox8 : Time stamp XXXXh ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th ZE9Th				1
ZE8Ph ZE90h ZE91h ZE92h ZE92h ZE93h ZE93		CANO Maille and a Time and are	-	VVVVI
ZE90h		CAINU IVIAIIDOXX : I IME stamp		XXXXN
ZE91h ZE92h ZE93h ZE94h ZE95h ZE94h ZE95h ZE95h ZE95h ZE97h ZE98h ZE97h ZE98h ZE99h ZE98h ZE98h ZE98h ZE98h ZE98h ZE98h ZE98h ZE98h ZE88h ZE88h ZE88h ZE88h ZE88h ZE88h ZE88h ZE8Ah ZEA8h ZEA8	2E8Fh			
ZE91h ZE92h ZE93h ZE94h ZE95h ZE94h ZE95h ZE95h ZE95h ZE97h ZE98h ZE97h ZE98h ZE99h ZE98h ZE98h ZE98h ZE98h ZE98h ZE98h ZE98h ZE98h ZE88h ZE88h ZE88h ZE88h ZE88h ZE88h ZE88h ZE8Ah ZEA8h ZEA8	2E90h	CANO Mailbox9: Message ID	C0MB9	XXXX XXXXh
ZE92h ZE93h ZE94h ZE95h CAN0 Mailbox9 : Data length XXh XXXX XXXX ZE97h ZE98h ZE99h ZE96h ZE96h ZE96h ZE96h ZE97h ZE98h ZE98				
ZE93h ZE95h ZE96h ZE96h ZE97h ZE98h ZE99h ZE98h ZE98		4		
ZE94h				
ZE95h				
ZE95h	2E94h			
ZE96h		CANO Mailbox9 : Data length		XXh
ZE98h	2E06h	CAND Mailbox 0: Data field	-	
ZE98h ZE99h ZE99h ZE90h ZE90h ZE90h ZE90h ZE90h ZE90h ZE99h ZE99h ZE99h ZE99h ZE99h ZE98h ZE98h ZE98h ZEA0h ZEA1h ZEA2h ZEA3h ZEA3		CANO Maliboxa . Data field		
2E99h 2E98h 2E9Ch 2E9Dh 2E9Dh 2E9Eh 2EA0h 2EA1h 2EA2h 2EA3h 2EA4h 2EA5h 2EA7h 2EA8h 2EA8				XXXX XXXXh
2E99h 2E98h 2E9Ch 2E9Dh 2E9Dh 2E9Eh 2EA0h 2EA1h 2EA2h 2EA3h 2EA4h 2EA5h 2EA7h 2EA8h 2EA8	2E98h			1
2E9Ah 2E9Bh 2E9Ch 2E9Dh 2E9Dh 2E9Eh 2E9Fh 2E9Fh 2E9Fh 2E9Fh 2E3Fh 2E3Fh 2E3Fh 2E3Fh 2E3Ah 2E3Ah 2E3ABh	2E99h			1
ZE9Bh		1		1
ZE9Ch ZE9Dh ZE9Eh CAN0 Mailbox9 : Time stamp XXXXh		1		
ZE9Ph				1
CANO Mailbox9 : Time stamp				
CANO Mailbox9 : Time stamp	2E9Dh			
2E9Fh 2EA0h CAN0 Mailbox10 : Message ID XXXX XXXXh 2EA1h 2EA2h XXXX XXXXh XXXX XXXXh 2EA3h 2EA4h XXh XXh 2EA5h CAN0 Mailbox10 : Data length XXh XXXX XXXX 2EA6h 2EA7h XXXX XXXXXh XXXX XXXXXh 2EA8h 2EA8h XXXX XXXXh XXXX XXXXXh 2EABh 2EACh XXXX XXXXh XXXXXh 2EACh XXXXh XXXXh XXXXh		CANO Mailhox9 · Time stamp	1	XXXXh
2EA0h CAN0 Mailbox10 : Message ID COMB10 XXXX XXXXh 2EA1h 2EA2h 2EA3h 2EA4h 2EA5h 2EA5h 2EA5h 2EA5h 2EA5h XXh XXh XXXX XXXX XXXX XXXX XXXX XXXXX XXXX XXXXX XXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	2E0Eh	Or the mailboxe . Time stamp		700001
2EA1h 2EA2h 2EA3h 2EA4h 2EA5h CAN0 Mailbox10 : Data length XXh 2EA6h XXXX XXXX 2EA7h XXXX XXXXX 2EA8h XXXX XXXXX 2EA9h XXXX XXXXX 2EA9h XXXX XXXXX 2EABh XXXX XXXXX 2EABh XXXXX 2EABh XXXXX 2EABh XXXXX 2EABh XXXXX 2EAFh XXXXX			0011010	1000010000
2EA2h 2EA3h 2EA4h 2EA5h CAN0 Mailbox10 : Data length 2EA6h XXh 2EA6h CAN0 Mailbox10 : Data field XXXX XXXX XXXX XXXXX 2EA8h 2EA8h 2EAAh 2EABh 2EACh 2EACh 2EACh 2EACh 2EAEh CAN0 Mailbox10 : Time stamp XXXXh		CANU Mailbox10 : Message ID	C0MB10	XXXX XXXXh
2EA2h 2EA3h 2EA4h 2EA5h CAN0 Mailbox10 : Data length 2EA6h XXh 2EA6h CAN0 Mailbox10 : Data field XXXX XXXX XXXX XXXXX 2EA8h 2EA8h 2EAAh 2EABh 2EACh 2EACh 2EACh 2EACh 2EAEh CAN0 Mailbox10 : Time stamp XXXXh	2EA1h			1
2EA3h 2EA4h 2EA5h CAN0 Mailbox10 : Data length 2EA6h CAN0 Mailbox10 : Data field 2EA7h 2EA8h 2EA8h 2EA9h 2EA8h 2EAAh 2EABh 2EACh 2EACh 2EADh 2EAEh CAN0 Mailbox10 : Time stamp XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX		1		
2EA4h CAN0 Mailbox10 : Data length XXh 2EA6h CAN0 Mailbox10 : Data field XXXX XXXX 2EA8h 2EA8h XXXX XXXXX 2EA9h 2EA8h XXXX XXXXX 2EA9h 2EABh XXXX XXXXX 2EABh 2EABh XXXX 2EABh XXXX 2EABh XXXX 2EABh XXXX 2EAFh XXXX	05401			
2EA5h CAN0 Mailbox10 : Data length XXh 2EA6h CAN0 Mailbox10 : Data field XXXX XXXX 2EA7h 2EA8h XXXX XXXX 2EA9h 2EAAh XXXX XXXX 2EAAh 2EAAh XXXX XXXX 2EAAh 2EACh XXXX 2EADh XXXXh 2EAFh XXXXh			-	<u> </u>
2EA6h CAN0 Mailbox10 : Data field 2EA7h 2EA8h 2EA9h 2EAAh 2EAAh 2EACh 2EACh 2EADh 2EAEh CAN0 Mailbox10 : Time stamp XXXX XXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX			_	
2EA6h CAN0 Mailbox10 : Data field 2EA7h 2EA8h 2EA9h 2EAAh 2EAAh 2EACh 2EACh 2EADh 2EAEh CAN0 Mailbox10 : Time stamp XXXX XXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	2EA5h	CAN0 Mailbox10 : Data length		
2EA7h 2EA8h 2EA9h 2EAAh 2EABh 2EACh 2EADh 2EAEh 2EAFh XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				XXXX XXXX
2EA8h 2EA9h 2EAAh 2EABh 2EACh 2EACh 2EACh 2EAEh CAN0 Mailbox10 : Time stamp XXXXh				
2EA9h 2EAAh 2EABh 2EACh 2EACh 2EADh 2EAEh 2EAFh XXXXh XXXXh		1		AAAA AAAAN
2EAAh 2EABh 2EACh 2EADh 2EAEh 2EAFh CAN0 Mailbox10 : Time stamp XXXXh				
2EABh 2EACh 2EADh 2EAEh 2EAFh CAN0 Mailbox10 : Time stamp XXXXh				
2EABh 2EACh 2EADh 2EAEh 2EAFh CAN0 Mailbox10 : Time stamp XXXXh	2EAAh			
2EACh 2EADh 2EAEh 2EAEh 2EAFh CAN0 Mailbox10 : Time stamp XXXXh		1		
2EADh 2EAEh 2EAFh CAN0 Mailbox10 : Time stamp XXXXh		1		
2EAEh CAN0 Mailbox10 : Time stamp XXXXXh				
2EAEh CAN0 Mailbox10 : Time stamp XXXXXh	2EADh			
2EAFh		CAN0 Mailbox10 : Time stamp		XXXXh
		1		
	Y : Undofined		L	

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (15) (1) **Table 4.15**

A -1 -1	Desistes	O: ::==b = l	A #4 4
Address	Register	Symbol	After reset
2EB0h	CAN0 Mailbox11 : Message ID	C0MB11	XXXX XXXXh
2EB1h			
2EB2h			
	4		
2EB3h		1	
2EB4h			
2EB5h	CAN0 Mailbox11 : Data length	1	XXh
2EB6h	CAN0 Mailbox11 : Data field	1	XXXX XXXX
2EB7h	of the management of the manag		
	4		XXXX XXXXh
2EB8h			
2EB9h			
2EBAh			
2EBBh			
2EBCh			
2EBDh	4		
		4	2000
2EBEh	CAN0 Mailbox11 : Time stamp		XXXXh
2EBFh			
2EC0h	CAN0 Mailbox12 : Message ID	C0MB12	XXXX XXXXh
2EC1h		· ·	
2EC2h			
2EC3h]	
2EC4h			
2EC5h	CAN0 Mailbox12 : Data length	1	XXh
2EC6h	CAN0 Mailbox12 : Data field	1	XXXX XXXX
2EC7h			
		1	XXXX XXXXh
2EC8h			
2EC9h			
2ECAh			
2ECBh			
2ECCh	1		
2ECDh			
	CANOM III 40 Ti	4	20000
2ECEh	CAN0 Mailbox12 : Time stamp		XXXXh
2ECFh			
2ED0h	CAN0 Mailbox13 : Message ID	C0MB13	XXXX XXXXh
2ED1h			
2ED2h			
2ED3h			
		4	
2ED4h		1	
2ED5h	CAN0 Mailbox13 : Data length		XXh
2ED6h	CAN0 Mailbox13 : Data field	1	XXXX XXXX
2ED7h	1		XXXX XXXXh
2ED8h			^^^^
2LD011	-		
2ED9h			
2EDAh			
2EDBh			
2EDCh	1		
2EDDh	†	1	
2EDEh	CANO Mailhay12 : Time atamp	1	XXXXh
	CAN0 Mailbox13 : Time stamp		^^^^!
2EDFh		L	
2EE0h	CAN0 Mailbox14 : Message ID	C0MB14	XXXX XXXXh
2EE1h			
2EE2h	1		
05501	1		
2EE3h		1	
2EE4h	LOANOM III. 44 B. (L. (I	4	200
2EE5h	CAN0 Mailbox14 : Data length	1	XXh
2EE6h	CAN0 Mailbox14 : Data field		XXXX XXXX
2EE7h			XXXX XXXXh
2EE8h	1		
2EE9h	†		
	1		
2EEAh			
2EEBh			
2EECh			
2EEDh		1	
2EEEh	CAN0 Mailbox14 : Time stamp	1	XXXXh
	Orato manbox 11. Timo stamp		700011
2EEFh		l	1
V · Undofined			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (16) (1) **Table 4.16**

Address	Register	Symbol	After reset
2EF0h	CAN0 Mailbox15 : Message ID	C0MB15	XXXX XXXXh
2EF1h	de la transmission de la massaga la	002.0	70001700011
	1		
2EF2h			
2EF3h			
2EF4h			
	CANO Mailbox45 : Data length	_	VVh
2EF5h	CANO Mailbox15 : Data length	-	XXh
2EF6h	CAN0 Mailbox15 : Data field		XXXX XXXX
2EF7h			XXXX XXXXh
2EF8h			
2EF9h			
	4		
2EFAh			
2EFBh			
2EFCh			
2EFDh			
	CANON III. 45 Ti	<u> </u>	2000
2EFEh	CAN0 Mailbox15 : Time stamp		XXXXh
2EFFh			
2F00h			
2F01h			
2F02h		+	+
		+	+
2F03h			
2F04h		1	
2F05h			
2F06h		+	
		+	+
2F07h			
2F08h			
2F09h			
2F0Ah		1	
2F0Bh			+
		1	
2F0Ch			
2F0Dh			
2F0Eh			
2F0Fh			+
		0014/50	1000000000
2F10h	CAN0 Mask Register 0	C0MKR0	XXXX XXXXh
2F11h			
2F12h			
2F13h	4		
		00111/01	1000000000
2F14h	CAN0 Mask Register 1	C0MKR1	XXXX XXXXh
2F15h			
2F16h			
2F17h			
		0014/00	100000000
2F18h	CAN0 Mask Register 2	C0MKR2	XXXX XXXXh
2F19h			
2F1Ah	1		
2F1Bh			
	CANON L. D	COMMISSO	100000000
2F1Ch	CAN0 Mask Register 3	C0MKR3	XXXX XXXXh
2F1Dh			
2F1Eh			
2F1Fh			
	CANO FIFO Description ID Company Description C	COLIDODO	VVVV VVVVI
2F20h	CAN0 FIFO Received ID Compare Register 0	C0FIDCR0	XXXX XXXXh
2F21h		1	1
2F22h		1	1
2F23h		1	1
2F24h	CAN0 FIFO Received ID Compare Register 1	C0FIDCR1	XXXX XXXXh
2F25h	Onition in a recognition by compare register 1	301 1001(1	700070000
		1	I
2F26h		1	I
2F27h		1	I
2F28h			
2F29h		†	
	CANO Mook Involid Posistor	COMKINALD	VVVVh
2F2Ah	CAN0 Mask Invalid Register	C0MKIVLR	XXXXh
2F2Bh			
2F2Ch		1	
2F2Dh			
2F2Eh	CAN0 Mailbox Interrupt Enable Register	COMIER	XXXXh
	On the manbox interrupt Enable Neglotei	JOINILIX	AAAAII
2F2Fh			
2F30h	CAN0 Message Control Register 0	C0MCTL0	00h
2F31h	CAN0 Message Control Register 1	C0MCTL1	00h
2F32h	CANO Message Control Register 2	C0MCTL2	00h
2F33h	CAN0 Message Control Register 3	C0MCTL3	00h
2F34h	CAN0 Message Control Register 4	C0MCTL4	00h
2F35h	CAN0 Message Control Register 5	C0MCTL5	00h
2F36h	CANO Message Control Register 6	C0MCTL6	00h
2F37h	CANO Message Control Register 7	COMCTL7	
			00h
2F38h	CAN0 Message Control Register 8	C0MCTL8	00h
2F39h	CAN0 Message Control Register 9	C0MCTL9	00h
2F3Ah	CAN0 Message Control Register 10	C0MCTL10	00h
		CONTOTETO	3011
X: Undefined			

X : Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	After reset
2F3Bh	CAN0 Message Control Register 11	C0MCTL11	00h
2F3Ch	CAN0 Message Control Register 12	C0MCTL12	00h
2F3Dh	CAN0 Message Control Register 13	C0MCTL13	00h
2F3Eh	CAN0 Message Control Register 14	C0MCTL14	00h
2F3Fh	CAN0 Message Control Register 15	C0MCTL15	00h
2F40h	CAN0 Control Register	C0CTLR	0000 0101b
2F41h			0000 0000b
2F42h	CAN0 Status Register	COSTR	0000 0101b
2F43h			0000 0000b
2F44h	CAN0 Bit Configuration Register	C0BCR	00 0000h
2F45h			
2F46h			
2F47h			
2F48h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
2F49h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
2F4Ah	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
2F4Bh	CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	XXh
2F4Ch	CAN0 Error Interrupt Enable Register	C0EIER	00h
2F4Dh	CAN0 Error Interrupt Factor Judge Register	C0EIFR	00h
2F4Eh	CAN0 Reception Error Count Register	C0RECR	00h
2F4Fh	CAN0 Transmission Error Count Register	C0TECR	00h
2F50h	CAN0 Error Code Store Register	C0ECSR	00h
2F51h	CAN0 Channel Search Support Register	C0CSSR	XXh
2F52h	CAN0 Mailbox Search Status Register	COMSSR	1000 0000b
2F53h	CAN0 Mailbox Search Mode Register	COMSMR	00h
2F54h	CAN0 Time Stamp Register	C0TSR	0000h
2F55h			
2F56h	CAN0 Acceptance Filter Support Register	C0AFSR	XXXXh
2F57h			
2F58h	CAN0 Test Control Register	C0TCR	00h
<u> </u>			
2FFFh			

X: Undefined

Table 4.18 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:	•		
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:	•		•
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
<u>:</u>			•
FFF3h	ID5		(Note 2)
<u>:</u>			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7	·	(Note 2)
<u>:</u>			
FFFFh	Option Function Select Register	OFS	(Note 1)

- The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
 Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
 - When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
- When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.

 The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

 Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh. When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user. When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

^{1.} The blank areas are reserved and cannot be accessed by users.

5. **Electrical Characteristics**

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

Table 5.1 **Absolute Maximum Ratings**

Symbol	Parameter	Condition	Rated Value	Unit
Vcc/AVcc	Supply voltage		-0.3 to 6.5	V
Vı	Input voltage (1)		-0.3 to Vcc + 0.3	V
IIN	Input current (1)	(2, 3, 4)	-4 to 4	mA
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	-40 °C ≤ Topr < 85 °C	300	mW
		$85 ^{\circ}C \leq T_{opr} < 125 ^{\circ}C$	125	mW
Topr	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
Tstg	Storage temperature		-65 to 150	°C

- 1. Meet the specified range for the input voltage or the input current.
- Applicable ports: P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5
 The total input current must be 12 mA or less.
- 4. Even if no voltage is supplied to Vcc, the input current may cause the MCU to be powered on and operate. When a voltage is supplied to Vcc, the input current may cause the supply voltage to rise. Since operations in any cases other than above are not guaranteed, use the power supply circuit in the system to ensure the supply voltage for the MCU is stable within the specified range.

Table 5.2 Recommended Operating Conditions (1)

Courselle ed		Parameter		Constitions	Standard			Unit	
Symbol				Conditions	Min.	Тур.	Max.	Unit	
Vcc/AVcc	Supply voltage					2.7	-	5.5	V
Vss/AVss	Supply voltage					-	0	-	V
VIH	Input "H" voltage	Other th	an CMOS inp	out		0.8 Vcc	-	Vcc	V
		CMOS	Inputlevel		4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	=	Vcc	V
		input	switching	: 0.35 Vcc	2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	=	Vcc	V
			function (I/O port)	Input level selection	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	=	Vcc	V
			(I/O port)	: 0.5 Vcc	2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	=	Vcc	V
					4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	=	Vcc	V
				: 0.7 Vcc	2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	=	Vcc	V
		Externa	l clock input	(XOUT)		1.2	-	Vcc	V
VIL	Input "L" voltage	Other th	an CMOS inp	out		0	-	0.2 Vcc	V
		CMOS Input level		Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	-	0.2 Vcc	V
		input			2.7 V ≤ Vcc < 4.0 V	0	-	0.2 Vcc	V
		(I/O port)	function	I/O port) Input level selection	4.0 V ≤ Vcc ≤ 5.5 V	0	-	0.4 Vcc	V
			(I/O port)		2.7 V ≤ Vcc < 4.0 V	0	-	0.3 Vcc	V
			Input level selection	4.0 V ≤ Vcc ≤ 5.5 V	0	-	0.55 Vcc	V	
					2.7 V ≤ Vcc < 4.0 V	0	-	0.45 Vcc	V
		Externa	nal clock input (XOUT)			0	-	0.4	V
IOH(sum)	Peak sum output "H"	current	Sum of all	pins IOH(peak)		=	-	-80	mA
IOH(sum)	Average sum output "I	d" current	Sum of all	pins IOH(avg)		=	-	-40	mΑ
IOH(peak)	Peak output "H" curre	ent				=	-	-10	mA
IOH(avg)	Average output "H" c	urrent				=	-	-5	mΑ
IOL(sum)	Peak sum output "L"	current	Sum of all	pins IOL(peak)		=	-	80	mΑ
IOL(sum)	Average sum output "l	L" current	Sum of all	pins IOL(avg)		=	-	40	mΑ
IOL(peak)	Peak output "L" curre	ent				=	-	10	mΑ
IOL(avg)	Average output "L" c	urrent				-	_	5	mΑ
f(XIN)	XIN clock input oscill	ation freq	tion frequency		2.7 V ≤ Vcc ≤ 5.5 V	=	-	20	MHz
fOCO40M	Count source for time	er RC, timer RD, or timer RG			2.7 V ≤ Vcc ≤ 5.5 V	32	-	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	=	-	20	MHz
=	System clock frequer	псу			2.7 V ≤ Vcc ≤ 5.5 V	=	-	20	MHz
f(BCLK)	CPU clock frequency	,			2.7 V ≤ Vcc ≤ 5.5 V	-	_	20	MHz

^{1.} Vcc = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.

^{2.} The average output current indicates the average value of current measured during 100 ms.

Table 5.3 Recommended Operating Conditions (2)

Symbol	Parameter		Conditions	;	Unit		
Syllibol			Conditions	Min.	Тур.	Max.	Offic
IIC(H)	High input injection current	P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5	V _I > V _{CC}	-	-	2	mA
IIC(L)	Low input injection current	P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5	V _I > V _{SS}	=	=	-2	mA
Σ IIC	Total injection curre	otal injection current		-	-	8	mA

1. Vcc = 2.7 to 5.5 V at $T_{OPT} = -40$ to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.

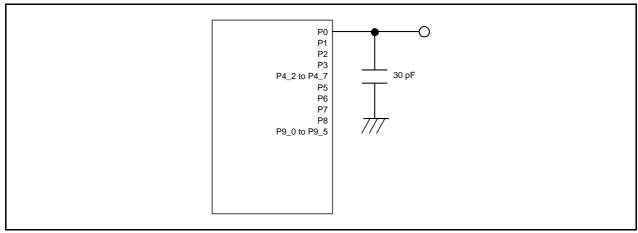


Figure 5.1 Ports P0 to P3, P4_2 to P4_7, P5 to P8, and P9_0 to P9_5 Timing Measurement Circuit

Table 5.4 A/D Converter Characteristics

Symbol	Doromo	Parameter Conditions		anditiona		Standard			
Syllibol	Faiaille	iei		Dialions	Min.	Тур.	Max.	Unit	
=	Resolution		Vref = AVCC		-	_	10	Bit	
-	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	-	_	±3	LSB	
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	-	-	±5	LSB	
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	-	-	±2	LSB	
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	-	-	±2	LSB	
φAD	A/D conversion cloc	k	$4.0 \le \text{Vref} = \text{AVCC} = \le 5.5 \ (2)$		2	_	20	MHz	
			2.7 ≤ Vref = AVCC = ≤ 5.5 ⁽²⁾		2	_	10	MHz	
_	Tolerance level impe	edance			_	3	_	kΩ	
Ivref	Vref current		Vcc = 5.0 V, XIN = f1	= φAD = 20 MHz	_	45	_	μА	
tconv	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, (AD = 20 MHz	2.2	=	-	μS	
		8-bit mode	Vref = AVCC = 5.0 V, (AD = 20 MHz	2.2	_	_	μS	
tsamp	Sampling time		φAD = 20 MHz		0.75	_	_	μS	
Vref	Reference voltage				2.7	_	AVcc	V	
VIA	Analog input voltage	(3)			0	_	Vref	V	
OCVREF	On-chip reference v	oltage	$2 \text{ MHz} \le \phi \text{AD} \le 4 \text{ MH}$	z	1.14	1.34	1.54	V	

- 1. $Vcc/AVcc = V_{ref} = 2.7 \text{ to } 5.5 \text{ V}$, Vss = 0 V at $T_{opr} = -40 \text{ to } 85^{\circ}\text{C}$ (J version) / -40 to 125°C (K version), unless otherwise specified.
- 2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
- 3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions		Stan	dard	Unit
Syllibol	Parameter	Conditions	Min.	Тур.	Max.	Ullit
=	Program/erase endurance (2)	R8C/38X, R8C/38Z Group	100 ⁽³⁾	=	=	times
		R8C/38W, R8C/38Y Group	1,000 (3)	-	-	times
=	Byte program time (program/erase endurance ≤ 1,000 times)		-	60	300	μS
=	Byte program time (program/erase endurance > 1,000 times)		-	60	500	μS
=	Word program time (program/erase endurance ≤ 1,000 times)		=	100	400	μS
=	Word program time (program/erase endurance > 1,000 times)		=	100	650	μS
_	Block erase time		_	0.3	4	S
td(SR-SUS)	Time delay from suspend request until suspend		=	_	5+CPU clock × 3 cycles	ms
=	Interval from erase start/restart until following suspend request		0	_	_	μS
=	Time from suspend until erase restart		-	_	30+CPU clock × 1 cycle	μS
td(CMDRST- READY)	Time from when command is forcibly terminated until reading is enabled		=	_	30+CPU clock × 1 cycle	μS
_	Program, erase voltage		2.7	_	5.5	V
_	Read voltage		2.7	_	5.5	V
=	Program, erase temperature		-40	_	85 (J version) 125 (K version)	°C
_	Data hold time (7)	Ambient temperature = 55°C (8)	20	-	-	year

- Notes: 1. VCC = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version) (under consideration), unless otherwise
 - 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.
 - If the programming and erasure endurance is n (n = 100, 1,000), each block can be erased n times. For example, if 1,024 1byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 - However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
 - 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
 - 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
 - 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
 - 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
 - The data hold time includes time that the power supply is off or the clock is not supplied.
 - 8. This data hold time includes 3,000 hours in Ta = 125°C and 7,000 hours in Ta = 85°C.

Table 5.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Cymphal	Dorometer	Conditions		Standard			
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
-	Program/erase endurance (2)		10,000 (3)	-	_	times	
_	Byte program time (program/erase endurance ≤ 1,000 times)		=	160	950	μS	
_	Byte program time (program/erase endurance > 1,000 times)		_	300	950	μS	
_	Block erase time (program/erase endurance ≤ 1,000 times)		_	0.2	1	S	
_	Block erase time (program/erase endurance > 1,000 times)		_	0.3	1	S	
td(SR-SUS)	Time delay from suspend request until suspend		-	-	3+CPU clock × 3 cycles	ms	
_	Interval from erase start/restart until following suspend request		0	-	_	μS	
_	Time from suspend until erase restart		-	-	30+CPU clock × 1 cycle	μS	
td(CMDRST- READY)	Time from when command is forcibly terminated until reading is enabled		-	-	30+CPU clock × 1 cycle	μS	
_	Program, erase voltage		2.7	-	5.5	V	
_	Read voltage		2.7	-	5.5	V	
_	Program, erase temperature		-40	-	85 (J version) 125 (K version)	°C	
=	Data hold time (7)	Ambient temperature = 55 °C (8)	20	-	-	year	

Notes:

- 1. Vcc = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100, 1,000, 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.
- 8. This data hold time includes 3,000 hours in Ta = 125°C and 7,000 hours in Ta = 85°C.

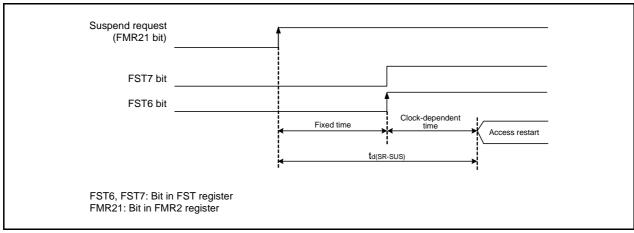


Figure 5.2 Time delay until Suspend

Table 5.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Syllibol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet0	Voltage detection level	At the falling of Vcc	2.70	2.85	3.00	V
_	Voltage detection 0 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet0 – 0.1) V	-	6	150	μS
=	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	-	1.5	-	μΑ
td(E-A)	Wait time until voltage detection circuit operation starts (2)		-	=	100	μS

Notes:

- 1. The measurement condition is Vcc = 2.7 V to 5.5 V and Topr = -40 to 85°C (J version) / -40 to 125°C (K version).
- 2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
- 3. Time until the voltage monitor 0 reset is generated after the voltage passes Vdeto.

Table 5.8 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition			Unit	
Symbol	Farameter	Condition	Min.	Тур.	Max. 3.45 3.60 3.75 3.90 4.05 4.20 4.35 4.50 —	Offic
Vdet1	Voltage detection level Vdet1_7 (2)	At the falling of Vcc	3.05	3.25	3.45	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.20	3.40	3.60	V
	Voltage detection level Vdet1_9 (2)	At the falling of Vcc	3.35	3.55	3.75	V
	Voltage detection level Vdet1_A (2)	At the falling of Vcc	3.50	3.70	3.90	V
	Voltage detection level Vdet1_B (2)	At the falling of Vcc	3.65	3.85	4.05	V
	Voltage detection level Vdet1_C (2)	At the falling of Vcc	3.80	4.00	4.20	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.95	4.15	4.35	V
	Voltage detection level Vdet1_E (2)	At the falling of Vcc	4.10	4.30	4.50	V
_	Hysteresis width at the rising of Vcc in voltage detection 1 circuit		-	0.1	-	V
=	Voltage detection 1 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet1_7 - 0.1) V	-	60	150	μS
=	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	=	1.7	=	μΑ
td(E-A)	Wait time until voltage detection circuit operation starts (4)		-	=	100	μS

Notes:

- 1. The measurement condition is Vcc = 2.7 V to 5.5 V and Topr = -40 to 85°C (J version) / -40 to 125°C (K version).
- 2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
- 3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
- 4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.9 Voltage Detection 2 Circuit Electrical Characteristics

Cumbal	Parameter	Condition		Unit		
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
Vdet2	Voltage detection level Vdet2	At the falling of Vcc	3.80	4.00	4.20	V
_	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		-	0.1	-	V
_	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet2 – 0.1) V	-	20	150	μS
_	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	-	1.7	-	μΑ
td(E-A)	Wait time until voltage detection circuit operation starts (3)		_	-	100	μЅ

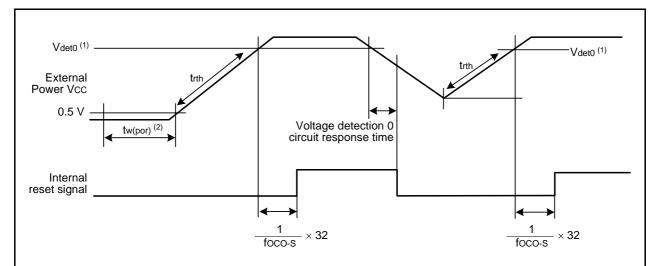
- 1. The measurement condition is Vcc = 2.7 V to 5.5 V and $T_{opr} = -40$ to $85^{\circ}C$ (J version) / -40 to $125^{\circ}C$ (K version).
- 2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.



Table 5.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽²⁾

Symbol	Parameter	Condition		Unit		
	Farameter	Condition	Min.	Тур.	Max.	Offic
trth	External power Vcc rise gradient	(1)	0	-	50000	mV/msec

- 1. The measurement condition is Vcc = 2.7 V to 5.5 V and $T_{opr} = -40$ to 85°C (J version) / -40 to 125°C (K version).
- 2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



- 1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware (REJ09B0613) for details.
- 2. tw(por) indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Standard		Unit	
Symbol	Farameter	Condition	Min.	Тур.	Max.	Orint	
_	High-speed on-chip oscillator frequency after reset	Vcc = 2.7 to 5.5 V, $-40^{\circ}C \leq T_{opr} \leq 85^{\circ}C \text{ (J version)} /$	-	40	_	MHz	
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽³⁾	-40°C ≤ Topr ≤ 125°C (K version)	=	36.864	=	MHz	
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register		-	32	=	MHz	
	High-speed on-chip oscillator frequency temperature • supply voltage dependence (2)		- 5	_	5	%	
_	Oscillation stabilization time		=	200	=	μS	
=	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	400	=	μΑ	

- 1. The measurement condition is Vcc = 2.7 to 5.5 V and Topr = -40 to 85°C (J version) / -40 to 125°C (K version).
- 2. This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.
- 3. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Faianielei	Condition	Min.	Тур.	Max.	Offit
fOCO-S	Low-speed on-chip oscillator frequency		112.5	125	137.5	kHz
fOCO-WDT	Low-speed on-chip oscillator frequency for watchdog timer		112.5	125	137.5	kHz
_	Oscillation stabilization time	Vcc = 5.0 V, Topr = 25°C	-	30	100	μS
-	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	3	_	μА

Note:

1. The measurement condition is Vcc = 2.7 to 5.5 V and Topr = -40 to 85°C (J version) / -40 to 125°C (K version).

Table 5.13 Power Supply Circuit Timing Characteristics

Svmbol	Parameter	Condition	0)	Unit		
Syllibol	r arameter	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		ı	ı	2000	μS

- 1. The measurement condition is Vcc = 2.7 to 5.5 V and $T_{opr} = -40$ to 85°C (J version) / -40 to 125°C (K version).
- 2. Wait time until the internal power supply generation circuit stabilizes during power-on.

Table 5.14 Timing Requirements of SSU (1)

Cumbal	Parameter		Conditions		Standard			
Symbol	Paramete) I	Conditions	Min.	Тур.	Max.	Unit	
tsucyc	SSCK clock cycle tim	е		4	=	=	tcyc (2)	
tHI	SSCK clock "H" width			0.4	_	0.6	tsucyc	
tLO	SSCK clock "L" width	SSCK clock "L" width		0.4	-	0.6	tsucyc	
trise	SSCK clock rising	Master		-	=	1	tcyc (2)	
<u></u>	time	Slave		-	=	1	μS	
tFALL	SSCK clock falling time	Master		-	=	1	tcyc (2)	
		Slave		-	-	1	μS	
tsu	SSO, SSI data input	setup time		100	=	=	ns	
tн	SSO, SSI data input I	nold time		1	=	=	tcyc (2)	
tLEAD	SCS setup time	Slave		1tcyc + 50	_	_	ns	
tlag	SCS hold time	Slave		1tcyc + 50	_	_	ns	
ton	SSO, SSI data output	t delay time		-	=	1	tcyc (2)	
tsa	SSI slave access time		2.7 V ≤ Vcc ≤ 5.5 V	-	-	1.5tcyc + 100	ns	
tor	SSI slave out open tir	me	2.7 V ≤ Vcc ≤ 5.5 V	-	=	1.5tcyc + 100	ns	

- 1. The measurement condition is Vcc = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
- 2. $1 \text{tcyc} = \frac{1}{f1(s)}$

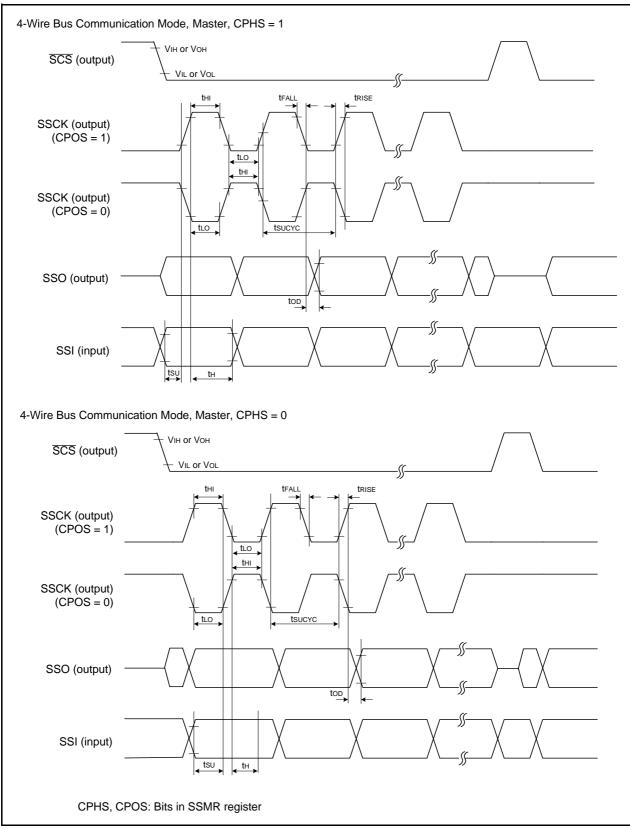


Figure 5.4 I/O Timing of SSU (Master)

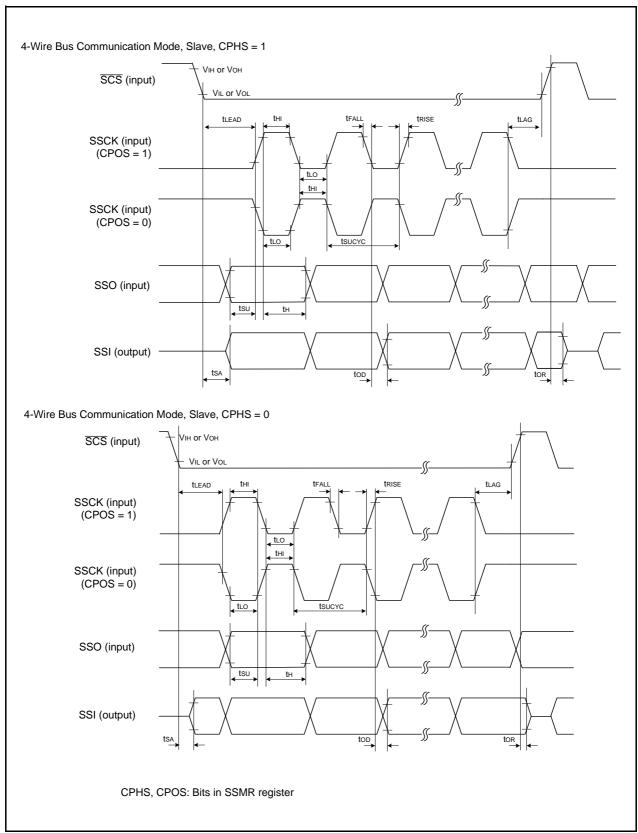


Figure 5.5 I/O Timing of SSU (Slave)

Figure 5.6 I/O Timing of SSU (Clock Synchronous Communication Mode)



Table 5.15 Electrical Characteristics (1) [4.2 V \leq Vcc \leq 5.5 V]

Symbol		Parameter	Condition	Si	tandard		Unit
Symbol		Parameter	Condition	Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Other than XOUT	Iон = −5 mA	Vcc - 2.0	1	Vcc	V
			Ioн = -200 μA	Vcc - 0.3	1	Vcc	V
		XOUT	IOH = -200 μA	1.0	1	Vcc	V
Vol	Output "L" voltage	Other than XOUT	IoL = 5 mA	=	_	2.0	V
			Ιοι = 200 μΑ	-	1	0.45	V
		XOUT	IOH = -200 μA	-	1	0.5	V
VT+-VT-	Hysteresis	INTO to INT4, KIO to KI3, TRAIOO, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOAO to TRDIODO, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, TRGCLKB, TRCTRG, ADTRG, RXD0 to RXD2, CLKO to CLK2, SDA2, SSO		0.1	1.2	-	V
		RESET		0.1	1.2	-	V
lін	Input "H" current		VI = 5 V	_	1	1.0	μΑ
lıL	Input "L" current		VI = 0 V	=	-	-1.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V	25	50	100	kΩ
RfXIN	Feedback resistance	XIN		-	0.3	-	ΜΩ
VRAM	RAM hold voltage	•	During stop mode	2.0	_	-	V

^{1.} $4.2 \text{ V} \le \text{Vcc} \le 5.5 \text{ V}$ at $\text{Topr} = -40 \text{ to } 85^{\circ}\text{C}$ (J version) / $-40 \text{ to } 125^{\circ}\text{C}$ (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.16 Electrical Characteristics (2) [3.3 V \leq Vcc \leq 5.5 V] (Topr = -40 to 85°C (J version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard	t	Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	7.0	15	mA
	Single-chip mode, output pins are open, other pins		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	5.6	12.5	mA
	are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	3.6	=	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	3.0	ı	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	2.2	-	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5	_	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	7.0	15	mA
		(1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	_	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	180	μА
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	15	110	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	5	100	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2.0	5.0	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	15.0	=	μА

The typical value (Typ.) indicates the current value when the CPU and the memory operate.
 The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 5.17 Electrical Characteristics (3) [3.3 V \leq Vcc \leq 5.5 V] (Topr = -40 to 125°C (K version), unless otherwise specified.)

Symbol	Doromotor		Condition		Standard	t	Unit
Symbol	Parameter			Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	7.0	15	mA
Single-chip mode, output pins are open, other pins		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	5.6	12.5	mA	
	are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	3.6	ı	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	I	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	2.2	-	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5	-	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	7.0	15	mA
	(1)	(1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	-	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	400	μΑ
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	15	330	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	5	320	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	2.0	5.0	μА
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	60.0	_	μА

The typical value (Typ.) indicates the current value when the CPU and the memory operate.
 The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Timing Requirements

(Unless Otherwise Specified: VCC = 5 V, VSS = 0 V at $Topr = -40^{\circ}\text{C}$ to 85°C (J ver)/ -40°C to 125°C (K ver))

Table 5.18 External clock input (XOUT)

Symbol	Parameter		Standard		
Symbol	Falanielei	Min.	Max.	Unit	
tc(XOUT)	XOUT input cycle time	50	-	ns	
twh(xout)	XOUT input "H" width	24	-	ns	
twl(xout)	XOUT input "L" width	24	-	ns	

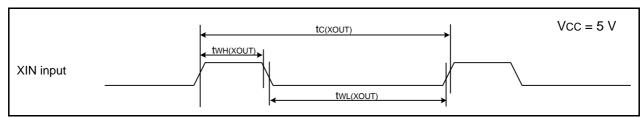


Figure 5.7 External Clock Input Timing Diagram when VCC = 5 V

Table 5.19 TRAIOi (i = 0 to 1) Input

Symbol	Parameter		Standard		
Symbol	Faianietei	Min. Max.	Unit		
tc(TRAIO)	TRAIOi (i = 0 to 1) input cycle time	100	=	ns	
twh(traio)	TRAIOi (i = 0 to 1) input "H" width	40	=	ns	
twl(traio)	TRAIOi (i = 0 to 1) input "L" width	40	=	ns	

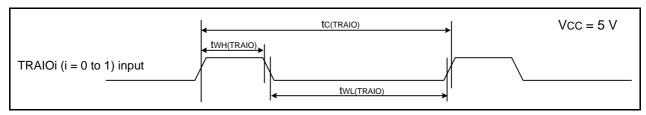


Figure 5.8 TRAIOi (i = 0 to 1) Input Timing Diagram when Vcc = 5 V

Table 5.20 TRFI Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(TRFI)	TRFI input cycle time	1200 (1)	-	ns	
twh(TRFI)	TRFI input "H" width	600 ⁽²⁾	_	ns	
tWL(TRFI)	TRFI input "L" width	600 (2)	=	ns	

- 1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
- 2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency \times 1.5) or above.

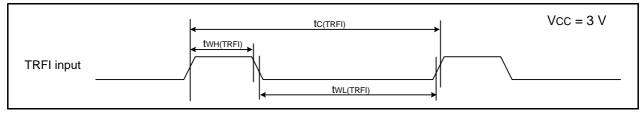


Figure 5.9 TRFI Input Timing Diagram when Vcc = 3 V

Table 5.21 Serial Interface

Symbol	Parameter		Standard		
			Max.	Unit	
tc(CK)	CLKi input cycle time	200	-	ns	
tW(CKH)	CLKi input "H" width	100	-	ns	
tW(CKL)	CLKi input "L" width	100	=	ns	
td(C-Q)	TXDi output delay time	=	90	ns	
th(C-Q)	TXDi hold time	0	=	ns	
tsu(D-C)	RXDi input setup time	50	=	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0 to 2

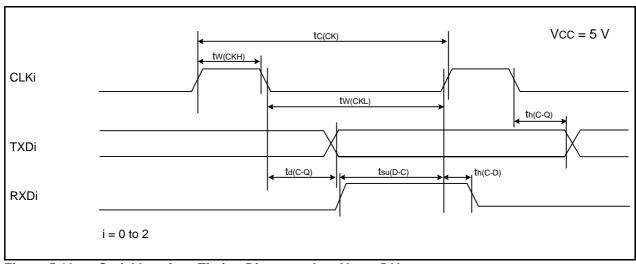


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.22 External Interrupt INTi (i = 0 to 4) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol	Parameter		Standard		
			Max.	Unit	
tW(INH)	INTi input "H" width, Kli input "H" width	250 (1)	-	ns	
tw(INL)	INTi input "L" width, Kli input "L" width	250 ⁽²⁾	I	ns	

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

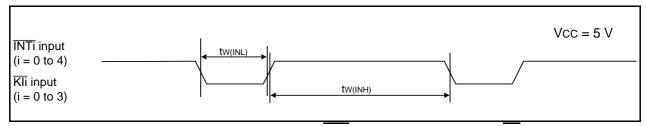


Figure 5.11 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 5 V

Table 5.23 Electrical Characteristics (4) [2.7 V \leq Vcc \leq 4.2 V]

Symbol	Parameter		Condition	St	Unit		
Symbol		Farameter	Condition	Min. Typ.		Max.	Offic
Vон	Output "H" voltage	Other than XOUT	IOH = −1 mA	Vcc - 0.5	-	Vcc	V
		XOUT	IoH = -200 μA	1.0	-	Vcc	V
Vol	Output "L" voltage	Other than XOUT	IoL = 1 mA	=	-	0.5	V
		XOUT	IoL = 200 μA	=	-	0.5	V
VT+-VT-	Hysteresis	INTO to INT4, KIO to KI3, TRAIOO, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOAO to TRDIODO, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, TRGCLKB, TRCTRG, ADTRG, RXD0 to RXD2, CLK0 to CLK2, SSI, SCL2, SDA2, SSO RESET		0.1	0.4	_	V
Іін	Input "H" current	REGET	VI = 3 V	=	=	1.0	μА
lıL	Input "L" current		VI = 0 V	=	=	-1.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V	42	84	168	kΩ
RfXIN	Feedback resistance	XIN		-	0.3	-	ΜΩ
VRAM	RAM hold voltage		During stop mode	2.0	=	_	V

^{1. 2.7} V ≤ Vcc ≤ 4.2 V at Topr = −40 to 85°C (J version) / −40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.24 Electrical Characteristics (5) [2.7 V \leq Vcc \leq 3.3 V] (Topr = -40 to 85°C (J version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
Cymbol				Min.	Тур.	Max.	OTIIL
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open,	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	7.0	14.5	mA
	other pins are Vss	er pins are Vss XIN = 16 MHZ (square wave)	ı	5.6	12.0	mA	
			I	3.6	1	mA	
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	1	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	=	2.2	=	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	_	mA
		High-speed on-chip oscillator	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	7.0	14.5	mA
		mode ⁽¹⁾	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	-	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	85	180	μА
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	15	110	μА
	Stop mode		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	=	5	100	μΑ
		XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	2.0	5.0	μА	
		XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	ļ	13.0	_	μА	

The typical value (Typ.) indicates the current value when the CPU and the memory operate.
 The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 5.25 Electrical Characteristics (6) [2.7 V \leq Vcc \leq 3.3 V] (Topr = -40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
3,				Min.	Тур.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open,	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	=	7.0	14.5	mA
	other pins are Vss		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	5.6	12.0	mA
	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	Low-speed on-chip oscillator on = 125 kHz	_	3.6	_	mA	
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8		3.0	-	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2.2	-	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	-	mA
	on-chi oscilla	High-speed on-chip oscillator	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	7.0	14.5	mA
		mode ⁽¹⁾	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	=	3.0	=	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	85	390	μА
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	=	15	320	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	5	310	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	2.0	5.0	μА
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	55.0	-	μА

The typical value (Typ.) indicates the current value when the CPU and the memory operate.
 The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Timing requirements

(Unless Otherwise Specified: VCC = 3 V, VSS = 0 V at $Topr = -40^{\circ}\text{C}$ to 85°C (J ver)/ -40°C to 125°C (K ver))

Table 5.26 External clock input (XOUT)

Symbol	Parameter		Standard		
			Max.	Unit	
tc(XOUT)	XOUT input cycle time	50	=	ns	
twh(xout)	XOUT input "H" width	24	=	ns	
twl(xout)	XOUT input "L" width	24	-	ns	

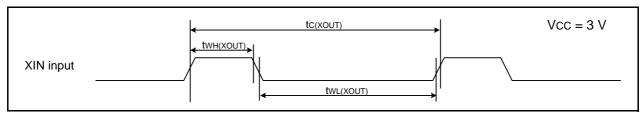


Figure 5.12 External Clock Input Timing Diagram when VCC = 3 V

Table 5.27 TRAIOi (i = 0 to 1) Input

Symbol	Parameter		Standard		
Symbol	raidilletei	Min.	Min. Max. 300 –	Unit	
tc(TRAIO)	TRAIOi (i = 0 to 1) input cycle time	300	=	ns	
tWH(TRAIO)	TRAIOi (i = 0 to 1) input "H" width	120	-	ns	
tWL(TRAIO)	TRAIOi (i = 0 to 1) input "L" width	120	-	ns	

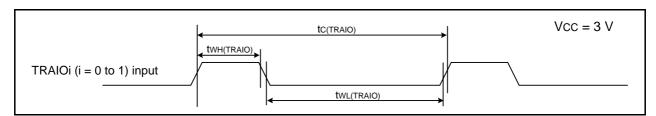


Figure 5.13 TRAIOi (i = 0 to 1) Input Timing Diagram when Vcc = 3 V

Table 5.28 TRFI Input

Symbol	Doromotor		Standard		
Symbol	Parameter	Min.	Min. Max. 400 (1) –	Unit	
tc(TRFI)	TRFI input cycle time	400 (1)	-	ns	
twh(TRFI)	TRFI input "H" width	200 (2)	_	ns	
twl(trfi)	TRFI input "L" width	200 (2)	=	ns	

- 1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
- 2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency \times 1.5) or above.

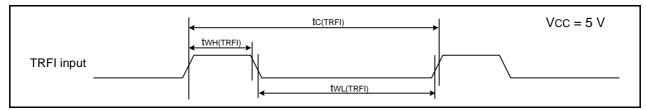


Figure 5.14 TRFI Input Timing Diagram when Vcc = 5 V

Table 5.29 Serial Interface

Symbol	Parameter	Standard		Unit
	Falanielei		Max.	
tc(CK)	CLKi input cycle time	300	-	ns
tW(CKH)	CLKi input "H" width	150	-	ns
tW(CKL)	CLKi Input "L" width	150	-	ns
td(C-Q)	TXDi output delay time	=	140	ns
th(C-Q)	TXDi hold time	0	=	ns
tsu(D-C)	RXDi input setup time	70	=	ns
th(C-D)	RXDi input hold time	90	=	ns

i = 0 to 2

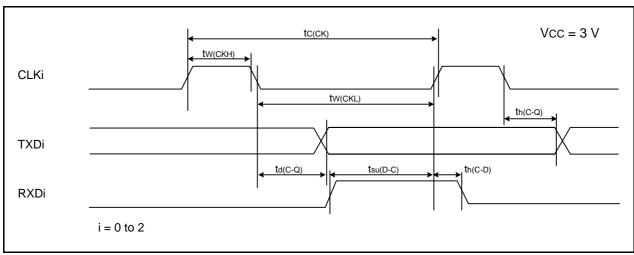


Figure 5.15 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.30 External Interrupt INTi (i = 0 to 4) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	Offic
tW(INH)	INTi input "H" width, Kli input "H" width	380 (1)	-	ns
tW(INL)	INTi input "L" width, Kli input "L" width	380 (2)	-	ns

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

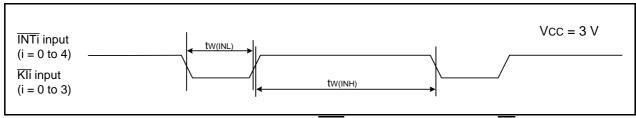
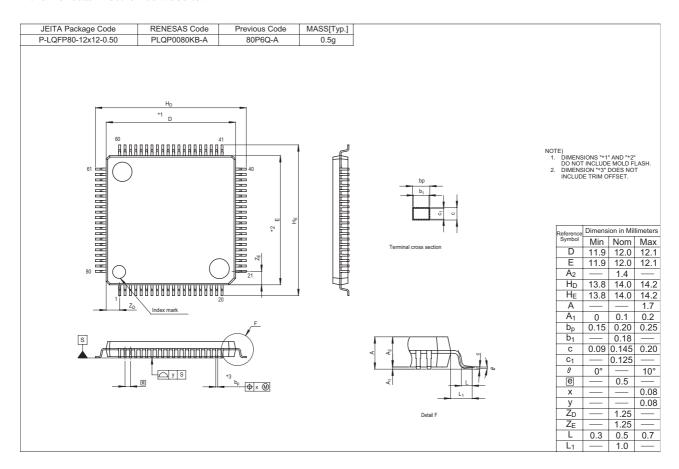


Figure 5.16 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 3 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Electronics website.



REVISION HISTORY	R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group
I REVIOIOIVIIIOTORI	Datasheet

Rev.	Date		Description		
		Page	Summary		
0.10	May 31, 2010	_	First Edition issued		

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

 The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

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Renesas Electronics America Inc. 2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A. Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited 1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH Arcadiastrasse 10, 40472 Düsseldorf, Germany Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Limites State United Programs From Limited Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong Tet: +952-2866-9318, Fax: +852-2866-9022/9044

Renesas Electronics Taiwan Co., Ltd.

7F, No. 363 Fu Shing North Road Taipei, Taiwar Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
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