# 1. Overview

## 1.1 Features

The R8C/38W Group, R8C/38X Group, R8C/38Y Group, and R8C/38Z Group of single-chip MCUs incorporate the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

The R8C/38W Group and R8C/38X Group have a single channel CAN module and are suitable for LAN systems in vehicles and for FA.

The R8C/38Y Group and R8C/38Z Group do not have CAN modules.

The R8C/38W Group and R8C/38Y Group have data flash (1 KB × 4 blocks) with the background operation (BGO) function.

### 1.1.1 Applications

Automobiles and others

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group
1. Overview

### 1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/38W Group, tables 1.3 and 1.4 outline the Specifications for R8C/38X Group, tables 1.5 and 1.6 outline the Specifications for R8C/38Y Group, and tables 1.7 and 1.8 outline the Specifications for R8C/38Z Group.

**Table 1.1    Specifications for R8C/38W Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>   50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operating mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.9 Product List for R8C/38W Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 75, selectable pull-up resistor |
| Clock | Clock generation circuits | 3 circuits:  XIN clock oscillation circuit (with on-chip feedback resistor),<br>         High-speed on-chip oscillator (with frequency adjustment function),<br>         Low-speed on-chip oscillator<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>   Standard operating mode (high-speed clock, high-speed on-chip oscillator,<br>   low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • Interrupt vectors: 69<br>• External: 9 sources (INT × 5, key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 40<br>• Transfer modes: 2 (normal mode, repeat mode) |

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                                1. Overview

**Table 1.2     Specifications for R8C/38W Group (2)**

| Item | Function | Specification |
|---|---|---|
| Timer | Timer RA0 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RA1 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits (with 4 capture/compare registers) × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits (with 4 capture/compare registers) × 2<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |
| | Timer RE | 8 bits × 1<br>Output compare mode |
| | Timer RF | 16 bits × 1<br>Input capture mode (input capture circuit), output compare mode (output compare circuit) |
| | Timer RG | 16 bits × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder) |
| Serial Interface | UART0, 1 | 2 channels<br>Clock synchronous serial I/O, UART |
| | UART2 | 1 channel<br>Clock synchronous serial I/O, UART, I$^2$C mode (I$^2$C-bus), IE mode (IEbus), multiprocessor communication function |
| Synchronous Serial Communication Unit (SSU) | | 1 channel |
| LIN Module | | Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1) |
| CAN Module | | 1 channel, 16 Mailboxes (conforms to the ISO 11898-1) |
| A/D Converter | | 10-bit resolution × 20 channels, includes sample and hold function, with sweep mode |
| Flash Memory | | • Programming and erasure voltage: VCC = 2.7 to 5.5 V<br>• Programming and erasure endurance: 10,000 times (data flash)<br>                                                                    1,000 times (program ROM)<br>• Program security: ROM code protect, ID code check<br>• Debug functions: On-chip debug, on-board flash rewrite function<br>• Background operation (BGO) function (data flash) |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) |
| Current Consumption | | Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) |
| Operating Ambient Temperature | | -40 to 85°C (J version)<br>-40 to 125°C (K version) [1] |
| Package | | 80-pin LQFP<br>   Package code: PLQP0080KB-A (previous code: 80P6Q-A) |

Note:
1.  Specify the K version if K version functions are to be used.

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                          1. Overview

**Table 1.3    Specifications for R8C/38X Group (1)**

| Item | Function | Specification |
|------|----------|---------------|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>    50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operating mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.10 Product List for R8C/38X Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 75, selectable pull-up resistor |
| Clock | Clock generation circuits | 3 circuits:  XIN clock oscillation circuit (with on-chip feedback resistor),<br>             High-speed on-chip oscillator (with frequency adjustment function),<br>             Low-speed on-chip oscillator<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>    Standard operating mode (high-speed clock, high-speed on-chip oscillator,<br>    low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • Interrupt vectors: 69<br>• External: 9 sources (INT × 5, key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 40<br>• Transfer modes: 2 (normal mode, repeat mode) |

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                     Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    1. Overview

**Table 1.4      Specifications for R8C/38X Group (2)**

| Item | Function | Specification |
|---|---|---|
| Timer | Timer RA0 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RA1 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits (with 4 capture/compare registers) × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits (with 4 capture/compare registers) × 2<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |
| | Timer RE | 8 bits × 1<br>Output compare mode |
| | Timer RF | 16 bits × 1<br>Input capture mode (input capture circuit), output compare mode (output compare circuit) |
| | Timer RG | 16 bits × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder) |
| Serial Interface | UART0, 1 | 2 channels<br>Clock synchronous serial I/O, UART |
| | UART2 | 1 channel<br>Clock synchronous serial I/O, UART, I$^2$C mode (I$^2$C-bus), IE mode (IEbus), multiprocessor communication function |
| Synchronous Serial Communication Unit (SSU) | | 1 channel |
| LIN Module | | Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1) |
| CAN Module | | 1 channel, 16 Mailboxes (conforms to the ISO 11898-1) |
| A/D Converter | | 10-bit resolution × 20 channels, includes sample and hold function, with sweep mode |
| Flash Memory | | • Programming and erasure voltage: VCC = 2.7 to 5.5 V<br>• Programming and erasure endurance: 100 times (program ROM)<br>• Program security: ROM code protect, ID code check<br>• Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) |
| Current Consumption | | Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) |
| Operating Ambient Temperature | | -40 to 85°C (J version)<br>-40 to 125°C (K version) [1] |
| Package | | 80-pin LQFP<br>Package code: PLQP0080KB-A (previous code: 80P6Q-A) |

Note:
 1.  Specify the K version if K version functions are to be used.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                              1. Overview

**Table 1.5    Specifications for R8C/38Y Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>  50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operating mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.11 Product List for R8C/38Y Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 75, selectable pull-up resistor |
| Clock | Clock generation circuits | 3 circuits:  XIN clock oscillation circuit (with on-chip feedback resistor),<br>             High-speed on-chip oscillator (with frequency adjustment function),<br>             Low-speed on-chip oscillator<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>  Standard operating mode (high-speed clock, high-speed on-chip oscillator,<br>  low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • Interrupt vectors: 69<br>• External: 9 sources (INT × 5, key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 40<br>• Transfer modes: 2 (normal mode, repeat mode) |

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    1. Overview

**Table 1.6    Specifications for R8C/38Y Group (2)**

| Item | Function | Specification |
|---|---|---|
| Timer | Timer RA0 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RA1 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits (with 4 capture/compare registers) × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits (with 4 capture/compare registers) × 2<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |
| | Timer RE | 8 bits × 1<br>Output compare mode |
| | Timer RF | 16 bits × 1<br>Input capture mode (input capture circuit), output compare mode (output compare circuit) |
| | Timer RG | 16 bits × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder) |
| Serial Interface | UART0, 1 | 2 channels<br>Clock synchronous serial I/O, UART |
| | UART2 | 1 channel<br>Clock synchronous serial I/O, UART, $I^2C$ mode ($I^2$C-bus), IE mode (IEbus), multiprocessor communication function |
| Synchronous Serial Communication Unit (SSU) | | 1 channel |
| LIN Module | | Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1) |
| A/D Converter | | 10-bit resolution × 20 channels, includes sample and hold function, with sweep mode |
| Flash Memory | | • Programming and erasure voltage: VCC = 2.7 to 5.5 V<br>• Programming and erasure endurance: 10,000 times (data flash)<br>                                                                    1,000 times (program ROM)<br>• Program security: ROM code protect, ID code check<br>• Debug functions: On-chip debug, on-board flash rewrite function<br>• Background operation (BGO) function (data flash) |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) |
| Current Consumption | | Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) |
| Operating Ambient Temperature | | -40 to 85°C (J version)<br>-40 to 125°C (K version) [1] |
| Package | | 80-pin LQFP<br>    Package code: PLQP0080KB-A (previous code: 80P6Q-A) |

Note:
1.  Specify the K version if K version functions are to be used.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group
1. Overview

**Table 1.7      Specifications for R8C/38Z Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>   50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operating mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.12 Product List for R8C/38Z Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 75, selectable pull-up resistor |
| Clock | Clock generation circuits | 3 circuits:  XIN clock oscillation circuit (with on-chip feedback resistor),<br>           High-speed on-chip oscillator (with frequency adjustment function),<br>           Low-speed on-chip oscillator<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>   Standard operating mode (high-speed clock, high-speed on-chip oscillator,<br>   low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • Interrupt vectors: 69<br>• External: 9 sources (INT × 5, key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 40<br>• Transfer modes: 2 (normal mode, repeat mode) |

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                            1. Overview

**Table 1.8    Specifications for R8C/38Z Group (2)**

| Item | Function | Specification |
|---|---|---|
| Timer | Timer RA0 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
|  | Timer RA1 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
|  | Timer RB | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
|  | Timer RC | 16 bits (with 4 capture/compare registers) × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
|  | Timer RD | 16 bits (with 4 capture/compare registers) × 2<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |
|  | Timer RE | 8 bits × 1<br>Output compare mode |
|  | Timer RF | 16 bits × 1<br>Input capture mode (input capture circuit), output compare mode (output compare circuit) |
|  | Timer RG | 16 bits × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder) |
| Serial Interface | UART0, 1 | 2 channels<br>Clock synchronous serial I/O, UART |
|  | UART2 | 1 channel<br>Clock synchronous serial I/O, UART, I$^2$C mode (I$^2$C-bus), IE mode (IEbus), multiprocessor communication function |
| Synchronous Serial Communication Unit (SSU) | | 1 channel |
| LIN Module | | Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1) |
| A/D Converter | | 10-bit resolution × 20 channels, includes sample and hold function, with sweep mode |
| Flash Memory | | • Programming and erasure voltage: VCC = 2.7 to 5.5 V<br>• Programming and erasure endurance: 100 times (program ROM)<br>• Program security: ROM code protect, ID code check<br>• Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) |
| Current Consumption | | Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) |
| Operating Ambient Temperature | | -40 to 85°C (J version)<br>-40 to 125°C (K version) [1] |
| Package | | 80-pin LQFP<br>Package code: PLQP0080KB-A (previous code: 80P6Q-A) |

Note:
1.  Specify the K version if K version functions are to be used.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                                      1. Overview

## 1.2    Product List

Table 1.9 lists Product List for R8C/38W Group, Table 1.10 lists Product List for R8C/38X Group, Table 1.11 lists Product List for R8C/38Y Group, and Table 1.12 lists Product List for R8C/38Z Group.

**Table 1.9    Product List for R8C/38W Group**                                 **Current of May 2010**

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|---|
| | Program ROM | Data flash | | | |
| R5F21388WJFP (D) | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0080KB-A | J version |
| R5F2138AWJFP (D) | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0080KB-A | |
| R5F2138CWJFP (D) | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0080KB-A | |
| R5F21388WKFP (D) | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0080KB-A | K version |
| R5F2138AWKFP (D) | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0080KB-A | |
| R5F2138CWKFP (D) | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0080KB-A | |

(D): Under development



Part No.    R 5 F 21 38 8 W J FP

Package type:
    FP: PLQP0080KB-A (0.50 mm pin-pitch, 12 mm square body)

CAN, Data Flash
    W: CAN module and Data Flash
    X : CAN module but no Data Flash
    Y : Data Flash but no CAN module
    Z : None

Classification
    J: Operating ambient temperature -40 °C to 85 °C
    K: Operating ambient temperature -40 °C to 125 °C

ROM capacity
    8: 64 KB
    A: 96 KB
    C: 128 KB

R8C/38W Group

R8C/3x Series

Memory type
    F: Flash memory

Renesas MCU

Renesas semiconductor

**Figure 1.1    Part Number, Memory Size, and Package of R8C/38W Group**

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                                          1. Overview

**Table 1.10      Product List for R8C/38X Group**                                             **Current of May 2010**

| Part No. | ROM Capacity Program ROM | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|
| R5F21388XJFP (D) | 64 Kbytes | 6 Kbytes | PLQP0080KB-A | J version |
| R5F2138AXJFP (D) | 96 Kbytes | 8 Kbytes | PLQP0080KB-A | |
| R5F2138CXJFP (D) | 128 Kbytes | 10 Kbytes | PLQP0080KB-A | |
| R5F21388XKFP (D) | 64 Kbytes | 6 Kbytes | PLQP0080KB-A | K version |
| R5F2138AXKFP (D) | 96 Kbytes | 8 Kbytes | PLQP0080KB-A | |
| R5F2138CXKFP (D) | 128 Kbytes | 10 Kbytes | PLQP0080KB-A | |

(D): Under development



Part No.   R 5 F 21 38 8 X J FP

Package type:
    FP: PLQP0080KB-A (0.50 mm pin-pitch, 12 mm square body)

CAN, Data Flash
    W: CAN module and Data Flash
    X : CAN module but no Data Flash
    Y : Data Flash but no CAN module
    Z : None

Classification
    J: Operating ambient temperature -40 °C to 85 °C
    K: Operating ambient temperature -40 °C to 125 °C

ROM capacity
    8: 64 KB
    A: 96 KB
    C: 128 KB

R8C/38X Group

R8C/3x Series

Memory type
    F: Flash memory

Renesas MCU

Renesas semiconductor

**Figure 1.2       Part Number, Memory Size, and Package of R8C/38X Group**

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group
1. Overview

**Table 1.11    Product List for R8C/38Y Group**    **Current of May 2010**

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|---|
| | Program ROM | Data flash | | | |
| R5F21388YJFP (D) | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0080KB-A | J version |
| R5F2138AYJFP (D) | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0080KB-A | |
| R5F2138CYJFP (D) | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0080KB-A | |
| R5F21388YKFP (D) | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0080KB-A | K version |
| R5F2138AYKFP (D) | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0080KB-A | |
| R5F2138CYKFP (D) | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0080KB-A | |

(D): Under development



Part No.    R 5 F 21 38 8 Y J FP

Package type:
    FP: PLQP0080KB-A (0.50 mm pin-pitch, 12 mm square body)

CAN, Data Flash
    W: CAN module and Data Flash
    X : CAN module but no Data Flash
    Y : Data Flash but no CAN module
    Z : None

Classification
    J: Operating ambient temperature -40 °C to 85 °C
    K: Operating ambient temperature -40 °C to 125 °C

ROM capacity
    8: 64 KB
    A: 96 KB
    C: 128 KB

R8C/38Y Group

R8C/3x Series

Memory type
    F: Flash memory

Renesas MCU

Renesas semiconductor

**Figure 1.3    Part Number, Memory Size, and Package of R8C/38Y Group**

*Under development* Preliminary document
Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    1. Overview

**Table 1.12      Product List for R8C/38Z Group**                    **Current of May 2010**

| Part No. | ROM Capacity Program ROM | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|
| R5F21388ZJFP (D) | 64 Kbytes | 6 Kbytes | PLQP0080KB-A | J version |
| R5F2138AZJFP (D) | 96 Kbytes | 8 Kbytes | PLQP0080KB-A | |
| R5F2138CZJFP (D) | 128 Kbytes | 10 Kbytes | PLQP0080KB-A | |
| R5F21388ZKFP (D) | 64 Kbytes | 6 Kbytes | PLQP0080KB-A | K version |
| R5F2138AZKFP (D) | 96 Kbytes | 8 Kbytes | PLQP0080KB-A | |
| R5F2138CZKFP (D) | 128 Kbytes | 10 Kbytes | PLQP0080KB-A | |

(D): Under development



Part No.   R 5 F 21 38 8 Z J FP

Package type:
    FP: PLQP0080KB-A (0.50 mm pin-pitch, 12 mm square body)

CAN, Data Flash
    W: CAN module and Data Flash
    X : CAN module but no Data Flash
    Y : Data Flash but no CAN module
    Z : None

Classification
    J: Operating ambient temperature -40 °C to 85 °C
    K: Operating ambient temperature -40 °C to 125 °C

ROM capacity
    8: 64 KB
    A: 96 KB
    C: 128 KB

R8C/38Z Group

R8C/3x Series

Memory type
    F: Flash memory

Renesas MCU

Renesas semiconductor

**Figure 1.4      Part Number, Memory Size, and Package of R8C/38Z Group**

*Under development* Preliminary document
Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

1. Overview

## 1.3 Block Diagram

Figure 1.5 shows a Block Diagram.



**Figure 1.5    Block Diagram**

*Under development* Preliminary document
Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    1. Overview
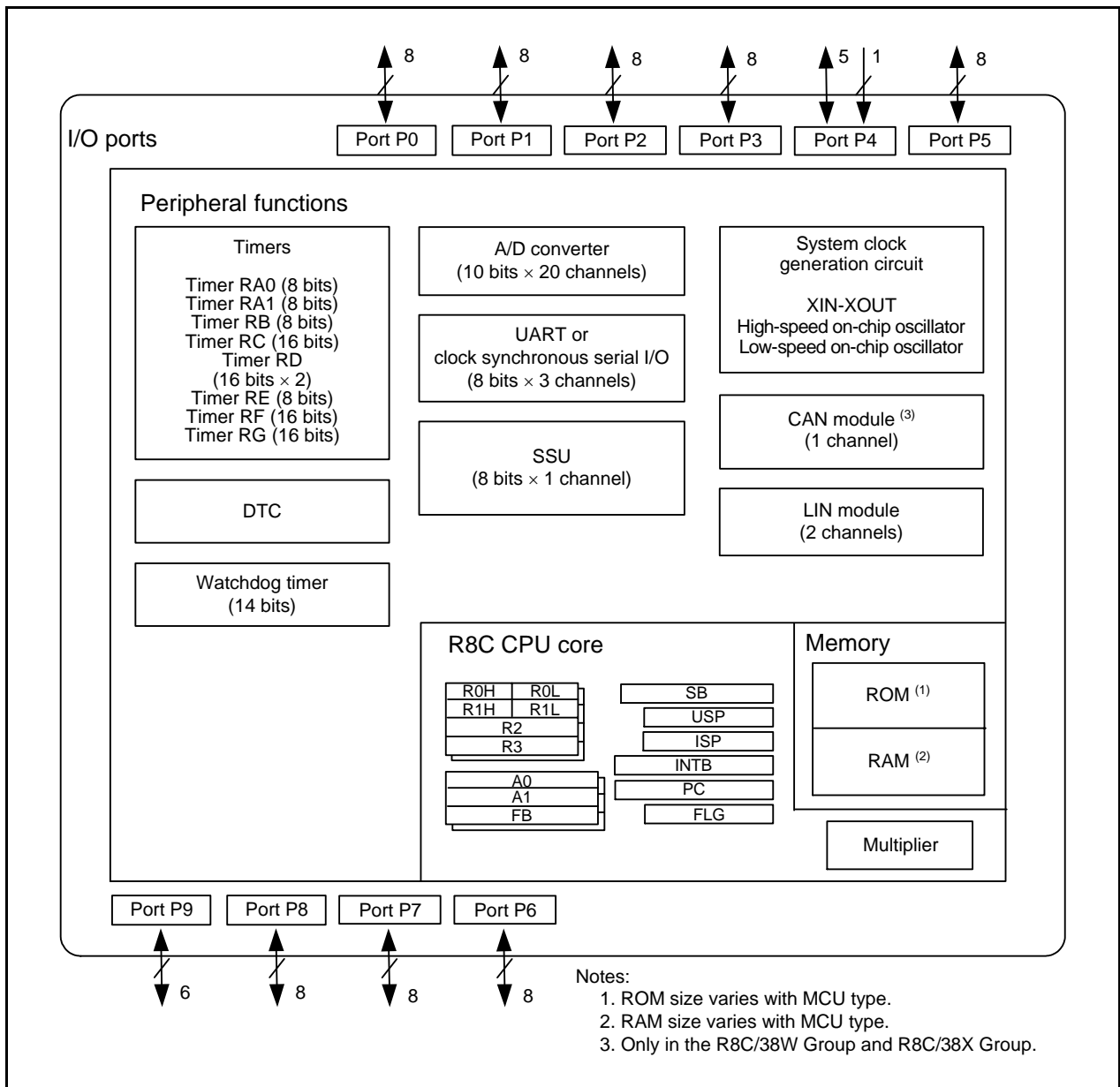
## 1.4    Pin Assignment

Figure 1.6 shows Pin Assignment (Top View). Tables 1.13 and 1.14 outline the Pin Name Information by Pin Number.



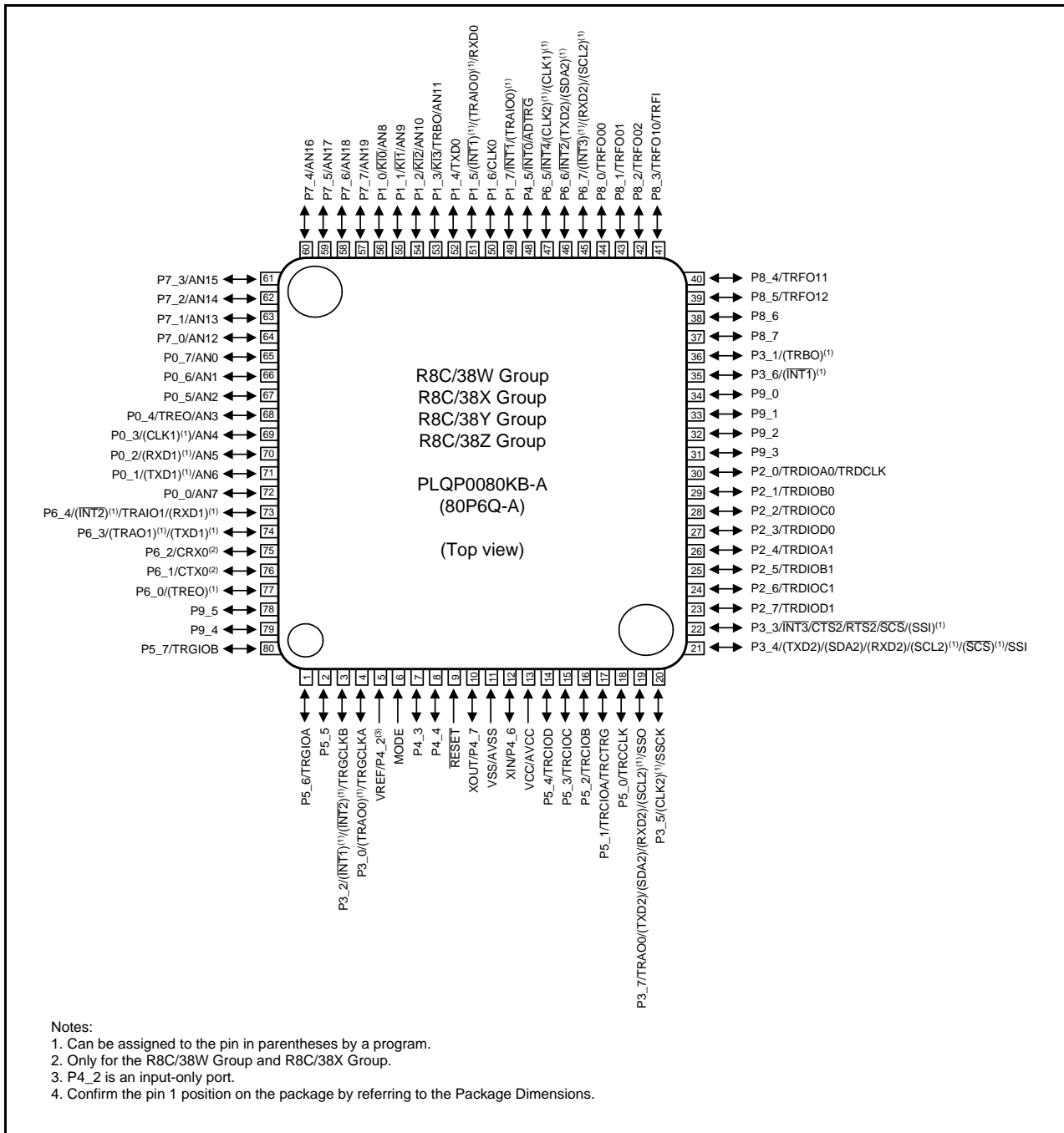**Figure 1.6      Pin Assignment (Top View)**

*Under development* Preliminary document
Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    1. Overview

### Table 1.13 Pin Name Information by Pin Number (1)

| Pin Number | Control Pin | Port | I/O Pin Functions for Peripheral Modules | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | SSU | CAN Module [2] | A/D Converter, Voltage Detection Circuit |
| 1 | | P5_6 | | TRGIOA | | | | |
| 2 | | P5_5 | | | | | | |
| 3 | | P3_2 | (INT1) [1]/ (INT2) [1] | TRGCLKB | | | | |
| 4 | | P3_0 | | (TRAO0) [1]/ TRGCLKA | | | | |
| 5 | | P4_2 | | | | | | VREF |
| 6 | MODE | | | | | | | |
| 7 | | P4_3 | | | | | | |
| 8 | | P4_4 | | | | | | |
| 9 | RESET | | | | | | | |
| 10 | XOUT | P4_7 | | | | | | |
| 11 | VSS/AVSS | | | | | | | |
| 12 | XIN | P4_6 | | | | | | |
| 13 | VCC/ AVCC | | | | | | | |
| 14 | | P5_4 | | TRCIOD | | | | |
| 15 | | P5_3 | | TRCIOC | | | | |
| 16 | | P5_2 | | TRCIOB | | | | |
| 17 | | P5_1 | | TRCIOA/ TRCTRG | | | | |
| 18 | | P5_0 | | TRCCLK | | | | |
| 19 | | P3_7 | | TRAO0 | (TXD2)/(SDA2)/ (RXD2)/(SCL2) [1] | SSO | | |
| 20 | | P3_5 | | | (CLK2) [1] | SSCK | | |
| 21 | | P3_4 | | | (TXD2)/(SDA2)/ (RXD2)/(SCL2) [1] | (SCS) [1]/SSI | | |
| 22 | | P3_3 | INT3 | | CTS2/RTS2 | SCS/(SSI) [1] | | |
| 23 | | P2_7 | | TRDIOD1 | | | | |
| 24 | | P2_6 | | TRDIOC1 | | | | |
| 25 | | P2_5 | | TRDIOB1 | | | | |
| 26 | | P2_4 | | TRDIOA1 | | | | |
| 27 | | P2_3 | | TRDIOD0 | | | | |
| 28 | | P2_2 | | TRDIOC0 | | | | |
| 29 | | P2_1 | | TRDIOB0 | | | | |
| 30 | | P2_0 | | TRDIOA0/ TRDCLK | | | | |
| 31 | | P9_3 | | | | | | |
| 32 | | P9_2 | | | | | | |
| 33 | | P9_1 | | | | | | |
| 34 | | P9_0 | | | | | | |
| 35 | | P3_6 | (INT1) [1] | | | | | |
| 36 | | P3_1 | | (TRBO) [1] | | | | |
| 37 | | P8_7 | | | | | | |
| 38 | | P8_6 | | | | | | |
| 39 | | P8_5 | | TRFO12 | | | | |
| 40 | | P8_4 | | TRFO11 | | | | |

Notes:
1. This can be assigned to the pin in parentheses by a program.
2. Only for the R8C/38W Group and R8C/38X Group.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group
1. Overview

**Table 1.14    Pin Name Information by Pin Number (2)**

| Pin Number | Control Pin | Port | I/O Pin Functions for Peripheral Modules | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | SSU | CAN Module (2) | A/D Converter, Voltage Detection Circuit |
| 41 | | P8_3 | | TRFO10/TRFI | | | | |
| 42 | | P8_2 | | TRFO02 | | | | |
| 43 | | P8_1 | | TRFO01 | | | | |
| 44 | | P8_0 | | TRFO00 | | | | |
| 45 | | P6_7 | (INT3) (1) | | (RXD2)/ (SCL2) (1) | | | |
| 46 | | P6_6 | INT2 | | (TXD2)/ (SDA2) (1) | | | |
| 47 | | P6_5 | INT4 | | (CLK2) (1)/ (CLK1) (1) | | | |
| 48 | | P4_5 | INT0 | | | | | ADTRG |
| 49 | | P1_7 | INT1 | (TRAIO0) (1) | | | | |
| 50 | | P1_6 | | | CLK0 | | | |
| 51 | | P1_5 | (INT1) (1) | (TRAIO0) (1) | RXD0 | | | |
| 52 | | P1_4 | | | TXD0 | | | |
| 53 | | P1_3 | KI3 | TRBO | | | | AN11 |
| 54 | | P1_2 | KI2 | | | | | AN10 |
| 55 | | P1_1 | KI1 | | | | | AN9 |
| 56 | | P1_0 | KI0 | | | | | AN8 |
| 57 | | P7_7 | | | | | | AN19 |
| 58 | | P7_6 | | | | | | AN18 |
| 59 | | P7_5 | | | | | | AN17 |
| 60 | | P7_4 | | | | | | AN16 |
| 61 | | P7_3 | | | | | | AN15 |
| 62 | | P7_2 | | | | | | AN14 |
| 63 | | P7_1 | | | | | | AN13 |
| 64 | | P7_0 | | | | | | AN12 |
| 65 | | P0_7 | | | | | | AN0 |
| 66 | | P0_6 | | | | | | AN1 |
| 67 | | P0_5 | | | | | | AN2 |
| 68 | | P0_4 | | TREO | | | | AN3 |
| 69 | | P0_3 | | | (CLK1) (1) | | | AN4 |
| 70 | | P0_2 | | | (RXD1) (1) | | | AN5 |
| 71 | | P0_1 | | | (TXD1) (1) | | | AN6 |
| 72 | | P0_0 | | | | | | AN7 |
| 73 | | P6_4 | (INT2) (1) | TRAIO1 | (RXD1) (1) | | | |
| 74 | | P6_3 | | (TRAO1) (1) | (TXD1) (1) | | | |
| 75 | | P6_2 | | | | | CRX0 (2) | |
| 76 | | P6_1 | | | | | CTX0 (2) | |
| 77 | | P6_0 | | (TREO) (1) | | | | |
| 78 | | P9_5 | | | | | | |
| 79 | | P9_4 | | | | | | |
| 80 | | P5_7 | | TRGIOB | | | | |

Notes:
1. This can be assigned to the pin in parentheses by a program.
2. Only for the R8C/38W Group and R8C/38X Group.

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    1. Overview

## 1.5 Pin Functions

Tables 1.15 and 1.16 list Pin Functions.

**Table 1.15    Pin Functions (1)**

| Item | Pin Name | I/O Type | Description |
|---|---|---|---|
| Power supply input | VCC, VSS | – | Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | – | Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Input "L" on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XIN clock input | XIN | I | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins [1]. To use an external clock, input it to the XOUT pin and leave the XIN pin open. |
| XIN clock output | XOUT | I/O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ | I | $\overline{\text{INT}}$ interrupt input pins. |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer RA0 Timer RA1 | TRAIO0, TRAIO1 | I/O | Timer RA I/O pin |
| | TRAO0, TRAO1 | O | Timer RA output pin |
| Timer RB | TRBO | O | Timer RB output pin |
| Timer RC | TRCCLK | I | External clock input pin |
| | TRCTRG | I | External trigger input pin |
| | TRCIOA, TRCIOB, TRCIOC, TRCIOD | I/O | Timer RC I/O pins |
| Timer RD | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | I/O | Timer RD I/O pins |
| | TRDCLK | I | External clock input pin |
| Timer RE | TREO | O | Divided clock output pin |
| Timer RF | TRFO00, TRFO10, TRFO01, TRFO11, TRFO02, TRFO12 | O | Timer RF output pins. |
| | TRFI | I | Timer RF input pin. |
| Timer RG | TRGIOA, TRGIOB | I/O | Timer RG I/O ports. |
| | TRGCLKA, TRGCLKB | I | External clock input pins. |
| Serial interface | CLK0, CLK1, CLK2 | I/O | Transfer clock I/O pins |
| | RXD0, RXD1, RXD2 | I | Serial data input pins |
| | TXD0, TXD1, TXD2 | O | Serial data output pins |
| | $\overline{\text{CTS2}}$ | I | Transmission control input pin |
| | $\overline{\text{RTS2}}$ | O | Reception control output pin |
| | SCL2 | I/O | I2C mode clock I/O pin |
| | SDA2 | I/O | I2C mode data I/O pin |
| SSU | SSI | I/O | Data I/O pin |
| | $\overline{\text{SCS}}$ | I/O | Chip-select signal I/O pin |
| | SSCK | I/O | Clock I/O pin |
| | SSO | I/O | Data I/O pin |

I: Input        O: Output        I/O: Input and output
Note:
1. Refer to the oscillator manufacturer for oscillation characteristics.

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    1. Overview

**Table 1.16      Pin Functions (2)**

| Item | Pin Name | I/O Type | Description |
|---|---|---|---|
| CAN module | CRX0 [1] | I | CAN data input pin |
|  | CTX0 [1] | O | CAN data output pin |
| Reference voltage input | VREF | I | Reference voltage input pin to A/D converter |
| A/D converter | AN0 to AN19 | I | Analog input pins to A/D converter |
|  | $\overline{\text{ADTRG}}$ | I | AD external trigger input pin |
| I/O port | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_5 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. |
| Input port | P4_2 | I | Input-only ports |

I: Input          O: Output              I/O: Input and output
Note:
　　1.　Only in the R8C/38W Group and R8C/38X Group.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    2. Central Processing Unit (CPU)

# 2.    Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.
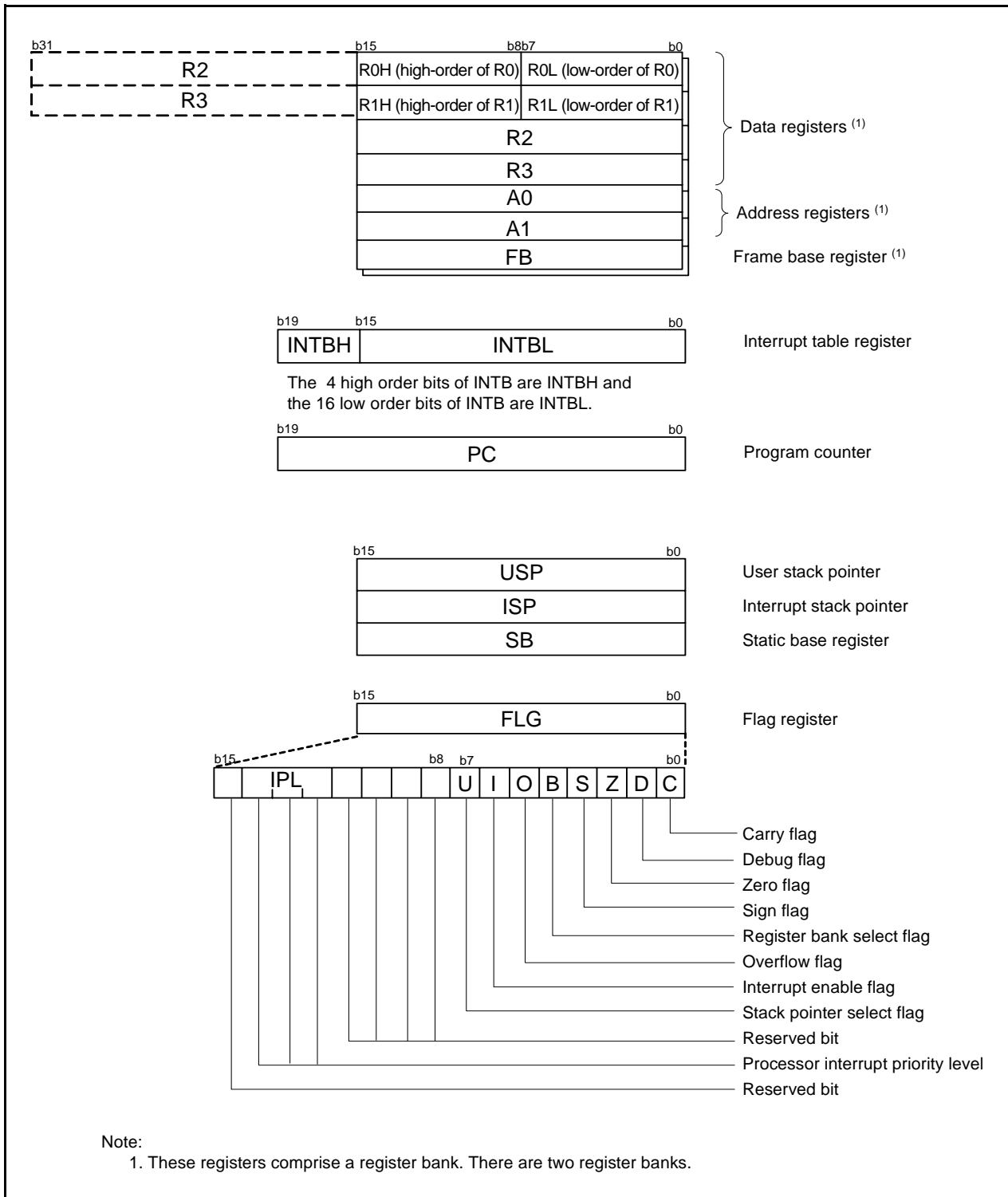


**Figure 2.1        CPU Registers**

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

2. Central Processing Unit (CPU)

## 2.1    Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2    Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3    Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4    Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5    Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6    User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7    Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8    Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1    Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2    Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3    Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4    Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5    Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6    Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    2. Central Processing Unit (CPU)

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                                                3. Memory

# 3.    Memory

## 3.1    R8C/38W Group

Figure 3.1 is a Memory Map of R8C/38W Group. The R8C/38W Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.
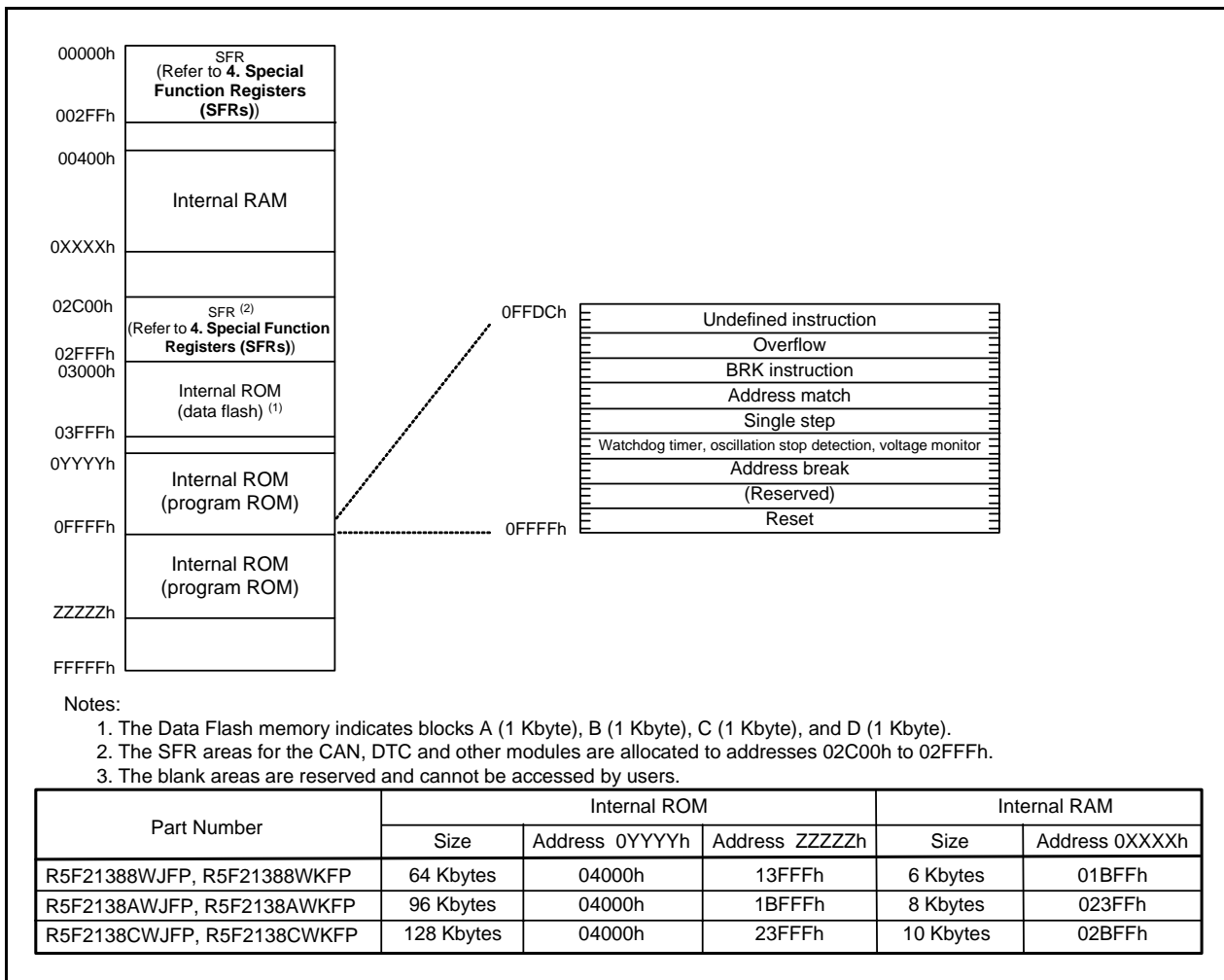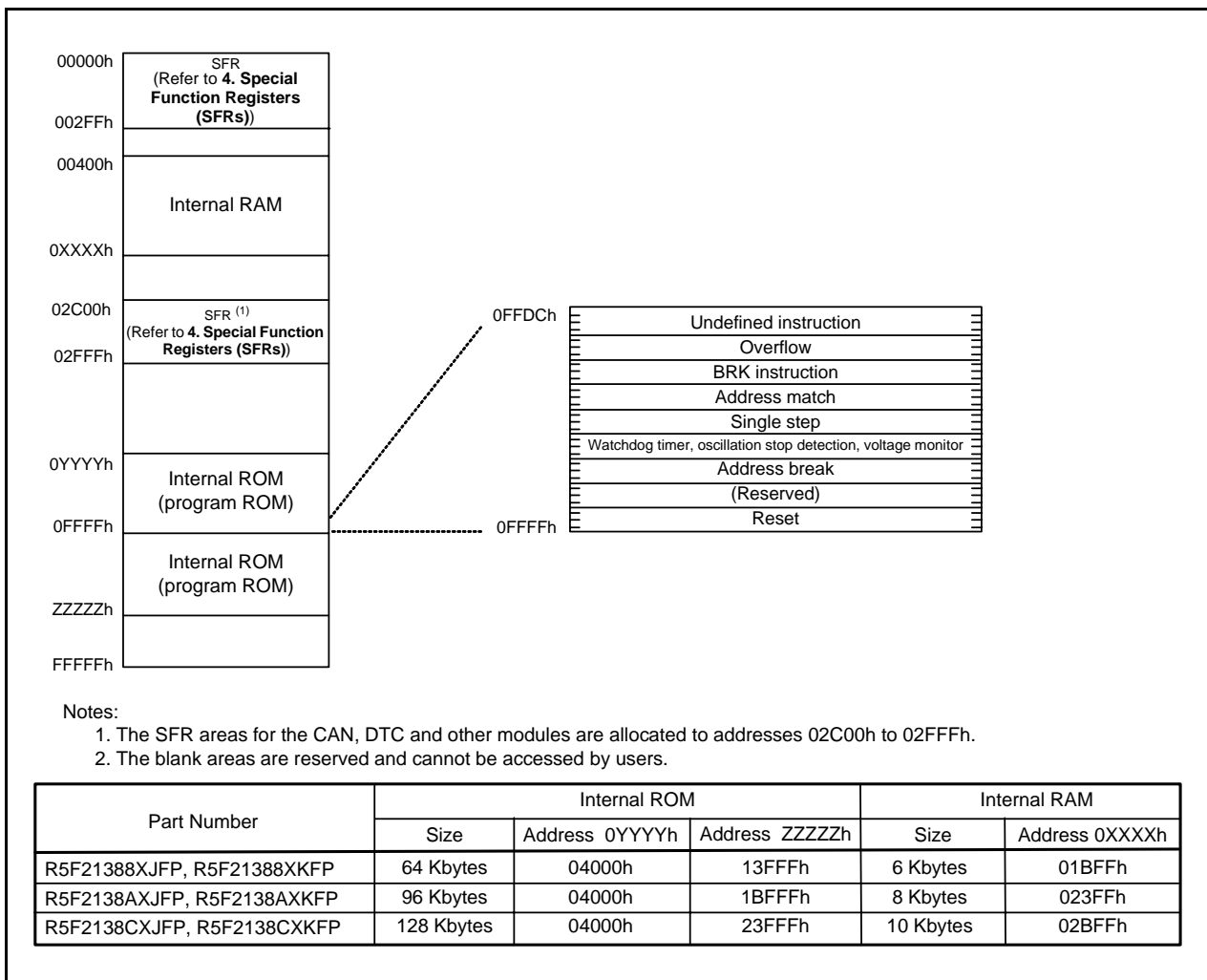


Notes:
1.  The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2.  The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3.  The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21388WJFP, R5F21388WKFP | 64 Kbytes | 04000h | 13FFFh | 6 Kbytes | 01BFFh |
| R5F2138AWJFP, R5F2138AWKFP | 96 Kbytes | 04000h | 1BFFFh | 8 Kbytes | 023FFh |
| R5F2138CWJFP, R5F2138CWKFP | 128 Kbytes | 04000h | 23FFFh | 10 Kbytes | 02BFFh |

**Figure 3.1      Memory Map of R8C/38W Group**

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    3. Memory

## 3.2    R8C/38X Group

Figure 3.2 is a Memory Map of R8C/38X Group. The R8C/38X Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.
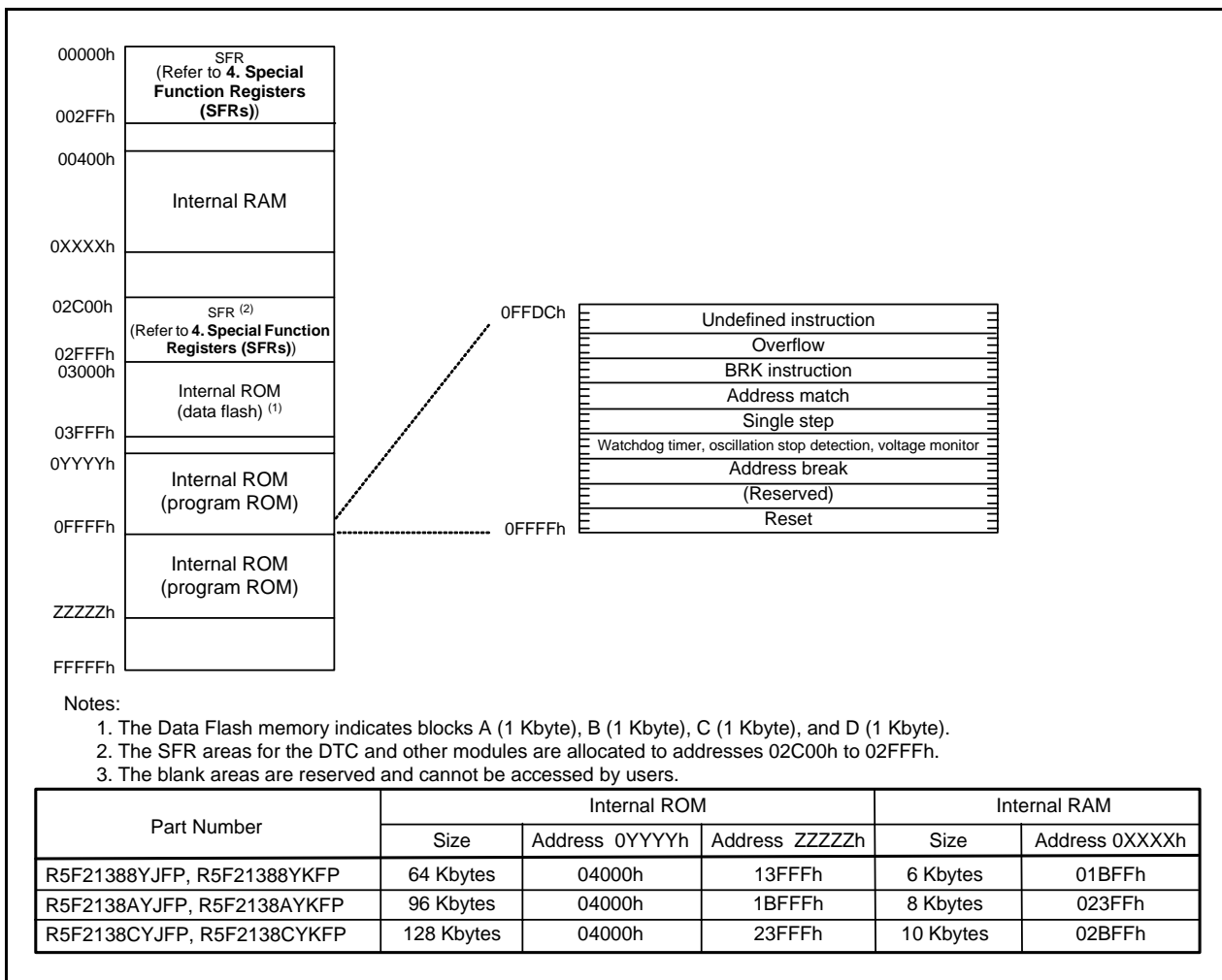


Notes:
1. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21388XJFP, R5F21388XKFP | 64 Kbytes | 04000h | 13FFFh | 6 Kbytes | 01BFFh |
| R5F2138AXJFP, R5F2138AXKFP | 96 Kbytes | 04000h | 1BFFFh | 8 Kbytes | 023FFh |
| R5F2138CXJFP, R5F2138CXKFP | 128 Kbytes | 04000h | 23FFFh | 10 Kbytes | 02BFFh |

**Figure 3.2      Memory Map of R8C/38X Group**

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                                3. Memory

## 3.3    R8C/38Y Group

Figure 3.3 is a Memory Map of R8C/38Y Group. The R8C/38Y Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.
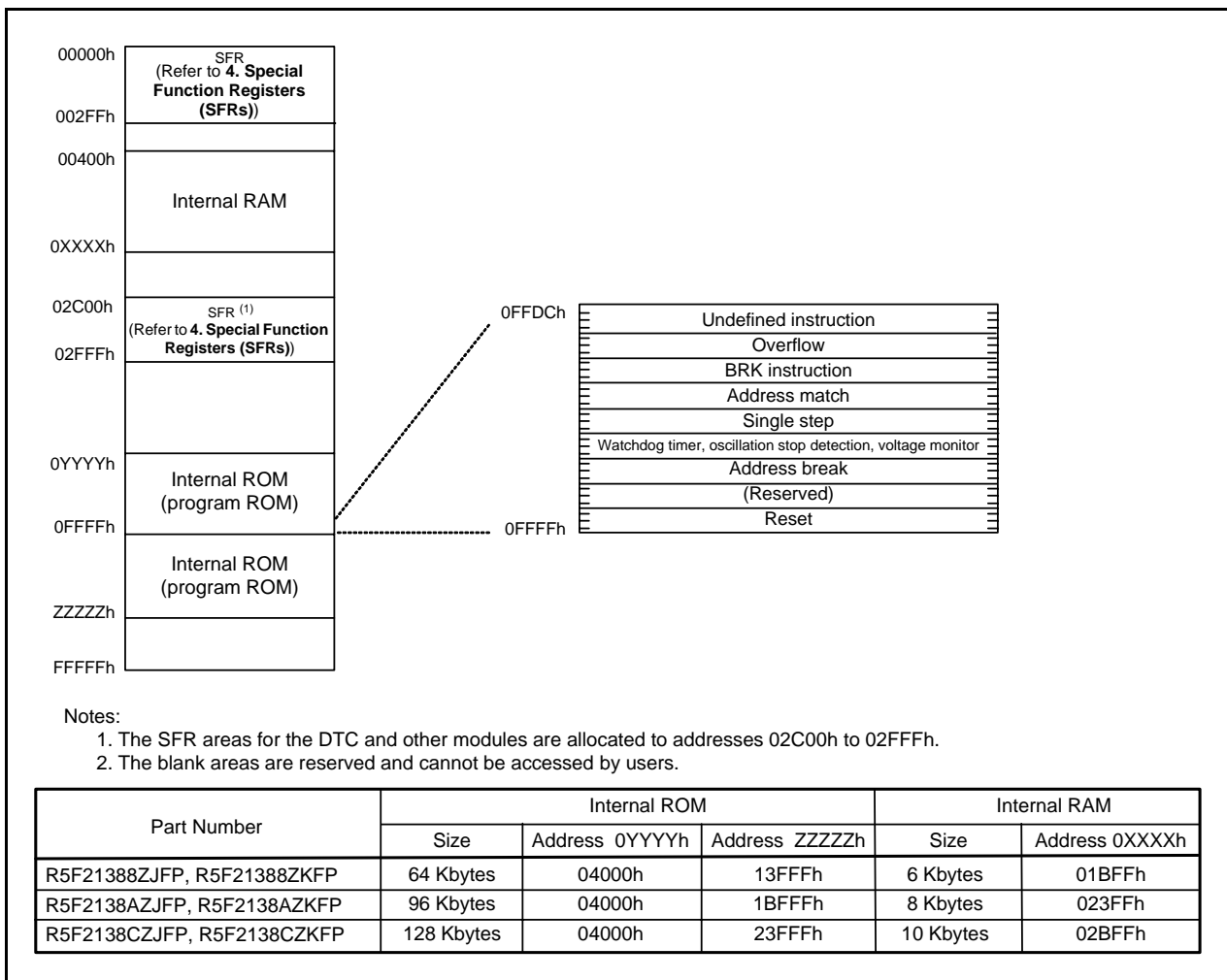


Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
| --- | --- | --- | --- | --- | --- |
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21388YJFP, R5F21388YKFP | 64 Kbytes | 04000h | 13FFFh | 6 Kbytes | 01BFFh |
| R5F2138AYJFP, R5F2138AYKFP | 96 Kbytes | 04000h | 1BFFFh | 8 Kbytes | 023FFh |
| R5F2138CYJFP, R5F2138CYKFP | 128 Kbytes | 04000h | 23FFFh | 10 Kbytes | 02BFFh |

**Figure 3.3      Memory Map of R8C/38Y Group**

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                                    3. Memory

## 3.4    R8C/38Z Group

Figure 3.4 is a Memory Map of R8C/38Z Group. The R8C/38Z Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21388ZJFP, R5F21388ZKFP | 64 Kbytes | 04000h | 13FFFh | 6 Kbytes | 01BFFh |
| R5F2138AZJFP, R5F2138AZKFP | 96 Kbytes | 04000h | 1BFFFh | 8 Kbytes | 023FFh |
| R5F2138CZJFP, R5F2138CZKFP | 128 Kbytes | 04000h | 23FFFh | 10 Kbytes | 02BFFh |

**Figure 3.4    Memory Map of R8C/38Z Group**

*Under development* Preliminary document
Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group 4. Special Function Registers (SFRs)

# 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.17 list the special function registers and Table 4.18 lists the ID Code Areas and Option Function Select Area.

**Table 4.1      SFR Information (1)** [1]

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 00101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | Module Standby Control Register | MSTCR | 00h |
| 0009h | System Clock Control Register 3 | CM3 | 00h |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | Reset Source Determination Register | RSTFR | 0XXXXXXXb [2] |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDTC | 00111111b |
| 0010h | | | |
| 0011h | | | |
| 0012h | | | |
| 0013h | | | |
| 0014h | | | |
| 0015h | High-Speed On-Chip Oscillator Control Register 7 | FRA7 | When shipping |
| 0016h | | | |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h 10000000b [3] |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | | | |
| 0021h | | | |
| 0022h | | | |
| 0023h | High-Speed On-Chip Oscillator Control Register 0 | FRA0 | 00h |
| 0024h | High-Speed On-Chip Oscillator Control Register 1 | FRA1 | When shipping |
| 0025h | High-Speed On-Chip Oscillator Control Register 2 | FRA2 | 00h |
| 0026h | On-Chip Reference Voltage Control Register | OCVREFCR | 00h |
| 0027h | | | |
| 0028h | | | |
| 0029h | High-Speed On-Chip Oscillator Control Register 4 | FRA4 | When Shipping |
| 002Ah | High-Speed On-Chip Oscillator Control Register 5 | FRA5 | When Shipping |
| 002Bh | High-Speed On-Chip Oscillator Control Register 6 | FRA6 | When Shipping |
| 002Ch | | | |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | High-Speed On-Chip Oscillator Control Register 3 | FRA3 | When shipping |
| 0030h | Voltage Monitor Circuit Control Register | CMPA | 00h |
| 0031h | Voltage Monitor Circuit Edge Select Register | VCAC | 00h |
| 0032h | | | |
| 0033h | Voltage Detect Register 1 | VCA1 | 00001000b |
| 0034h | Voltage Detect Register 2 | VCA2 | 00h [4] 00100000b [5] |
| 0035h | | | |
| 0036h | Voltage Detection 1 Level Select Register | VD1LS | 00000111b |
| 0037h | | | |
| 0038h | Voltage Monitor 0 Circuit Control Register | VW0C | 1100X010b [4] 1100X011b [5] |
| 0039h | Voltage Monitor 1 Circuit Control Register | VW1C | 10001010b |

X : Undefined
Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group       4. Special Function Registers (SFRs)

**Table 4.2        SFR Information (2)** [1]

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 003Ah | Voltage Monitor 2 Circuit Control Register | VW2C | 10000010b |
| 003Bh | | | |
| 003Ch | | | |
| 003Dh | | | |
| 003Eh | | | |
| 003Fh | | | |
| 0040h | | | |
| 0041h | Flash Memory Ready Interrupt Control Register | FMRDYIC | XXXXX000b |
| 0042h | Timer RA1 Interrupt Control Register | TRA1IC | XXXXX000b |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | INT4 Interrupt Control Register | INT4IC | XX00X000b |
| 0047h | Timer RC Interrupt Control Register | TRCIC | XXXXX000b |
| 0048h | Timer RD0 Interrupt Control Register | TRD0IC | XXXXX000b |
| 0049h | Timer RD1 Interrupt Control Register | TRD1IC | XXXXX000b |
| 004Ah | Timer RE Interrupt Control Register | TREIC | XXXXX000b |
| 004Bh | UART2 Transmit Interrupt Control Register | S2TIC | XXXXX000b |
| 004Ch | UART2 Receive Interrupt Control Register | S2RIC | XXXXX000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | SSU Interrupt Control Register | SSUIC | XXXXX000b |
| 0050h | Timer RF Compare1 Interrupt Control Register | CMP1IC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | INT2 Interrupt Control Register | INT2IC | XX00X000b |
| 0056h | Timer RA0 Interrupt Control Register | TRA0IC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer RB Interrupt Control Register | TRBIC | XXXXX000b |
| 0059h | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Ah | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 005Bh | Timer RF Interrupt Control Register | TRFIC | XXXXX000b |
| 005Ch | Timer RF Compare0 Interrupt Control Register | CMP0IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | UART2 Bus Collision Detection Interrupt Control Register | U2BCNIC | XXXXX000b |
| 005Fh | Timer RF Capture Interrupt Control Register | CAPIC | XXXXX000b |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | Timer RG Interrupt Control Register | TRGIC | XXXXX000b |
| 006Ch | CAN0 Successful Reception Interrupt Control Register | C0RIC | XXXXX000b |
| 006Dh | CAN0 Successful Transmission Interrupt Control Register | C0TIC | XXXXX000b |
| 006Eh | CAN0 Receive FIFO Interrupt Control Register | C0FRIC | XXXXX000b |
| 006Fh | CAN0 Transmit FIFO Interrupt Control Register | C0FTIC | XXXXX000b |
| 0070h | CAN0 Error Interrupt Control Register | C0EIC | XXXXX000b |
| 0071h | CAN0 Wake-up Interrupt Control Register | C0WIC | XXXXX000b |
| 0072h | Voltage Monitor 1 Level Interrupt Control Register | VCMP1IC | XXXXX000b |
| 0073h | Voltage Monitor 2 Level Interrupt Control Register | VCMP2IC | XXXXX000b |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                4. Special Function Registers (SFRs)

**Table 4.3     SFR Information (3)** [(1)]

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0080h | DTC Activation Control Register | DTCTL | 00h |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h | | | |
| 0088h | DTC Activation Enable Register 0 | DTCEN0 | 00h |
| 0089h | DTC Activation Enable Register 1 | DTCEN1 | 00h |
| 008Ah | DTC Activation Enable Register 2 | DTCEN2 | 00h |
| 008Bh | DTC Activation Enable Register 3 | DTCEN3 | 00h |
| 008Ch | DTC Activation Enable Register 4 | DTCEN4 | 00h |
| 008Dh | DTC Activation Enable Register 5 | DTCEN5 | 00h |
| 008Eh | DTC Activation Enable Register 6 | DTCEN6 | 00h |
| 008Fh | | | |
| 0090h | Timer RF Register | TRF | 00h |
| 0091h | | | 00h |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | | | |
| 0097h | | | |
| 0098h | | | |
| 0099h | | | |
| 009Ah | Timer RF Control Register 0 | TRFCR0 | 00h |
| 009Bh | Timer RF Control Register 1 | TRFCR1 | 00h |
| 009Ch | Capture and Compare 0 Register | TRFM0 | 00h |
| 009Dh | | | 00h |
| 009Eh | Compare 1 Register | TRFM1 | FFh |
| 009Fh | | | FFh |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 00A9h | UART2 Bit Rate Register | U2BRG | XXh |
| 00AAh | UART2 Transmit Buffer Register | U2TB | XXh |
| 00ABh | | | XXh |
| 00ACh | UART2 Transmit/Receive Control Register 0 | U2C0 | 00001000b |
| 00ADh | UART2 Transmit/Receive Control Register 1 | U2C1 | 00000010b |
| 00AEh | UART2 Receive Buffer Register | U2RB | XXh |
| 00AFh | | | XXh |
| 00B0h | UART2 Digital Filter Function Select Register | URXDF | 00h |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | | | |
| 00B9h | | | |
| 00BAh | | | |
| 00BBh | UART2 Special Mode Register 5 | U2SMR5 | 00h |
| 00BCh | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 00BDh | UART2 Special Mode Register 3 | U2SMR3 | 000X0X0Xb |
| 00BEh | UART2 Special Mode Register 2 | U2SMR2 | X0000000b |
| 00BFh | UART2 Special Mode Register | U2SMR | X0000000b |

X :  Undefined
Note:
  1.  The blank areas are reserved and cannot be accessed by users.

*Under development*  Preliminary document
Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group            4. Special Function Registers (SFRs)

**Table 4.4    SFR Information (4)** [1]

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 00C0h | A/D Register 0 | AD0 | XXh |
| 00C1h | | | 000000XXb |
| 00C2h | A/D Register 1 | AD1 | XXh |
| 00C3h | | | 000000XXb |
| 00C4h | A/D Register 2 | AD2 | XXh |
| 00C5h | | | 000000XXb |
| 00C6h | A/D Register 3 | AD3 | XXh |
| 00C7h | | | 000000XXb |
| 00C8h | A/D Register 4 | AD4 | XXh |
| 00C9h | | | 000000XXb |
| 00CAh | A/D Register 5 | AD5 | XXh |
| 00CBh | | | 000000XXb |
| 00CCh | A/D Register 6 | AD6 | XXh |
| 00CDh | | | 000000XXb |
| 00CEh | A/D Register 7 | AD7 | XXh |
| 00CFh | | | 000000XXb |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Mode Register | ADMOD | 00h |
| 00D5h | A/D Input Select Register | ADINSEL | 11000000b |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | XXh |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | Port P2 Register | P2 | XXh |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | Port P5 Register | P5 | XXh |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | Port P5 Direction Register | PD5 | 00h |
| 00ECh | Port P6 Register | P6 | XXh |
| 00EDh | Port P7 Register | P7 | XXh |
| 00EEh | Port P6 Direction Register | PD6 | 00h |
| 00EFh | Port P7 Direction Register | PD7 | 00h |
| 00F0h | Port P8 Register | P8 | XXh |
| 00F1h | Port P9 Register | P9 | XXh |
| 00F2h | Port P8 Direction Register | PD8 | 00h |
| 00F3h | Port P9 Direction Register | PD9 | 00h |
| 00F4h | | | |
| 00F5h | | | |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | | | |
| 00F9h | | | |
| 00FAh | | | |
| 00FBh | | | |
| 00FCh | | | |
| 00FDh | | | |
| 00FEh | | | |
| 00FFh | | | |

X : Undefined
Note:
1.    The blank areas are reserved and cannot be accessed by users.

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group    4. Special Function Registers (SFRs)

**Table 4.5    SFR Information (5) [1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0100h | Timer RA0 Control Register | TRA0CR | 00h |
| 0101h | Timer RA0 I/O Control Register | TRA0IOC | 00h |
| 0102h | Timer RA0 Mode Register | TRA0MR | 00h |
| 0103h | Timer RA0 Prescaler Register | TRA0PRE | FFh |
| 0104h | Timer RA0 Register | TRA0 | FFh |
| 0105h | LIN0 Control Register 2 | LIN0CR2 | 00h |
| 0106h | LIN0 Control Register | LIN0CR | 00h |
| 0107h | LIN0 Status Register | LIN0ST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | Timer RA1 Control Register | TRA1CR | 00h |
| 0111h | Timer RA1 I/O Control Register | TRA1IOC | 00h |
| 0112h | Timer RA1 Mode Register | TRA1MR | 00h |
| 0113h | Timer RA1 Prescaler Register | TRA1PRE | FFh |
| 0114h | Timer RA1 Register | TRA1 | FFh |
| 0115h | LIN1 Control Register 2 | LIN1CR2 | 00h |
| 0116h | LIN1 Control Register | LIN1CR | 00h |
| 0117h | LIN1 Status Register | LIN1ST | 00h |
| 0118h | Timer RE Counter Data Register | TRESEC | 00h |
| 0119h | Timer RE Compare Data Register | TREMIN | 00h |
| 011Ah | | | |
| 011Bh | | | |
| 011Ch | Timer RE Control Register 1 | TRECR1 | 00h |
| 011Dh | Timer RE Control Register 2 | TRECR2 | 00h |
| 011Eh | Timer RE Count Source Select Register | TRECSR | 00001000b |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011000b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | Timer RC Trigger Control Register | TRCADCR | 00h |
| 0134h | | | |
| 0135h | | | |
| 0136h | Timer RD Trigger Control Register | TRDADCR | 00h |
| 0137h | Timer RD Start Register | TRDSTR | 11111100b |
| 0138h | Timer RD Mode Register | TRDMR | 00001110b |
| 0139h | Timer RD PWM Mode Register | TRDPMR | 10001000b |
| 013Ah | Timer RD Function Control Register | TRDFCR | 10000000b |
| 013Bh | Timer RD Output Master Enable Register 1 | TRDOER1 | FFh |
| 013Ch | Timer RD Output Master Enable Register 2 | TRDOER2 | 01111111b |
| 013Dh | Timer RD Output Control Register | TRDOCR | 00h |
| 013Eh | Timer RD Digital Filter Function Select Register 0 | TRDDF0 | 00h |
| 013Fh | Timer RD Digital Filter Function Select Register 1 | TRDDF1 | 00h |

Note:
1.   The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    4. Special Function Registers (SFRs)

**Table 4.6        SFR Information (6) [1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0140h | Timer RD Control Register 0 | TRDCR0 | 00h |
| 0141h | Timer RD I/O Control Register A0 | TRDIORA0 | 10001000b |
| 0142h | Timer RD I/O Control Register C0 | TRDIORC0 | 10001000b |
| 0143h | Timer RD Status Register 0 | TRDSR0 | 11100000b |
| 0144h | Timer RD Interrupt Enable Register 0 | TRDIER0 | 11100000b |
| 0145h | Timer RD PWM Mode Output Level Control Register 0 | TRDPOCR0 | 11111000b |
| 0146h | Timer RD Counter 0 | TRD0 | 00h |
| 0147h |  |  | 00h |
| 0148h | Timer RD General Register A0 | TRDGRA0 | FFh |
| 0149h |  |  | FFh |
| 014Ah | Timer RD General Register B0 | TRDGRB0 | FFh |
| 014Bh |  |  | FFh |
| 014Ch | Timer RD General Register C0 | TRDGRC0 | FFh |
| 014Dh |  |  | FFh |
| 014Eh | Timer RD General Register D0 | TRDGRD0 | FFh |
| 014Fh |  |  | FFh |
| 0150h | Timer RD Control Register 1 | TRDCR1 | 00h |
| 0151h | Timer RD I/O Control Register A1 | TRDIORA1 | 10001000b |
| 0152h | Timer RD I/O Control Register C1 | TRDIORC1 | 10001000b |
| 0153h | Timer RD Status Register 1 | TRDSR1 | 11000000b |
| 0154h | Timer RD Interrupt Enable Register 1 | TRDIER1 | 11100000b |
| 0155h | Timer RD PWM Mode Output Level Control Register 1 | TRDPOCR1 | 11111000b |
| 0156h | Timer RD Counter 1 | TRD1 | 00h |
| 0157h |  |  | 00h |
| 0158h | Timer RD General Register A1 | TRDGRA1 | FFh |
| 0159h |  |  | FFh |
| 015Ah | Timer RD General Register B1 | TRDGRB1 | FFh |
| 015Bh |  |  | FFh |
| 015Ch | Timer RD General Register C1 | TRDGRC1 | FFh |
| 015Dh |  |  | FFh |
| 015Eh | Timer RD General Register D1 | TRDGRD1 | FFh |
| 015Fh |  |  | FFh |
| 0160h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 0161h | UART1 Bit Rate Register | U1BRG | XXh |
| 0162h | UART1 Transmit Buffer Register | U1TB | XXh |
| 0163h |  |  | XXh |
| 0164h | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 0165h | UART1 Transmit/Receive Control Register 1 | U1C1 | 00000010b |
| 0166h | UART1 Receive Buffer Register | U1RB | XXh |
| 0167h |  |  | XXh |
| 0168h |  |  |  |
| 0169h |  |  |  |
| 016Ah |  |  |  |
| 016Bh |  |  |  |
| 016Ch |  |  |  |
| 016Dh |  |  |  |
| 016Eh |  |  |  |
| 016Fh |  |  |  |
| 0170h | Timer RG Mode Register | TRGMR | 01000000b |
| 0171h | Timer RG Count Control Register | TRGCNTC | 00000000b |
| 0172h | Timer RG Control Register | TRGCR | 10000000b |
| 0173h | Timer RG Interrupt Enable Register | TRGIER | 11110000b |
| 0174h | Timer RG Status Register | TRGSR | 11100000b |
| 0175h | Timer RG I/O Control Register | TRGIOR | 00000000b |
| 0176h | Timer RG Counter | TRG | 00h |
| 0177h |  |  | 00h |
| 0178h | Timer RG General Register A | TRGGRA | FFh |
| 0179h |  |  | FFh |
| 017Ah | Timer RG General Register B | TRGGRB | FFh |
| 017Bh |  |  | FFh |
| 017Ch | Timer RG General Register C | TRGGRC | FFh |
| 017Dh |  |  | FFh |
| 017Eh | Timer RG General Register D | TRGGRD | FFh |
| 017Fh |  |  | FFh |

X :  Undefined
Note:
    1.   The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group 4. Special Function Registers (SFRs)

**Table 4.7 SFR Information (7) [1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0180h | Timer RA Pin Select Register | TRASR | 00h |
| 0181h | Timer RB/RC Pin Select Register | TRBRCSR | 00h |
| 0182h | Timer RC Pin Select Register 0 | TRCPSR0 | 00h |
| 0183h | Timer RC Pin Select Register 1 | TRCPSR1 | 00h |
| 0184h | Timer RD Pin Select Register 0 | TRDPSR0 | 00h |
| 0185h | Timer RD Pin Select Register 1 | TRDPSR1 | 00h |
| 0186h | Timer Pin Select Register | TIMSR | 00h |
| 0187h | Timer RF Output Control Register | TRFOUT | 00h |
| 0188h | UART0 Pin Select Register | U0SR | 00h |
| 0189h | UART1 Pin Select Register | U1SR | 00h |
| 018Ah | UART2 Pin Select Register 0 | U2SR0 | 00h |
| 018Bh | UART2 Pin Select Register 1 | U2SR1 | 00h |
| 018Ch | SSU Pin Select Register | SSUIICSR | 00h |
| 018Dh | | | |
| 018Eh | INT Interrupt Input Pin Select Register | INTSR | 00h |
| 018Fh | I/O Function Pin Select Register | PINSR | 00h |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | SS Bit Counter Register | SSBR | 11111000b |
| 0194h | SS Transmit Data Register | SSTDR | FFh |
| 0195h | | | FFh |
| 0196h | SS Receive Data Register | SSRDR | FFh |
| 0197h | | | FFh |
| 0198h | SS Control Register H | SSCRH | 00h |
| 0199h | SS Control Register L | SSCRL | 01111101b |
| 019Ah | SS Mode Register | SSMR | 00010000b |
| 019Bh | SS Enable Register | SSER | 00h |
| 019Ch | SS Status Register | SSSR | 00h |
| 019Dh | SS Mode Register 2 | SSMR2 | 00h |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | Flash Memory Status Register | FST | 10000X00b |
| 01B3h | | | |
| 01B4h | Flash Memory Control Register 0 | FMR0 | 00h |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 00h |
| 01B6h | Flash Memory Control Register 2 | FMR2 | 00h |
| 01B7h | | | |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| 01BBh | | | |
| 01BCh | | | |
| 01BDh | | | |
| 01BEh | | | |
| 01BFh | | | |

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    4. Special Function Registers (SFRs)

**Table 4.8      SFR Information (8) [1]**

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 01C0h | Address Match Interrupt Register 0 | RMAD0 | XXh |
| 01C1h | | | XXh |
| 01C2h | | | 0000XXXXb |
| 01C3h | Address Match Interrupt Enable Register 0 | AIER0 | 00h |
| 01C4h | Address Match Interrupt Register 1 | RMAD1 | XXh |
| 01C5h | | | XXh |
| 01C6h | | | 0000XXXXb |
| 01C7h | Address Match Interrupt Enable Register 1 | AIER1 | 00h |
| 01C8h | | | |
| 01C9h | | | |
| 01CAh | | | |
| 01CBh | | | |
| 01CCh | | | |
| 01CDh | | | |
| 01CEh | | | |
| 01CFh | | | |
| 01D0h | | | |
| 01D1h | | | |
| 01D2h | | | |
| 01D3h | | | |
| 01D4h | | | |
| 01D5h | | | |
| 01D6h | | | |
| 01D7h | | | |
| 01D8h | | | |
| 01D9h | | | |
| 01DAh | | | |
| 01DBh | | | |
| 01DCh | | | |
| 01DDh | | | |
| 01DEh | | | |
| 01DFh | | | |
| 01E0h | Pull-Up Control Register 0 | PUR0 | 00h |
| 01E1h | Pull-Up Control Register 1 | PUR1 | 00h |
| 01E2h | Pull-Up Control Register 2 | PUR2 | 00h |
| 01E3h | | | |
| 01E4h | | | |
| 01E5h | | | |
| 01E6h | | | |
| 01E7h | | | |
| 01E8h | | | |
| 01E9h | | | |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | | | |
| 01EDh | | | |
| 01EEh | | | |
| 01EFh | | | |
| 01F0h | | | |
| 01F1h | | | |
| 01F2h | | | |
| 01F3h | | | |
| 01F4h | | | |
| 01F5h | Input Threshold Control Register 0 | VLT0 | 00h |
| 01F6h | Input Threshold Control Register 1 | VLT1 | 00h |
| 01F7h | Input Threshold Control Register 2 | VLT2 | 00h |
| 01F8h | | | |
| 01F9h | | | |
| 01FAh | External Input Enable Register 0 | INTEN | 00h |
| 01FBh | External Input Enable Register 1 | INTEN1 | 00h |
| 01FCh | INT Input Filter Select Register 0 | INTF | 00h |
| 01FDh | INT Input Filter Select Register 1 | INTF1 | 00h |
| 01FEh | Key Input Enable Register 0 | KIEN | 00h |
| 01FFh | | | |

X : Undefined
Note:
   1. The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group          4. Special Function Registers (SFRs)

**Table 4.9     SFR Information (9)** [1]

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2C00h | DTC Transfer Vector Area | | XXh |
| 2C01h | DTC Transfer Vector Area | | XXh |
| 2C02h | DTC Transfer Vector Area | | XXh |
| 2C03h | DTC Transfer Vector Area | | XXh |
| 2C04h | DTC Transfer Vector Area | | XXh |
| 2C05h | | | |
| 2C06h | | | |
| 2C07h | | | |
| 2C08h | DTC Transfer Vector Area | | XXh |
| 2C09h | DTC Transfer Vector Area | | XXh |
| 2C0Ah | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| 2C3Ah | | | |
| 2C3Bh | | | |
| 2C3Ch | | | |
| 2C3Dh | | | |
| 2C3Eh | | | |
| 2C3Fh | | | |
| 2C40h | DTC Control Data 0 | DTCD0 | XXh |
| 2C41h | | | XXh |
| 2C42h | | | XXh |
| 2C43h | | | XXh |
| 2C44h | | | XXh |
| 2C45h | | | XXh |
| 2C46h | | | XXh |
| 2C47h | | | XXh |
| 2C48h | DTC Control Data 1 | DTCD1 | XXh |
| 2C49h | | | XXh |
| 2C4Ah | | | XXh |
| 2C4Bh | | | XXh |
| 2C4Ch | | | XXh |
| 2C4Dh | | | XXh |
| 2C4Eh | | | XXh |
| 2C4Fh | | | XXh |
| 2C50h | DTC Control Data 2 | DTCD2 | XXh |
| 2C51h | | | XXh |
| 2C52h | | | XXh |
| 2C53h | | | XXh |
| 2C54h | | | XXh |
| 2C55h | | | XXh |
| 2C56h | | | XXh |
| 2C57h | | | XXh |
| 2C58h | DTC Control Data 3 | DTCD3 | XXh |
| 2C59h | | | XXh |
| 2C5Ah | | | XXh |
| 2C5Bh | | | XXh |
| 2C5Ch | | | XXh |
| 2C5Dh | | | XXh |
| 2C5Eh | | | XXh |
| 2C5Fh | | | XXh |
| 2C60h | DTC Control Data 4 | DTCD4 | XXh |
| 2C61h | | | XXh |
| 2C62h | | | XXh |
| 2C63h | | | XXh |
| 2C64h | | | XXh |
| 2C65h | | | XXh |
| 2C66h | | | XXh |
| 2C67h | | | XXh |
| 2C68h | DTC Control Data 5 | DTCD5 | XXh |
| 2C69h | | | XXh |
| 2C6Ah | | | XXh |
| 2C6Bh | | | XXh |
| 2C6Ch | | | XXh |
| 2C6Dh | | | XXh |
| 2C6Eh | | | XXh |
| 2C6Fh | | | XXh |

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group      4. Special Function Registers (SFRs)

**Table 4.10    SFR Information (10)** [1]

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2C70h | DTC Control Data 6 | DTCD6 | XXh |
| 2C71h | | | XXh |
| 2C72h | | | XXh |
| 2C73h | | | XXh |
| 2C74h | | | XXh |
| 2C75h | | | XXh |
| 2C76h | | | XXh |
| 2C77h | | | XXh |
| 2C78h | DTC Control Data 7 | DTCD7 | XXh |
| 2C79h | | | XXh |
| 2C7Ah | | | XXh |
| 2C7Bh | | | XXh |
| 2C7Ch | | | XXh |
| 2C7Dh | | | XXh |
| 2C7Eh | | | XXh |
| 2C7Fh | | | XXh |
| 2C80h | DTC Control Data 8 | DTCD8 | XXh |
| 2C81h | | | XXh |
| 2C82h | | | XXh |
| 2C83h | | | XXh |
| 2C84h | | | XXh |
| 2C85h | | | XXh |
| 2C86h | | | XXh |
| 2C87h | | | XXh |
| 2C88h | DTC Control Data 9 | DTCD9 | XXh |
| 2C89h | | | XXh |
| 2C8Ah | | | XXh |
| 2C8Bh | | | XXh |
| 2C8Ch | | | XXh |
| 2C8Dh | | | XXh |
| 2C8Eh | | | XXh |
| 2C8Fh | | | XXh |
| 2C90h | DTC Control Data 10 | DTCD10 | XXh |
| 2C91h | | | XXh |
| 2C92h | | | XXh |
| 2C93h | | | XXh |
| 2C94h | | | XXh |
| 2C95h | | | XXh |
| 2C96h | | | XXh |
| 2C97h | | | XXh |
| 2C98h | DTC Control Data 11 | DTCD11 | XXh |
| 2C99h | | | XXh |
| 2C9Ah | | | XXh |
| 2C9Bh | | | XXh |
| 2C9Ch | | | XXh |
| 2C9Dh | | | XXh |
| 2C9Eh | | | XXh |
| 2C9Fh | | | XXh |
| 2CA0h | DTC Control Data 12 | DTCD12 | XXh |
| 2CA1h | | | XXh |
| 2CA2h | | | XXh |
| 2CA3h | | | XXh |
| 2CA4h | | | XXh |
| 2CA5h | | | XXh |
| 2CA6h | | | XXh |
| 2CA7h | | | XXh |
| 2CA8h | DTC Control Data 13 | DTCD13 | XXh |
| 2CA9h | | | XXh |
| 2CAAh | | | XXh |
| 2CABh | | | XXh |
| 2CACh | | | XXh |
| 2CADh | | | XXh |
| 2CAEh | | | XXh |
| 2CAFh | | | XXh |

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group　　　　4. Special Function Registers (SFRs)

**Table 4.11 SFR Information (11) [1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2CB0h | DTC Control Data 14 | DTCD14 | XXh |
| 2CB1h | | | XXh |
| 2CB2h | | | XXh |
| 2CB3h | | | XXh |
| 2CB4h | | | XXh |
| 2CB5h | | | XXh |
| 2CB6h | | | XXh |
| 2CB7h | | | XXh |
| 2CB8h | DTC Control Data 15 | DTCD15 | XXh |
| 2CB9h | | | XXh |
| 2CBAh | | | XXh |
| 2CBBh | | | XXh |
| 2CBCh | | | XXh |
| 2CBDh | | | XXh |
| 2CBEh | | | XXh |
| 2CBFh | | | XXh |
| 2CC0h | DTC Control Data 16 | DTCD16 | XXh |
| 2CC1h | | | XXh |
| 2CC2h | | | XXh |
| 2CC3h | | | XXh |
| 2CC4h | | | XXh |
| 2CC5h | | | XXh |
| 2CC6h | | | XXh |
| 2CC7h | | | XXh |
| 2CC8h | DTC Control Data 17 | DTCD17 | XXh |
| 2CC9h | | | XXh |
| 2CCAh | | | XXh |
| 2CCBh | | | XXh |
| 2CCCh | | | XXh |
| 2CCDh | | | XXh |
| 2CCEh | | | XXh |
| 2CCFh | | | XXh |
| 2CD0h | DTC Control Data 18 | DTCD18 | XXh |
| 2CD1h | | | XXh |
| 2CD2h | | | XXh |
| 2CD3h | | | XXh |
| 2CD4h | | | XXh |
| 2CD5h | | | XXh |
| 2CD6h | | | XXh |
| 2CD7h | | | XXh |
| 2CD8h | DTC Control Data 19 | DTCD19 | XXh |
| 2CD9h | | | XXh |
| 2CDAh | | | XXh |
| 2CDBh | | | XXh |
| 2CDCh | | | XXh |
| 2CDDh | | | XXh |
| 2CDEh | | | XXh |
| 2CDFh | | | XXh |
| 2CE0h | DTC Control Data 20 | DTCD20 | XXh |
| 2CE1h | | | XXh |
| 2CE2h | | | XXh |
| 2CE3h | | | XXh |
| 2CE4h | | | XXh |
| 2CE5h | | | XXh |
| 2CE6h | | | XXh |
| 2CE7h | | | XXh |
| 2CE8h | DTC Control Data 21 | DTCD21 | XXh |
| 2CE9h | | | XXh |
| 2CEAh | | | XXh |
| 2CEBh | | | XXh |
| 2CECh | | | XXh |
| 2CEDh | | | XXh |
| 2CEEh | | | XXh |
| 2CEFh | | | XXh |

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    4. Special Function Registers (SFRs)

**Table 4.12    SFR Information (12) [1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2CF0h | DTC Control Data 22 | DTCD22 | XXh |
| 2CF1h | | | XXh |
| 2CF2h | | | XXh |
| 2CF3h | | | XXh |
| 2CF4h | | | XXh |
| 2CF5h | | | XXh |
| 2CF6h | | | XXh |
| 2CF7h | | | XXh |
| 2CF8h | DTC Control Data 23 | DTCD23 | XXh |
| 2CF9h | | | XXh |
| 2CFAh | | | XXh |
| 2CFBh | | | XXh |
| 2CFCh | | | XXh |
| 2CFDh | | | XXh |
| 2CFEh | | | XXh |
| 2CFFh | | | XXh |
| 2D00h | | | |
| 2D01h | | | |
| : | | | |
| 2E00h | CAN0 Mailbox 0 : Message ID | C0MB0 | XXXX XXXXh |
| 2E01h | | | |
| 2E02h | | | |
| 2E03h | | | |
| 2E04h | | | |
| 2E05h | CAN0 Mailbox 0 : Data length | | XXh |
| 2E06h | CAN0 Mailbox 0 : Data field | | XXXX XXXX |
| 2E07h | | | XXXX XXXXh |
| 2E08h | | | |
| 2E09h | | | |
| 2E0Ah | | | |
| 2E0Bh | | | |
| 2E0Ch | | | |
| 2E0Dh | | | |
| 2E0Eh | CAN0 Mailbox 0 : Time stamp | | XXXXh |
| 2E0Fh | | | |
| 2E10h | CAN0 Mailbox 1 : Message ID | C0MB1 | XXXX XXXXh |
| 2E11h | | | |
| 2E12h | | | |
| 2E13h | | | |
| 2E14h | | | |
| 2E15h | CAN0 Mailbox 1 : Data length | | XXh |
| 2E16h | CAN0 Mailbox 1 : Data field | | XXXX XXXX |
| 2E17h | | | XXXX XXXXh |
| 2E18h | | | |
| 2E19h | | | |
| 2E1Ah | | | |
| 2E1Bh | | | |
| 2E1Ch | | | |
| 2E1Dh | | | |
| 2E1Eh | CAN0 Mailbox 1 : Time stamp | | XXXXh |
| 2E1Fh | | | |
| 2E20h | CAN0 Mailbox 2 : Message ID | C0MB2 | XXXX XXXXh |
| 2E21h | | | |
| 2E22h | | | |
| 2E23h | | | |
| 2E24h | | | |
| 2E25h | CAN0 Mailbox 2 : Data length | | XXh |
| 2E26h | CAN0 Mailbox 2 : Data field | | XXXX XXXX |
| 2E27h | | | XXXX XXXXh |
| 2E28h | | | |
| 2E29h | | | |
| 2E2Ah | | | |
| 2E2Bh | | | |
| 2E2Ch | | | |
| 2E2Dh | | | |
| 2E2Eh | CAN0 Mailbox 2 : Time stamp | | XXXXh |
| 2E2Fh | | | |

X : Undefined
Note:
1.    The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group    4. Special Function Registers (SFRs)

**Table 4.13    SFR Information (13) [1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2E30h | CAN0 Mailbox 3 : Message ID | C0MB3 | XXXX XXXXh |
| 2E31h | | | |
| 2E32h | | | |
| 2E33h | | | |
| 2E34h | | | |
| 2E35h | CAN0 Mailbox 3 : Data length | | XXh |
| 2E36h | CAN0 Mailbox 3 : Data field | | XXXX XXXX |
| 2E37h | | | XXXX XXXXh |
| 2E38h | | | |
| 2E39h | | | |
| 2E3Ah | | | |
| 2E3Bh | | | |
| 2E3Ch | | | |
| 2E3Dh | | | |
| 2E3Eh | CAN0 Mailbox3 : Time stamp | | XXXXh |
| 2E3Fh | | | |
| 2E40h | CAN0 Mailbox4 : Message ID | C0MB4 | XXXX XXXXh |
| 2E41h | | | |
| 2E42h | | | |
| 2E43h | | | |
| 2E44h | | | |
| 2E45h | CAN0 Mailbox4 : Data length | | XXh |
| 2E46h | CAN0 Mailbox4 : Data field | | XXXX XXXX |
| 2E47h | | | XXXX XXXXh |
| 2E48h | | | |
| 2E49h | | | |
| 2E4Ah | | | |
| 2E4Bh | | | |
| 2E4Ch | | | |
| 2E4Dh | | | |
| 2E4Eh | CAN0 Mailbox4 : Time stamp | | XXXXh |
| 2E4Fh | | | |
| 2E50h | CAN0 Mailbox5 : Message ID | C0MB5 | XXXX XXXXh |
| 2E51h | | | |
| 2E52h | | | |
| 2E53h | | | |
| 2E54h | | | |
| 2E55h | CAN0 Mailbox5 : Data length | | XXh |
| 2E56h | CAN0 Mailbox5 : Data field | | XXXX XXXX |
| 2E57h | | | XXXX XXXXh |
| 2E58h | | | |
| 2E59h | | | |
| 2E5Ah | | | |
| 2E5Bh | | | |
| 2E5Ch | | | |
| 2E5Dh | | | |
| 2E5Eh | CAN0 Mailbox5 : Time stamp | | XXXXh |
| 2E5Fh | | | |
| 2E60h | CAN0 Mailbox6 : Message ID | C0MB6 | XXXX XXXXh |
| 2E61h | | | |
| 2E62h | | | |
| 2E63h | | | |
| 2E64h | | | |
| 2E65h | CAN0 Mailbox6 : Data length | | XXh |
| 2E66h | CAN0 Mailbox6 : Data field | | XXXX XXXX |
| 2E67h | | | XXXX XXXXh |
| 2E68h | | | |
| 2E69h | | | |
| 2E6Ah | | | |
| 2E6Bh | | | |
| 2E6Ch | | | |
| 2E6Dh | | | |
| 2E6Eh | CAN0 Mailbox6 : Time stamp | | XXXXh |
| 2E6Fh | | | |

X :  Undefined
Note:
    1.    The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group         4. Special Function Registers (SFRs)

**Table 4.14    SFR Information (14) [1]**

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 2E70h | CAN0 Mailbox7 : Message ID | C0MB7 | XXXX XXXXh |
| 2E71h | | | |
| 2E72h | | | |
| 2E73h | | | |
| 2E74h | | | |
| 2E75h | CAN0 Mailbox7 : Data length | | XXh |
| 2E76h | CAN0 Mailbox7 : Data field | | XXXX XXXX |
| 2E77h | | | XXXX XXXXh |
| 2E78h | | | |
| 2E79h | | | |
| 2E7Ah | | | |
| 2E7Bh | | | |
| 2E7Ch | | | |
| 2E7Dh | | | |
| 2E7Eh | CAN0 Mailbox7 : Time stamp | | XXXXh |
| 2E7Fh | | | |
| 2E80h | CAN0 Mailbox8 : Message ID | C0MB8 | XXXX XXXXh |
| 2E81h | | | |
| 2E82h | | | |
| 2E83h | | | |
| 2E84h | | | |
| 2E85h | CAN0 Mailbox8 : Data length | | XXh |
| 2E86h | CAN0 Mailbox8 : Data field | | XXXX XXXX |
| 2E87h | | | XXXX XXXXh |
| 2E88h | | | |
| 2E89h | | | |
| 2E8Ah | | | |
| 2E8Bh | | | |
| 2E8Ch | | | |
| 2E8Dh | | | |
| 2E8Eh | CAN0 Mailbox8 : Time stamp | | XXXXh |
| 2E8Fh | | | |
| 2E90h | CAN0 Mailbox9 : Message ID | C0MB9 | XXXX XXXXh |
| 2E91h | | | |
| 2E92h | | | |
| 2E93h | | | |
| 2E94h | | | |
| 2E95h | CAN0 Mailbox9 : Data length | | XXh |
| 2E96h | CAN0 Mailbox9 : Data field | | XXXX XXXX |
| 2E97h | | | XXXX XXXXh |
| 2E98h | | | |
| 2E99h | | | |
| 2E9Ah | | | |
| 2E9Bh | | | |
| 2E9Ch | | | |
| 2E9Dh | | | |
| 2E9Eh | CAN0 Mailbox9 : Time stamp | | XXXXh |
| 2E9Fh | | | |
| 2EA0h | CAN0 Mailbox10 : Message ID | C0MB10 | XXXX XXXXh |
| 2EA1h | | | |
| 2EA2h | | | |
| 2EA3h | | | |
| 2EA4h | | | |
| 2EA5h | CAN0 Mailbox10 : Data length | | XXh |
| 2EA6h | CAN0 Mailbox10 : Data field | | XXXX XXXX |
| 2EA7h | | | XXXX XXXXh |
| 2EA8h | | | |
| 2EA9h | | | |
| 2EAAh | | | |
| 2EABh | | | |
| 2EACh | | | |
| 2EADh | | | |
| 2EAEh | CAN0 Mailbox10 : Time stamp | | XXXXh |
| 2EAFh | | | |

X : Undefined
Note:
    1.  The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group         4. Special Function Registers (SFRs)

**Table 4.15    SFR Information (15)** [(1)]

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2EB0h | CAN0 Mailbox11 : Message ID | C0MB11 | XXXX XXXXh |
| 2EB1h | | | |
| 2EB2h | | | |
| 2EB3h | | | |
| 2EB4h | | | |
| 2EB5h | CAN0 Mailbox11 : Data length | | XXh |
| 2EB6h | CAN0 Mailbox11 : Data field | | XXXX XXXX |
| 2EB7h | | | XXXX XXXXh |
| 2EB8h | | | |
| 2EB9h | | | |
| 2EBAh | | | |
| 2EBBh | | | |
| 2EBCh | | | |
| 2EBDh | | | |
| 2EBEh | CAN0 Mailbox11 : Time stamp | | XXXXh |
| 2EBFh | | | |
| 2EC0h | CAN0 Mailbox12 : Message ID | C0MB12 | XXXX XXXXh |
| 2EC1h | | | |
| 2EC2h | | | |
| 2EC3h | | | |
| 2EC4h | | | |
| 2EC5h | CAN0 Mailbox12 : Data length | | XXh |
| 2EC6h | CAN0 Mailbox12 : Data field | | XXXX XXXX |
| 2EC7h | | | XXXX XXXXh |
| 2EC8h | | | |
| 2EC9h | | | |
| 2ECAh | | | |
| 2ECBh | | | |
| 2ECCh | | | |
| 2ECDh | | | |
| 2ECEh | CAN0 Mailbox12 : Time stamp | | XXXXh |
| 2ECFh | | | |
| 2ED0h | CAN0 Mailbox13 : Message ID | C0MB13 | XXXX XXXXh |
| 2ED1h | | | |
| 2ED2h | | | |
| 2ED3h | | | |
| 2ED4h | | | |
| 2ED5h | CAN0 Mailbox13 : Data length | | XXh |
| 2ED6h | CAN0 Mailbox13 : Data field | | XXXX XXXX |
| 2ED7h | | | XXXX XXXXh |
| 2ED8h | | | |
| 2ED9h | | | |
| 2EDAh | | | |
| 2EDBh | | | |
| 2EDCh | | | |
| 2EDDh | | | |
| 2EDEh | CAN0 Mailbox13 : Time stamp | | XXXXh |
| 2EDFh | | | |
| 2EE0h | CAN0 Mailbox14 : Message ID | C0MB14 | XXXX XXXXh |
| 2EE1h | | | |
| 2EE2h | | | |
| 2EE3h | | | |
| 2EE4h | | | |
| 2EE5h | CAN0 Mailbox14 : Data length | | XXh |
| 2EE6h | CAN0 Mailbox14 : Data field | | XXXX XXXX |
| 2EE7h | | | XXXX XXXXh |
| 2EE8h | | | |
| 2EE9h | | | |
| 2EEAh | | | |
| 2EEBh | | | |
| 2EECh | | | |
| 2EEDh | | | |
| 2EEEh | CAN0 Mailbox14 : Time stamp | | XXXXh |
| 2EEFh | | | |

X : Undefined
Note:
    1.    The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    4. Special Function Registers (SFRs)

### Table 4.16 SFR Information (16) [1]

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2EF0h | CAN0 Mailbox15 : Message ID | C0MB15 | XXXX XXXXh |
| 2EF1h | | | |
| 2EF2h | | | |
| 2EF3h | | | |
| 2EF4h | | | |
| 2EF5h | CAN0 Mailbox15 : Data length | | XXh |
| 2EF6h | CAN0 Mailbox15 : Data field | | XXXX XXXX |
| 2EF7h | | | XXXX XXXXh |
| 2EF8h | | | |
| 2EF9h | | | |
| 2EFAh | | | |
| 2EFBh | | | |
| 2EFCh | | | |
| 2EFDh | | | |
| 2EFEh | CAN0 Mailbox15 : Time stamp | | XXXXh |
| 2EFFh | | | |
| 2F00h | | | |
| 2F01h | | | |
| 2F02h | | | |
| 2F03h | | | |
| 2F04h | | | |
| 2F05h | | | |
| 2F06h | | | |
| 2F07h | | | |
| 2F08h | | | |
| 2F09h | | | |
| 2F0Ah | | | |
| 2F0Bh | | | |
| 2F0Ch | | | |
| 2F0Dh | | | |
| 2F0Eh | | | |
| 2F0Fh | | | |
| 2F10h | CAN0 Mask Register 0 | C0MKR0 | XXXX XXXXh |
| 2F11h | | | |
| 2F12h | | | |
| 2F13h | | | |
| 2F14h | CAN0 Mask Register 1 | C0MKR1 | XXXX XXXXh |
| 2F15h | | | |
| 2F16h | | | |
| 2F17h | | | |
| 2F18h | CAN0 Mask Register 2 | C0MKR2 | XXXX XXXXh |
| 2F19h | | | |
| 2F1Ah | | | |
| 2F1Bh | | | |
| 2F1Ch | CAN0 Mask Register 3 | C0MKR3 | XXXX XXXXh |
| 2F1Dh | | | |
| 2F1Eh | | | |
| 2F1Fh | | | |
| 2F20h | CAN0 FIFO Received ID Compare Register 0 | C0FIDCR0 | XXXX XXXXh |
| 2F21h | | | |
| 2F22h | | | |
| 2F23h | | | |
| 2F24h | CAN0 FIFO Received ID Compare Register 1 | C0FIDCR1 | XXXX XXXXh |
| 2F25h | | | |
| 2F26h | | | |
| 2F27h | | | |
| 2F28h | | | |
| 2F29h | | | |
| 2F2Ah | CAN0 Mask Invalid Register | C0MKIVLR | XXXXh |
| 2F2Bh | | | |
| 2F2Ch | | | |
| 2F2Dh | | | |
| 2F2Eh | CAN0 Mailbox Interrupt Enable Register | C0MIER | XXXXh |
| 2F2Fh | | | |
| 2F30h | CAN0 Message Control Register 0 | C0MCTL0 | 00h |
| 2F31h | CAN0 Message Control Register 1 | C0MCTL1 | 00h |
| 2F32h | CAN0 Message Control Register 2 | C0MCTL2 | 00h |
| 2F33h | CAN0 Message Control Register 3 | C0MCTL3 | 00h |
| 2F34h | CAN0 Message Control Register 4 | C0MCTL4 | 00h |
| 2F35h | CAN0 Message Control Register 5 | C0MCTL5 | 00h |
| 2F36h | CAN0 Message Control Register 6 | C0MCTL6 | 00h |
| 2F37h | CAN0 Message Control Register 7 | C0MCTL7 | 00h |
| 2F38h | CAN0 Message Control Register 8 | C0MCTL8 | 00h |
| 2F39h | CAN0 Message Control Register 9 | C0MCTL9 | 00h |
| 2F3Ah | CAN0 Message Control Register 10 | C0MCTL10 | 00h |

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group    4. Special Function Registers (SFRs)

**Table 4.17     SFR Information (17)** [1]

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 2F3Bh | CAN0 Message Control Register 11 | C0MCTL11 | 00h |
| 2F3Ch | CAN0 Message Control Register 12 | C0MCTL12 | 00h |
| 2F3Dh | CAN0 Message Control Register 13 | C0MCTL13 | 00h |
| 2F3Eh | CAN0 Message Control Register 14 | C0MCTL14 | 00h |
| 2F3Fh | CAN0 Message Control Register 15 | C0MCTL15 | 00h |
| 2F40h | CAN0 Control Register | C0CTLR | 0000 0101b |
| 2F41h | | | 0000 0000b |
| 2F42h | CAN0 Status Register | C0STR | 0000 0101b |
| 2F43h | | | 0000 0000b |
| 2F44h | CAN0 Bit Configuration Register | C0BCR | 00 0000h |
| 2F45h | | | |
| 2F46h | | | |
| 2F47h | | | |
| 2F48h | CAN0 Receive FIFO Control Register | C0RFCR | 1000 0000b |
| 2F49h | CAN0 Receive FIFO Pointer Control Register | C0RFPCR | XXh |
| 2F4Ah | CAN0 Transmit FIFO Control Register | C0TFCR | 1000 0000b |
| 2F4Bh | CAN0 Transmit FIFO Pointer Control Register | C0TFPCR | XXh |
| 2F4Ch | CAN0 Error Interrupt Enable Register | C0EIER | 00h |
| 2F4Dh | CAN0 Error Interrupt Factor Judge Register | C0EIFR | 00h |
| 2F4Eh | CAN0 Reception Error Count Register | C0RECR | 00h |
| 2F4Fh | CAN0 Transmission Error Count Register | C0TECR | 00h |
| 2F50h | CAN0 Error Code Store Register | C0ECSR | 00h |
| 2F51h | CAN0 Channel Search Support Register | C0CSSR | XXh |
| 2F52h | CAN0 Mailbox Search Status Register | C0MSSR | 1000 0000b |
| 2F53h | CAN0 Mailbox Search Mode Register | C0MSMR | 00h |
| 2F54h | CAN0 Time Stamp Register | C0TSR | 0000h |
| 2F55h | | | |
| 2F56h | CAN0 Acceptance Filter Support Register | C0AFSR | XXXXh |
| 2F57h | | | |
| 2F58h | CAN0 Test Control Register | C0TCR | 00h |
| : | | | |
| 2FFFh | | | |

X :  Undefined
Note:
1.   The blank areas are reserved and cannot be accessed by users.

**Table 4.18     ID Code Areas and Option Function Select Area**

| Address | Area Name | Symbol | After Reset |
|---------|-----------|--------|-------------|
| : | | | |
| FFDBh | Option Function Select Register 2 | OFS2 | (Note 1) |
| : | | | |
| FFDFh | ID1 | | (Note 2) |
| : | | | |
| FFE3h | ID2 | | (Note 2) |
| : | | | |
| FFEBh | ID3 | | (Note 2) |
| : | | | |
| FFEFh | ID4 | | (Note 2) |
| : | | | |
| FFF3h | ID5 | | (Note 2) |
| : | | | |
| FFF7h | ID6 | | (Note 2) |
| : | | | |
| FFFBh | ID7 | | (Note 2) |
| : | | | |
| FFFFh | Option Function Select Register | OFS | (Note 1) |

Notes:
1.   The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
     Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select
     area is set to FFh.
     When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
     When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2.   The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
     Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
     When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
     When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group　　　　　　　　　　　5. Electrical Characteristics

# 5.　Electrical Characteristics

**Table 5.1　Absolute Maximum Ratings**

| Symbol | Parameter | Condition | Rated Value | Unit |
|---|---|---|---|---|
| $V_{CC}/AV_{CC}$ | Supply voltage | | −0.3 to 6.5 | V |
| $V_I$ | Input voltage [1] | | −0.3 to $V_{CC}$ + 0.3 | V |
| IIN | Input current [1] | (2, 3, 4) | −4 to 4 | mA |
| $V_O$ | Output voltage | | −0.3 to $V_{CC}$ + 0.3 | V |
| $P_d$ | Power dissipation | −40 °C ≤ $T_{opr}$ < 85 °C | 300 | mW |
| | | 85 °C ≤ $T_{opr}$ < 125 °C | 125 | mW |
| $T_{opr}$ | Operating ambient temperature | | −40 to 85 (J version) / −40 to 125 (K version) | °C |
| $T_{stg}$ | Storage temperature | | −65 to 150 | °C |

Notes:
1. Meet the specified range for the input voltage or the input current.
2. Applicable ports: P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5
3. The total input current must be 12 mA or less.
4. Even if no voltage is supplied to Vcc, the input current may cause the MCU to be powered on and operate. When a voltage is supplied to Vcc, the input current may cause the supply voltage to rise. Since operations in any cases other than above are not guaranteed, use the power supply circuit in the system to ensure the supply voltage for the MCU is stable within the specified range.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group
5. Electrical Characteristics

### Table 5.2    Recommended Operating Conditions (1)

| Symbol | Parameter | | | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Typ. | Max. | |
| $V_{CC}/AV_{CC}$ | Supply voltage | | | | | 2.7 | – | 5.5 | V |
| $V_{SS}/AV_{SS}$ | Supply voltage | | | | | – | 0 | – | V |
| $V_{IH}$ | Input "H" voltage | Other than CMOS input | | | | 0.8 $V_{CC}$ | – | $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection : 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.5 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.55 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | Input level selection : 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.65 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.7 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | Input level selection : 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.85 $V_{CC}$ | – | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.85 $V_{CC}$ | – | $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 1.2 | – | $V_{CC}$ | V |
| $V_{IL}$ | Input "L" voltage | Other than CMOS input | | | | 0 | – | 0.2 $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection : 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.2 $V_{CC}$ | V |
| | | | | Input level selection : 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.4 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.3 $V_{CC}$ | V |
| | | | | Input level selection : 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 0.55 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | – | 0.45 $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 0 | – | 0.4 | V |
| $I_{OH(sum)}$ | Peak sum output "H" current | Sum of all pins $I_{OH(peak)}$ | | | | – | – | −80 | mA |
| $I_{OH(sum)}$ | Average sum output "H" current | Sum of all pins $I_{OH(avg)}$ | | | | – | – | −40 | mA |
| $I_{OH(peak)}$ | Peak output "H" current | | | | | – | – | −10 | mA |
| $I_{OH(avg)}$ | Average output "H" current | | | | | – | – | −5 | mA |
| $I_{OL(sum)}$ | Peak sum output "L" current | Sum of all pins $I_{OL(peak)}$ | | | | – | – | 80 | mA |
| $I_{OL(sum)}$ | Average sum output "L" current | Sum of all pins $I_{OL(avg)}$ | | | | – | – | 40 | mA |
| $I_{OL(peak)}$ | Peak output "L" current | | | | | – | – | 10 | mA |
| $I_{OL(avg)}$ | Average output "L" current | | | | | – | – | 5 | mA |
| $f_{(XIN)}$ | XIN clock input oscillation frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| fOCO40M | Count source for timer RC, timer RD, or timer RG | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | 32 | – | 40 | MHz |
| fOCO-F | fOCO-F frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| – | System clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| $f_{(BCLK)}$ | CPU clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |

Notes:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                              5. Electrical Characteristics

**Table 5.3    Recommended Operating Conditions (2)**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|--------|-----------|--|-----------|----------|--|--|------|
| | | | | Min. | Typ. | Max. | |
| $I_{IC(H)}$ | High input injection current | P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5 | $V_I > V_{CC}$ | – | – | 2 | mA |
| $I_{IC(L)}$ | Low input injection current | P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5 | $V_I > V_{SS}$ | – | – | −2 | mA |
| $\Sigma|I_{IC}|$ | Total injection current | | | – | – | 8 | mA |

Note:
  1.  $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version), unless otherwise specified.
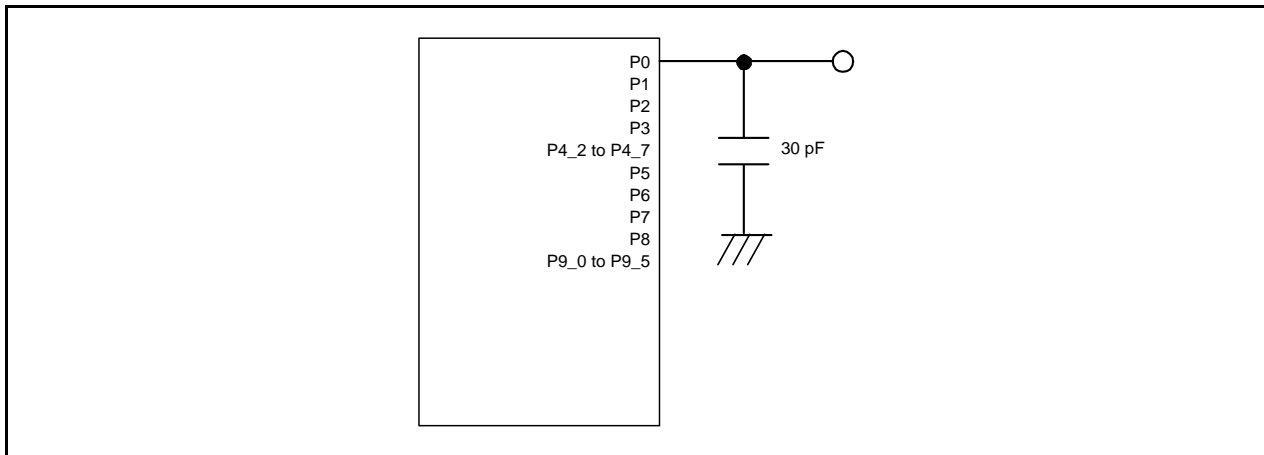


**Figure 5.1    Ports P0 to P3, P4_2 to P4_7, P5 to P8, and P9_0 to P9_5 Timing Measurement Circuit**

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group 5. Electrical Characteristics

### Table 5.4 A/D Converter Characteristics

| Symbol | Parameter | | Conditions | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| − | Resolution | | $V_{ref}$ = AVCC | | − | − | 10 | Bit |
| − | Absolute accuracy | 10-bit mode | $V_{ref}$ = AVCC = 5.0 V | AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input | − | − | ±3 | LSB |
| | | | $V_{ref}$ = AVCC = 3.0 V | AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input | − | − | ±5 | LSB |
| | | 8-bit mode | $V_{ref}$ = AVCC = 5.0 V | AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input | − | − | ±2 | LSB |
| | | | $V_{ref}$ = AVCC = 3.0 V | AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input | − | − | ±2 | LSB |
| $\phi$AD | A/D conversion clock | | $4.0 \leq V_{ref}$ = AVCC = $\leq 5.5$ [2] | | 2 | − | 20 | MHz |
| | | | $2.7 \leq V_{ref}$ = AVCC = $\leq 5.5$ [2] | | 2 | − | 10 | MHz |
| − | Tolerance level impedance | | | | − | 3 | − | k$\Omega$ |
| Ivref | $V_{ref}$ current | | VCC = 5.0 V, XIN = f1 = $\phi$AD = 20 MHz | | − | 45 | − | $\mu$A |
| tCONV | Conversion time | 10-bit mode | $V_{ref}$ = AVCC = 5.0 V, $\phi$AD = 20 MHz | | 2.2 | − | − | $\mu$s |
| | | 8-bit mode | $V_{ref}$ = AVCC = 5.0 V, $\phi$AD = 20 MHz | | 2.2 | − | − | $\mu$s |
| tSAMP | Sampling time | | $\phi$AD = 20 MHz | | 0.75 | − | − | $\mu$s |
| $V_{ref}$ | Reference voltage | | | | 2.7 | − | AVCC | V |
| VIA | Analog input voltage [3] | | | | 0 | − | $V_{ref}$ | V |
| OCVREF | On-chip reference voltage | | 2 MHz $\leq \phi$AD $\leq$ 4 MHz | | 1.14 | 1.34 | 1.54 | V |

Notes:
1. VCC/AVCC = $V_{ref}$ = 2.7 to 5.5 V, VSS = 0 V at Topr = −40 to 85°C (J version) / −40 to 125°C (K version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group　　　　　　　　　　　5. Electrical Characteristics

**Table 5.5　Flash Memory (Program ROM) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance [2] | R8C/38X, R8C/38Z Group | 100 [3] | – | – | times |
| | | R8C/38W, R8C/38Y Group | 1,000 [3] | – | – | times |
| – | Byte program time (program/erase endurance $\leq$ 1,000 times) | | – | 60 | 300 | μs |
| – | Byte program time (program/erase endurance > 1,000 times) | | – | 60 | 500 | μs |
| – | Word program time (program/erase endurance $\leq$ 1,000 times) | | – | 100 | 400 | μs |
| – | Word program time (program/erase endurance > 1,000 times) | | – | 100 | 650 | μs |
| – | Block erase time | | – | 0.3 | 4 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 5+CPU clock × 3 cycles | ms |
| – | Interval from erase start/restart until following suspend request | | 0 | – | – | μs |
| – | Time from suspend until erase restart | | – | – | 30+CPU clock × 1 cycle | μs |
| $t_{d(CMDRST-READY)}$ | Time from when command is forcibly terminated until reading is enabled | | – | – | 30+CPU clock × 1 cycle | μs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.7 | – | 5.5 | V |
| – | Program, erase temperature | | –40 | – | 85 (J version) 125 (K version) | °C |
| – | Data hold time [7] | Ambient temperature = 55°C [8] | 20 | – | – | year |

Notes:
1. VCC = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version) (under consideration), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100, 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.
8. This data hold time includes 3,000 hours in Ta = 125°C and 7,000 hours in Ta = 85°C.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

5. Electrical Characteristics

**Table 5.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| − | Program/erase endurance [2] | | 10,000 [3] | − | − | times |
| − | Byte program time (program/erase endurance ≤ 1,000 times) | | − | 160 | 950 | μs |
| − | Byte program time (program/erase endurance > 1,000 times) | | − | 300 | 950 | μs |
| − | Block erase time (program/erase endurance ≤ 1,000 times) | | − | 0.2 | 1 | s |
| − | Block erase time (program/erase endurance > 1,000 times) | | − | 0.3 | 1 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | − | − | 3+CPU clock × 3 cycles | ms |
| − | Interval from erase start/restart until following suspend request | | 0 | − | − | μs |
| − | Time from suspend until erase restart | | − | − | 30+CPU clock × 1 cycle | μs |
| $t_{d(CMDRST-READY)}$ | Time from when command is forcibly terminated until reading is enabled | | − | − | 30+CPU clock × 1 cycle | μs |
| − | Program, erase voltage | | 2.7 | − | 5.5 | V |
| − | Read voltage | | 2.7 | − | 5.5 | V |
| − | Program, erase temperature | | −40 | − | 85 (J version) 125 (K version) | °C |
| − | Data hold time [7] | Ambient temperature = 55 °C [8] | 20 | − | − | year |

Notes:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100, 1,000, 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.
8. This data hold time includes 3,000 hours in Ta = 125°C and 7,000 hours in Ta = 85°C.
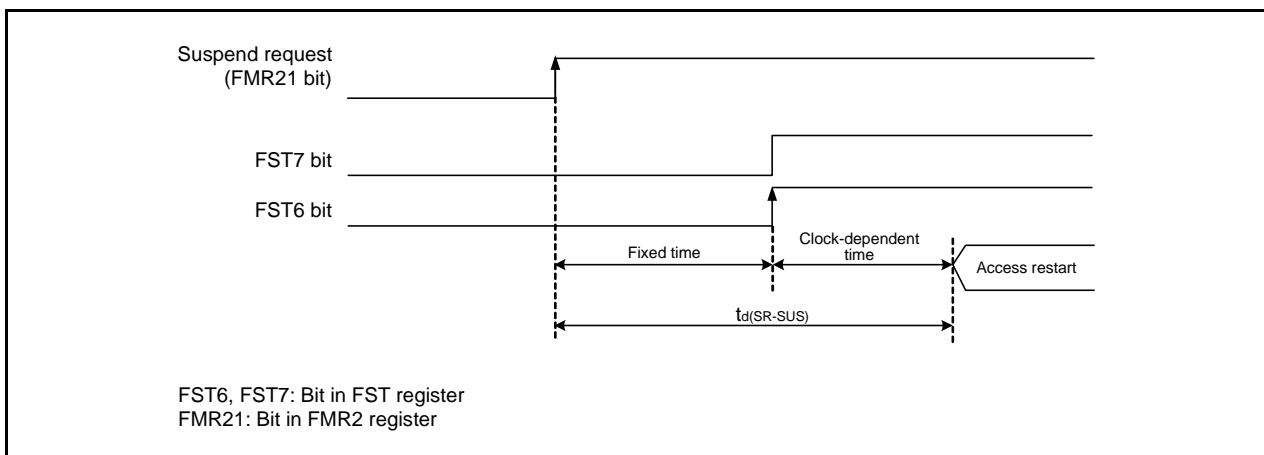


**Figure 5.2 Time delay until Suspend**

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**Table 5.7     Voltage Detection 0 Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det0}$ | Voltage detection level | At the falling of $V_{CC}$ | 2.70 | 2.85 | 3.00 | V |
| – | Voltage detection 0 circuit response time [3] | At the falling of Vcc from 5 V to (Vdet0 − 0.1) V | – | 6 | 150 | μs |
| – | Voltage detection circuit self power consumption | VCA25 = 1, Vcc = 5.0 V | – | 1.5 | – | μA |
| $t_{d(E-A)}$ | Wait time until voltage detection circuit operation starts [2] | | – | – | 100 | μs |

Notes:
1. The measurement condition is $V_{CC}$ = 2.7 V to 5.5 V and $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes $V_{det0}$.

**Table 5.8     Voltage Detection 1 Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level Vdet1_7 [2] | At the falling of $V_{CC}$ | 3.05 | 3.25 | 3.45 | V |
| | Voltage detection level Vdet1_8 [2] | At the falling of $V_{CC}$ | 3.20 | 3.40 | 3.60 | V |
| | Voltage detection level Vdet1_9 [2] | At the falling of $V_{CC}$ | 3.35 | 3.55 | 3.75 | V |
| | Voltage detection level Vdet1_A [2] | At the falling of $V_{CC}$ | 3.50 | 3.70 | 3.90 | V |
| | Voltage detection level Vdet1_B [2] | At the falling of $V_{CC}$ | 3.65 | 3.85 | 4.05 | V |
| | Voltage detection level Vdet1_C [2] | At the falling of $V_{CC}$ | 3.80 | 4.00 | 4.20 | V |
| | Voltage detection level Vdet1_D [2] | At the falling of $V_{CC}$ | 3.95 | 4.15 | 4.35 | V |
| | Voltage detection level Vdet1_E [2] | At the falling of $V_{CC}$ | 4.10 | 4.30 | 4.50 | V |
| – | Hysteresis width at the rising of Vcc in voltage detection 1 circuit | | – | 0.1 | – | V |
| – | Voltage detection 1 circuit response time [3] | At the falling of Vcc from 5 V to (Vdet1_7 − 0.1) V | – | 60 | 150 | μs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, Vcc = 5.0 V | – | 1.7 | – | μA |
| $t_{d(E-A)}$ | Wait time until voltage detection circuit operation starts [4] | | – | – | 100 | μs |

Notes:
1. The measurement condition is $V_{CC}$ = 2.7 V to 5.5 V and $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes $V_{det1}$.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 5.9     Voltage Detection 2 Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level Vdet2 | At the falling of $V_{CC}$ | 3.80 | 4.00 | 4.20 | V |
| – | Hysteresis width at the rising of Vcc in voltage detection 2 circuit | | – | 0.1 | – | V |
| – | Voltage detection 2 circuit response time [2] | At the falling of Vcc from 5 V to (Vdet2 − 0.1) V | – | 20 | 150 | μs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, Vcc = 5.0 V | – | 1.7 | – | μA |
| $t_{d(E-A)}$ | Wait time until voltage detection circuit operation starts [3] | | – | – | 100 | μs |

Notes:
1. The measurement condition is $V_{CC}$ = 2.7 V to 5.5 V and $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

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**Table 5.10    Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics[2]**

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|-----------|-----------|------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{rth}$ | External power $V_{CC}$ rise gradient | [1] | 0 | − | 50000 | mV/msec |

Notes:
1. The measurement condition is $V_{CC}$ = 2.7 V to 5.5 V and $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version).
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.
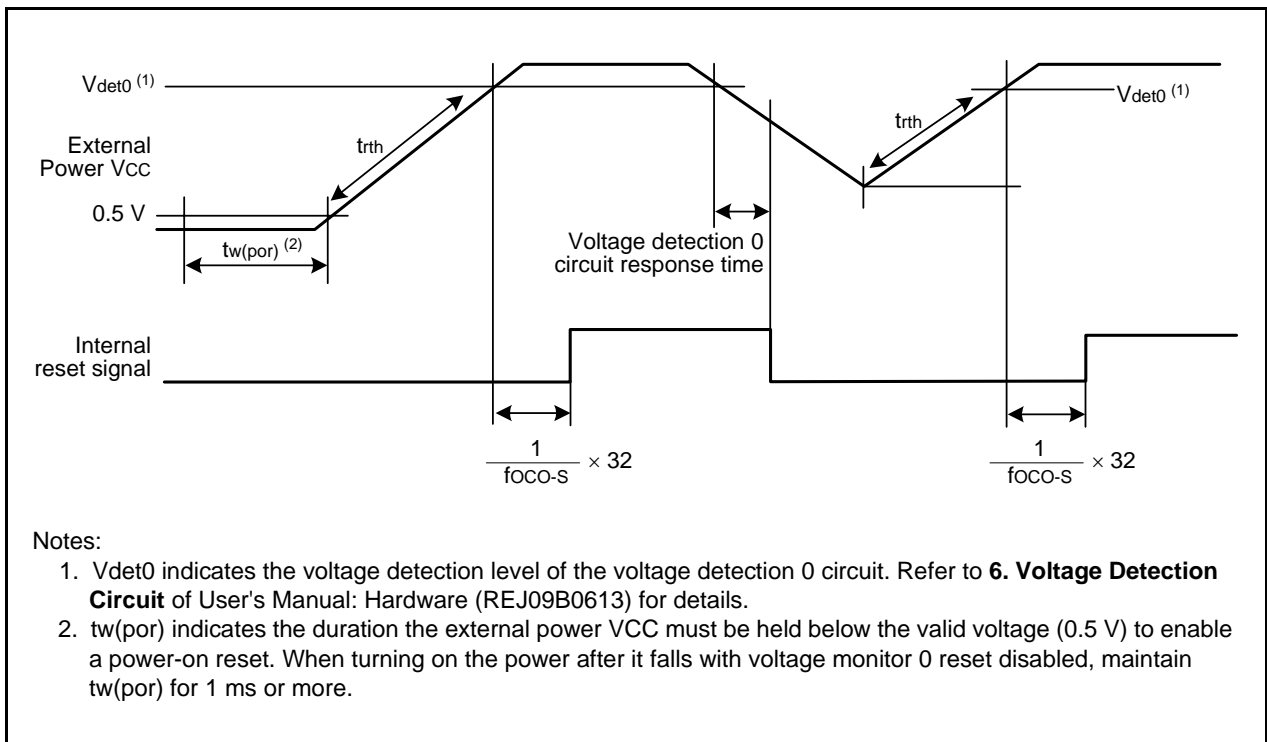


Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware (REJ09B0613) for details.
2. tw(por) indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.

**Figure 5.3    Power-on Reset Circuit Electrical Characteristics**

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**Table 5.11    High-speed On-Chip Oscillator Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | High-speed on-chip oscillator frequency after reset | $V_{CC}$ = 2.7 to 5.5 V, $-40°C \leq T_{opr} \leq 85°C$ (J version) / $-40°C \leq T_{opr} \leq 125°C$ (K version) | – | 40 | – | MHz |
| | High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register [3] | | – | 36.864 | – | MHz |
| | High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register | | – | 32 | – | MHz |
| | High-speed on-chip oscillator frequency temperature • supply voltage dependence [2] | | –5 | – | 5 | % |
| – | Oscillation stabilization time | | – | 200 | – | μs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 400 | – | μA |

Notes:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version).
2. This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.
3. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 5.12    Low-speed On-Chip Oscillator Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 112.5 | 125 | 137.5 | kHz |
| fOCO-WDT | Low-speed on-chip oscillator frequency for watchdog timer | | 112.5 | 125 | 137.5 | kHz |
| – | Oscillation stabilization time | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 30 | 100 | μs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 3 | – | μA |

Note:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version).

**Table 5.13    Power Supply Circuit Timing Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on [2] | | – | – | 2000 | μs |

Notes:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version).
2. Wait time until the internal power supply generation circuit stabilizes during power-on.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group  5. Electrical Characteristics

### Table 5.14 Timing Requirements of SSU [1]

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $t_{SUCYC}$ | SSCK clock cycle time | | | 4 | – | – | $t_{CYC}$ [2] |
| $t_{HI}$ | SSCK clock "H" width | | | 0.4 | – | 0.6 | $t_{SUCYC}$ |
| $t_{LO}$ | SSCK clock "L" width | | | 0.4 | – | 0.6 | $t_{SUCYC}$ |
| $t_{RISE}$ | SSCK clock rising time | Master | | – | – | 1 | $t_{CYC}$ [2] |
| | | Slave | | – | – | 1 | µs |
| $t_{FALL}$ | SSCK clock falling time | Master | | – | – | 1 | $t_{CYC}$ [2] |
| | | Slave | | – | – | 1 | µs |
| $t_{SU}$ | SSO, SSI data input setup time | | | 100 | – | – | ns |
| $t_{H}$ | SSO, SSI data input hold time | | | 1 | – | – | $t_{CYC}$ [2] |
| $t_{LEAD}$ | $\overline{SCS}$ setup time | Slave | | 1$t_{CYC}$ + 50 | – | – | ns |
| $t_{LAG}$ | $\overline{SCS}$ hold time | Slave | | 1$t_{CYC}$ + 50 | – | – | ns |
| $t_{OD}$ | SSO, SSI data output delay time | | | – | – | 1 | $t_{CYC}$ [2] |
| $t_{SA}$ | SSI slave access time | | 2.7 V ≤ Vcc ≤ 5.5 V | – | – | 1.5$t_{CYC}$ + 100 | ns |
| $t_{OR}$ | SSI slave out open time | | 2.7 V ≤ Vcc ≤ 5.5 V | – | – | 1.5$t_{CYC}$ + 100 | ns |

Notes:
1. The measurement condition is Vcc = 2.7 to 5.5 V and $T_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version).
2. 1$t_{CYC}$ = 1/f1(s)

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group
5. Electrical Characteristics
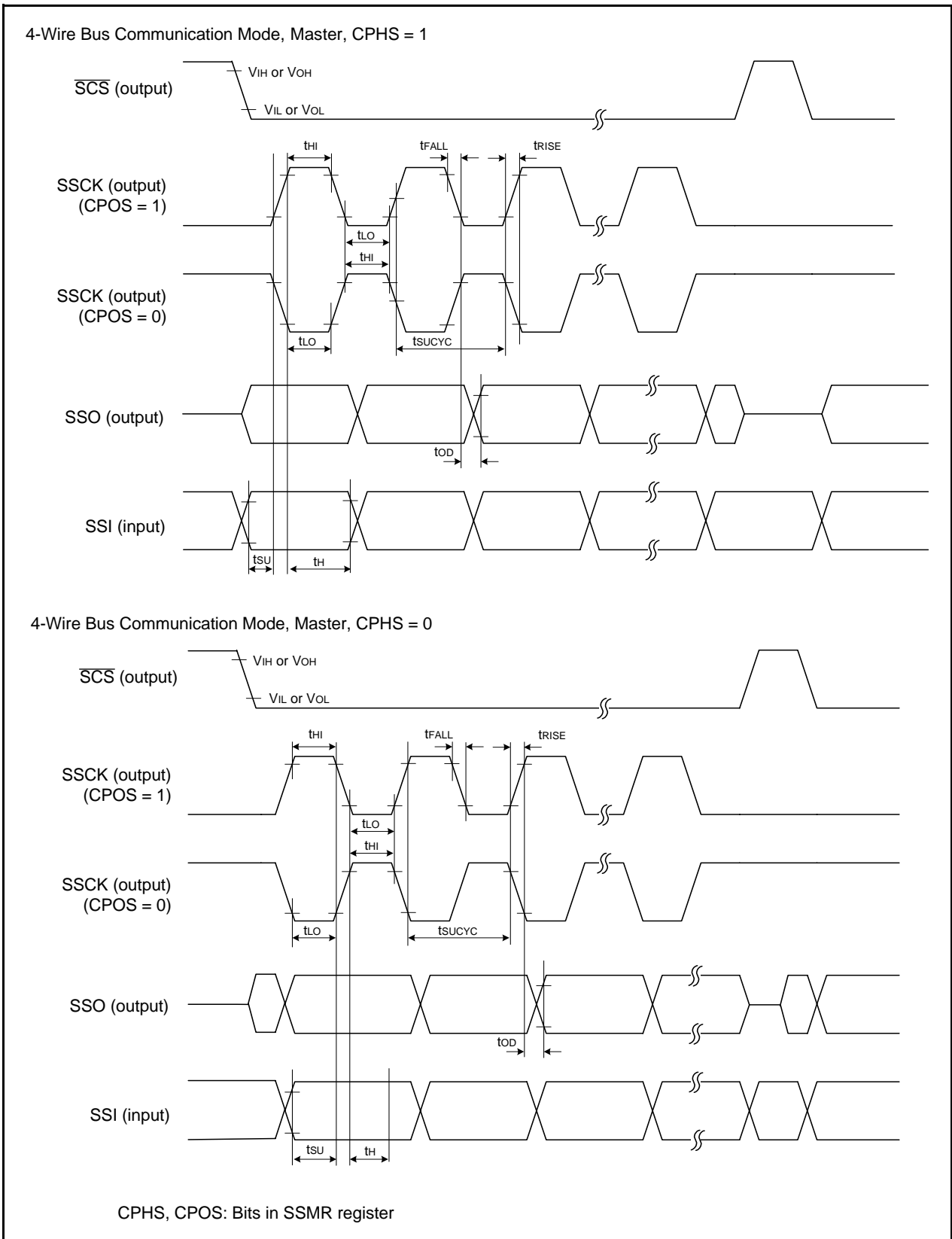
**Figure 5.4    I/O Timing of SSU (Master)**

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    5. Electrical Characteristics
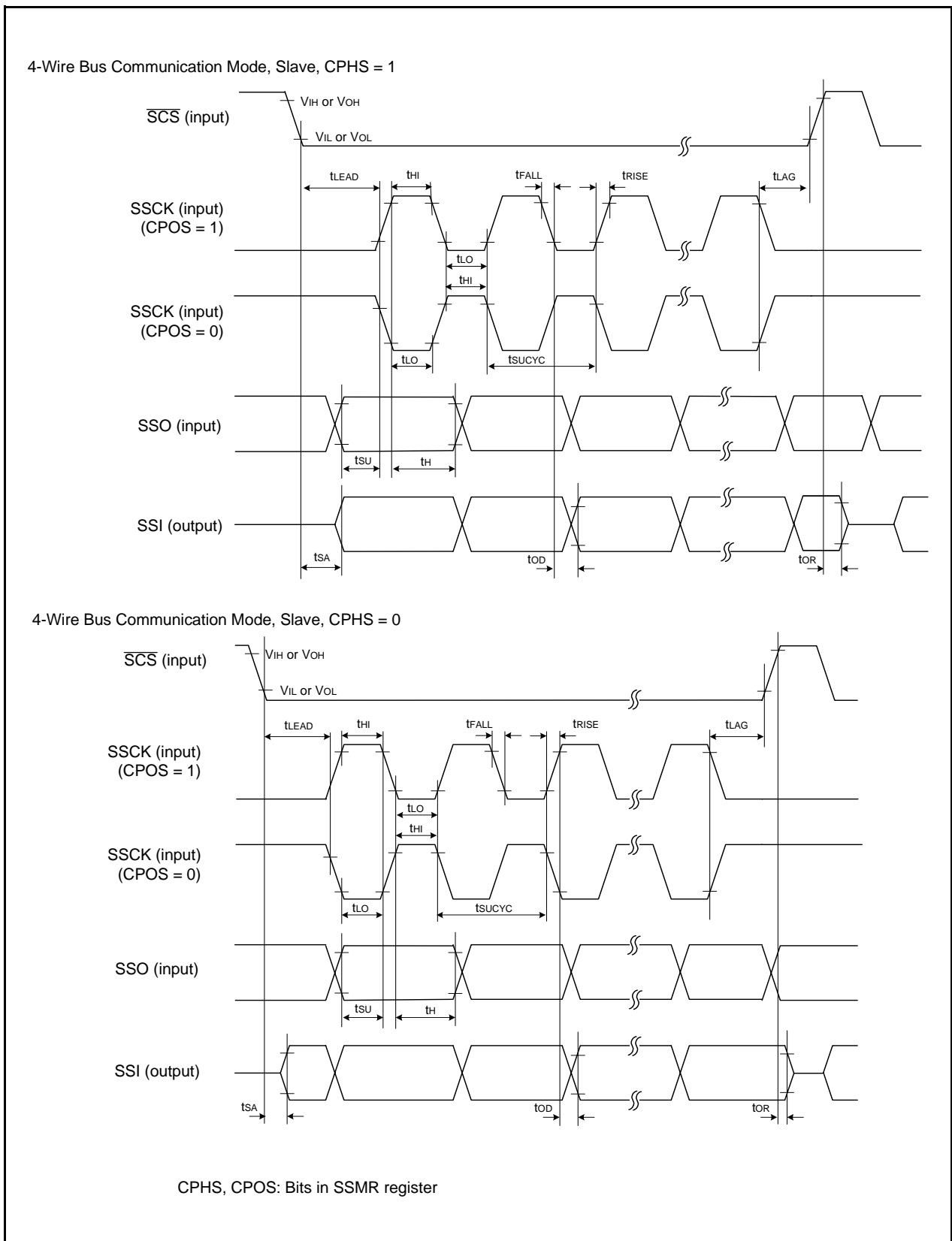
**Figure 5.5    I/O Timing of SSU (Slave)**

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    5. Electrical Characteristics
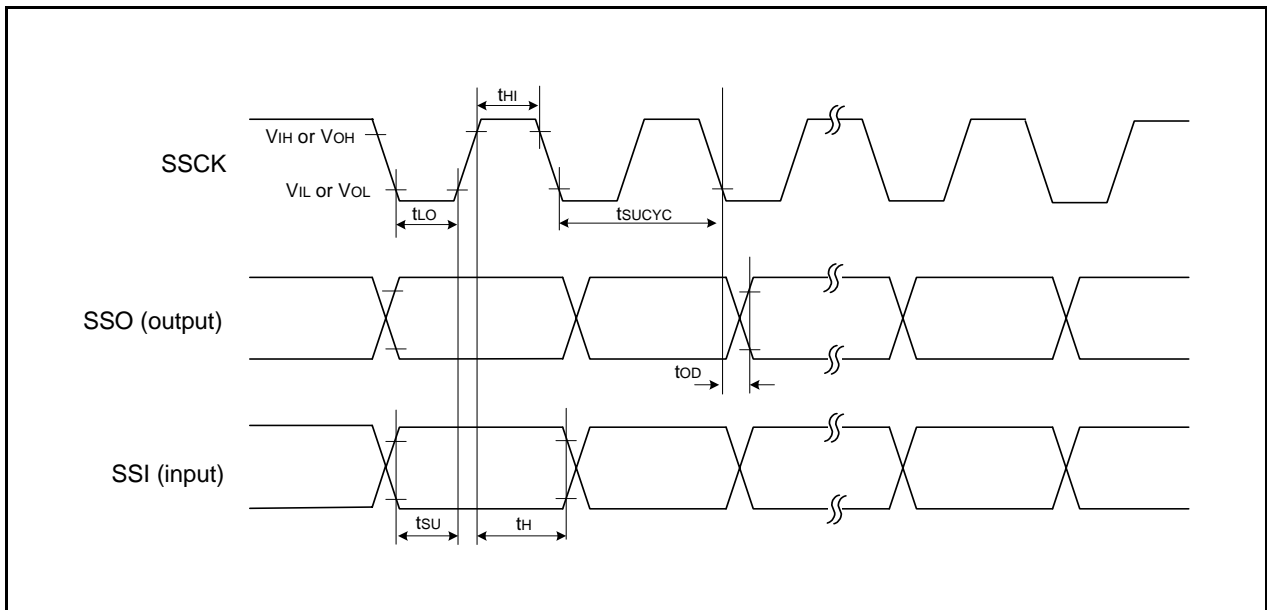
**Figure 5.6      I/O Timing of SSU (Clock Synchronous Communication Mode)**

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group 5. Electrical Characteristics

### Table 5.15 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

| Symbol | Parameter | | Condition | Standard | | | Unit |
|--------|-----------|--|-----------|-----|------|------|------|
| | | | | Min. | Typ. | Max. | |
| V$_{OH}$ | Output "H" voltage | Other than XOUT | I$_{OH}$ = −5 mA | V$_{CC}$ − 2.0 | – | V$_{CC}$ | V |
| | | | I$_{OH}$ = −200 μA | V$_{CC}$ − 0.3 | – | V$_{CC}$ | V |
| | | XOUT | I$_{OH}$ = −200 μA | 1.0 | – | V$_{CC}$ | V |
| V$_{OL}$ | Output "L" voltage | Other than XOUT | I$_{OL}$ = 5 mA | – | – | 2.0 | V |
| | | | I$_{OL}$ = 200 μA | – | – | 0.45 | V |
| | | XOUT | I$_{OH}$ = −200 μA | – | – | 0.5 | V |
| V$_{T+}$-V$_{T-}$ | Hysteresis | $\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRAIO0, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOA0 to TRDIOD0, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, TRGCLKB, TRCTRG, ADTRG, RXD0 to RXD2, CLK0 to CLK2, SSI, SCL2, SDA2, SSO | | 0.1 | 1.2 | – | V |
| | | $\overline{RESET}$ | | 0.1 | 1.2 | – | V |
| I$_{IH}$ | Input "H" current | | VI = 5 V | – | – | 1.0 | μA |
| I$_{IL}$ | Input "L" current | | VI = 0 V | – | – | −1.0 | μA |
| R$_{PULLUP}$ | Pull-up resistance | | VI = 0 V | 25 | 50 | 100 | kΩ |
| R$_{fXIN}$ | Feedback resistance | XIN | | – | 0.3 | – | MΩ |
| V$_{RAM}$ | RAM hold voltage | | During stop mode | 2.0 | – | – | V |

Note:
1. 4.2 V ≤ V$_{CC}$ ≤ 5.5 V at T$_{opr}$ = −40 to 85°C (J version) / −40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

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### Table 5.16 Electrical Characteristics (2) [3.3 V $\leq$ Vcc $\leq$ 5.5 V] (T$_{opr}$ = $-$40 to 85°C (J version), unless otherwise specified.)

| Symbol | Parameter | Condition | | Standard Min. | Standard Typ. | Standard Max. | Unit |
|---|---|---|---|---|---|---|---|
| Icc | Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode [1] | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | $-$ | 7.0 | 15 | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | $-$ | 5.6 | 12.5 | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | $-$ | 3.6 | $-$ | mA |
| | | | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | $-$ | 3.0 | $-$ | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | $-$ | 2.2 | $-$ | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | $-$ | 1.5 | $-$ | mA |
| | | High-speed on-chip oscillator mode [1] | XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division | $-$ | 7.0 | 15 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | $-$ | 3.0 | $-$ | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0 | $-$ | 90 | 180 | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | $-$ | 15 | 110 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | $-$ | 5 | 100 | μA |
| | | Stop mode | XIN clock off, T$_{opr}$ = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | $-$ | 2.0 | 5.0 | μA |
| | | | XIN clock off, T$_{opr}$ = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | $-$ | 15.0 | $-$ | μA |

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

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5. Electrical Characteristics

**Table 5.17 Electrical Characteristics (3) [3.3 V $\leq$ Vcc $\leq$ 5.5 V]**
**(T$_{opr}$ = $-$40 to 125$°$C (K version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode [1] | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | $-$ | 7.0 | 15 | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | $-$ | 5.6 | 12.5 | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | $-$ | 3.6 | $-$ | mA |
| | | | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | $-$ | 3.0 | $-$ | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | $-$ | 2.2 | $-$ | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | $-$ | 1.5 | $-$ | mA |
| | | High-speed on-chip oscillator mode [1] | XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division | $-$ | 7.0 | 15 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | $-$ | 3.0 | $-$ | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0 | $-$ | 90 | 400 | $\mu$A |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | $-$ | 15 | 330 | $\mu$A |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | $-$ | 5 | 320 | $\mu$A |
| | | Stop mode | XIN clock off, T$_{opr}$ = 25$°$C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | $-$ | 2.0 | 5.0 | $\mu$A |
| | | | XIN clock off, T$_{opr}$ = 125$°$C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | $-$ | 60.0 | $-$ | $\mu$A |

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

*Under development* Preliminary document
Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    5. Electrical Characteristics

### Timing Requirements
### (Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = −40°C to 85°C (J ver)/−40°C to 125°C (K ver))

#### Table 5.18    External clock input (XOUT)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 50 | – | ns |
| $t_{WH(XOUT)}$ | XOUT input "H" width | 24 | – | ns |
| $t_{WL(XOUT)}$ | XOUT input "L" width | 24 | – | ns |
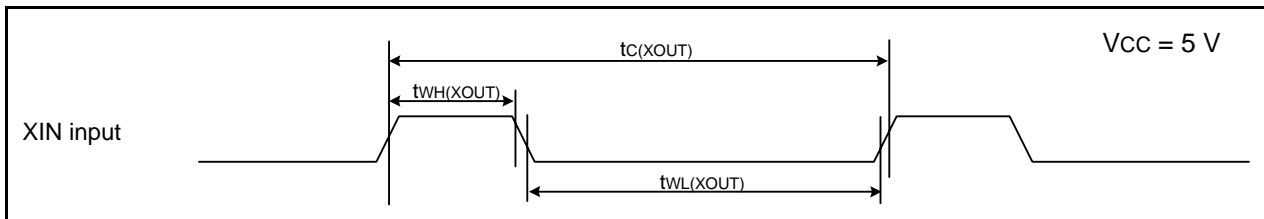


**Figure 5.7    External Clock Input Timing Diagram when VCC = 5 V**

#### Table 5.19    TRAIOi (i = 0 to 1) Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIOi (i = 0 to 1) input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIOi (i = 0 to 1) input "H" width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIOi (i = 0 to 1) input "L" width | 40 | – | ns |
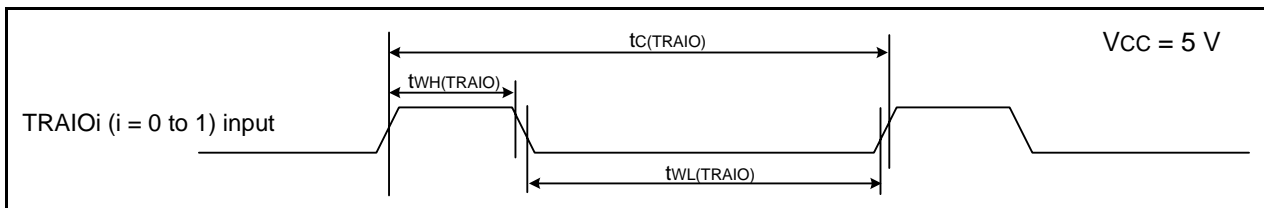


**Figure 5.8    TRAIOi (i = 0 to 1) Input Timing Diagram when Vcc = 5 V**

#### Table 5.20    TRFI Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRFI)}$ | TRFI input cycle time | 1200 [1] | – | ns |
| $t_{WH(TRFI)}$ | TRFI input "H" width | 600 [2] | – | ns |
| $t_{WL(TRFI)}$ | TRFI input "L" width | 600 [2] | – | ns |

Notes:
1.  When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2.  When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.
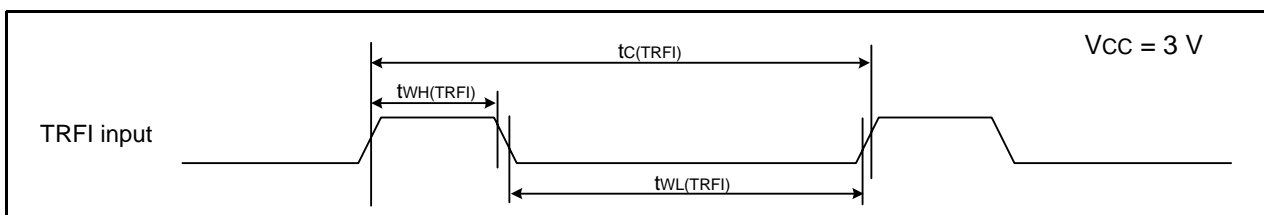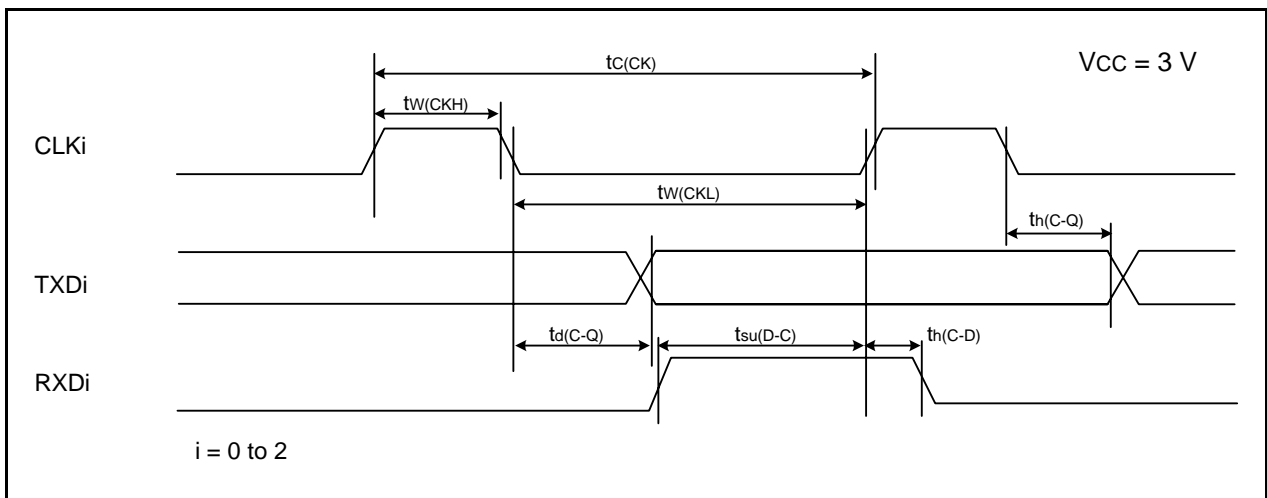


**Figure 5.9    TRFI Input Timing Diagram when Vcc = 3 V**

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    5. Electrical Characteristics

**Table 5.21    Serial Interface**

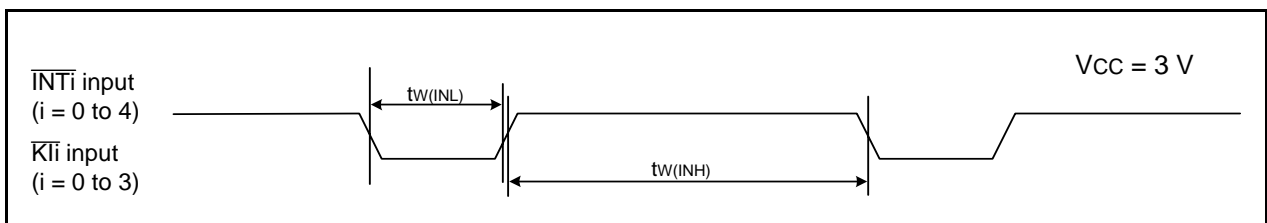| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|--------|-----------|------|------|------|
| $t_{C(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{W(CKH)}$ | CLKi input "H" width | 100 | – | ns |
| $t_{W(CKL)}$ | CLKi input "L" width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 90 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 to 2
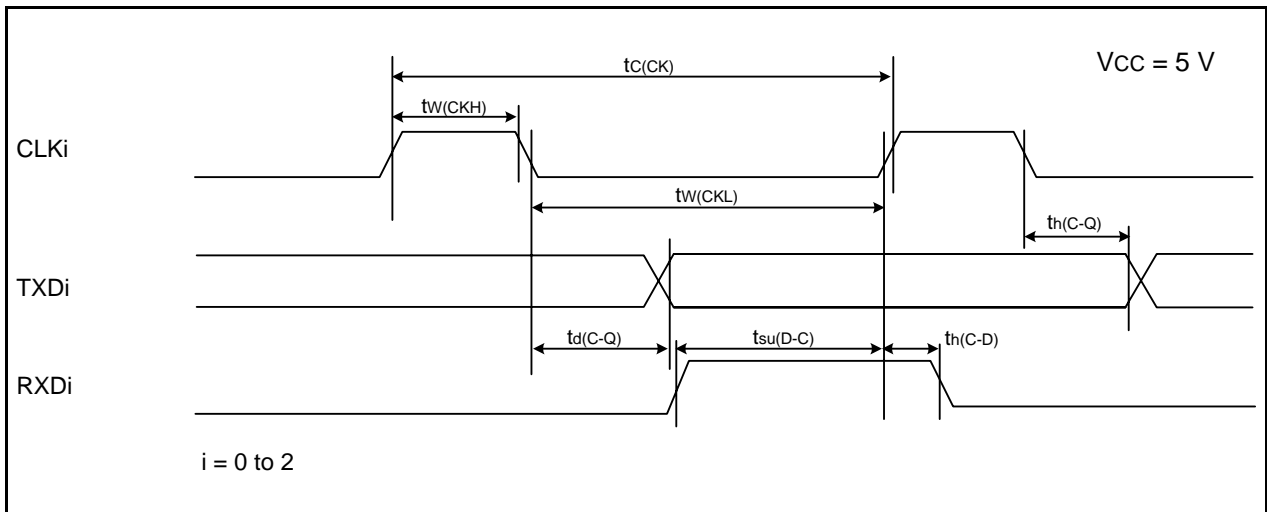


**Figure 5.10    Serial Interface Timing Diagram when V_CC = 5 V**

**Table 5.22    External Interrupt INTi (i = 0 to 4) Input, Key Input Interrupt KIi (i = 0 to 3)**

| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|--------|-----------|------|------|------|
| $t_{W(INH)}$ | INTi input "H" width, KIi input "H" width | 250 [1] | – | ns |
| $t_{W(INL)}$ | INTi input "L" width, KIi input "L" width | 250 [2] | – | ns |

Notes:
1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
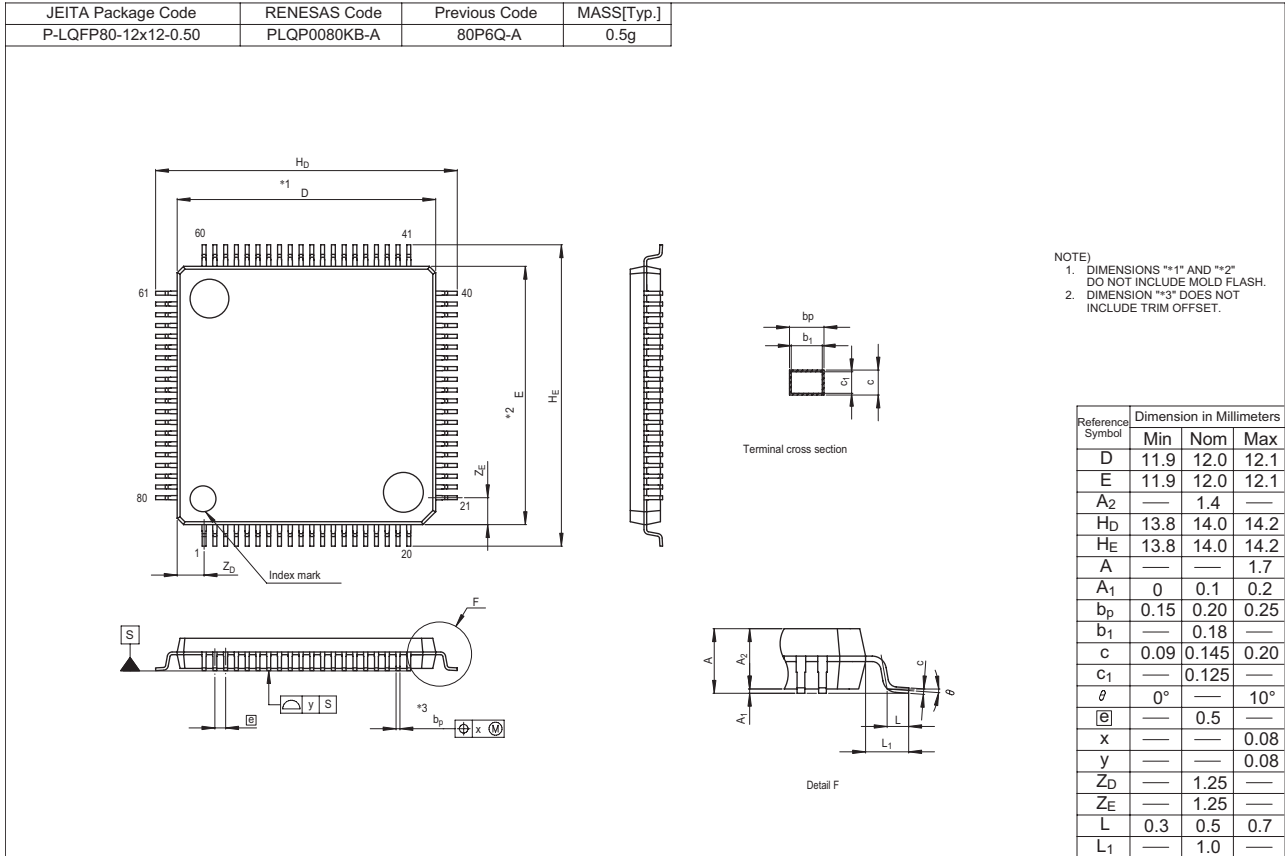2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
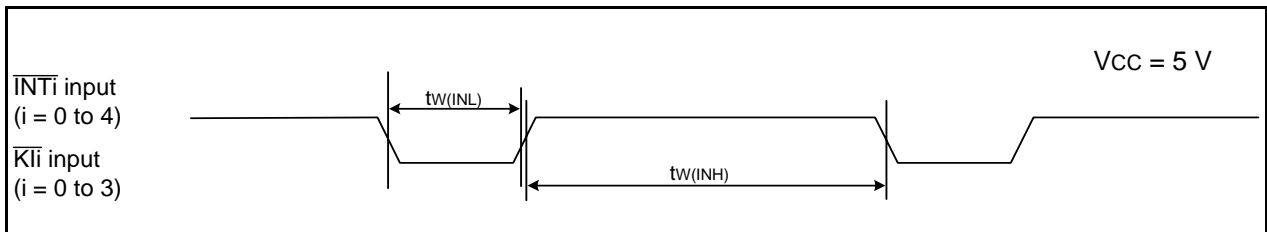


**Figure 5.11    Input Timing for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 5 V**

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                     5. Electrical Characteristics

**Table 5.23    Electrical Characteristics (4) [2.7 V $\leq$ Vcc $\leq$ 4.2 V]**

| Symbol | Parameter | | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| VOH | Output "H" voltage | Other than XOUT | IOH = −1 mA | Vcc − 0.5 | − | Vcc | V |
| | | XOUT | IOH = −200 μA | 1.0 | − | Vcc | V |
| VOL | Output "L" voltage | Other than XOUT | IOL = 1 mA | − | − | 0.5 | V |
| | | XOUT | IOL = 200 μA | − | − | 0.5 | V |
| VT+-VT- | Hysteresis | $\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRAIO0, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOA0 to TRDIOD0, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, TRGCLKB, TRCTRG, ADTRG, RXD0 to RXD2, CLK0 to CLK2, SSI, SCL2, SDA2, SSO | | 0.1 | 0.4 | − | V |
| | | $\overline{RESET}$ | | 0.1 | 0.5 | − | V |
| IIH | Input "H" current | | VI = 3 V | − | − | 1.0 | μA |
| IIL | Input "L" current | | VI = 0 V | − | − | −1.0 | μA |
| RPULLUP | Pull-up resistance | | VI = 0 V | 42 | 84 | 168 | kΩ |
| RfXIN | Feedback resistance | XIN | | − | 0.3 | − | MΩ |
| VRAM | RAM hold voltage | | During stop mode | 2.0 | − | − | V |

Note:
1.   2.7 V $\leq$ Vcc $\leq$ 4.2 V at Topr = −40 to 85°C (J version) / −40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

*Under development*  Preliminary document
Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                   5. Electrical Characteristics

### Table 5.24  Electrical Characteristics (5) [2.7 V $\leq$ Vcc $\leq$ 3.3 V]
### (T$_{opr}$ = $-$40 to 85°C (J version), unless otherwise specified.)

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| I$_{CC}$ | Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode [1] | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 7.0 | 14.5 | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 5.6 | 12.0 | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 3.6 | − | mA |
| | | | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 3.0 | − | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 2.2 | − | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 1.5 | − | mA |
| | | High-speed on-chip oscillator mode [1] | XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division | − | 7.0 | 14.5 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 3.0 | − | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0 | − | 85 | 180 | µA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | − | 15 | 110 | µA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | − | 5 | 100 | µA |
| | | Stop mode | XIN clock off, T$_{opr}$ = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | − | 2.0 | 5.0 | µA |
| | | | XIN clock off, T$_{opr}$ = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | − | 13.0 | − | µA |

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                        5. Electrical Characteristics

**Table 5.25    Electrical Characteristics (6) [2.7 V ≤ Vcc ≤ 3.3 V]**
**(Topr = −40 to 125°C (K version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode (1) | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 7.0 | 14.5 | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 5.6 | 12.0 | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | − | 3.6 | − | mA |
| | | | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 3.0 | − | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 2.2 | − | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 1.5 | − | mA |
| | | High-speed on-chip oscillator mode (1) | XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division | − | 7.0 | 14.5 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | − | 3.0 | − | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0 | − | 85 | 390 | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | − | 15 | 320 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | − | 5 | 310 | μA |
| | | Stop mode | XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | − | 2.0 | 5.0 | μA |
| | | | XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | − | 55.0 | − | μA |

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                    5. Electrical Characteristics

### Timing requirements
### (Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = −40°C to 85°C (J ver)/−40°C to 125°C (K ver))

#### Table 5.26    External clock input (XOUT)

| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|---|---|---|---|---|
| t$_{C(XOUT)}$ | XOUT input cycle time | 50 | – | ns |
| t$_{WH(XOUT)}$ | XOUT input "H" width | 24 | – | ns |
| t$_{WL(XOUT)}$ | XOUT input "L" width | 24 | – | ns |
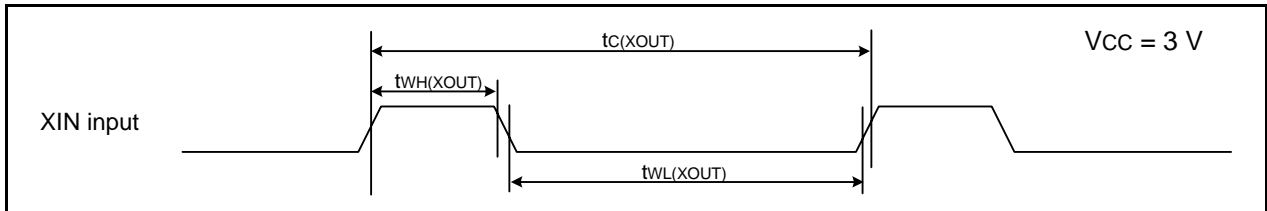


**Figure 5.12    External Clock Input Timing Diagram when VCC = 3 V**

#### Table 5.27    TRAIOi (i = 0 to 1) Input

| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|---|---|---|---|---|
| t$_{C(TRAIO)}$ | TRAIOi (i = 0 to 1) input cycle time | 300 | – | ns |
| t$_{WH(TRAIO)}$ | TRAIOi (i = 0 to 1) input "H" width | 120 | – | ns |
| t$_{WL(TRAIO)}$ | TRAIOi (i = 0 to 1) input "L" width | 120 | – | ns |
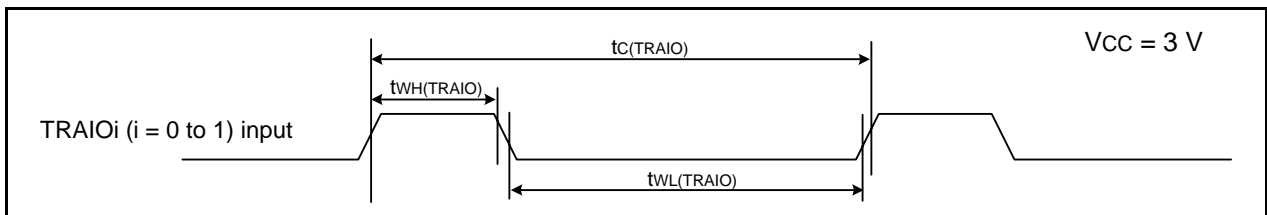


**Figure 5.13    TRAIOi (i = 0 to 1) Input Timing Diagram when Vcc = 3 V**

#### Table 5.28    TRFI Input

| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|---|---|---|---|---|
| t$_{C(TRFI)}$ | TRFI input cycle time | 400 [1] | – | ns |
| t$_{WH(TRFI)}$ | TRFI input "H" width | 200 [2] | – | ns |
| t$_{WL(TRFI)}$ | TRFI input "L" width | 200 [2] | – | ns |

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.
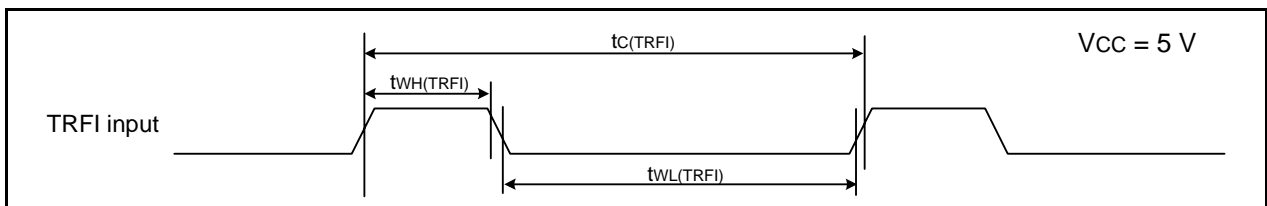


**Figure 5.14    TRFI Input Timing Diagram when Vcc = 5 V**

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                          5. Electrical Characteristics

**Table 5.29    Serial Interface**

| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|--------|-----------|------|------|------|
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{W(CKH)}$ | CLKi input "H" width | 150 | – | ns |
| $t_{W(CKL)}$ | CLKi Input "L" width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 140 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 to 2



**Figure 5.15    Serial Interface Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.30    External Interrupt INTi (i = 0 to 4) Input, Key Input Interrupt KIi (i = 0 to 3)**

| Symbol | Parameter | Standard Min. | Standard Max. | Unit |
|--------|-----------|------|------|------|
| $t_{W(INH)}$ | INTi input "H" width, KIi input "H" width | 380 [1] | – | ns |
| $t_{W(INL)}$ | INTi input "L" width, KIi input "L" width | 380 [2] | – | ns |

Notes:
1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



**Figure 5.16    Input Timing for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 3 V**

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Specifications in this document are tentative and subject to change.

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group                                    Package Dimensions

# Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Electronics website.

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP80-12x12-0.50 | PLQP0080KB-A | 80P6Q-A | 0.5g |



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section

Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 11.9 | 12.0 | 12.1 |
| E | 11.9 | 12.0 | 12.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 13.8 | 14.0 | 14.2 |
| $H_E$ | 13.8 | 14.0 | 14.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 10° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.3 | 0.5 | 0.7 |
| $L_1$ | — | 1.0 | — |

| Rev. | Date | Description | |
| --- | --- | --- | --- |
| | | Page | Summary |
| 0.10 | May 31, 2010 | — | First Edition issued |
| | | | |

# General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

# RENESAS

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