

### Features

- N-Channel enhancement mode device
- DMOS structure
- Lower capacitances for broadband operation
- Common source configuration
- Lower noise floor
- 100 MHz to 500 MHz operation

### ABSOLUTE MAXIMUM RATINGS AT 25°C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	$V_{DS}$	65	V
Gate-Source Voltage	$V_{GS}$	20	V
Drain-Source Current	$I_{DS}$	1.4*	A
Power Dissipation	$P_D$	26.9	W
Junction Temperature	$T_J$	200	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C
Thermal Resistance	$\theta_{JC}$	6.5	°C/W

### TYPICAL DEVICE IMPEDANCES

F (MHz)	$Z_{IN}$ ( $\Omega$ )	$Z_{LOAD}$ ( $\Omega$ )
100	30.0-j150.0	70.0+j110.0
300	15.0-j90.0	55.0+j80.0
500	4.2-j46.0	48.0+j50.0

$V_{DD}=28V, I_{DQ}=100\text{ Ma}, P_{OUT}=10.0\text{ W}$

$Z_{IN}$  is the series equivalent input impedance of the device from gate to gate.

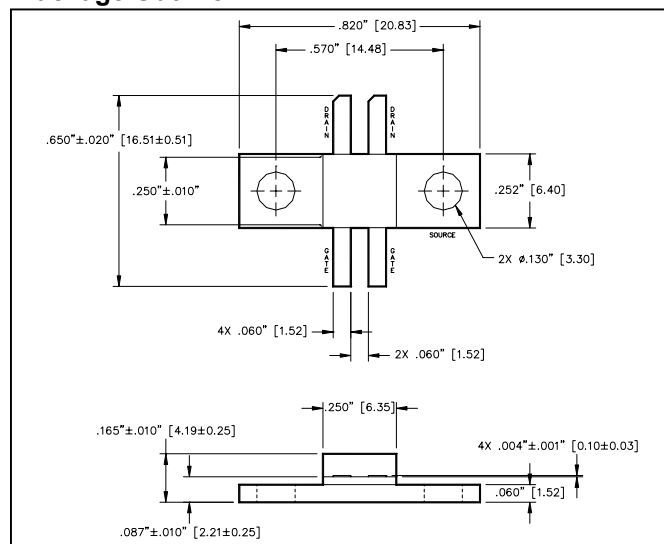
$Z_{LOAD}$  is the optimum series equivalent load impedance as measured from drain to drain.

### ELECTRICAL CHARACTERISTICS AT 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	$BV_{DSS}$	65	-	V	$V_{GS} = 0.0\text{ V}, I_{DS} = 2.0\text{ mA}$
Drain-Source Leakage Current	$I_{DSS}$	-	1.0	mA	$V_{GS} = 28.0\text{ V}, V_{DS} = 0.0\text{ V}$
Gate-Source Leakage Current	$I_{GSS}$	-	1.0	$\mu\text{A}$	$V_{GS} = 20.0\text{ V}, V_{DS} = 0.0\text{ V}$
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	$V_{DS} = 10.0\text{ V}, I_{DS} = 10.0\text{ mA}$
Forward Transconductance	$G_M$	80	-	S	$V_{DS} = 10.0\text{ V}, I_{DS} = 100.0\text{ mA}, \Delta V_{GS} = 1.0\text{V}, 80\ \mu\text{s Pulse}$
Input Capacitance	$C_{ISS}$	-	7	pF	$V_{DS} = 28.0\text{ V}, F = 1.0\text{ MHz}$
Output Capacitance	$C_{OSS}$	-	5	pF	$V_{DS} = 28.0\text{ V}, F = 1.0\text{ MHz}$
Reverse Capacitance	$C_{RSS}$	-	2.4	pF	$V_{DS} = 28.0\text{ V}, F = 1.0\text{ MHz}$
Power Gain	$G_P$	10	-	dB	$V_{DD} = 28.0\text{ V}, I_{DQ} = 100.0\text{ mA}, P_{OUT} = 50.0\text{ W } F = 500\text{ MHz}$
Drain Efficiency	$\eta_D$	50	-	%	$V_{DD} = 28.0\text{ V}, I_{DQ} = 100.0\text{ mA}, P_{OUT} = 50.0\text{ W } F = 500\text{ MHz}$
Load Mismatch Tolerance	VSWR-T	-	20:1	-	$V_{DD} = 28.0\text{ V}, I_{DQ} = 100.0\text{ mA}, P_{OUT} = 50.0\text{ W } F = 500\text{ MHz}$

\*Per side

### Package Outline



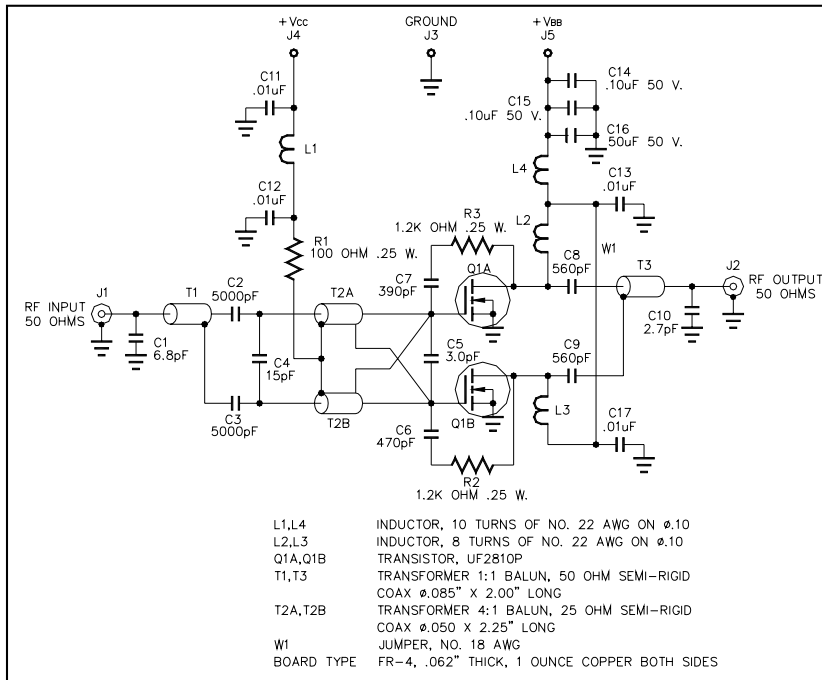
UNLESS OTHERWISE NOTED, TOLERANCES ARE INCHES  $\pm .005$ " [MILLIMETERS  $\pm 0.13\text{mm}$ ]

# UF2810P

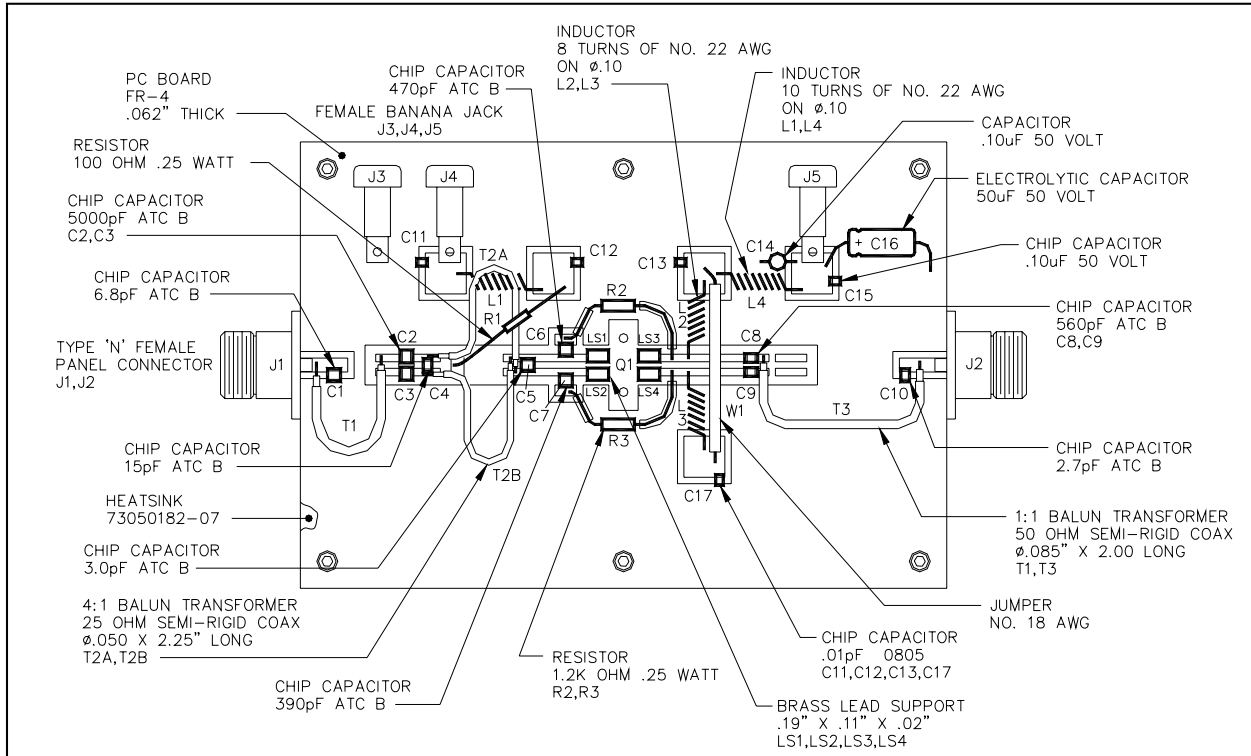
**RF Power MOSFET Transistor**  
**10W, 100-500 MHz, 28V**

**M/A-COM Products**  
**Released; RoHS Compliant**

## TEST FIXTURE SCHEMATIC



## TEST FIXTURE ASSEMBLY



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