

- Structure
- Product
- Model
- Functions

Semiconductor integrated circuit
DSC/DVC system power LSI

BD9639MWV

- (1) 6ch DC/DC converter
 - CH1 Boost FET embedded Start-up ch, Motor
 - CH2 Buck FET embedded Core
 - CH3 Buck-Boost FET embedded CMOS
 - CH4 Buck-Boost FET embedded Digital
 - CH5 Buck FET embedded CMOS, Memory
 - CH6 Boost FET embedded LED
- (2) Low voltage operation 2.5[V]
- (3) CH1 supply voltage output for internal circuit
- (4) CH1 PWM/PFM selectable
- (5) CH3,CH4 Boost-Buck auto switching
- (6) CH6 integrated Boost output shutdown (CH6 Load switch embedded)
- (7) Soft-start correspondence to each channel
- (8) Ground short protection (CH2~CH6)
- (9) Error amp phase compensation(CH1~CH6)
- (10) Operating frequency 1.5[MHz] (CH1~CH6)
- (11) Package of mounting on high heat radiation side (UQFN056V7070)

■ Absolute maximum ratings (Ta=25[°C])

ITEM	SYMBOL	Rating	Unit
Supply voltage	VBAT VBAT2·3·4·5·6	-0.3~7	V
SW6 permissible voltage	SW6	24.0	V
VOUT1 permissible current output	I _{VOUT1}	1.0	A
SW1 permissible current output	I _{SW1}	1.0	A
SW2 permissible current output	I _{SW2}	2.0	A
VOUT3 permissible current output	I _{VOUT3}	1.0	A
DSW3 permissible current output	I _{DSW3}	1.0	A
USW3 permissible current output	I _{USW3}	1.0	A
VOUT4 permissible current output	I _{VOUT4}	1.0	A
DSW4 permissible current output	I _{DSW4}	1.0	A
USW4 permissible current output	I _{USW4}	1.0	A
SW5 permissible current output	I _{SW5}	0.5	A
SW6 permissible current output	I _{SW6}	0.2	A
Power dissipation	Pd	4.83 (*1)	W
Operating temperature range	Topt	-20~+85	°C
Storage temperature range	Tstg	-55~+150	°C
Junction temperature	Tjmax	+150	°C

(*1) Implemented on Glass epoxy board (ROHM standard board: 74.2x74.2x1.6[mm³] 4 layers)

Power dissipation depends on the mounted wiring pattern.

■ Operating supply voltage

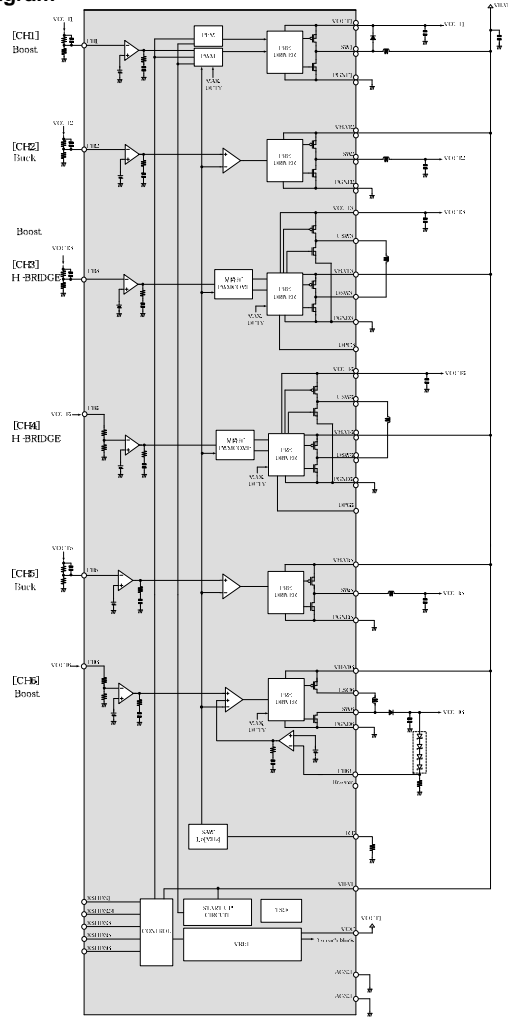
ITEM	Symbol	LIMIT			Unit
		MIN	TYP	MAX	
VBAT supply voltage	VBAT	2.5	3.7	5.5	V
	VBAT2	2.5	3.7	5.5	V
	VBAT3	2.5	3.7	5.5	V
	VBAT4	2.5	3.7	5.5	V
	VBAT5	2.5	3.7	5.5	V
	VBAT6	2.5	3.7	5.5	V

No radiation-proof design

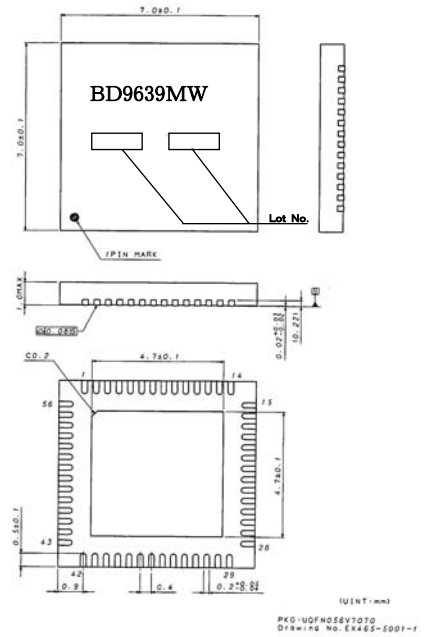
Electrical characteristics (Unless otherwise specified, VBAT=VBAT2,3,4,5,6=3.7[V], VCC=3.7[V], Ta=25[°C])

ITEM	Symbol	LIMIT			Unit	NOTE
		MIN	TYP	MAX		
Current consumption (PFM)	ICC1	-	72	150	μA	•XSHDN1=H, XSHDN24=L •FB1=0.5[V] •sum of VBAT terminal, and VOUT1 terminal
Current consumption (PWM)	ICC2	1.57	2.35	3.53	mA	•XSHDN1=H, XSHDN24=H, TEST1=H •FB1=0.5[V] •sum of VBAT terminal, and VOUT1 terminal
Shut current consumption	ICC3	-	0	10	μA	•all setting terminal=L •sum of VBAT terminal, and VOUT1 terminal
H input voltage 1	VIH1	VBAT -0.3	-	-	V	XSHDN1
L input voltage 1	VIL1	-	-	GND +0.3	V	
H input voltage 2	VIH3	2.5	-	-	V	XSHDN24,XSHDN3,XSHDN5,XSHDN6
L input voltage 2	VIL3	-	-	GND +0.3	V	
H Input current 1	IIH1	4.63	9.25	18.5	μA	Power supply 3.7[V] XSHDN24,XSHDN3,XSHDN5,XSHDN6
Oscillating frequency 1	FOSC1	1.2	1.5	1.8	MHz	RT=10[kΩ]
Reduced-voltage detection voltage	VUVLO1	1.75	1.95	2.15	V	
Reduced-voltage return voltage	VUVLO2	1.95	2.15	2.35	V	
[CH1]						
Start-up time 85%	TSS1	310	620	930	μs	Start-up period 100% 730[us](TYP) XSHDN24=L
Error amp reference voltage	EREF1	0.388	0.400	0.412	V	XSHDN24=H
PMOS On resistance	RONP1	-	0.24	0.38	Ω	Power supply 3.7[V]
NMOS On resistance	RONN1	-	0.14	0.23	Ω	Power supply 3.7[V]
Maximum duty	DMAX1	76.5	85.0	93.5	%	XSHDN24=H
[CH2]						
Error amp reference voltage	EREF2	0.390	0.400	0.410	V	
Soft-start period 85%	TSS2	0.43	0.85	1.27	ms	Start-up period 100% 1.0[ms](TYP)
PMOS On resistance	RONP2	-	0.13	0.21	Ω	Power supply 3.7[V]
NMOS On resistance	RONN2	-	0.08	0.14	Ω	Power supply 3.7[V]
[CH3]						
Error amp reference voltage	EREF3	0.390	0.400	0.410	V	
Soft-start period 85%	TSS3	0.85	1.70	2.55	ms	Start-up period 100% 2.0[ms](TYP)
PMOS On resistance DOWN side	RONPD3	-	0.24	0.39	Ω	Power supply 3.7[V]
NMOS On resistance DOWN side	RONND3	-	0.25	0.40	Ω	Power supply 3.7[V]
PMOS On resistance UP side	RONPU3	-	0.26	0.42	Ω	Power supply 3.7[V]
NMOS On resistance UP side	RONNU3	-	0.16	0.27	Ω	Power supply 3.7[V]
Maximum duty	DMAX3	65	80	95	%	
[CH4]						
Error amp reference voltage	EREF4	0.390	0.400	0.410	V	
Soft-start period 85%	TSS4	1.28	2.55	3.83	ms	Start-up period 100% 3.0[ms](TYP)
PMOS On resistance DOWN side	RONPD4	-	0.16	0.26	Ω	Power supply 3.7[V]
NMOS On resistance DOWN side	RONND4	-	0.21	0.33	Ω	Power supply 3.7[V]
PMOS On resistance UP side	RONPU4	-	0.24	0.38	Ω	Power supply 3.7[V]
NMOS On resistance UP side	RONNU4	-	0.16	0.26	Ω	Power supply 3.7[V]
Maximum duty	DMAX4	65	80	95	%	
[CH5]						
Error amp reference voltage	EREF5	0.390	0.400	0.410	V	
Soft-start period 85%	TSS5	0.85	1.70	2.55	ms	Start-up period 100% 2.0[ms](TYP)
PMOS On resistance	RONP5	-	0.26	0.42	Ω	Power supply 3.7[V]
NMOS On resistance	RONN5	-	0.17	0.28	Ω	Power supply 3.7[V]
[CH6]						
Error amp reference voltage 1	EREF6	0.380	0.400	0.420	V	Constant voltage control side
Error amp reference voltage 2	EREF6.1	0.380	0.400	0.420	V	Constant current control side
Soft-start period 85%	TSS6	2.55	5.10	7.65	ms	Start-up period 100% 6.0[ms](TYP)
Load switch On resistance	RONP6	-	0.23	0.37	Ω	Power supply 3.7[V]
NMOS On resistance	RONN6	-	0.47	0.73	Ω	Power supply 3.7[V]
Maximum duty	DMAX6	83	90	97	%	

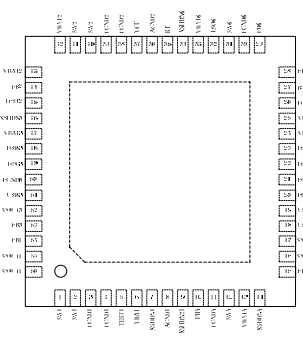
■ Block diagram



■ Package outline



■ Terminal No./Terminal name



■ Terminal description

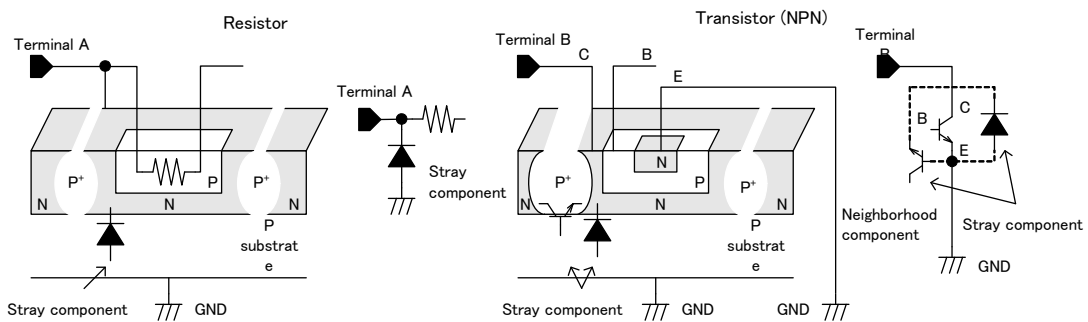
Terminal No.	Name	Equivalent circuit	
1	SW1	CH1 switching terminal	O
2	SW1	CH1 switching terminal	O
3	PGND1	CH1 DRIVER GND terminal	G
4	PGND1	CH1 DRIVER GND terminal	G
5	TEST1	Test terminal	O-G
6	VBAT	Battery input terminal	V
7	XSHDN1	CH1 shutdown terminal	G
8	AGND1	Analog GND terminal	G
9	XSHDN24	CH2-4 shutdown terminal	O-G
10	FB5	CH5 feed back terminal	G
11	PGND5	CH5 DRIVER GND terminal	G
12	SW5	CH5 switching terminal	O
13	VBAT5	CH5 DRIVER power supply terminal	V
14	XSHDN5	CH5 shutdown terminal	O-G
15	FB4	CH4 feed back terminal	G
16	VOUT4	CH4 output terminal	O
17	VOUT4	CH4 output terminal	O
18	USW4	CH4 Boost side switching terminal	O
19	USW4	CH4 Boost side switching terminal	O
20	PGND4	CH4 DRIVER GND terminal	G
21	PGND4	CH4 DRIVER GND terminal	G
22	DSW4	CH4 Buck side switching terminal	O
23	DSW4	CH4 Buck side switching terminal	O
24	VBAT4	CH4 DRIVER power supply terminal	V
25	VBAT4	CH4 DRIVER power supply terminal	V
26	DPG4	CH4 gate connecting terminal	O
27	Reserve	Reserve terminal	O-G
28	FB61	CH6 feed back terminal (Constant current side)	G

Terminal No	Name	Equivalent circuit	
29	FB6	CH6 feed back terminal (Constant current side)	G
30	PGND6	CH6 DRIVER GND terminal	G
31	SW6	CH6 switching terminal	O
32	LSO6	CH6 Load switch output terminal	O
33	VBAT6	CH6 Load switch input terminal	V
34	XSHDN6	CH6 shutdown terminal	O-G
35	RT	Triangle wave setting resistor terminal (*1)	
36	AGND2	Analog GND terminal	G
37	VCC	Analog power supply terminal	V
38	PGND2	CH2 DRIVER GND terminal	G
39	PGND2	CH2 DRIVER GND terminal	G
40	SW2	CH2 switching terminal	O
41	SW2	CH2 switching terminal	O
42	VBAT2	CH2 DRIVER power supply terminal	V
43	VBAT2	CH2 DRIVER power supply terminal	V
44	FB2	CH2 feed back terminal	G
45	TEST2	Test terminal	O-G
46	XSHDN3	CH3 shutdown terminal	O-G
47	VBAT3	CH3 DRIVER power supply terminal	V
48	DSW3	CH3 Buck side switching terminal	O
49	DPG3	CH3 gate connecting terminal	O
50	PGND3	CH3 DRIVER GND terminal	G
51	USW3	CH3 Boost side switching terminal	O
52	VOUT3	CH3 output terminal	O
53	FB3	CH3 feed back terminal	G
54	FB1	CH1 feed back terminal	G
55	VOUT1	CH1 output terminal	O
56	VOUT1	CH1 output terminal	O

The alphabet on a right edge of the above-mentioned terminal explanation is processing of unused.
 O...OPEN G...GND O-G...OPEN or GND V...Power supply (VBAT)
 (*1)...10[KΩ] Pull-down

■Instruction for use

1. Board patterning
 - VBAT,VBAT2,VBAT3,VBAT4,VBAT5,VBAT6 are must be connected to power supply on the board.
 - VCC must be connected to VOUT1 output on the board.
 - ALL PGND and AGND must be connected to GND on the board.
 - ALL power supply line and GND terminals must be wired with wide/short pattern in order to achieve substantially low impedance.
2. Peripheral circuitry
 - Use low ESR ceramic capacitor for bypass condenser between power supply and GND terminal and place capacitor right next to the IC pins.
 - Place external components such as L and C by IC with wide/short pattern.
 - Draw output voltage from each end of capacitor.
 - Causing short circuit at CH1 output will overload the external diode and may breakdown the component.
 - Prepare physical countermeasures by adding poli-switches and fuses to avoid excess current flow.
3. Start-up
 - Keep light load condition by starting up the device.
 - Make it to PWM mode (XSHDN2=L→H) after CH1 is started up in PFM mode (XSHDN1=L→H), and the VOUT1 output voltage stands up.
 - Moreover, start it about the start of CH3·CH5·CH6 since the PWM mode (Contain it simultaneously).
4. Absolute maximum ratings
 - The quality control of the product has exercised adequate care, however operating above the absolute maximum ratings of supply voltage and/or operational temperature range may cause decay and destroy the IC. If specific mode such that exceeding the Absolute Maximum ratings is expected, please have physical countermeasure such as adding fuses and poli-switches etc.
5. Thermal design
 - Take consideration of power dissipation at actual device usage to ensure the satisfactory thermal design margin. (Refer page 6)
6. Terminal to Terminal short / mis-mounting
 - While mounting IC on the board, check direction and shift of the IC. If inadequately mounted, IC might be breakdown. Additionally short circuit from unwanted contamination at power supply and GND and/or between any terminals also may cause the defect.
7. Operating in strong electromagnetic field
 - Please pay attention using device in the strong electromagnetic field. Device may cause malfunction.
8. Thermal shut down.(TSD)
 - Main purpose of TSD is to shutting IC down from runaway effect. It is not to compensate or to protect IC itself . Therefore, please do not continuously operate the IC after TSD circuit is activated and/or premise operations such that TSD circuit function to be used.
9. Inspection with set board
 - While connecting capacitor to Low impedance pins, please discharge capacitor by one process by another to prevent stressing the IC. While mounting and removing the IC to/from the Board in the inspection process, be sure to turn off the power supply by each action. Moreover equip ground earth in assembling process for ESD protection and handle with care during the test and/or transportation.
10. Input terminals
 - This IC is a monolithic IC, and has P⁺ isolation and P substrate for the element separation. Therefore, a parasitic PN junction is formed in this P-layer and N-layer of each element. For example shown in below picture, the resistor or the transistor is connected to the terminal. When the GND voltage potential is greater than the voltage potential at Terminals A or B, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by applying lower voltage than GND (P substrate) to input terminals. Moreover, please apply each input terminal with lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage being applied



simplified IC structure

11. Usage of this product
 - This IC is designed to be used in DSC/DVD application.
 - Upon using our product to equipments or devices other than above mentioned application, please be sure to consult with our sales representative in advance.

Notes

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