PAS6167 CMOS QCIF+ DIGITAL IMAGE SENSOR

General Description

The PAS6167 is a highly integrated CMOS active-pixel image sensor that has output of 176 x 220 pixels. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. PAS6167 outputs YUV/YCrCb 4:2:2 or RGB 565/555/444 data through the parallel/serial data bus. It is available in CSP-20pin package.

The PAS6167 can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **Active Pixels: 188 x 236 pixels**
- **Resolution: 176 x 220 pixels, 1/13" Lens**
- **Bayer-RGB color filter array**
- **Output format (parallel/serial):**
  - **YUV/YCrCb 4:2:2 (QCIF+, and other sizes …)**
  - **RGB 565/555/444 (QCIF+, and other sizes …)**
- **On-chip 11-bit pipelined A/D converter**
- **On-chip 2-stage background compensation DAC**
- **On-chip manual analog gain control**
- **Continuous variable frame time & exposure time**
- **I2C™ Interface**
- **Support 1.8V~3.3V I/O power**
- **low power-down dissipation**
- **Automatic Background Compensation**
- **DSP function:**
  - **AEC & AGC**
  - **AWB**
  - **Gamma**
  - **Color matrix**
  - **Sharpness**
  - **De-noise**
  - **Color saturation**
  - **Defect compensation**
  - **Lens shading compensation**
- **WOI & Sub-sampling**
- **PLL**
- **Module size : 5.0 * 5.0 * 3.0 mm**

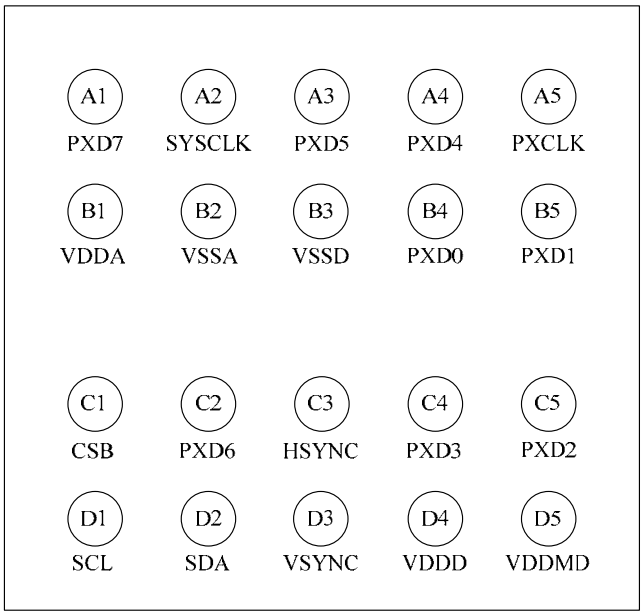
Key Specification

Active Pixel		188(H) x 236(V)
Resolution		176 (H) x 220 (V)
Power	**Analog**	2.5V ~ 2.8V
	I/O	1.8V ~ 3.3V
	Core	1.8V
Pixel Size		4.5µm x 4.5µm, 1/13" Lens
Lens Chief Ray Angle		< 22degree
Max. Frame rate		30 fps, QCIF+ YUV mode
Max. System clock rate		52 MHz
Max. SPI clock rate		26 MHz, QCIF+ YUV mode
Sensitivity		3.9V/Lux-sec
Color filter		RGB Bayer Pattern
Exposure Time		~ Frame time to Line time
Scan Mode		Progressive
S/N Ratio		39dB
Dynamic range		60dB
Package		CSP-20pin (PAS6167LT)

PixArt Imaging Inc.
E-mail: fae_service@pixart.com.tw

1. Pin Assignment

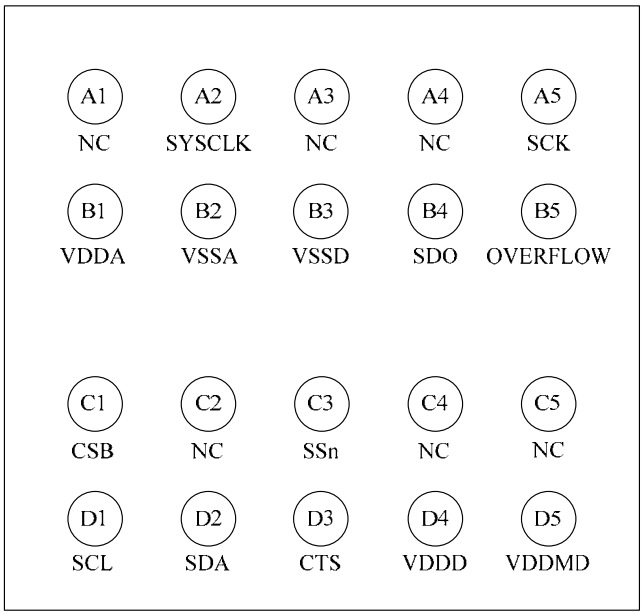
Parallel mode



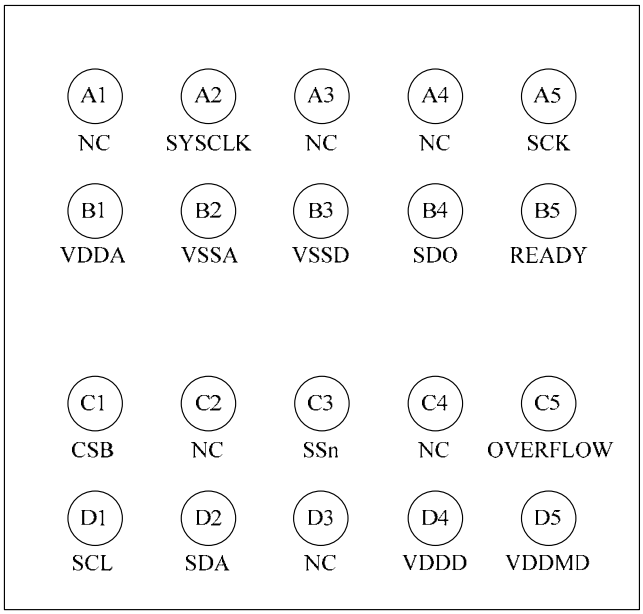
PAS6167LT
(parallel mode)
-- Top View --

Pin No.	Name	Type	Description
A1	PXD7	OUT	Digital pixel data [7], MSB
A2	SYSCLK	IN	External clock input
A3	PXD5	OUT	Digital pixel data [5]
A4	PXD4	OUT	Digital pixel data [4]
A5	PXCLK	OUT	Pixel clock output
B1	VDDA	PWR	Analog power, 2.5V ~ 2.8V
B2	VSSA	GND	Analog ground
B3	VSSD	GND	Digital ground
B4	PXD0	OUT	Digital pixel data [0], LSB
B5	PXD1	OUT	Digital pixel data [1]
C1	CSB	IN	Power down enable, active high
C2	PXD6	OUT	Digital pixel data [6]
C3	HSYNC	OUT	Horizontal synchronization signal output
C4	PXD3	OUT	Digital pixel data [3]
C5	PXD2	OUT	Digital pixel data [2]
D1	SCL	IN	I2C clock input
D2	SDA	I/O	I2C data
D3	VSYNC	OUT	Vertical synchronization signal output
D4	VDDD	PWR	Digital core power, 1.8V
D5	VDDMD	PWR	I/O power, 1.8V ~ 3.3V

Serial mode



PAS6167LT
(SPI master mode)
-- Top View --



PAS6167LT
(SPI slave mode)
-- Top View --

Pin No.	Name	Type	Description
A1	NC	--	--
A2	SYSCLK	IN	External clock input
A3	NC	--	--
A4	NC	--	--
A5	SCK	OUT	SPI clock output (SPI master mode)
		IN	SPI clock input (SPI slave mode)
B1	VDDA	PWR	Analog power, 2.5V ~ 2.8V
B2	VSSA	GND	Analog ground
B3	VSSD	GND	Digital ground
B4	SDO	OUT	SPI data output
B5	OVERFLOW	OUT	FIFO overflow (SPI master mode)
	READY	OUT	Data ready (SPI slave mode)
C1	CSB	IN	Power down enable, active high
C2	NC	--	--
C3	SSn	OUT	SPI frame sync (SPI master mode)
		IN	SPI select (SPI slave mode)
C4	NC	--	--
C5	NC	--	--
	OVERFLOW	OUT	FIFO overflow (SPI slave mode)
D1	SCL	IN	I2C clock input
D2	SDA	I/O	I2C data
D3	CTS	IN	Pause output data (SPI master mode)
	NC	--	--
D4	VDDD	PWR	Digital core power, 1.8V
D5	VDDMD	PWR	I/O power, 1.8V ~ 3.3V

2. Specifications

Absolute Maximum Ratings

Ambient Storage Temperature		-40℃~60℃
Supply Voltage (with respect to ground)	V_{DDD}	3.0V
	V_{DDA}	4.5V
	V_{DDMD}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to VDDMD+0.5V
Lead-free temperature, Surface-mount process		245℃
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDA}	DC supply voltage – Analog	2.45		2.8	V
V_{DDD}	DC supply voltage – Digital core	1.62	1.8	1.98	V
V_{DDMD}	DC supply voltage – I/O	1.62		3.3	V
I_{DD}	Operating Current (see Note[a])		15.8		mA
I_{PWDN}	Power Down Current (see Note[b])		10		μA
Type : IN & I/O Reset and System Clock(input clock)					
V_{IH}	Input Voltage HIGH	VDDMD * 0.7			V
V_{IL}	Input Voltage LOW			VDDMD * 0.3	V
Type : OUT & I/O for PX0 : 9, SDA, H/VSYNC and PXCLK(output clock)					
V_{OH}	Output Voltage HIGH	VDDMD * 0.9			V
V_{OL}	Output Voltage LOW			VDDMD * 0.1	V

Note[a]: VDDA=2.8V, VDDD=1.8V, VDDMD=3.3V, 30fps / QCIF+ / YUV output, without I/O loading

Note[b]: VDDA=2.8V, VDDMD=2.8V

AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency		13		MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%

Sensor Characteristics

Parameter	Typ.	Unit
Sensitivity	3.9	V/Lux-sec
Signal to Noise Ratio	39	dB
Dynamic Range	60	dB

3. I2C™ Bus

PAS6167 supports I2C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1000000" and supports receiving / transmitting speed as maximum 400KHz.

I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 2.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 2.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

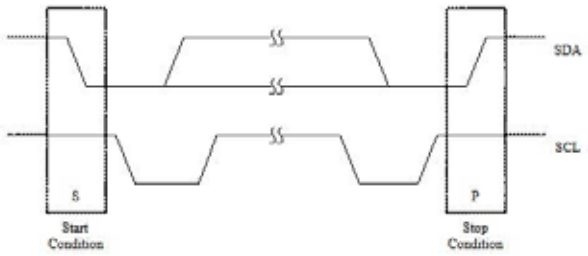


Figure 2.1 Start and Stop conditions

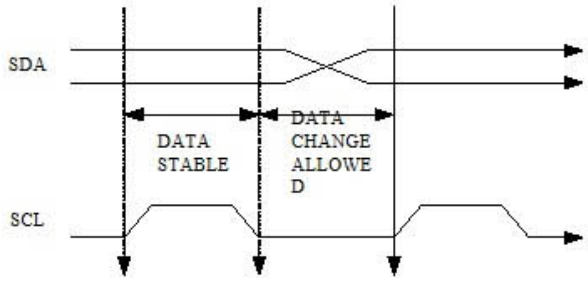
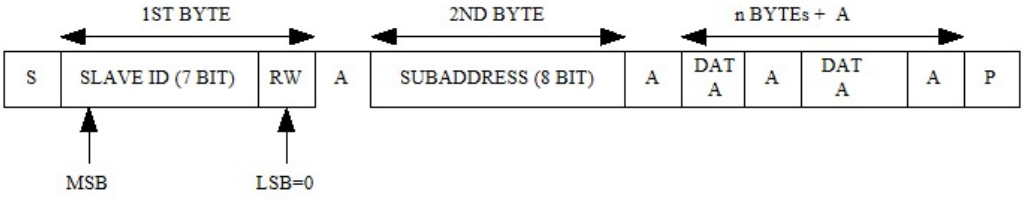


Figure 2.2 Valid Data

Data Transfer Format

Master transmits data to salve (write cycle)

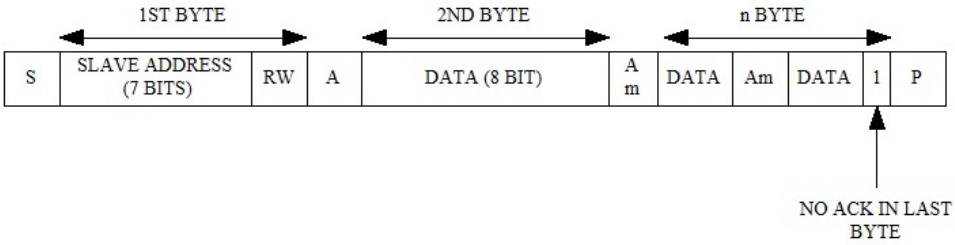
- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAS6167 internal control registers. (Please refer to PAS6167 register description)



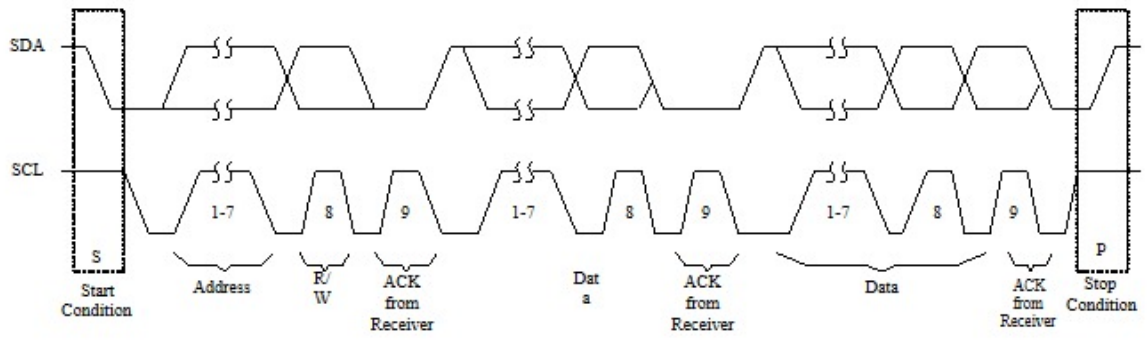
During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAS6167) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the PAS6167 acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS6167 control register (address was assigned by 2nd byte). After PAS6167 issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS6167 sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS6167 can be programming via this way.

Slave transmits data to master (read cycle)

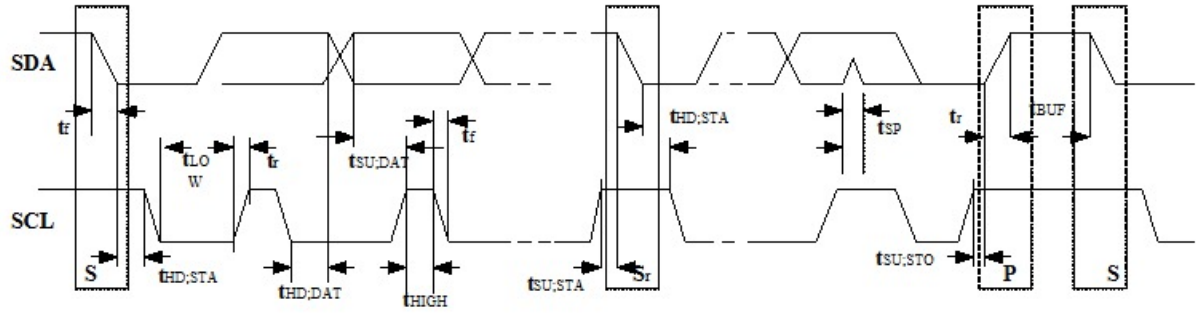
- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.



During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS6167. The 8 bits data was read from PAS6167 internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS6167 place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS6167) must releases SDA line to master to generate STOP condition.



I2C™ Bus Timing



I2C™ Bus Timing Specification

Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	µs
High period of the SCL clock.	t_{HIGH}	0.75	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	µs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	µs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

4. Registers

Register Table

Bank0 (set address_0xEF=0)

Address (Hex)		Register name	Default	Description
4	[4:0]	AE_stage_indoor[4:0]	0x0b	Min. AE stage clamp in door
6	[0]	in_door	0x00	AE In door enable
F	[7:0]	AWB_Window_X[7:0]	0xa0	AWB window width
11	[7:0]	AWB_Window_Y[7:0]	0xc0	AWB window height
13	[7:0]	lpf_min[7:0]	0xf6	Lpf minimum value for AE
14	[2:0]	lpf_min[10:8]	0x00	Lpf minimum value for AE
	[7:4]	ny_min[3:0]	0x09	Ny minimum value for AE
15	[7:0]	AE_Window_X[7:0]	0xa0	AE window width
17	[7:0]	AE_Window_Y[7:0]	0xc0	AE window height
35	[0]	AC_freq	0x01	AC frequency (1: 60Hz, 0: 50Hz)
56	[7:0]	AG_stage_UB	0x3f	AG_stage upper bound at max. AE_stage
58	[7:0]	ISP_Y0	0x04	ISP Gamma Y0, (ISP_UpdateFlag=1, update)
59	[7:0]	ISP_Y1	0x08	ISP Gamma Y1, (ISP_UpdateFlag=1, update)
5A	[7:0]	ISP_Y2	0x10	ISP Gamma Y2, (ISP_UpdateFlag=1, update)
5B	[7:0]	ISP_Y3	0x20	ISP Gamma Y3, (ISP_UpdateFlag=1, update)
5C	[7:0]	ISP_Y4	0x32	ISP Gamma Y4, (ISP_UpdateFlag=1, update)
5D	[7:0]	ISP_Y5	0x44	ISP Gamma Y5, (ISP_UpdateFlag=1, update)
5E	[7:0]	ISP_Y6	0x71	ISP Gamma Y6, (ISP_UpdateFlag=1, update)
5F	[7:0]	ISP_Y7	0x90	ISP Gamma Y7, (ISP_UpdateFlag=1, update)
60	[7:0]	ISP_Y8	0xae	ISP Gamma Y8, (ISP_UpdateFlag=1, update)
61	[7:0]	ISP_Y9	0xca	ISP Gamma Y9, (ISP_UpdateFlag=1, update)
62	[0]	ISP_Gamma_EnH	0x01	ISP gamma correction enable, (ISP_UpdateFlag=1, update)
66	[0]	freq_60	0x01	Set de-flicker frequency 0/1: 50/60Hz
	[4]	AE_EnH	0x00	AE enable
67	[7:0]	SysClk_freq[7:0]	0x97	R_SysClk_freq_Div8 = 0 : Input_frequency/2048 R_SysClk_freq_Div8 = 1 : Input_frequency/256
68	[6:0]	SysClk_freq[13:8]	0x31	R_SysClk_freq_Div8 = 0 : Input_frequency/2048 R_SysClk_freq_Div8 = 1 : Input_frequency/256
	[7]	SysClk_freq_Div8	0x01	R_SysClk_freq_Div8
6B	[4:0]	AE_minStage[4:0]	0x05	Minimum AE stage
6C	[4:0]	AE_maxStage[4:0]	0x1a	Maximum AE stage (AE_maxStage<=28)
6F	[7:0]	Ytar8bit	0x64	0~255, Target luminance of AE
72	[0]	AWB_EnH	0x00	Auto-white balance enable
	[4]	AWB_Gain_rst	0x00	AWB gain gain reset
73	[7:0]	Ylow	0x70	Low bond of “light-pixel” in AWB
74	[7:0]	Yhigh	0xf0	High bond of “light-pixel” in AWB
8F	[7:0]	ImgEffect_c0	0x40	Image Effect parameter 0, (ISP_UpdateFlag=1, update)
90	[7:0]	ImgEffect_c1	0x40	Image Effect parameter 1, (ISP_UpdateFlag=1, update)
91	[7:0]	ImgEffect_c2	0x10	Image Effect parameter 2, (ISP_UpdateFlag=1, update)

92	[7:0]	ImgEffect_c3	0x80	Image Effect parameter 3, (ISP_UpdateFlag=1, update)
93	[3:0]	ImgEffectMode	0x00	Image Effect mode 1: monochrome; 2: negative 3: Sepia; 4: Emboss; 5: Sketch 6: Black Board; 7: White Board 8: Solarize; 9: Color range R 10: Color range G; 11: Color range B; 12: Contrast (ISP_UpdateFlag=1, update)
	[5:4]	ImgEffectFilter	0x00	Image Effect emboss filter type, (ISP_UpdateFlag=1, update)
94	[0]	ISP_ImgEffect_En	0x00	(ISP_UpdateFlag=1, update)
97	[4]	Shading_EnH	0x00	Lens shading enable
	[5]	Shading_On	0x00	Shading on/off status (read only)
99	[6:0]	BYcoef_D	0x1f	Lens Shading Y coefficient of color B (down)
9A	[6:0]	BXcoef_R	0x1f	Lens Shading X coefficient of color B (right)
9B	[6:0]	BYcoef_U	0x1f	Lens Shading Y coefficient of color B (up)
9C	[6:0]	BXcoef_L	0x1f	Lens Shading X coefficient of color B (left)
9D	[6:0]	GbYcoef_D	0x1f	Lens Shading Y coefficient of color Gb (down)
9E	[6:0]	GbXcoef_R	0x1f	Lens Shading X coefficient of color Gb (right)
9F	[6:0]	GbYcoef_U	0x1f	Lens Shading Y coefficient of color Gb (up)
A0	[6:0]	GbXcoef_L	0x1f	Lens Shading X coefficient of color Gb (left)
A1	[6:0]	GrYcoef_D	0x1f	Lens Shading Y coefficient of color Gr (down)
A2	[6:0]	GrXcoef_R	0x1f	Lens Shading X coefficient of color Gr (right)
A3	[6:0]	GrYcoef_U	0x1f	Lens Shading Y coefficient of color Gr (up)
A4	[6:0]	GrXcoef_L	0x1f	Lens Shading X coefficient of color Gr (left)
A5	[6:0]	RYcoef_D	0x1f	Lens Shading Y coefficient of color R (down)
A6	[6:0]	RXcoef_R	0x1f	Lens Shading X coefficient of color R (right)
A7	[6:0]	RYcoef_U	0x1f	Lens Shading Y coefficient of color R (up)
A8	[6:0]	RXcoef_L	0x1f	Lens Shading X coefficient of color R (left)
A9	[7:0]	brightestX[7:0]	0x40	Lens Shading brightest X
AA	[1:0]	brightestX[9:8]	0x01	Lens Shading brightest X
AB	[7:0]	brightestY[7:0]	0xf0	Lens Shading brightest Y
AC	[1:0]	brightestY[9:8]	0x00	Lens Shading brightest Y
AD	[2:0]	LensShfBit[2:0]	0x00	Lens shading coefficient right shift bit
E2	[6:4]	DigFilter_mode_NL[2:0]	0x00	0 : DigFilter off @ NL, 1 : DigFilter level-1 @ NL, 2 : DigFilter level-2 @ NL,
	[2:0]	DigFilter_mode_LL[2:0]	0x00	0 : DigFilter off @ LL, 1 : DigFilter level-1 @ LL, 2 : DigFilter level-2 @ LL,
E3	[4:0]	DigFilterAE_stageLL[4:0]	0x00	Digital Filter @Low Light
E4	[4:0]	DigFilterAE_stageNL[4:0]	0x00	Digital Filter @Normal Light
ED	[0]	ISP_Update		ISP_UpdateFlag
	[4]	ISP_FrameSkip		(ISP_UpdateFlag=1, update)

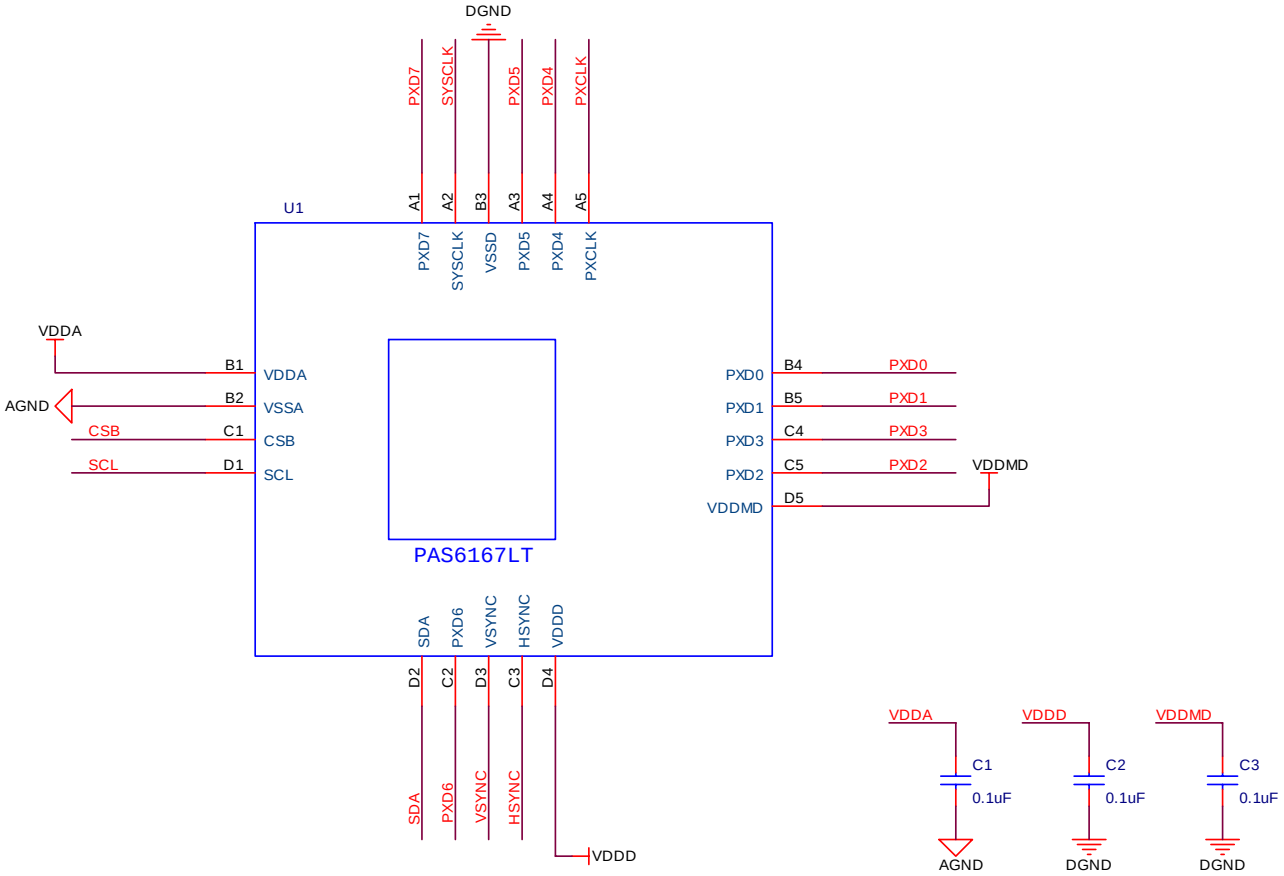
Bank2 (set address_0xEF=2)

Address (Hex)		Register name	Default	Description
0	[0]	ISP2_Update	0x00	ISP2_UpdateFlag
4	[7:0]	R_ImgEffect_R_Gain[7:0]	0x00	ImageEffect R Gain (ISP2_UpdateFlag=1, update)
5	[7:0]	R_ImgEffect_G_Gain[7:0]	0x00	ImageEffect G Gain (ISP2_UpdateFlag=1, update)
6	[7:0]	R_ImgEffect_B_Gain[7:0]	0x00	ImageEffect B Gain (ISP2_UpdateFlag=1, update)
7	[7:0]	R_ImgEffect_R_offset[7:0]	0x00	ImageEffect R Offset (ISP2_UpdateFlag=1, update)
8	[7:0]	R_ImgEffect_G_offset[7:0]	0x00	ImageEffect G Offset (ISP2_UpdateFlag=1, update)
9	[7:0]	R_ImgEffect_B_offset[7:0]	0x00	ImageEffect B Offset (ISP2_UpdateFlag=1, update)
A	[0]	R_ISP_ImgEffect_1_En	0x00	Enable ImageEffect Gain, Offset (ISP2_UpdateFlag=1, update)
17	[0]	R_Curve_EnH	0x01	ISP tone curve Enable
18	[7:0]	R_Curve_Y0[7:0]	0x1a	ISP tone curve Y0
19	[7:0]	R_Curve_Y1[7:0]	0x34	ISP tone curve Y1
1A	[7:0]	R_Curve_Y2[7:0]	0x49	ISP tone curve Y2
1B	[7:0]	R_Curve_Y3[7:0]	0x5b	ISP tone curve Y3
1C	[7:0]	R_Curve_Y4[7:0]	0x6d	ISP tone curve Y4
1D	[7:0]	R_Curve_Y5[7:0]	0x7d	ISP tone curve Y5
1E	[7:0]	R_Curve_Y6[7:0]	0x9a	ISP tone curve Y6
1F	[7:0]	R_Curve_Y7[7:0]	0xb6	ISP tone curve Y7
20	[7:0]	R_Curve_Y8[7:0]	0xcf	ISP tone curve Y8
21	[7:0]	R_Curve_Y9[7:0]	0xe8	ISP tone curve Y9
22	[3]	R_Defect_EnH	0x00	Defect Enable
28	[5:0]	R_Defect_NL_th[5:0]	0x0a	Defect test threshold @ Normal Light
29	[5:0]	R_Defect_LL_th[5:0]	0x05	Defect test threshold @ Low Light
2A	[3:0]	R_FlatRatio[3:0]	0x08	ISP flat ratio
	[6]	R_Flat_En	0x00	ISP flat enable
	[7]	R_ISP_Edge_En0	0x01	ISP edge enhancement enable
2C	[7:0]	R_Edge_UB[7:0]	0x32	ISP edge enhancement value upper bound
2D	[7:0]	R_Edge_LB[7:0]	0x14	ISP edge enhancement value lower bound
2F	[4:0]	R_AE_stage_LL[4:0]	0x1b	AE_stage > R_AE_stage_LL =>Low Light
30	[4:0]	R_AE_stage_NL[4:0]	0x14	AE_stage < R_AE_stage_NL =>Normal Light
38	[4:0]	R_AE_Middle_Stage[4:0]	0x0e	Apply Middle Gain when AE_stage >= R_AE_Middle_Stage
	[7]	R_AE_Middle_Gain_En	0x01	AE Middle Gain Enable
39	[4:0]	R_AE_Middle_Gain[4:0]	0x09	AE Middle Gain value
3D	[0]	R_CCMb_En	0x01	CCM Enable
3E	[2:0]	R_CCMb0_0[10:8]	0x80	CCM matrix coefficient
3F	[7:0]	R_CCMb0_0[7:0]	0xb5	CCM matrix coefficient
40	[2:0]	R_CCMb0_1[10:8]	0x07	CCM matrix coefficient
41	[7:0]	R_CCMb0_1[7:0]	0xcb	CCM matrix coefficient
42	[2:0]	R_CCMb0_2[10:8]	0x00	CCM matrix coefficient
43	[7:0]	R_CCMb0_2[7:0]	0x00	CCM matrix coefficient
44	[2:0]	R_CCMb1_0[10:8]	0x07	CCM matrix coefficient
45	[7:0]	R_CCMb1_0[7:0]	0xc8	CCM matrix coefficient
46	[2:0]	R_CCMb1_1[10:8]	0x00	CCM matrix coefficient
47	[7:0]	R_CCMb1_1[7:0]	0xea	CCM matrix coefficient
48	[2:0]	R_CCMb1_2[10:8]	0x07	CCM matrix coefficient

49	[7:0]	R_CCMb1_2[7:0]	0xcf	CCM matrix coefficient
4A	[2:0]	R_CCMb2_0[10:8]	0x07	CCM matrix coefficient
4B	[7:0]	R_CCMb2_0[7:0]	0xf7	CCM matrix coefficient
4C	[2:0]	R_CCMb2_1[10:8]	0x07	CCM matrix coefficient
4D	[7:0]	R_CCMb2_1[7:0]	0x7e	CCM matrix coefficient
4E	[2:0]	R_CCMb2_2[10:8]	0x01	CCM matrix coefficient
4F	[7:0]	R_CCMb2_2[7:0]	0x0b	CCM matrix coefficient
58	[4:0]	R_EdgeRatio_NL[4:0]	0x05	Edge ratio @Normal Light
C0	[0]	R_UV_Swap	0x00	U V Swap
	[1]	R_YC_Swap	0x01	Y C Swap
	[3:2]	R_RGB565_mode[1:0]	0x00	RGB565_mode
	[4]	R_RGB565_En	0x00	RGB565 Enable (ISP2_UpdateFlag=1, update)
	[5]	R_RGB555_En	0x00	RGB555 Enable (ISP2_UpdateFlag=1, update)
	[6]	R_RGB444_En	0x00	RGB444 Enable (ISP2_UpdateFlag=1, update)
C3	[5:0]	R_SPI_SysClk_Div[5:0]	0x01	SPI SCK freq div
C4	[0]	R_SPI_En	0x00	SPI Master Mode Enable
	[1]	R_SPI_SSn_VsyncTim	0x00	SPI SSn vsync timing (Master mode)
	[2]	R_SPI_Slave_En	0x00	SPI Slave Mode Enable
	[3]	R_SPI_CTS_En	0x00	SPI CTS Enable (Master mode)

5. Reference Circuit Schematic

Parallel mode



Note:

Sensor pwdn pin, "CSB", high active
(connect to DGND if un-used)

VDDA, analog power, 2.5V ~ 2.8V

VDDMD, I/O power, 1.8V ~ 3.3V

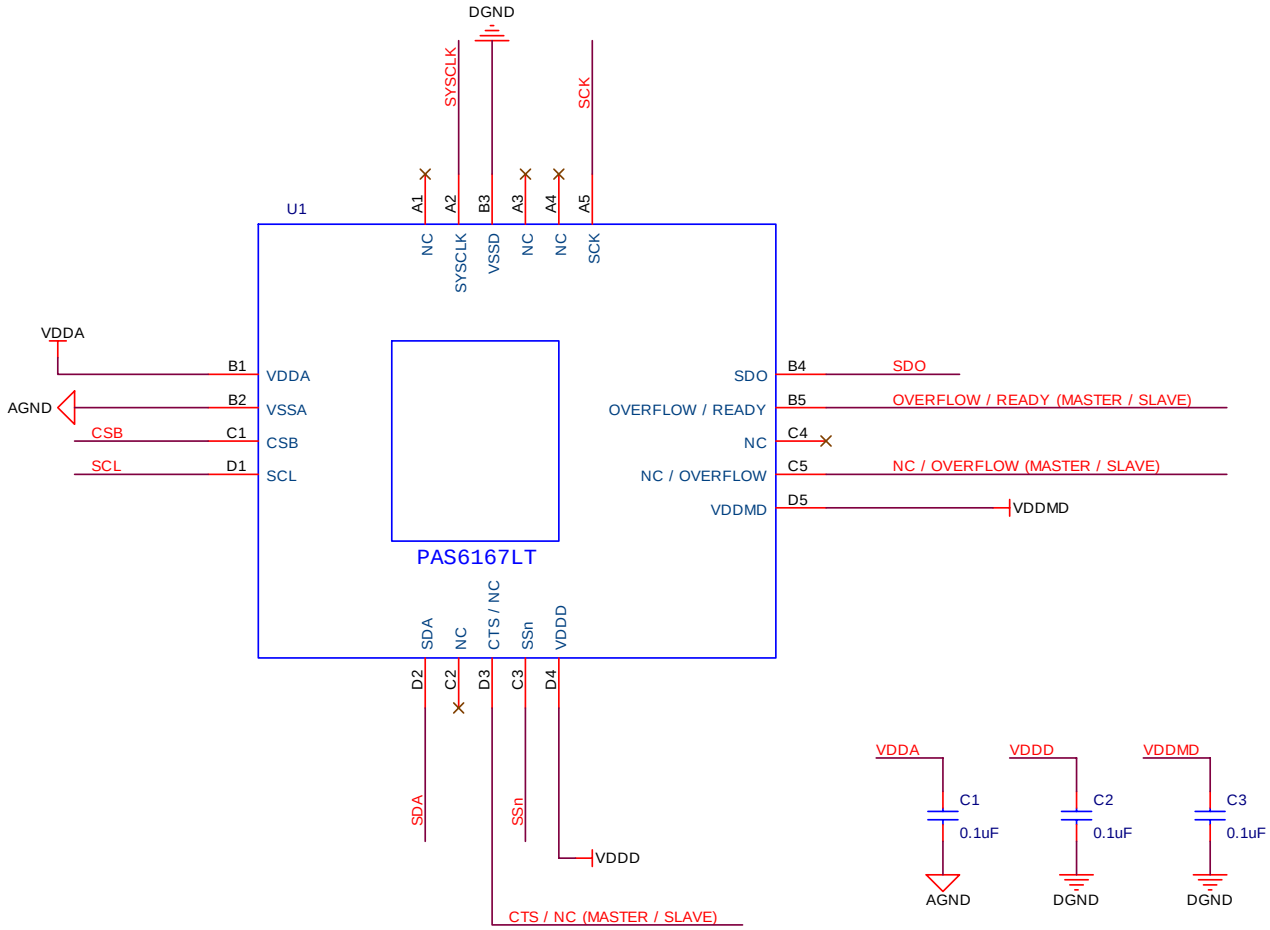
VDDD, digital core power, 1.8V

DGND, digital ground

AGND, analog ground

All capacitors must be close to the sensor as possible

Serial mode



Note:

Sensor pwdn pin, "CSB", high active
(connect to DGND if un-used)

VDDA, analog power, 2.5V ~ 2.8V

VDDMD, I/O power, 1.8V ~ 3.3V

VDDD, digital core power, 1.8V

DGND, digital ground

AGND, analog ground

All capacitors must be close to the sensor as possible

6. Package Information

	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	2985	2960	3010
Package Body Dimension Y	B	2837	2812	2862
Package Height	C	850	790	910
Ball Height	C1	130	100	160
Package Body Thickness	C2	720	675	765
Thickness of Glass surface to wafer	C3	545	525	565
Ball Diameter	D	250	220	280
Total Pin Count	N	20		
Pin Count X axis	N1	5		
Pin Count Y axis	N2	4		
Pins Pitch X axis	J1	500		
Pins Pitch Y axis	J2	500/850		
Edge to Pin Center Distance along	S1	493	463	523
Edge to Pin Center Distance along	S2	493	463	523

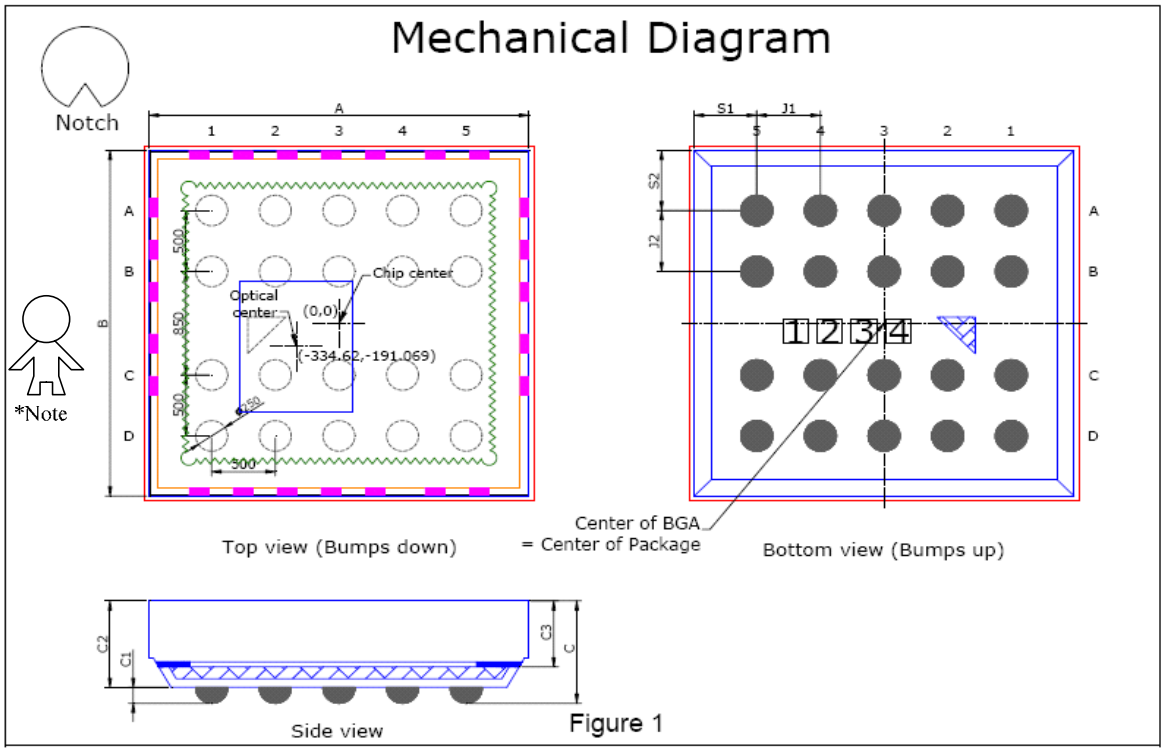
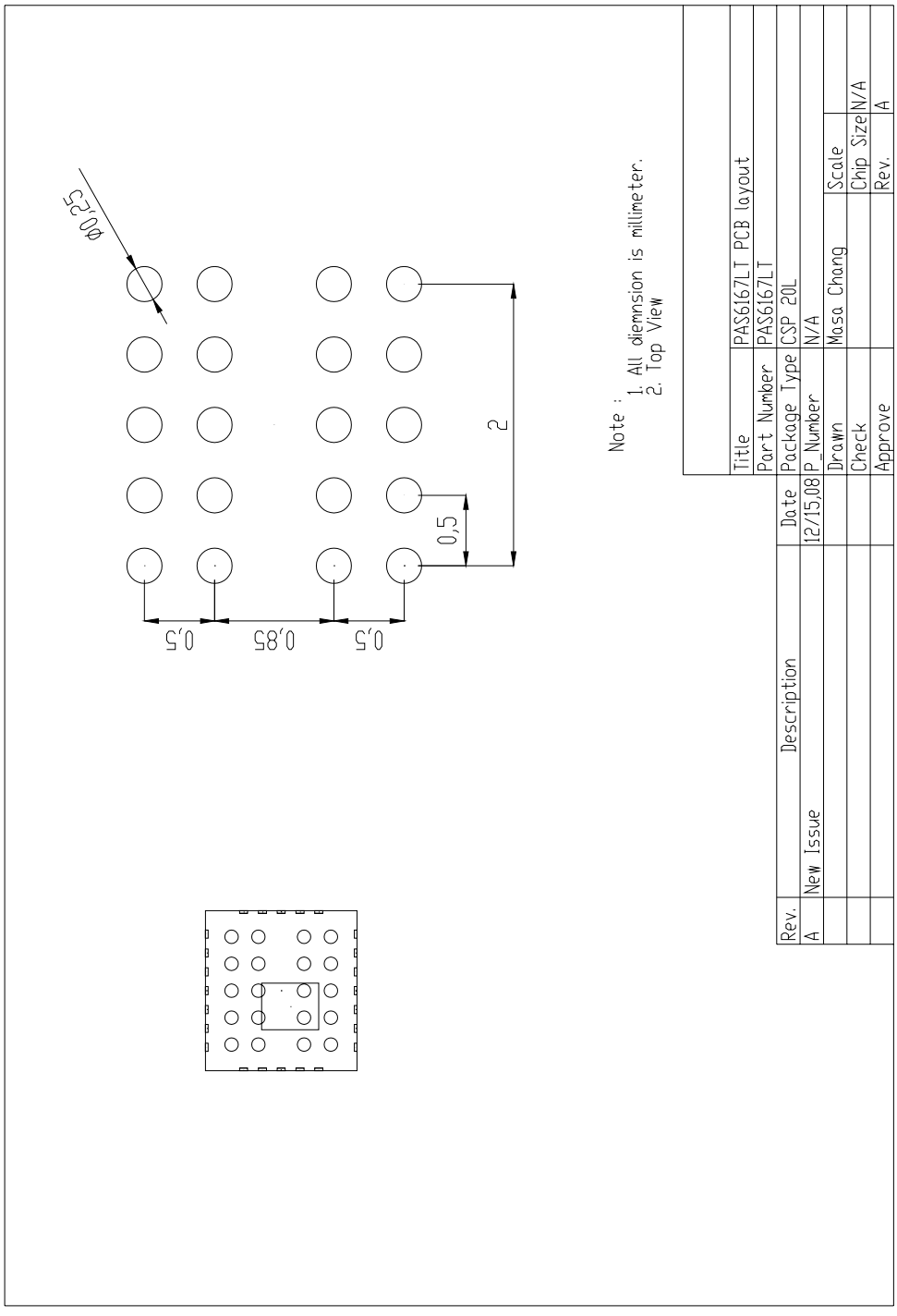


Figure 1

*Note:

The formation of image is the result formed by package Top view(A1 : left-up) and general Lens(invert and mirror the image).

Recommended Layout PCB



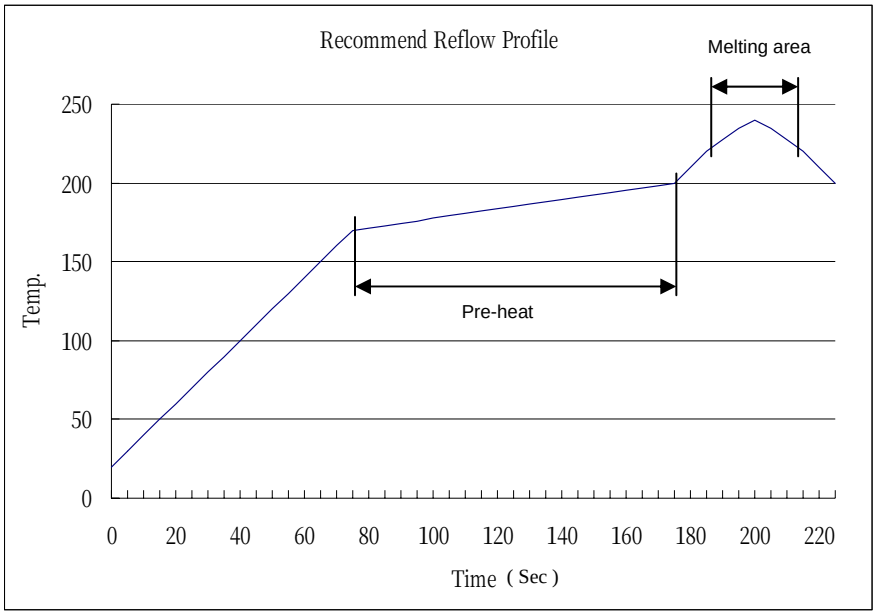
Recommended Condition For Infrared Reflow

Carefully observe the mounting conditions, recommended temperature profile when

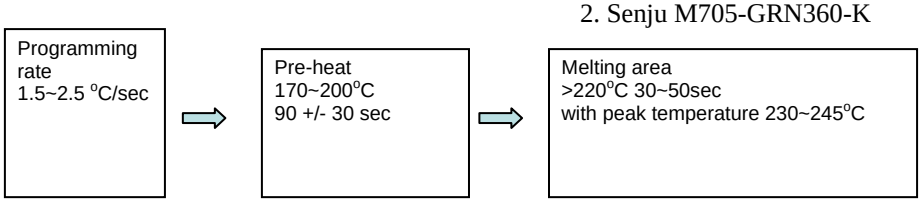
Mounting infrared reflows is show in the figure below.

After mounting on the mother board, it must be dispense epoxy in side of the CSP package.

⊙ Reflow Profile



Recommend Pb-free solder paste vender & type : 1. Almit LFM-48W TM-HP
2. Senju M705-GRN360-K



⊙ Dispense Epoxy