# 13 Gbps, 2:1 SELECTOR w/ PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

## Typical Applications

The HMC748LC3C is ideal for:

- 2:1 Multiplexer up to 13 Gbps
- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 13 Gbps
- Redundant Path Switching
- Built-in Test

## Features

Supports High Data Rates: up to 13 Gbps

Single-ended inputs

Differential & Single-ended outputs

Fast Rise and Fall Times: 22 / 22 ps

Low Power Consumption: 250 mW typ.

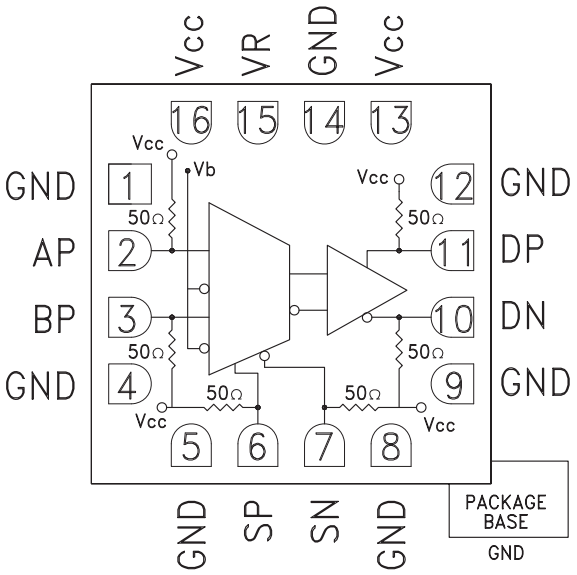
Programmable Differential
Output Voltage Swing: 600 - 1200 mV

Propagation Delay: 125 ps

Single Supply: +3.3V

16 Lead Ceramic 3x3mm SMT Package: $9mm^2$

## Functional Diagram




## General Description

The HMC748LC3C is a 2:1 Selector designed to support data transmission rates of up to 13 Gbps, and selector port operation of up to 13 GHz. The selector routes one of the two single-ended inputs to the differential output upon assertion of the proper select port. The HMC748LC3C also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All single-ended input signals to the HMC748LC3C are terminated with 50 ohms to Vcc on-chip, and may be either AC or DC coupled. The outputs of the HMC748LC3C may be operated either differentially or single-ended. Inputs or outputs can be connected directly to a 50 ohm to Vcc terminated system, while DC blocking capacitors may be used if the terminating system is 50 ohms to ground. The HMC748LC3C operates from a single +3.3V DC supply and is housed in a ceramic RoHS compliant 3x3 mm SMT package.

## Electrical Specifications, $T_A$ = +25°C, Vcc = +3.3V

| Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| Power Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| Power Supply Current | | | 76 | | mA |
| Maximum Data Rate | | | 13 | | Gbps |
| Maximum Select Rate | | | 13 | | GHz |
| Maximum Serial Transmission Rate | | | 26 | | Gbps |
| Input High Voltage | | 2.8 | | 3.8 | V |
| Input Low Voltage | | 2.1 | | 3.3 | V |
| Input Return Loss | Frequency <13 GHz | | 10 | | dB |
| Output Amplitude | Single-Ended, peak-to-peak | | 550 | | mVpp |
| | Differential, peak-to-peak | | 1100 | | mVpp |
| Output High Voltage | | | 3.25 | | V |

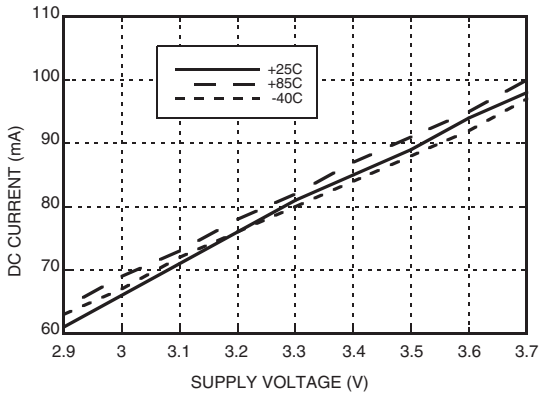
## Electrical Specifications (continued)

| Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| Output Low Voltage | | | 2 | | V |
| Output Rise / Fall Time | Differential, 20% - 80% | | 22 / 22 | | ps |
| Output Return Loss | Frequency <13 GHz | | 10 | | dB |
| Random Jitter, Jr | rms [1] | | | 0.2 | ps rms |
| Deterministic Jitter, Jd | peak-to-peak, $2^{15}$-1 PRBS input [2] | | 2 | | ps, pp |
| Propagation Delay, A or B to $D_{OUT}$, td | | | 125 | | ps |
| Propagation Delay Select to Data, tds | | | 135 | | ps |
| Set Up & Hold Time, $t_{SH}$ | | | 6 | | ps |

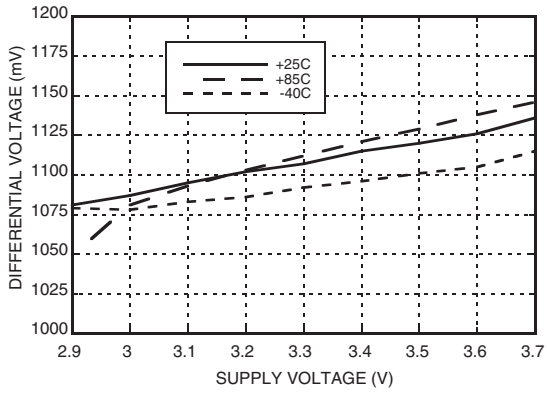
[1] Upper limit of random jitter, Jr, determined by measuring and integrating output phase noise with a sinusoidal input at 5, 10, and 13.5 GHz over temperature

[2] Deterministic jitter calculated by simultaneously measuring the jitter of a 200 mV, 12.5 GHz, $2^{15}$-1 PRBS input, and a single-ended output

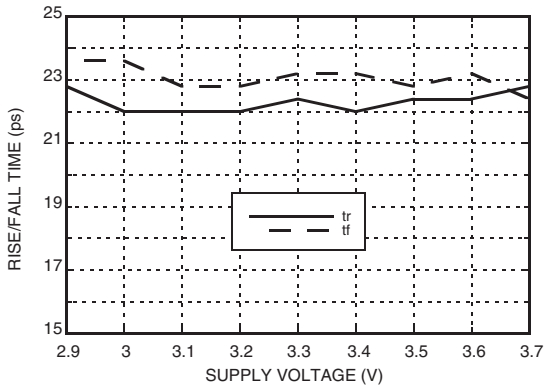
### DC Current vs. Supply Voltage [1] [2]



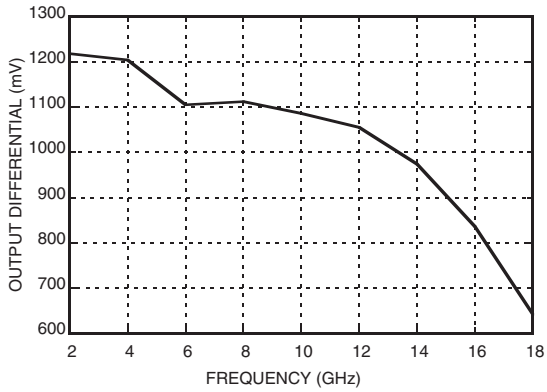

### Output Differential vs. Supply Voltage [1] [2]




### Rise / Fall Time vs. Supply Voltage [1] [2]

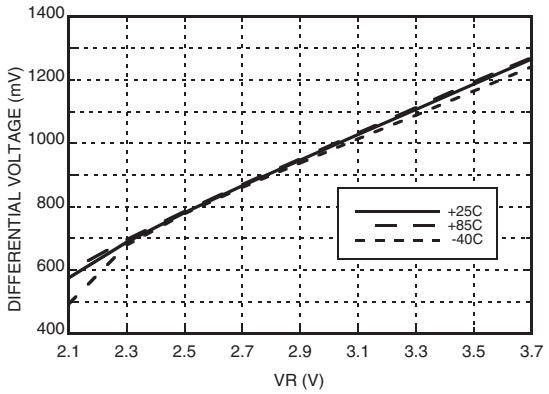



### Output Differential vs. Frequency [1]

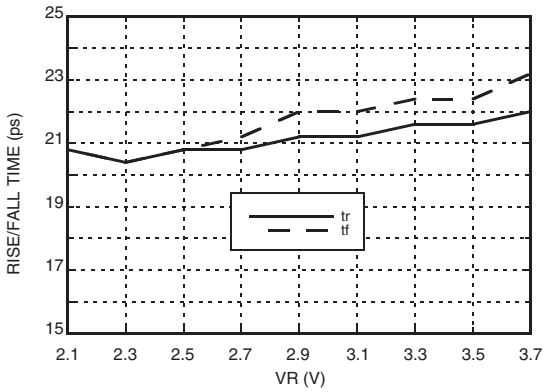



[1] VR = +3.3V [2] Frequency = 13 GHz

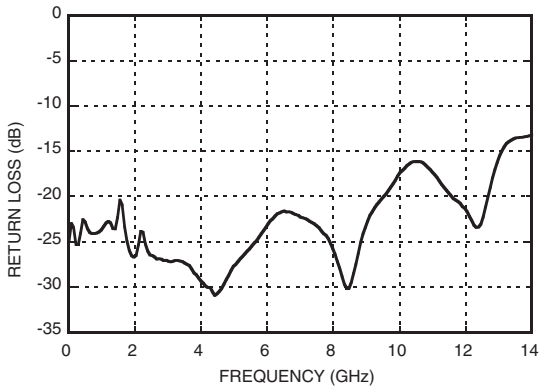
### Output Differential vs. VR [2]



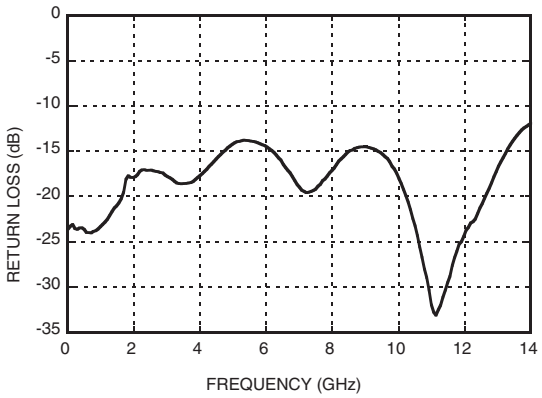

### Rise / Fall Time vs. VR [2]



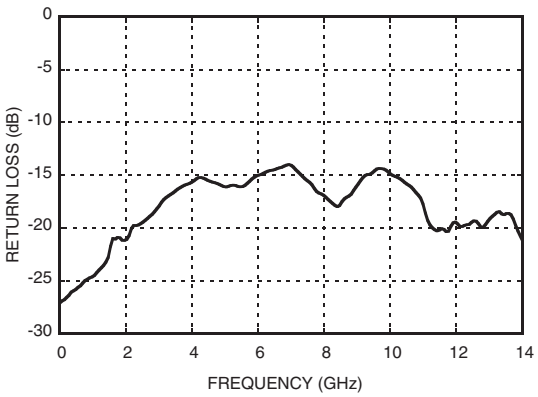

### Input Return Loss vs. Frequency




### Output Return Loss vs. Frequency




### Select Port Return Loss vs. Frequency




[1] VR = +3.3V [2] Frequency = 13 GHz

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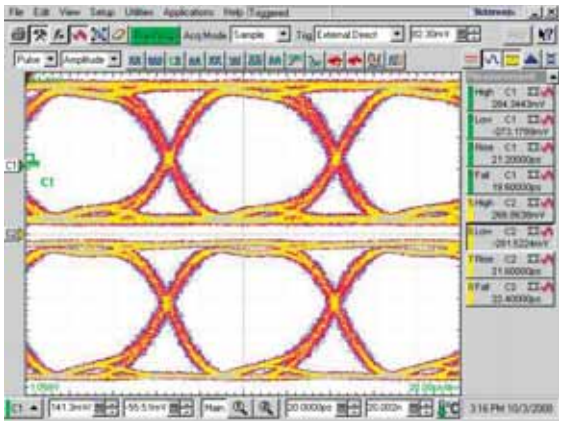
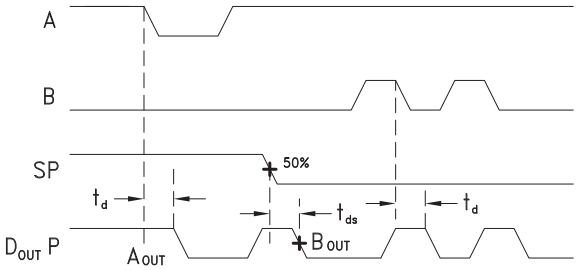
## Eye Diagram



[1] Test Conditions:
Waveform generated with an Agilent N4903A J-Bert.
Rate = 13 GHz
Eye Diagram data presented on a Tektronix CSA 8000
Device is AC coupled to scope.

## Timing Diagram




td = propagation delay, A or B to Dout
tds = propagation delay, Select to Dout

## Truth Table

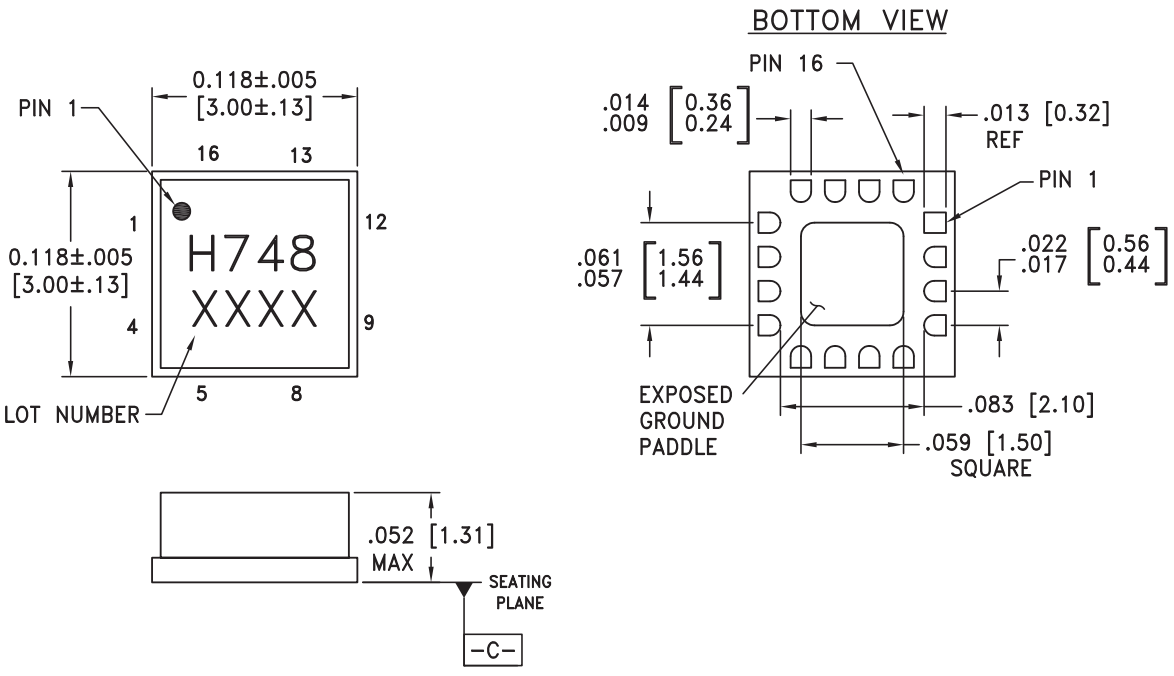
| Inputs | | Outputs |
|---|---|---|
| SP | SN | DP |
| L | H | A -> D |
| H | L | B -> D |
| H = Negative Voltage Level<br>L = Positive Voltage Level | | |
| Notes:<br>D = DP - DN<br>S = SP - SN | | |

## Absolute Maximum Ratings

| | |
|---|---|
| Power Supply Voltage (Vcc) | -0.5V to +3.7V |
| Input Signals | Vcc - 2V to Vcc + 0.5V |
| Output Signals | +1V to +3.7V |
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | -40°C to +85°C |

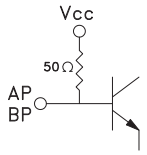
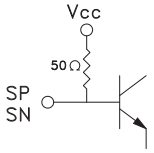
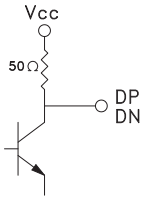
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Outline Drawing

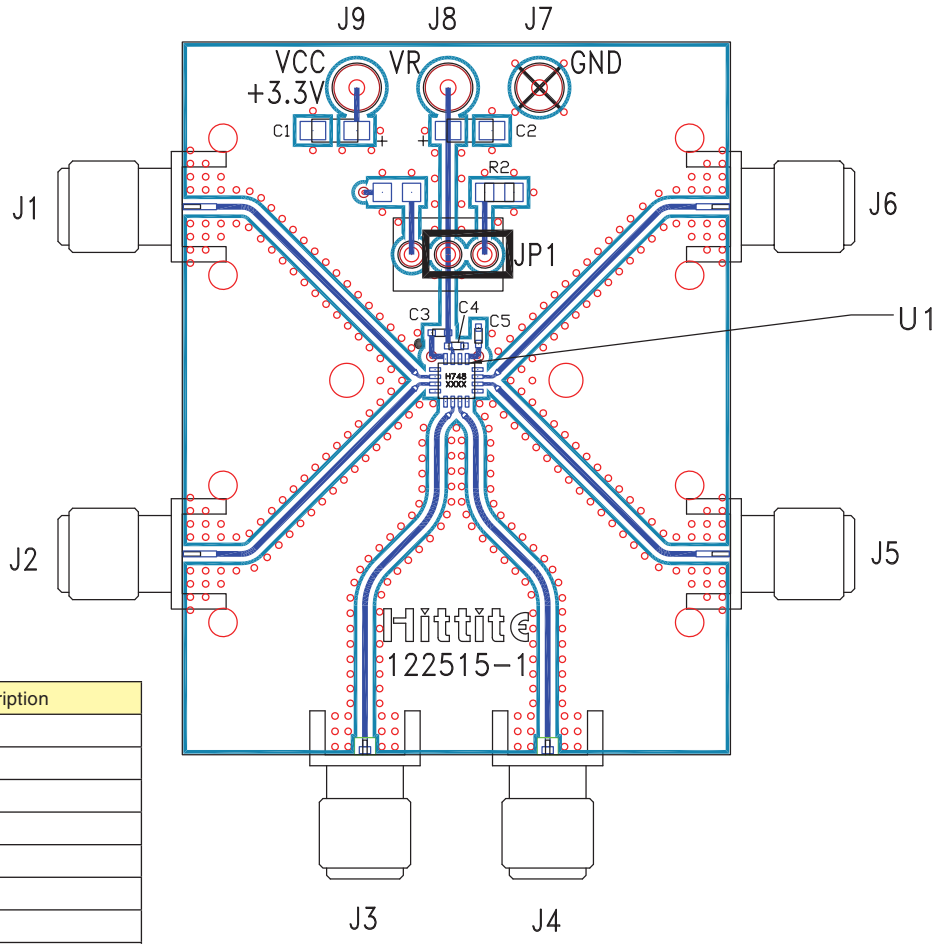



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 4, 5, 8, 9, 12 | GND | Signal Grounds |   |
| 2, 3 | AP, BP | Data Inputs |   |
| 6, 7 | SP, SN | Select Inputs |   |
| 10, 11 | DN, DP | Data Outputs |   |
| 13, 16 | Vcc | Positive Supply | |
| 14, Package Base | GND | Supply Ground |   |
| 15 | VR | Output level control. Output level may be adjusted by applying a voltage to VR per "Output Differential vs. VR" plot. |   |

### Evaluation PCB




| Item | Description |
|---|---|
| J1 | AP |
| J2 | BP |
| J3 | SP |
| J4 | SN |
| J5 | DN |
| J6 | DP |
| J7 | GND |
| J8 | VR |
| J9 | Vcc |

### List of Materials for Evaluation PCB 122517 [1]

| Item | Description |
|---|---|
| J1 - J6 | PCB Mount SMA RF Connectors |
| J7 - J9 | DC Pin |
| JP1 | Shorting Jumper |
| C1, C2 | 4.7 µF Capacitor, Tantalum |
| C3 - C5 | 100 pF Capacitor, 0402 Pkg. |
| R2 | 10 Ohm Resistor, 0603 Pkg. |
| U1 | HMC748LC3C<br>High Speed Logic, 2:1 Selector |
| PCB [2] | 122515 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

### Application Circuit