DDR3 SDRAM Unbuffered DIMMs
Based on 2Gb M version

HMT351U6MFR8C
HMT351U7MFR8C

** Contents are subject to change without prior notice.

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial draft for internal review	Sep. 2008	Preliminary
0.2	Modified Speed grade	Nov. 2008	
0.3	Added IDD Spec	Jan. 2009	

Table of Contents

1. Description

This Hynix unbuffered Dual In-Line Memory Module(DIMM) series consists of 2Gb M version. DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 240 pin glass-epoxy substrate. This DDR3 Unbuffered DIMM series based on 2Gb M ver. provide a high performance 8 byte interface in 133.35mm width form factor of industry standard. It is suitable for easy interchange and addition.

1.1 Device Features & Ordering Information

1.1.1 Features

- VDD=VDDQ=1.5V
- VDDSPD=3.3V to 3.6V
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- On chip DLL align DQ, DQS and /DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, and (11) supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- DDR3 SDRAM Package: JEDEC standard 82ball FBGA(x4/x8)) with support balls
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Auto Self Refresh supported
- On Die Thermal Sensor supported (JEDEC optional)

1.1.2 Ordering Information

Part Name	Density	Org.	# of DRAMs	# of ranks	Materials	ECC	TS
HMT351U6MFR8C-S6/G7/H9	4GB	512Mx64	16	2	Halogen-free	None	No
HMT351U7MFR8C-S6/G7/H9	4GB	512Mx72	18	2	Halogen-free	ECC	Yes

1.2 Speed Grade & Key Parameters

MT/S	DDR3-800	DDR3-1066	DDR3-1333	Unit
Grade	-S6	-G7	-H9	
tCK(min)	2.5	1.875	1.5	ns
CAS Latency	6	7	9	tCK
tRCD(min)	15	13.125	13.5	ns
tRP(min)	15	13.125	13.5	ns
tRAS(min)	37.5	37.5	36	ns
tRC(min)	52.5	50.625	49.5	ns
CL-tRCD-tRP	6-6-6	7-7-7	9-9-9	tCK

1.3 Address Table

	HMT351U6MFR8C	HMT351U7MFR8C
Organization	512M x 64	512M x 72
Refresh Method	8K/64ms	8K/64ms
Row Address	A0-A14	A0-A14
Column Address	A0-A9	A0-A9
Bank Address	BA0-BA2	BA0-BA2
Page Size	1KB	1KB
# of Rank	2	2
# of Device	16	18

2. Pin Architecture

2.1 Pin Definition

Pin Name	Description	Pin Name	Description
A0–A14	SDRAM address bus	SCL	I^2C serial bus clock for EEPROM
BA0–BA2	SDRAM bank select	SDA	I^2C serial bus data line for EEPROM
$\overline{RAS}$	SDRAM row address strobe	SA0–SA2	I^2C slave address select for EEPROM
$\overline{CAS}$	SDRAM column address strobe	V_{DD}*	SDRAM core power supply
$\overline{WE}$	SDRAM write enable	V_{DDQ}*	SDRAM I/O Driver power supply
$\overline{S}$0–$\overline{S}$1	DIMM Rank Select Lines	V_{REF}DQ	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	V_{REF}CA	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	V_{SS}	Power supply return (ground)
DQ0–DQ63	DIMM memory data bus	V_{DDSPD}	Serial EEPROM positive power supply
CB0–CB7	DIMM ECC check bits	NC	Spare pins (no connect)
DQS0–DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Memory bus analysis tools (unused on memory DIMMS)
$\overline{DQS0}$–$\overline{DQS8}$	SDRAM data strobes (negative line of differential pair)	RESET	Set DRAMs to Known State
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	V_{TT}	SDRAM I/O termination supply
CK0–CK1	SDRAM clocks (positive line of differential pair)	RFU	Reserved for future use
$\overline{CK0}$–$\overline{CK1}$	SDRAM clocks (negative line of differential pair)	-	-

***The V_{DD} and V_{DDQ} pins are tied common to a single power-plane on these designs**

2.2 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0–CK1 $\overline{CK0}$–$\overline{CK1}$	SSTL	Differential crossing	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is reference to the crossing of CK and $\overline{CK}$ (Both directions of crossing).
CKE0–CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S}$0–$\overline{S}$1	SSTL	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	SSTL	Active Low	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (ALONG WITH $\overline{S}$) define the command being entered.
ODT0–ODT1	SSTL	Active High	When high, termination resistance is enabled for all DQ, DQS, $\overline{DQS}$ and DM pins, assuming this function is enabled in the Mode Register 1 (MR1).
V_{REF}DQ	Supply		Reference voltage for SSTL15 I/O inputs.
V_{REF}CA	Supply		Reference voltage for SSTL 15 command/address inputs.
V_{DD}Q	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, V_{DD}Q shares the same power plane as V_{DD} pins.
BA0–BA2	SSTL	—	Selects which SDRAM bank of eight is activated.
A0–A13	SSTL	—	During a Bank Activate command cycle, Address input defines the row address (RA0–RA15). During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
DQ0–DQ63, CB0–CB7	SSTL	—	Data and Check Bit Input/Output pins.
DM0–DM8	SSTL	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR3 SDRAM input buffers, and core logic. V_{DD} and V_{DD}Q pins are tied to V_{DD}/V_{DD}Q planes on these modules.

Symbol	Type	Polarity	Function
$\overline{DQS0}$–$\overline{DQS8}$ DQS0–DQS8	SSTL	Differential crossing	Data strobe for input and output data.
SA0–SA2		—	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to VDDSPD to act as a pullup on the system board.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to VDDSPD to act as a pullup on the system board.
VDDSPD	Supply		Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V.

2.3 Pin Assignment

Front Side(left 1–60)			Back Side(right 121–180)			Front Side(left 61–120)			Back Side(right 181–240)		
Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC
1	VREFDQ	VREFDQ	121	VSS	VSS	61	A2	A2	181	A1	A1
2	VSS	VSS	122	DQ4	DQ4	62	VDD	VDD	182	VDD	VDD
3	DQ0	DQ0	123	DQ5	DQ5	63	CK1	CK1	183	VDD	VDD
4	DQ1	DQ1	124	VSS	VSS	64	$\overline{CK1}$	$\overline{CK1}$	184	CK0	CK0
5	VSS	VSS	125	DM0	DM0	65	VDD	VDD	185	$\overline{CK0}$	$\overline{CK0}$
6	$\overline{DQS0}$	$\overline{DQS0}$	126	NC	NC	66	VDD	VDD	186	VDD	VDD
7	DQS0	DQS0	127	VSS	VSS	67	VREFCA	VREFCA	187	NC	NC
8	VSS	VSS	128	DQ6	DQ6	68	NC	NC	188	A0	A0
9	DQ2	DQ2	129	DQ7	DQ7	69	VDD	VDD	189	VDD	VDD
10	DQ3	DQ3	130	VSS	VSS	70	A10	A10	190	BA1[2]	BA1[2]
11	VSS	VSS	131	DQ12	DQ12	71	BA0[2]	BA0[2]	191	VDD	VDD
12	DQ8	DQ8	132	DQ13	DQ13	72	VDD	VDD	192	$\overline{RAS}$	$\overline{RAS}$
13	DQ9	DQ9	133	VSS	VSS	73	$\overline{WE}$	$\overline{WE}$	193	$\overline{S0}$	$\overline{S0}$
14	VSS	VSS	134	DM1	DM1	74	$\overline{CAS}$	$\overline{CAS}$	194	VDD	VDD
15	$\overline{DQS1}$	$\overline{DQS1}$	135	NC	NC	75	VDD	VDD	195	ODT0	ODT0
16	DQS1	DQS1	136	VSS	VSS	76	S1	S1	196	A13	A13

NC = No Connect; RFU = Reserved Future Use

1. NC pins should not be connected to anything on the DIMM, including bussing within the NC group.
2. Address pins A3–A8 and BA0 and BA1 can be mirrored or not mirrored. Please refer to Section 4.1 for more information on mirrored addresses.

Front Side(left 1–60)			Back Side(right 121–180)			Front Side(left 61–120)			Back Side(right 181–240)		
Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC
17	VSS	VSS	137	DQ14	DQ14	77	ODT1	ODT1	197	VDD	VDD
18	DQ10	DQ10	138	DQ15	DQ15	78	VDD	VDD	198	NC	NC
19	DQ11	DQ11	139	VSS	VSS	79	NC	NC	199	VSS	VSS
20	VSS	VSS	140	DQ20	DQ20	80	VSS	VSS	200	DQ36	DQ36
21	DQ16	DQ16	141	DQ21	DQ21	81	DQ32	DQ32	201	DQ37	DQ37
22	DQ17	DQ17	142	VSS	VSS	82	DQ33	DQ33	202	VSS	VSS
23	VSS	VSS	143	DM2	DM2	83	VSS	VSS	203	DM4	DM4
24	$\overline{\text{DQS2}}$	$\overline{\text{DQS2}}$	144	$\overline{\text{NC}}$	$\overline{\text{NC}}$	84	$\overline{\text{DQS4}}$	$\overline{\text{DQS4}}$	204	NC	NC
25	DQS2	DQS2	145	VSS	VSS	85	DQS4	DQS4	205	VSS	VSS
26	VSS	VSS	146	DQ22	DQ22	86	VSS	VSS	206	DQ38	DQ38
27	DQ18	DQ18	147	DQ23	DQ23	87	DQ34	DQ34	207	DQ39	DQ39
28	DQ19	DQ19	148	VSS	VSS	88	DQ35	DQ35	208	VSS	VSS
29	VSS	VSS	149	DQ28	DQ28	89	VSS	VSS	209	DQ44	DQ44
30	DQ24	DQ24	150	DQ29	DQ29	90	DQ40	DQ40	210	DQ45	DQ45
31	DQ25	DQ25	151	VSS	VSS	91	DQ41	DQ41	211	VSS	VSS
32	VSS	VSS	152	DM3	DM3	92	VSS	VSS	212	DM5	DM5
33	$\overline{\text{DQS3}}$	$\overline{\text{DQS3}}$	153	NC	NC	93	$\overline{\text{DQS5}}$	$\overline{\text{DQS5}}$	213	NC	NC
34	DQS3	DQS3	154	VSS	VSS	94	DQS5	DQS5	214	VSS	VSS
35	VSS	VSS	155	DQ30	DQ30	95	VSS	VSS	215	DQ46	DQ46
36	DQ26	DQ26	156	DQ31	DQ31	96	DQ42	DQ42	216	DQ47	DQ47
37	DQ27	DQ27	157	VSS	VSS	97	DQ43	DQ43	217	VSS	VSS
38	VSS	VSS	158	NC	CB4	98	VSS	VSS	218	DQ52	DQ52
39	NC	CB0	159	NC	CB5	99	DQ48	DQ48	219	DQ53	DQ53
40	NC	CB1	160	VSS	VSS	100	DQ49	DQ49	220	VSS	VSS
41	VSS	VSS	161	DM8	DM8	101	VSS	VSS	221	DM6	DM6
42	NC	$\overline{\text{DQS8}}$	162	NC	NC	102	$\overline{\text{DQS6}}$	$\overline{\text{DQS6}}$	222	NC	NC
43	NC	DQS8	163	VSS	VSS	103	DQS6	DQS6	223	VSS	VSS
44	VSS	VSS	164	NC	CB6	104	VSS	VSS	224	DQ54	DQ54
45	NC	CB2	165	NC	CB7	105	DQ50	DQ50	225	DQ55	DQ55
46	NC	CB3	166	VSS	VSS	106	DQ51	DQ51	226	VSS	VSS
47	VSS	VSS	167	NC	NC	107	VSS	VSS	227	DQ60	DQ60

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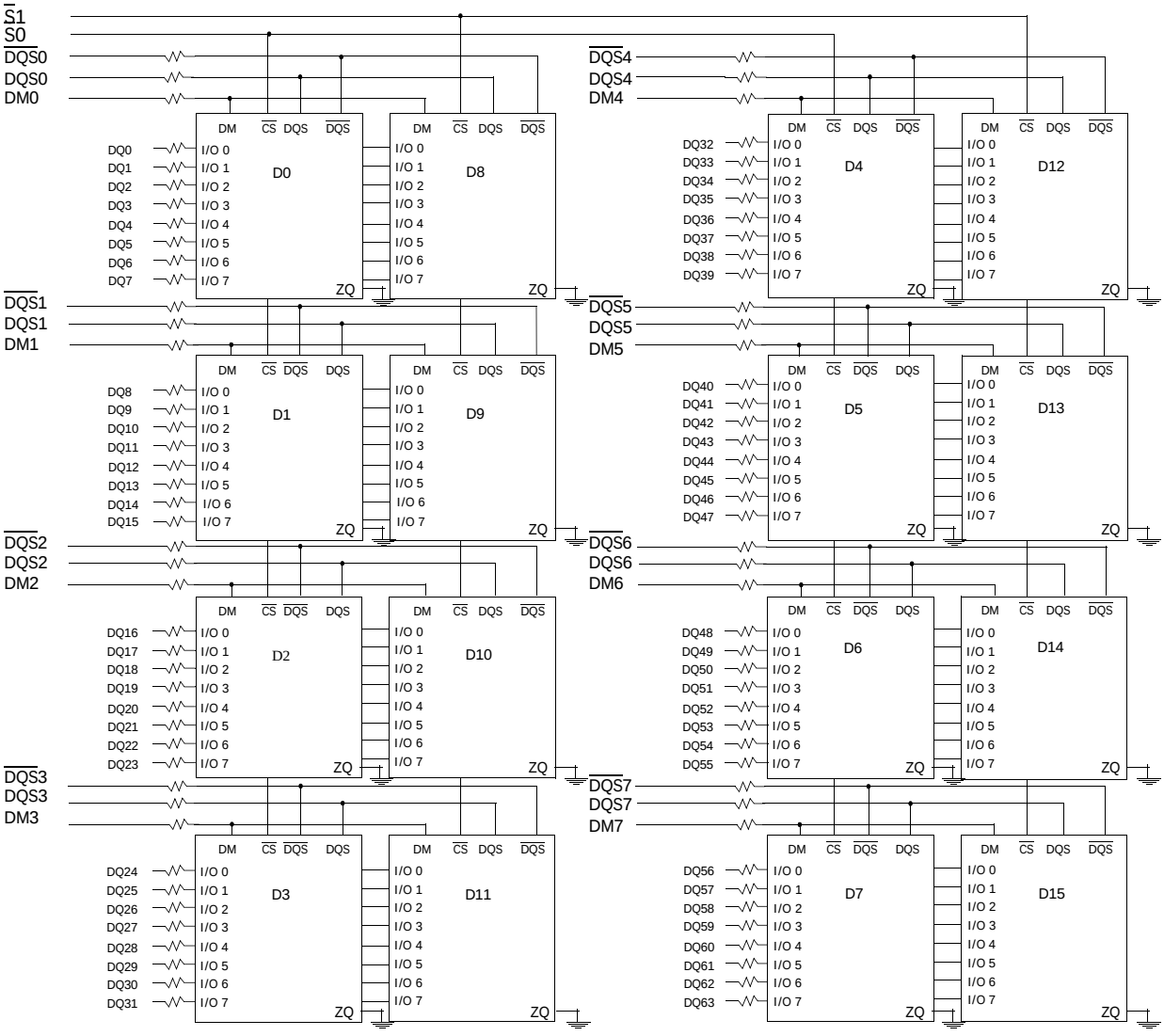
2. Address pins A3–A8 and BA0 and BA1 can be mirrored or not mirrored. Please refer to Section 4.1 for more information on mirrored addresses.

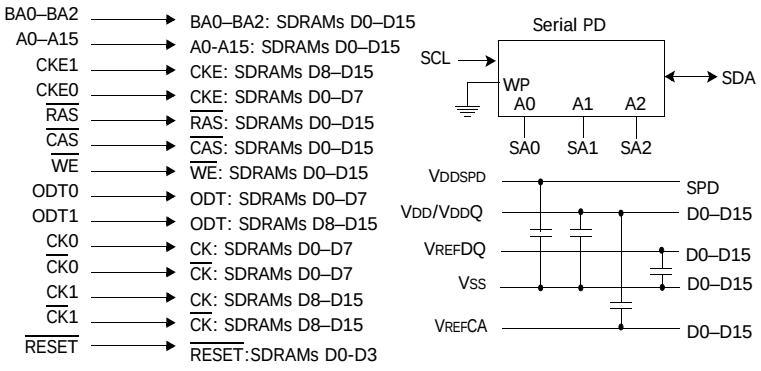
Front Side(left 1–60)			Back Side(right 121–180)			Front Side(left 61–120)			Back Side(right 181–240)		
Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC
48	NC	NC	168	Reset	Reset	108	DQ56	DQ56	228	DQ61	DQ61
KEY			KEY			109	DQ57	DQ57	229	V_{SS}	V_{SS}
49	NC	NC	169	CKE1/NC	CKE1/NC	110	V_{SS}	V_{SS}	230	DM7	DM7
50	CKE0	CKE0	170	V_{DD}	V_{DD}	111	$\overline{DQS}$7	$\overline{DQS}$7	231	NC	NC
51	V_{DD}	V_{DD}	171	NC	NC	112	DQS7	DQS7	232	V_{SS}	V_{SS}
52	BA2	BA2	172	NC	NC	113	V_{SS}	V_{SS}	233	DQ62	DQ62
53	NC	NC	173	V_{DD}	V_{DD}	114	DQ58	DQ58	234	DQ63	DQ63
54	V_{DD}	V_{DD}	174	A12	A12	115	DQ59	DQ59	235	V_{SS}	V_{SS}
55	All	All	175	A9	A9	116	V_{SS}	V_{SS}	236	V_{DDSPD}	V_{DDSPD}
56	A7[2]	A7[2]	176	V_{DD}	V_{DD}	117	SA0	SA0	237	SA1	SA1
57	V_{DD}	V_{DD}	177	A8[2]	A8[2]	118	SCL	SCL	238	SDA	SDA
58	A5[2]	A5[2]	178	A6[2]	A6[2]	119	SA2	SA2	239	V_{SS}	V_{SS}
59	A4[2]	A4[2]	179	V_{DD}	V_{DD}	120	V_{TT}	V_{TT}	240	V_{TT}	V_{TT}
60	V_{DD}	V_{DD}	180	A3[2]	A3[2]						

NC = No Connect; RFU = Reserved Future Use

1. NC pins should not be connected to anything on the DIMM, including bussing within the NC group.
2. Address pins A3–A8 and BA0 and BA1 can be mirrored or not mirrored. Please refer to Section 4.1 for more information on mirrored addresses.

3.1 4GB, 512Mx64 Module(2Rank of x8)

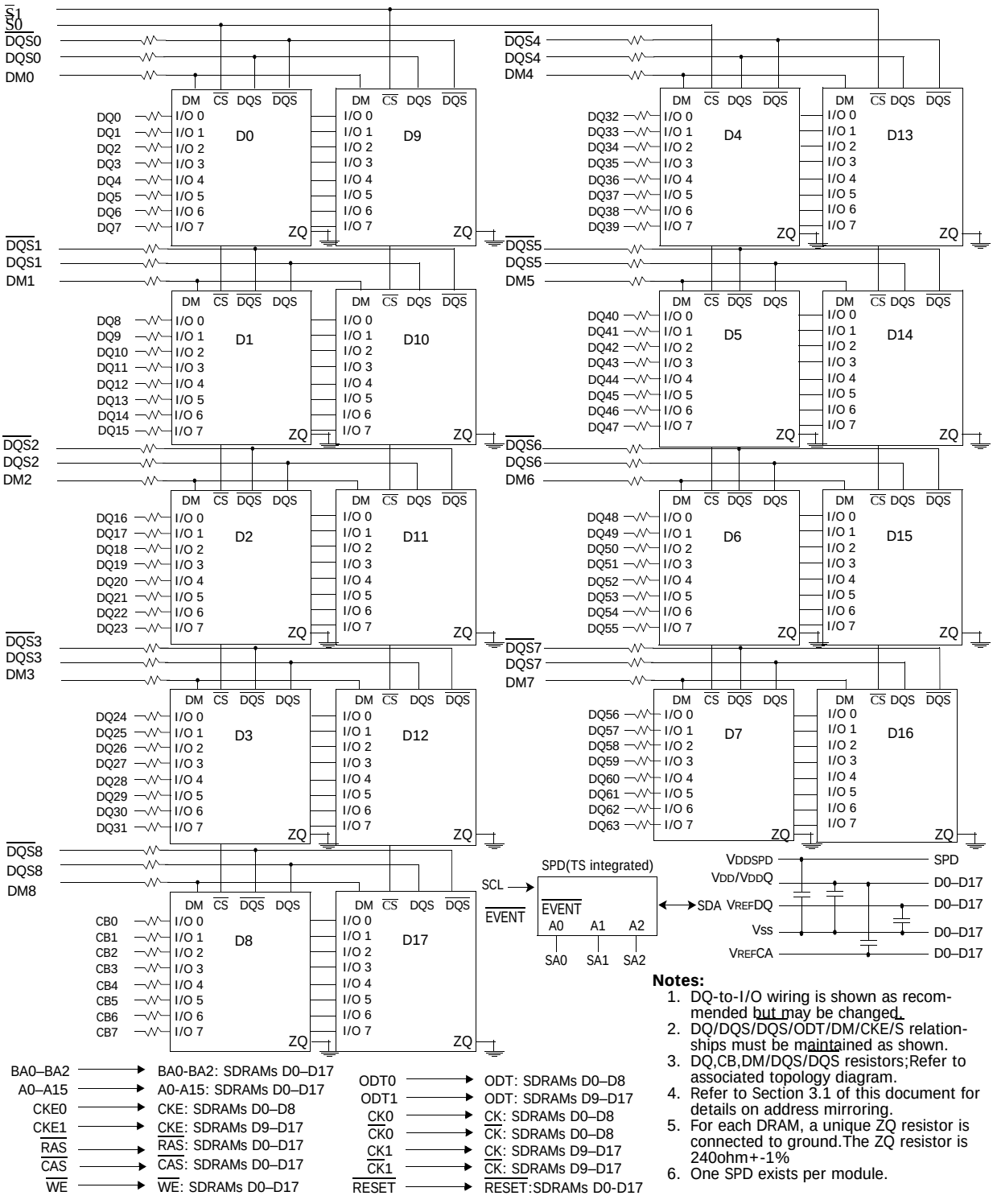




Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ,DM,DQS,DQS resistors;Refer to associated topology diagram.
4. Refer to Section 3.1 of this document for details on address mirroring.
5. For each DRAM, a unique ZQ resistor is connected to ground.The ZQ resistor is 240ohm+-1%
6. One SPD exists per module.

3.2 4GB, 512Mx72 Module(2Rank of x8)



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ,CB,DM/DQS/DQS resistors;Refer to associated topology diagram.
4. Refer to Section 3.1 of this document for details on address mirroring.
5. For each DRAM, a unique ZQ resistor is connected to ground.The ZQ resistor is 240ohm+-1%
6. One SPD exists per module.

4. Address Mirroring Feature

There is a via grid located under the SDRAMs for wiring the CA signals (address, bank address, command, and control lines) to the SDRAM pins. The length of the traces from the via to the SDRAMs places limitations on the bandwidth of the module. The shorter these traces, the higher the bandwidth. To extend the bandwidth of the CA bus for DDR3 modules, a scheme was defined to reduce the length of these traces.The pins on the SDRAM are defined in a manner that allows for these short trace lengths. The CA bus pins in Columns 2 and 8, ignoring the mechanical support pins, do not have any special functions (secondary functions). This allows the most flexibility with these pins. These are address pins A3, A4, A5, A6, A7, A8 and bank address pins BA0 and BA1. Refer to Table . Rank 0 SDRAM pins are wired straight, with no mismatch between the connector pin assignment and the SDRAM pin assignment. Some of the Rank 1 SDRAM pins are cross wired as defined in the table. Pins not listed in the table are wired straight.

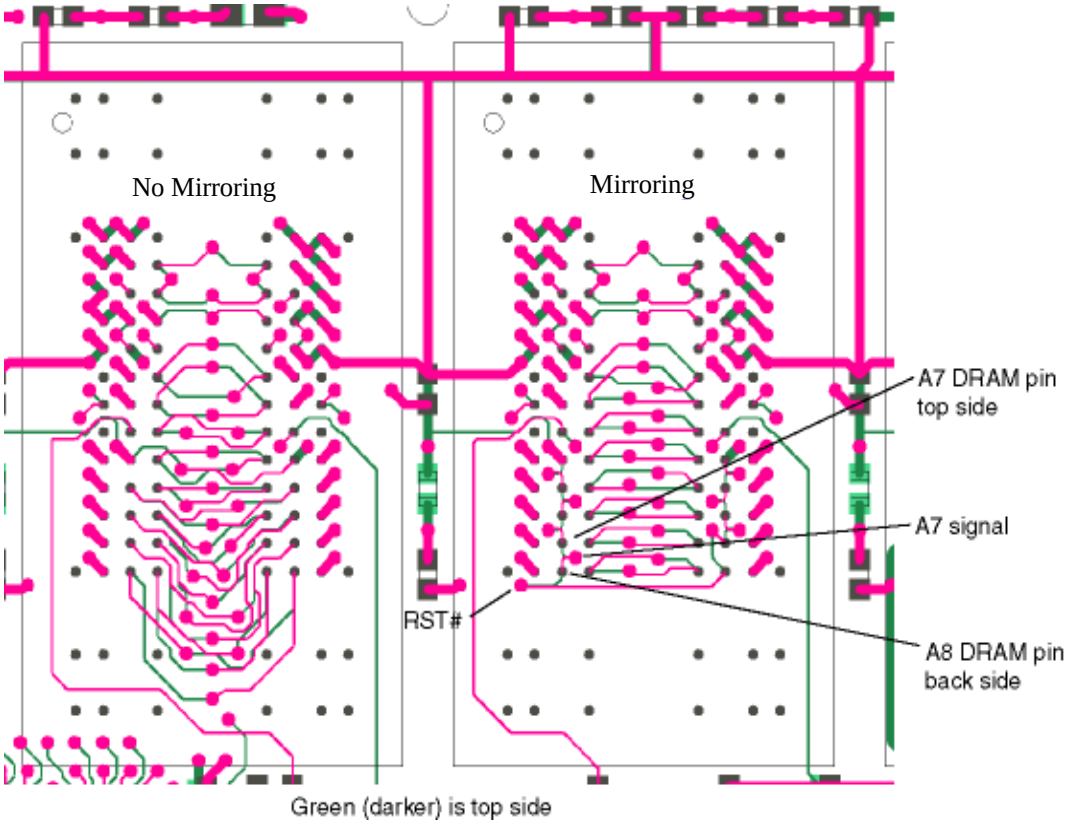
4.1 DRAM Pin Wiring for Mirroring

Connector Pin	SDRAM Pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

<Table 4.1: SDRAM Pin Wiring for Mirroring >

The table 4.1 illustrates the wiring in both the mirrored and non-mirrored case.

The lengths of the traces to the SDRAM pins, is obviously shorter. The via grid is smaller as well.



< Figure 4.1: Wiring Differences for Mirrored and Non-Mirrored Addresses >

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. This requires a few rules. Mirroring is done on 2 rank modules and can only be done on the second rank. There is not a requirement that the second rank be mirrored. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR3 UDIMM SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the second rank.

5. ABSOLUTE MAXIMUM RATINGS

5.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VIN, VOUT	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	
TSTG	Storage Temperature	-55 to +100 ℃	℃	, 2

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must be not greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

5.2 DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Temperature Range	0 to 85	℃	,2
	Extended Temperature Range	85 to 95	℃	1,3

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°... and 95°... case temperature.
   Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. (This double refresh requirement may not apply for some devices.) It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/ or the DIMM SPD for option avail ability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, than it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0band MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

6. AC & DC Operating Conditions

6.1 Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD abd VDDQ tied together.

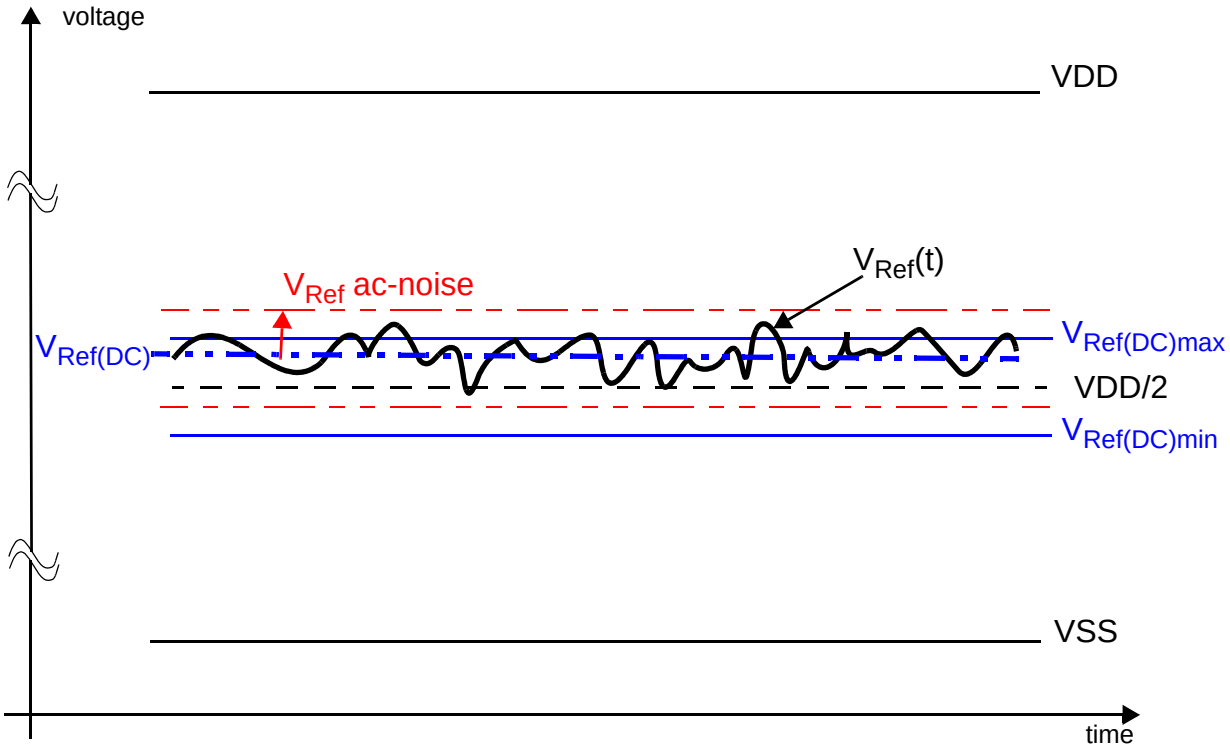
6.2 DC & AC Logic Input Levels

6.2.1 DC & AC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333		Unit	Notes
		Min	Max		
VIH(DC)	DC input logic high	Vref + 0.100	-	V	1, 2
VIL(DC)	DC input logic low		Vref - 0.100	V	1, 2
VIH(AC)	AC input logic high	Vref + 0.175	-	V	1, 2
VIL(AC)	AC input logic low		Vref - 0.175	V	1, 2
VRefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VRefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VTT	Termination voltage for DQ, DQS outputs	VDDQ/2 - TBD	VDDQ/2 + TBD	V	

1. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
2. The “t.b.d.” entries might change based on overshoot and undershoot specification.
3. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
   For reference: approx. VDD/2 +/- 15 mV.

The dc-tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in figure 6.2.1. It shows a valid reference voltage VRef(t) as a function of time. (VRef stands for VRefCA and VRefDQ like-wise).VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 1. Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD.



< Figure 6.2.1: Illustration of Vref(DC) tolerance and Vref AC-noise limits >

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VRef. "VRef " shall be understood as VRef(DC), as defined in Figure 6.2.1
This clarifies, that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VRef(DC) deviations from the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

6.2.2 DC & AC Logic Input Levels for Differential Signals

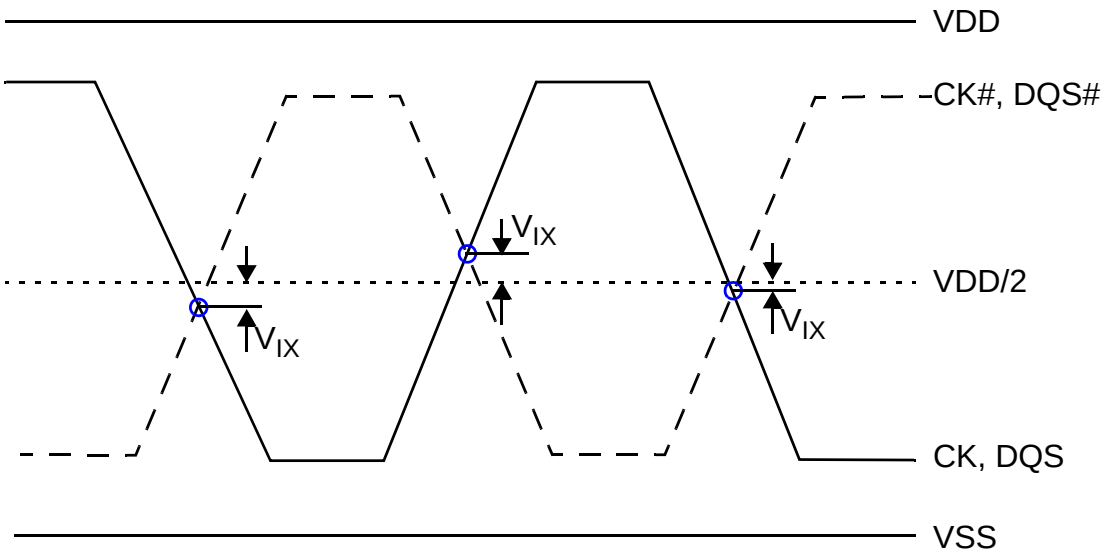
Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333		Unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+ 0.200	-	V	1
VILdiff	Differential input logic low		- 0.200	V	1

Note1:

Refer to “Overshoot and Undershoot Specification section 6.5 on 26 page

6.2.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table 6.2.3 The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



< Figure 6.2.3 Vix Definition >

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2	- 150	+ 150	mV	

< Table 6.2.3: Cross point voltage for differential input signals (CK, DQS) >

6.3 Slew Rate Definitions

6.3.1 For Single Ended Input Signals

- Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL(AC)max.

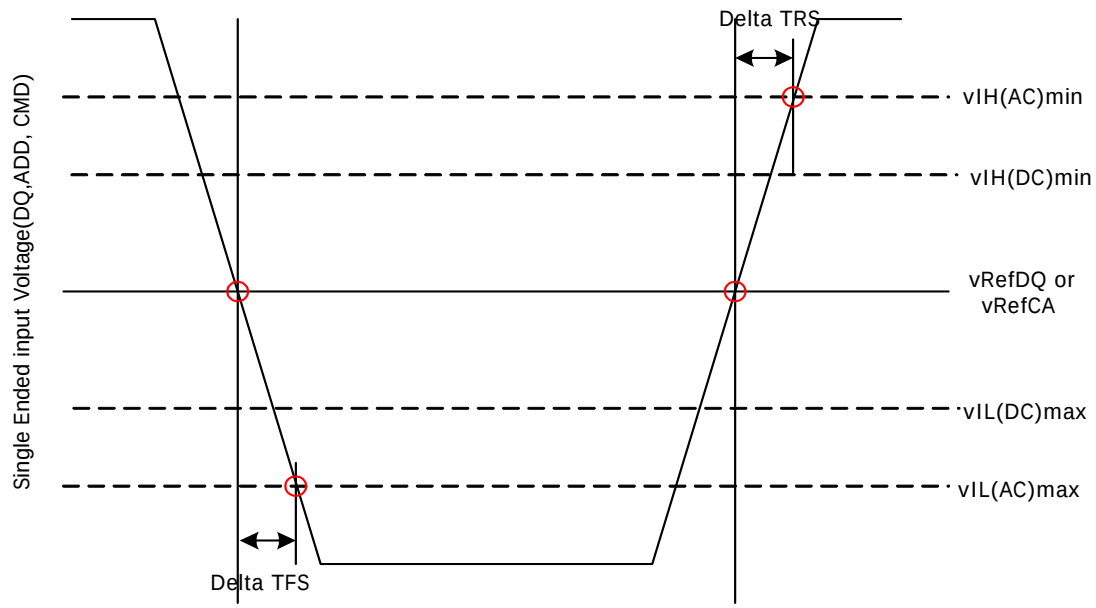
- Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VRef. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VRef.

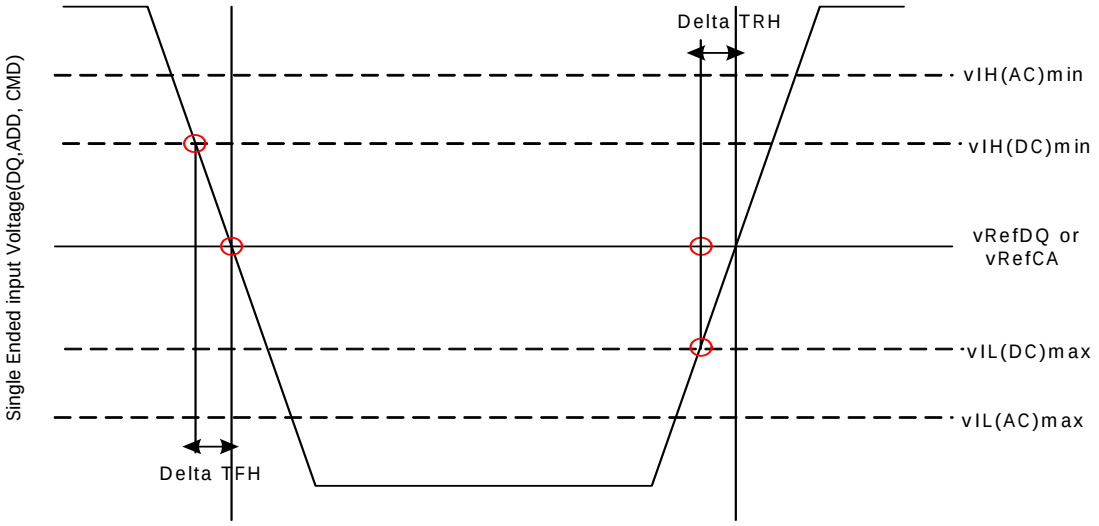
Description	Measured		Defined by	Applicable for
	Min	Max		
Input slew rate for rising edge	Vref	VIH(AC)min	$\frac{\text{VIH(AC)min-Vref}}{\text{Delta TRS}}$	Setup (tIS, tDS)
Input slew rate for falling edge	Vref	VIL(AC)max	$\frac{\text{Vref-VIL(AC)max}}{\text{Delta TFS}}$	
Input slew rate for rising edge	VIL(DC)max	Vref	$\frac{\text{Vref-VIL(DC)max}}{\text{Delta TFH}}$	Hold (tIH, tDH)
Input slew rate for falling edge	VIH(DC)min	Vref	$\frac{\text{VIH(DC)min-Vref}}{\text{Delta TRH}}$	

< Table 6.3.1: Single-Ended Input Slew Rate Definition >

Part A: Set up



Part B: Hold



< Figure 6.3.1: Input Nominal Slew Rate Definition for Single-Ended Signals >

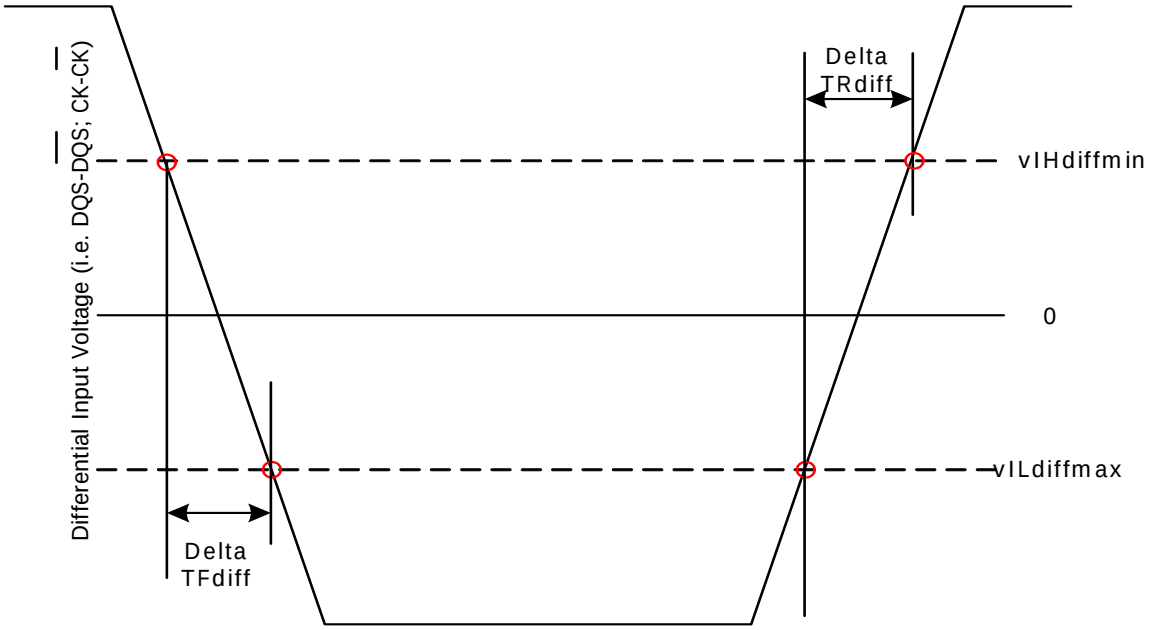
6.3.2 Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in below Table and Figure .

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-CK and DQS-DQS)	VILdiffmax	VIHdiffmin	$\frac{\text{VIHdiffmin-VILdiffmax}}{\overline{\text{DeltaTRdiff}}}$
Differential input slew rate for falling edge (CK-CK and DQS-DQS)	VIHdiffmin	VILdiffmax	$\frac{\text{VIHdiffmin-VILdiffmax}}{\overline{\text{DeltaTFdiff}}}$

Note:

The differential signal (i.e. CK-CK and DQS-DQS) must be linear between these thresholds.



< Figure 6.3.2: Differential Input Slew Rate Definition for DQS,DQS# and CK,CK# >

6.4 DC & AC Output Buffer Levels

6.4.1 Single Ended DC & AC Output Levels

Below table shows the output levels used for measurements of single ended signals.

Symbol	Parameter	DDR3-800, 1066, 1333	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

1. The swing of ± 0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ / 2.

6.4.2 Differential DC & AC Output Levels

Below table shows the output levels used for measurements of differential signals.

Symbol	Parameter	DDR3-800, 1066, 1333	Unit	Notes
VOHdiff (AC)	AC differential output high measurement level (for output SR)	+ 0.2 x VDDQ	V	1
VOLdiff (AC)	AC differential output low measurement level (for output SR)	- 0.2 x VDDQ	V	1

1. The swing of °æ 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swingwith a driver impedance of 40ßŸ and an effective test load of 25ßŸ to VTT = VDDQ/2 at each of the differential output

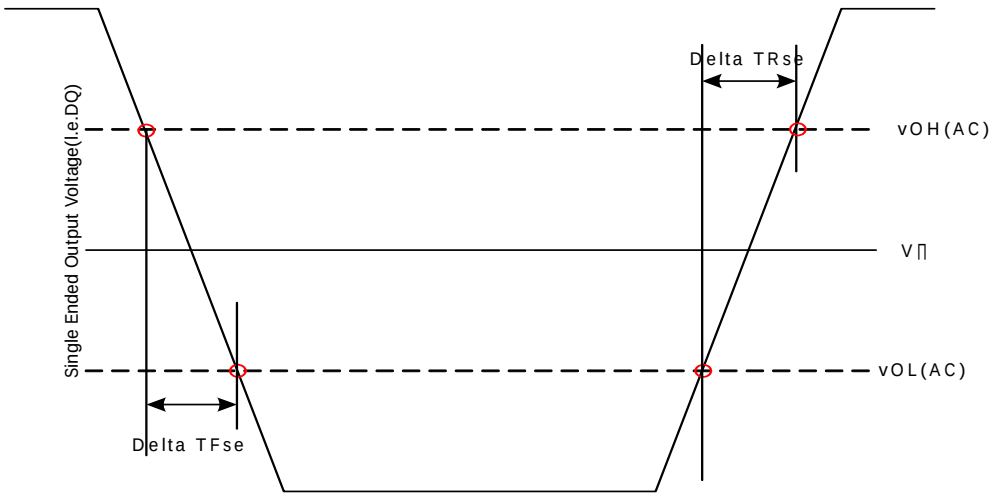
6.4.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below Table and Figure 6.4.3.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{\overline{DeltaTRse}}$
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{VOH(AC)-VOL(AC)}{\overline{DeltaTFse}}$

Note:

Output slew rate is verified by design and characterization, and may not be subject to production test.



< Figure 6.4.3: Single Ended Output Slew Rate Definition >

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	V/ns

***** Description:**
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
For Ron = RZQ/7 setting

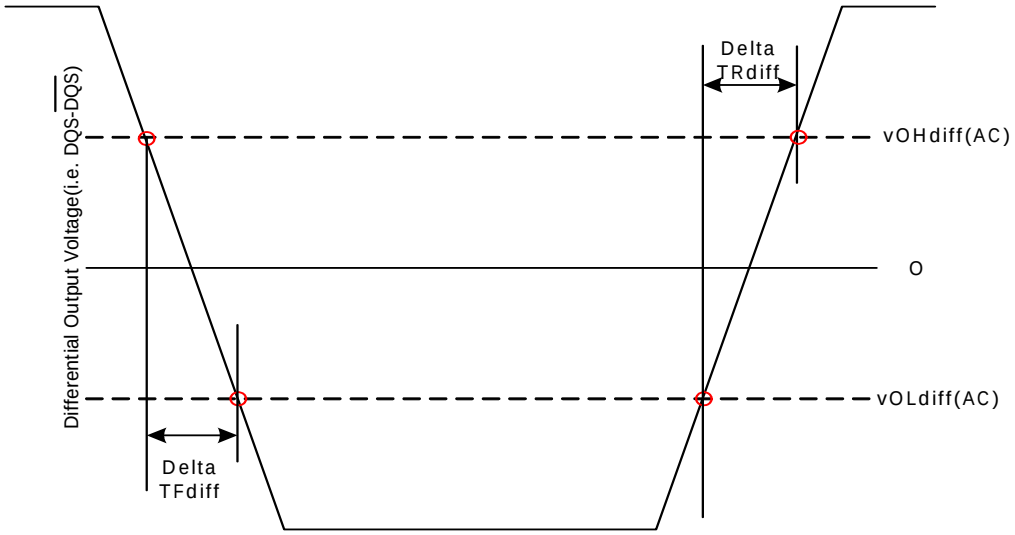
< Table 6.4.3: Output Slew Rate (single-ended) >

6.4.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in below Table and Figure 6.4.4

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / DeltaTFdiff

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.



< Figure 6.4.4: Differential Output Slew Rate Definition >

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	V/ns

*****Description:**
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

< Table 6.6.4: Differential Output Slew Rate >

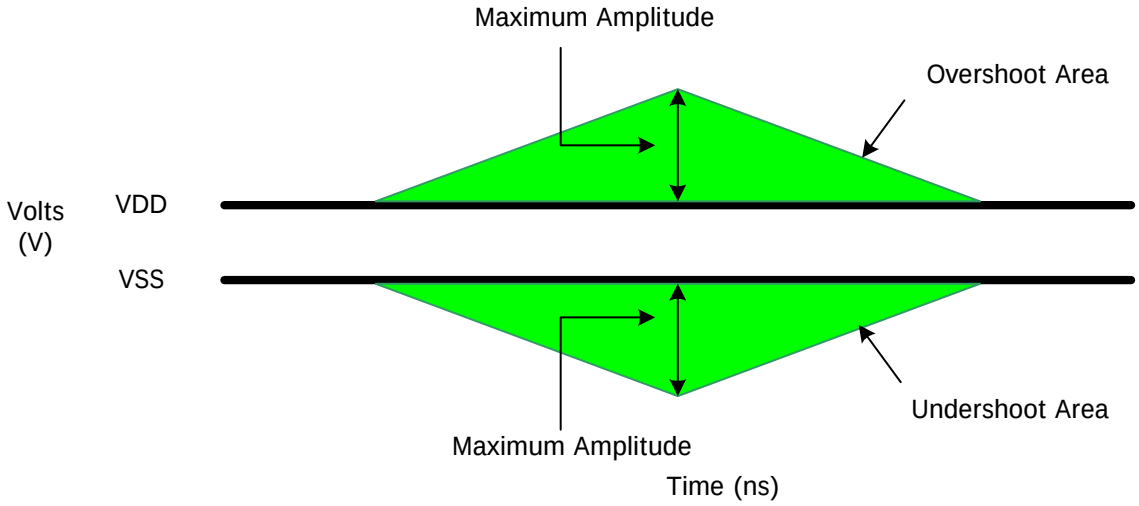
6.5 Overshoot and Undershoot Specifications

6.5.1 Address and Control Overshoot and Undershoot Specifications

Description	Specification		
	DDR3-800	DDR3-1066	DDR3-1333
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns
Maximum undershoot area below VSS (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns

< Table 6.5.1: AC Overshoot/Undershoot Specification for Address and Control Pins >

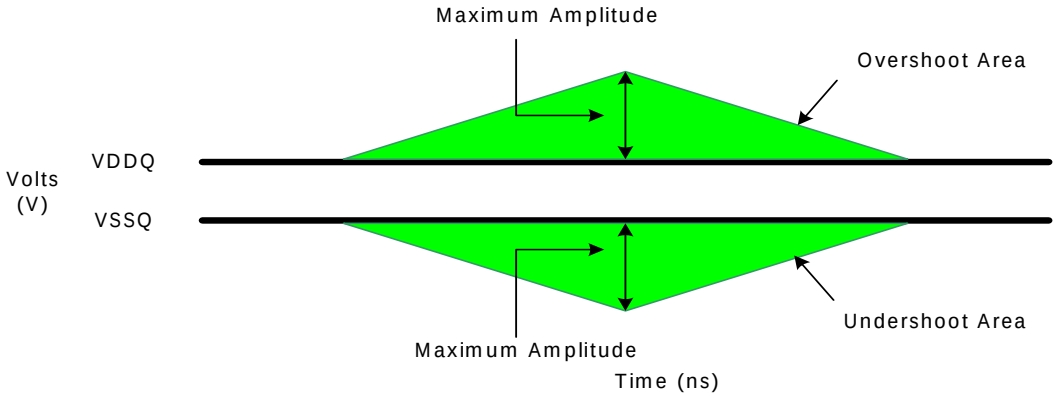
< Figure 6.5.1: Address and Control Overshoot and Undershoot Definition >



6.5.2 Clock,Data,Strobe and Mask Overshoot and Undershoot Specifications

Description	Specification		
	DDR3-800	DDR3-1066	DDR3-1333
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V
Maximum overshoot area above VDDQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns
Maximum undershoot area below VSSQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns

< Table 6.5.2: AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask >



Clock, Data Strobe and Mask Overshoot and Undershoot Definition

< Figure 6.5.2: Clock, Data, Strobe and Mask Overshoot and Undershoot Definition >

6.6 Pin Capacitance

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS, TDQS#)	C_{IO}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2,3
Input capacitance, CK and CK#	C_{CK}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,5
Input capacitance delta CK and CK#	C_{DCK}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,4
Input capacitance (All other input-only pins)	C_{I}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,6
Input capacitance delta, DQS and DQS#	C_{DDQS}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,12
Input capacitance delta (All CTRL input-only pins)	C_{DI_CTRL}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,9, 10
Input/output capacitance delta (DQ, DM, DQS, DQS#)	C_{DIO}	TBD	TBD	TBD	TBD	TBD	TBD	pF	2,3,11

Notes:

1. TDQS/TDQS# are not necessarily input function but since TDQS is sharing DM pin and the parasitic characterization of TDQS/TDQS# should be close as much as possible, Cio&Cdio requirement is applied (recommend deleting note or changing to “Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.”)
2. This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147(“PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)”) with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-C_{CK}#.
5. The minimum C_{CK} will be equal to the minimum C_{I}.
6. Input only pins include: ODT, CS, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. CTRL pins defined as ODT, CS and CKE.
8. $C_{DI\_CTRL}=C_{I}(CNTL) - 0.5 * C_{I}(CLK) + C_{I}(CLK\#))$
9. ADD pins defined as A0-A15, BA0-BA2 and CMD pins are defined as RAS#, CAS# and WE#.
10. $C_{DI\_ADD\_CMD}=C_{I}(ADD\_CMD) - 0.5*(C_{I}(CLK)+C_{I}(CLK\#))$
11. $C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS\#))$
12. Absolute value of $C_{IO}(DQS) - C_{IO}(DQS\#)$

6.7 IDD Specifications(T_{CASE}: 0 to 95°C)

4GB, 512M x 64 U-DIMM: HMT351U6MFR8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	1152	1376	1552	mA	
IDD1	1320	1536	1704	mA	
IDD2N	848	1072	1232	mA	
IDD2NT	864	1104	1264	mA	
IDDQ2NT	1232	1264	1248	mA	
IDD2P0	208	208	208	mA	
IDD2P1	400	528	560	mA	
IDD2Q	832	1056	1200	mA	
IDD3N	912	1152	1328	mA	
IDD3P	512	672	752	mA	
IDD4R	1680	2096	2456	mA	
IDDQ4R	920	1048	1136	mA	
IDD4W	1456	1856	2176	mA	
IDD5B	2488	2704	2864	mA	
IDD6	192	192	192	mA	
IDD6ET	192	192	192	mA	
IDD6TC	192	192	192	mA	
IDD7	2560	2888	3472	mA	

4GB, 512M x 72 U-DIMM: HMT351U7MFR8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	1296	1548	1746	mA	
IDD1	1485	1728	1917	mA	
IDD2N	954	1206	1386	mA	
IDD2NT	972	1242	1422	mA	
IDDQ2NT	1386	1422	1404	mA	
IDD2P0	234	234	234	mA	
IDD2P1	450	594	630	mA	
IDD2Q	936	1188	1350	mA	
IDD3N	1026	1296	1494	mA	
IDD3P	576	756	846	mA	
IDD4R	1890	2358	2763	mA	
IDDQ4R	1035	1179	1278	mA	
IDD4W	1638	2088	2448	mA	
IDD5B	2799	3042	3222	mA	
IDD6	216	216	216	mA	
IDD6ET	216	216	216	mA	
IDD6TC	216	216	216	mA	
IDD7	2880	3249	3906	mA	

6.7 IDD Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(max)}$.
- “FLOATING” is defined as inputs are VREF - VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1 on Page 26.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2 on page 26.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 on page 30 through Table 10 on page 36.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}
- Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}

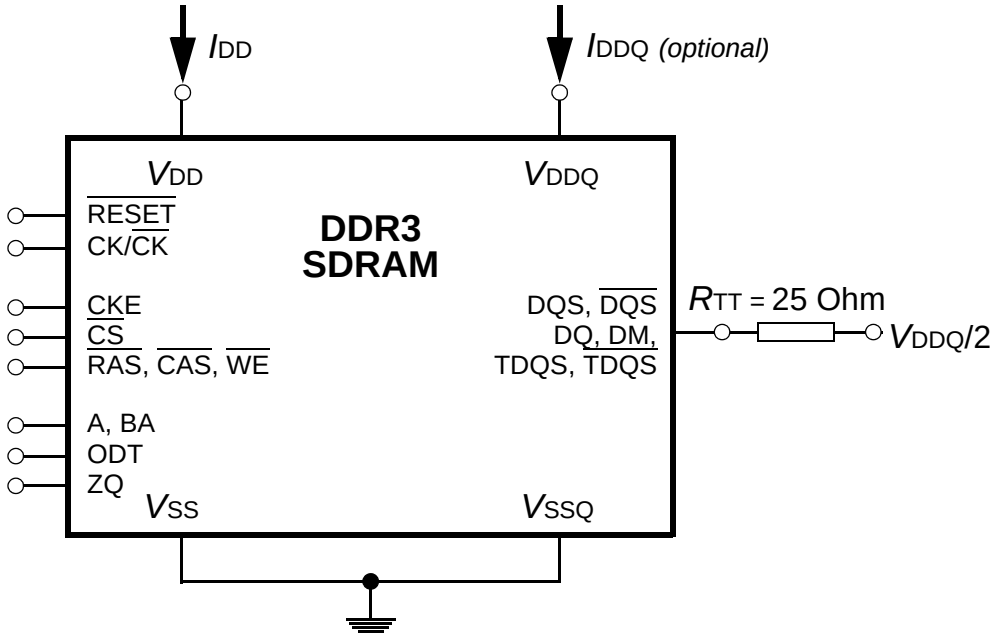


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements [Note: DIMM level Output test load condition may be different from above]

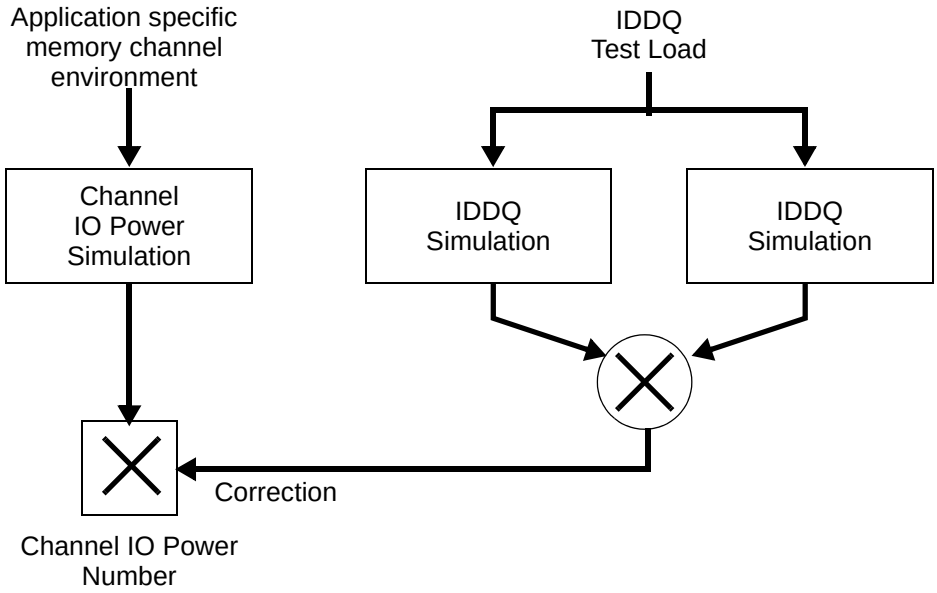


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3-800	DDR3-1066	DDR3-1333	Unit
		5-5-5	7-7-7	9-9-9	
t_{CK}		2.5	1.875	1.5	ns
CL		5	7	9	nCK
n_{RCD}		5	7	9	nCK
n_{RC}		20	27	33	nCK
n_{RAS}		15	20	24	nCK
n_{RP}		5	7	9	nCK
n_{FAW}	x4/x8	16	20	20	nCK
	x16	20	27	30	nCK
n_{RRD}	x4/x8	4	4	4	nCK
	x16	4	6	5	nCK
n_{RFC} -512Mb		36	48	60	nCK
n_{RFC}-1 Gb		44	59	74	nCK
n_{RFC}- 2 Gb		64	86	107	nCK
n_{RFC}- 4 Gb		120	160	200	nCK
n_{RFC}- 8 Gb		140	187	234	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3 on page 30; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3 on page 30); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 3 on page 30
I_{DD1}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4 on page 31; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4 on page 31); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 4 page 31

I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5 on page 32; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5 on page 32
I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6 on page 32; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: toggling according to Table 6 on page 32; Pattern Details: see Table 6 on page 32
I_{DDQ2NT} (optional)	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DDQ4R} (optional)	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current

I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5 on page 32; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5 on page 32
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7 on page 33; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7 on page 33; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7 on page 33); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 7 on page 33
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8 on page 34; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8 on page 34; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8 on page 34); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at HIGH; Pattern Details: see Table 8 on page 34
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9 on page 35; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9 on page 35); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 9 on page 35

I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range (optional)[f] T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Extended[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING
I_{DD6TC}	Auto Self-Refresh Current (optional)[f] T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Enabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING
I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1 on page 26; BL: 8[a]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10 on page 36; Data IO: read data burst with different data between one burst and the next one according to Table 10 on page 36; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, wee Table 10 on page 36; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 10 on page 36

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit
d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range
f) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	00	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 4 - IDD1 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	00000000
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 7 - IDD4R and IDDQ24RMeasurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are FLOATING.

Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
			...	Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
			...	Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	0	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		14	3*nFAW+4*nRRD	D	1	0	0	0	0	0	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

7. Electrical Characteristics and AC Timing

7.1 Refresh Parameters by Device Density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units
REF command to ACT or REF command time	tRFC		90	110	160	300	350	ns
Average periodic refresh interval	tREFI	0 ×C < T_{CASE} < 85 ×C	7.8	7.8	7.8	7.8	7.8	ms
		85 ×C < T_{CASE} < 95 ×C	3.9	3.9	3.9	3.9	3.9	ms

7.2 DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin

DDR3 800 Speed Bin			DDR3-800E		Unit	Notes
CL - nRCD - nRP			6-6-6			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	—	ns	
PRE command period		t_{RP}	15	—	ns	
ACT to ACT or REF command period		t_{RC}	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1)2)3)
Supported CL Settings			6		n_{CK}	
Supported CWL Settings			5		n_{CK}	

DDR3 1066 Speed Bin			DDR3-1066F		Unit	Note
CL - nRCD - nRP			7-7-7			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.125	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.125	—	ns	
PRE command period		t_{RP}	13.125	—	ns	
ACT to ACT or REF command period		t_{RC}	50.625	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1)2)3)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1)2)3)4)
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1)2)3)
Supported CL Settings			6, 7, 8		n_{CK}	
Supported CWL Settings			5, 6		n_{CK}	

DDR3 1333 Speed Bin			DDR3-1333H		Unit	Note
CL - nRCD - nRP			9-9-9			
Parameter		Symbol	min	max		
Internal read command to first		t_{AA}	13.125	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.125	—	ns	
PRE command period		t_{RP}	13.125	—	ns	
ACT to ACT or REF command period		t_{RC}	49.125	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings			6, 7, 8, 9		n_{CK}	
Supported CWL Settings			5, 6, 7		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

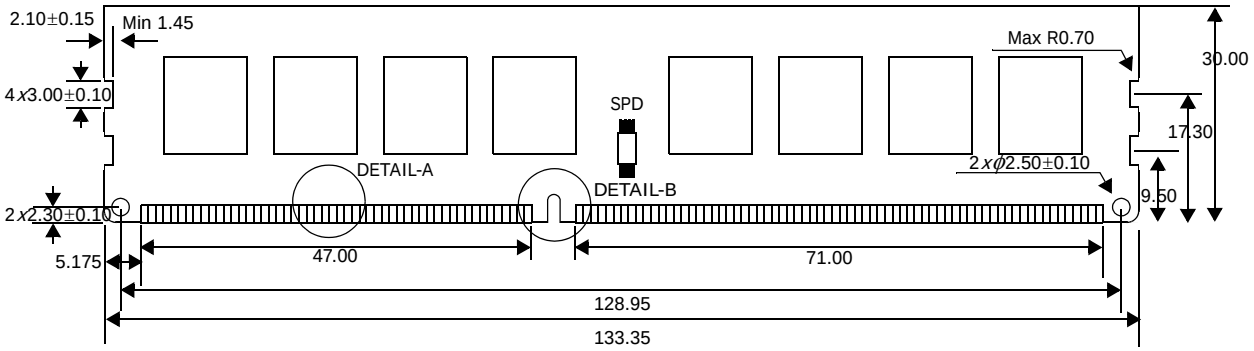
Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CLSELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

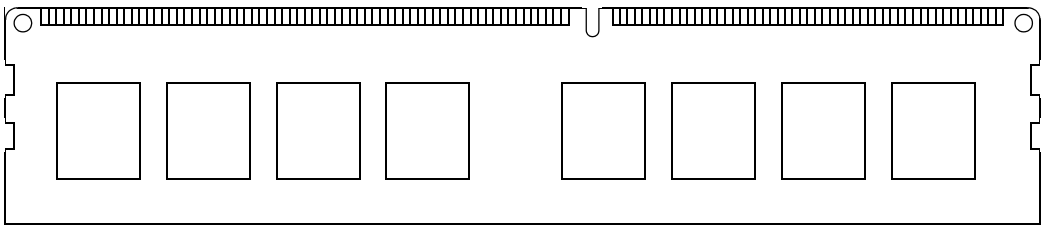
8. Dimm Outline Diagram

8.1 512Mx64 - HMT351U6MFR8C

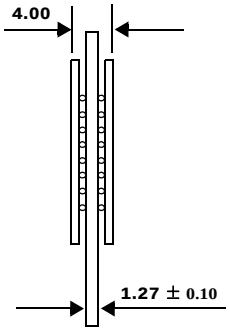
Front



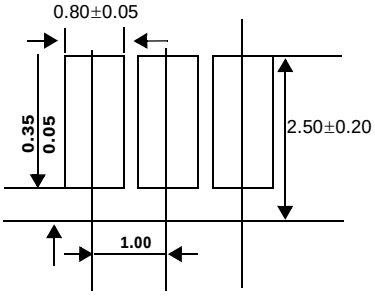
Back



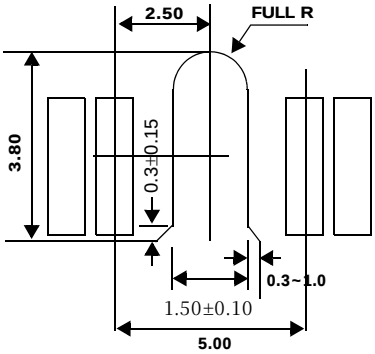
Side



Detail - A



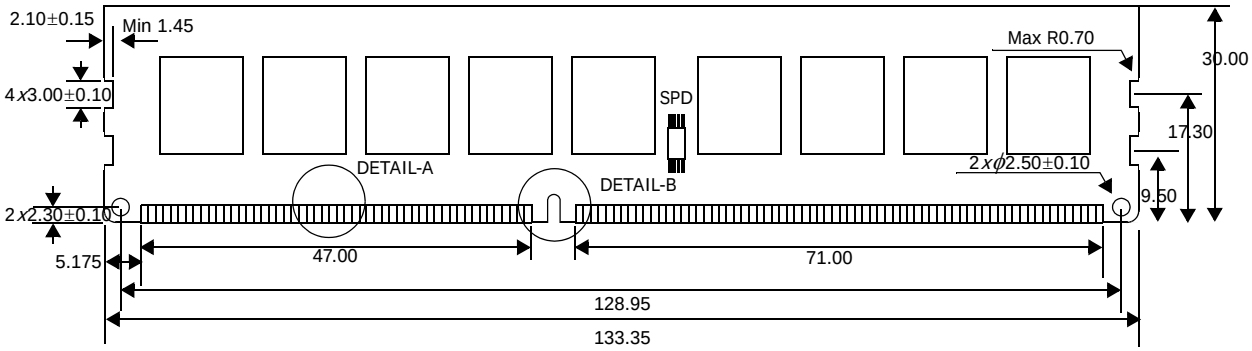
Detail - B



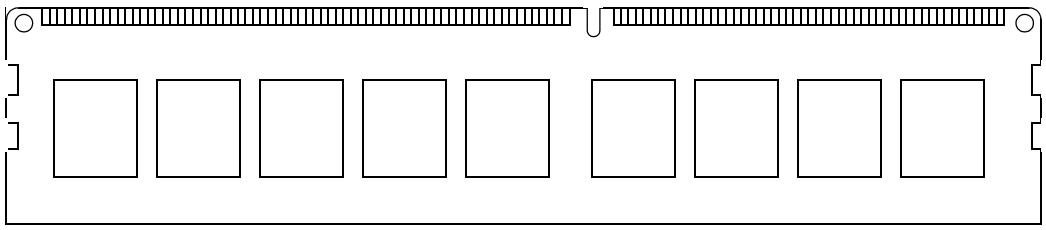
Note) All dimensions are in millimeters unless otherwise stated.

8.2 512Mx72 - HMT351U7MFR8C

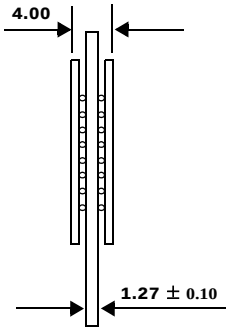
Front



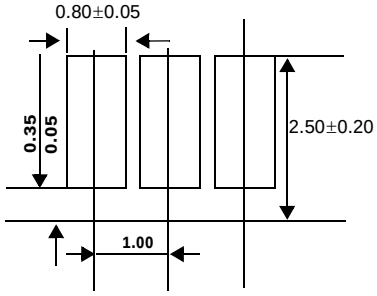
Back



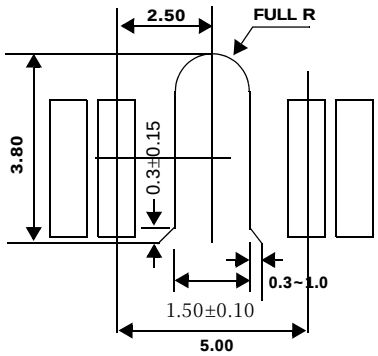
Side



Detail - A



Detail - B



Note) All dimensions are in millimeters unless otherwise stated.