11-MD118B

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8-BIT DAC VCM Driver with I^2C Interface

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11-MD118B

8-Bit DAC VCM Driver with I²C Interface

General Specifications

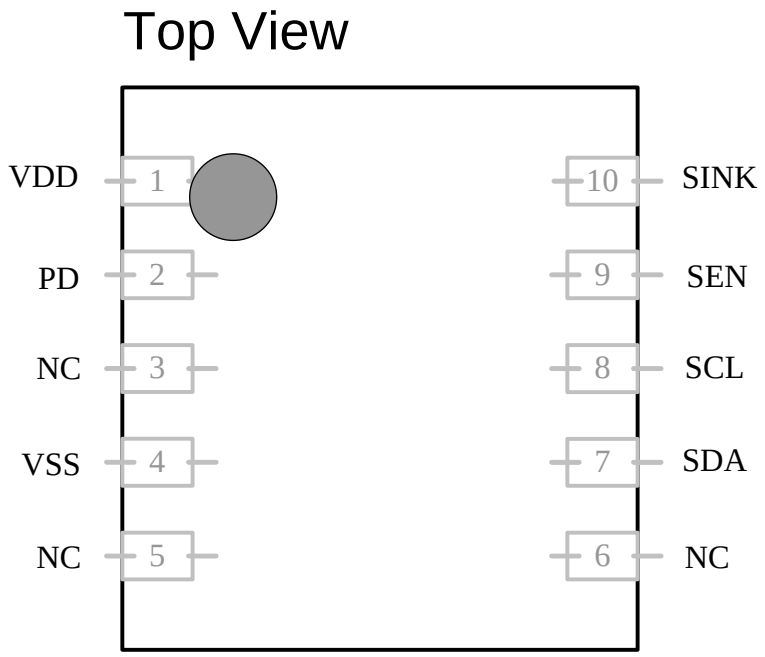
The 11-MD118B is a VCM driver IC with I²C interface control that is capable of programmable output current sinking. It has a built-in internal voltage reference and operates in a wide supply voltage range from 2.4V to 5.5V. The DAC is controlled by a 2-wire I²C serial interface which operates in I²C fast mode (400 kHz). The 11-MD118B is designed for applications like image stabilization, auto-focus, and optical zoom in camera phones, digital still cameras, and other portable module devices.

Features and Benefits

- Programmable output current sinking
- I²C serial interface
- 8-BIT DAC resolution
- 2.4V – 5.5V power supply
- Low voltage control for digital pin (PD, SDA, SCL)
- Power down operation
- Power on reset
- Constant current control
- Ultra small package: WLCSP1(0.84*1.84*0.5 mm), WLCSP2(1.0*2.0*0.45 mm) and DFN10 (3*3*0.8 mm)

Pin Assignment

Pin Assignment of DFN10 (3*3*0.8 mm)



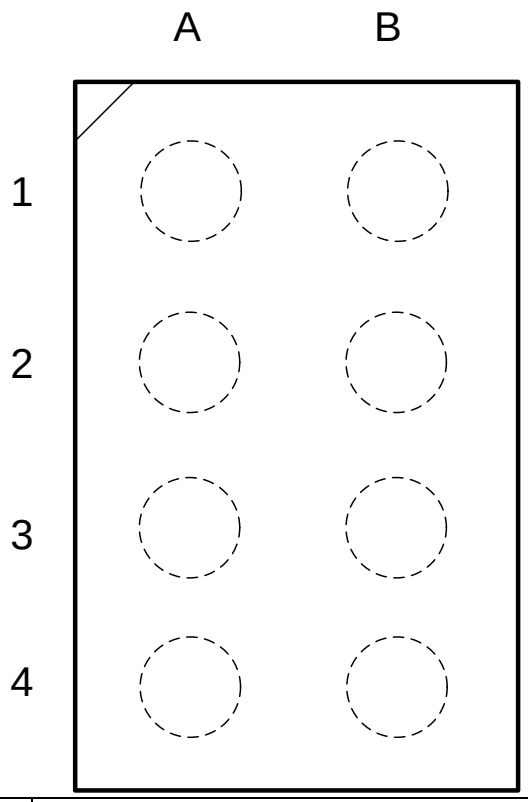
Pin Descriptions

Pin NO.	Pin Name	Description
1	VDD	Power Supply Pin
2	PD	Digital Input: Power Down Mode(High power down, Low operation)
3	NC	
4	VSS	Ground Pin
5	NC	
6	NC	
7	SDA	I^2C Interface Data
8	SCL	I^2C Interface Data
9	SEN	Analog Output : Programmable FSR Current Sinking
10	SINK	Analog Output : Output Current Sink

1. The I^2C slave 7-bit address of 11-MD118B is 0001-1xx.

Pin Assignment of WLCSP1 (0.84*1.84*0.5mm)

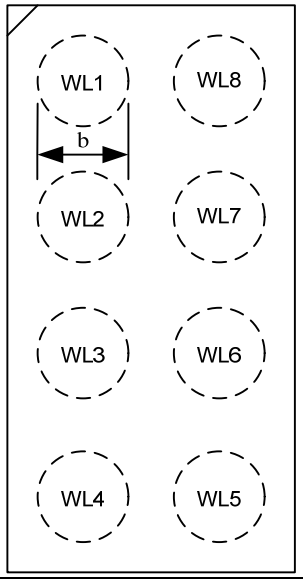
TOP View



Pin NO.	Pin Name	Description
A1	SEN	Analog Output : Programmable FSR Current Sinking
A2	PD	Digital Input: Power Down Mode(Logic 'H': power down)
A3	SDA	I^2C Interface Data
A4	SCL	I^2C Interface Data
B4	VSS	Ground Pin
B3	VSS	Ground Pin
B2	SINK	Analog Output : Output Current Sink
B1	VDD	IC Power Pin

Pin Assignment of WLCSP2 (1.0*2.0*0.45mm)

TOP View



Pin NO.	Pin Name	Description
WL1	SEN	Analog Output : Programmable FSR Current Sinking
WL2	PD	Digital Input: Power Down Mode(Logic 'H': power down)
WL3	SDA	I^2C Interface Data
WL4	SCL	I^2C Interface Data
WL5	VSS	Ground Pin
WL6	VSS	Ground Pin
WL7	VDD	Power Supply Pin
WL8	SINK	Analog Output : Output Current Sink

Absolute Maximum Ratings

Unless otherwise noted, T_A= 25℃

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{DD}	5.5	V
Input Voltage	V_{IN}	V_{DD}+0.4	V
Maximum Output Current	I_{OUT}	130	mA
Operating Temperature Range	T_{OPR}	-40 ~ 125	°C
Storage Temperature Range	T_{STG}	-65 ~ 150	°C

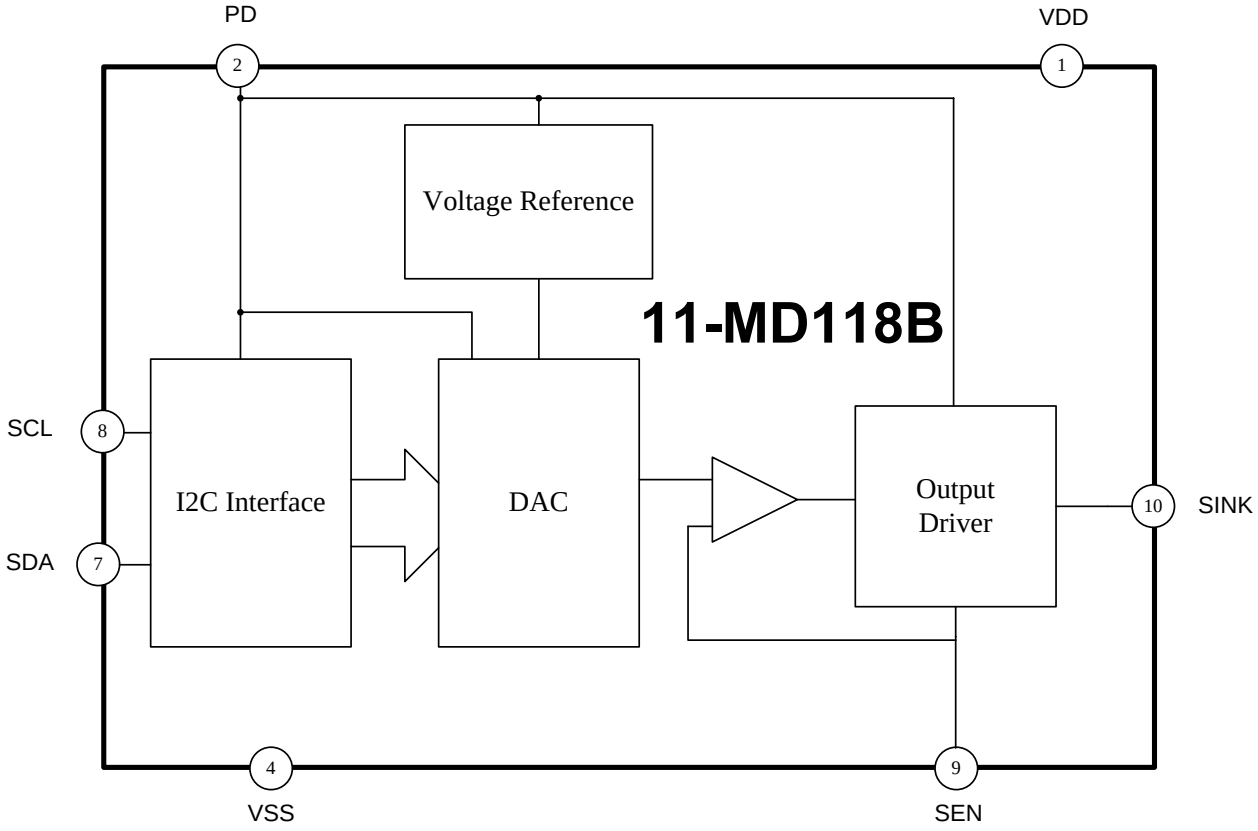
Electrical Characteristic

Unless otherwise noted, T_A= 25℃, V_{DD} = 2.8 V and VCM loading = 28.5Ω

Item	Sym.	Condition	Limit			Unit
			Min.	Typ.	Max.	
Power Supply						
Supply Voltage	V_{DD}		2.4	2.8	5.5	V
Supply Current (I_{DD})	I_{PD}	PD = H (Power down mode)	-	-	±0.5	uA
	I_{DD}	PD = L (Operation mode)	-	3.5	4	mA
PD, SDA, SCL digital control pin						
Input Voltage “H”	V_{IH}	-	0.6*V_{DD}	-	V_{DD}+0.4	V
Input Voltage “L”	V_{IL}	-	-0.4	-	0.2*V_{DD}	V
Parameters						
Resolution				8		Bits
INL				±0.8	±1	LSB
DNL				±0.8	±1	LSB
Zero Code Error	I_{OS}	@ **R_{SEN}** = 3.3 Ω		5	7	mA
Full Scale Voltage	V_{FSR}	Voltage on the **SEN** Pin	360	380	400	mV
Least Significant Bit	LSB	@ **R_{SEN}** = 3.3 Ω	0.42	0.44	0.46	mA
Output Current Settling Time	t_s	VDD = 2.8V, C_L=1 μF , @ **R_{SEN}** = 3.3 Ω, VCM(28.5 Ω, 460 μH)		120	200	μs
Saturation Voltage	V_{SAT}	I_{OUT} = 120 mA	-	0.1	0.15	V

Block Diagram

(DFN10)



Terminology

Resolution

The DAC resolution is defined by the number of distinct analog levels corresponding to the number of bits it uses.

N-bit resolution -> 2^N distinct analog levels

Differential Nonlinearity (DNL) error

The variation in analog step sizes away from 1 LSB by any two adjacent codes. Usually, gain and offset errors have been removed.

Integral Nonlinearity (INL)

It is the deviation of actual transfer response from a straight line. Usually, INL error is referred to as the maximum INL error.

Zero-Code Error

Zero-Code error is the output error as the bits ‘0000-0000-00’ are loaded into DAC register.

Full Scale Voltage

Full scale voltage is the maximum output voltage of the I^2C DAC (**SEN** pin) as the bits ‘1111-1111-00’ are loaded into 11-MD118B.

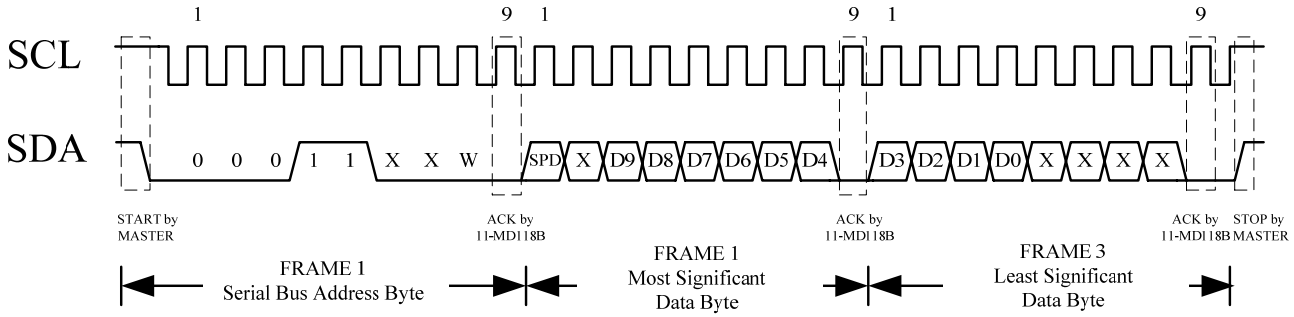
Sink Current

Sink Current is the input current driven by the power MOS embedded in the 11-MD118B.

Data Format

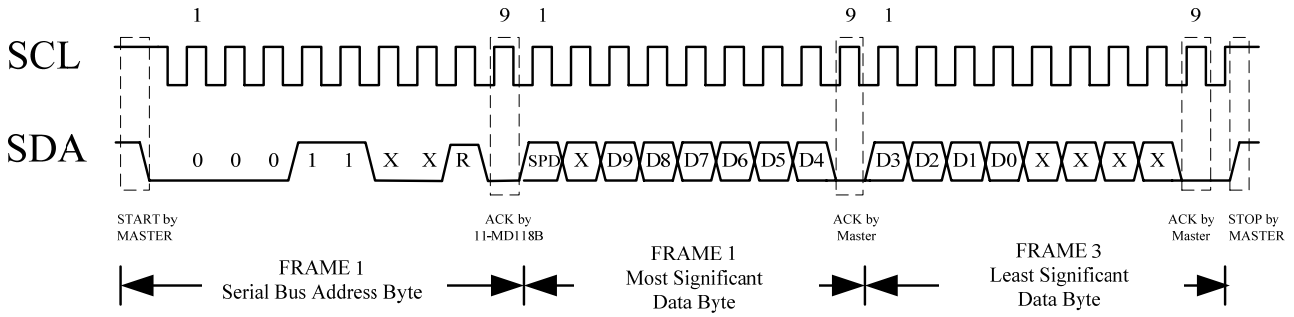
11-MD118B Write Mode

When in the write mode, data is written to the 11-MD118B and shifted step-by-step into the 16-bit input register. When all data has been loaded in and master signal receives a STOP condition, the loaded data in the input register is transferred to the DAC.



11-MD118B Read Mode

When 11-MD118B is in the write mode, data is read back from IC to master in the same bit order.



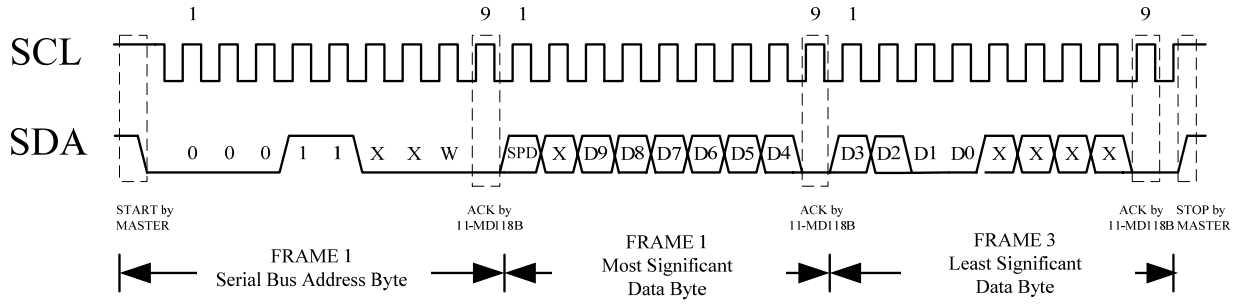
Table

	MSB								LSB							
Serial Data Bits	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Input Register	R15	R14	R13	R12	R11	R10	R09	R08	R07	R06	R05	R04	R03	R02	R01	R00
Function	SPD	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

- SPD (Soft Power Down, 2nd standby mode): L denotes IC active, and H just reset the DAC registers (D9~D0 -> 0) without shutdown any analog cell for reducing recovery time consideration. Regarding to all kinds of IC operation situations please refers to following table.

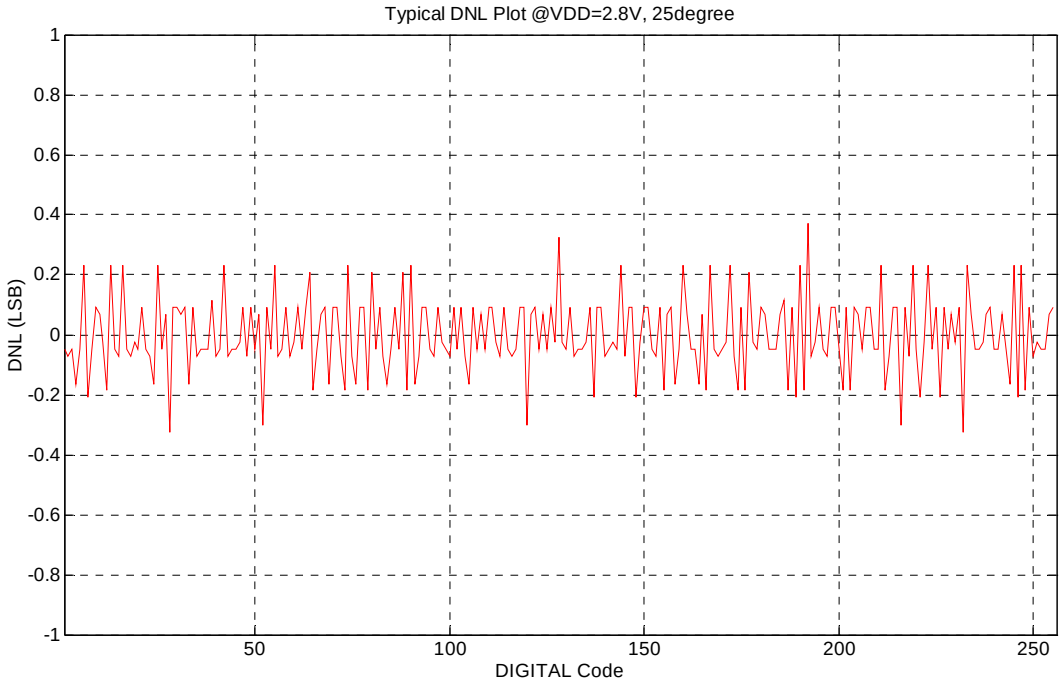
PD	SPD	IC status
H	-	Power down
L	L	IC Active
	H	Soft power down

- X denotes “Don’t care/Unused”.
- D9, D0 denote MSB and LSB of DAC, respectively.
- D(n), n = 2~9, are for 8-bit DAC data programming while D1 and D0 are forced to logic 0 assignment in order to guarantee 8-bit DAC resolution. The diagram shows the example of write mode.

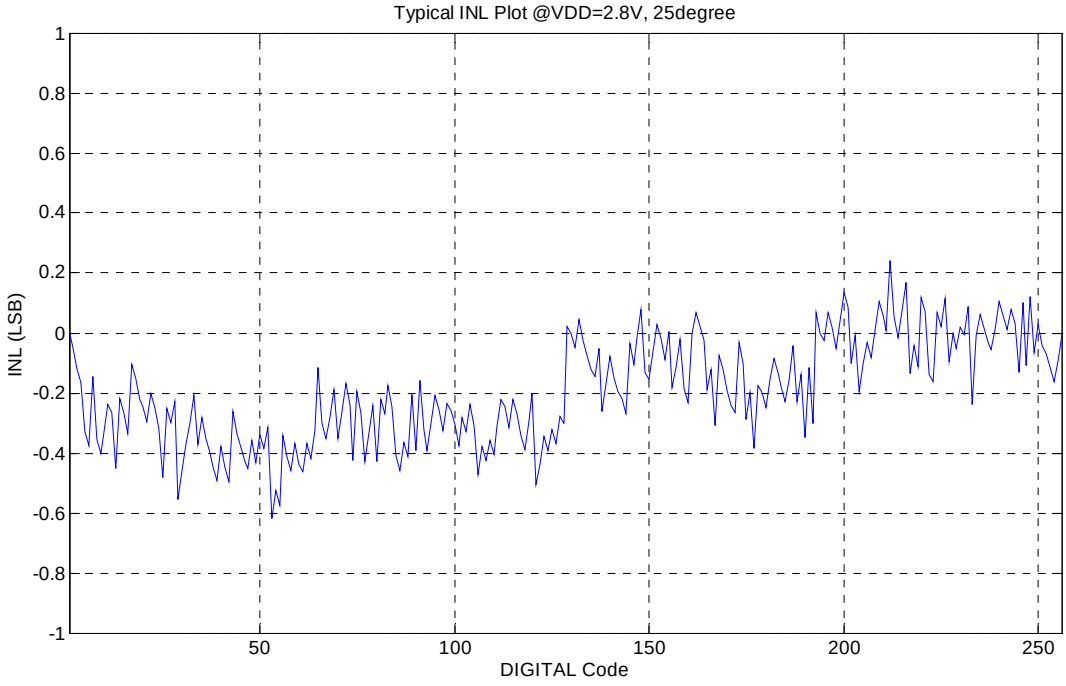


Performance Characteristic

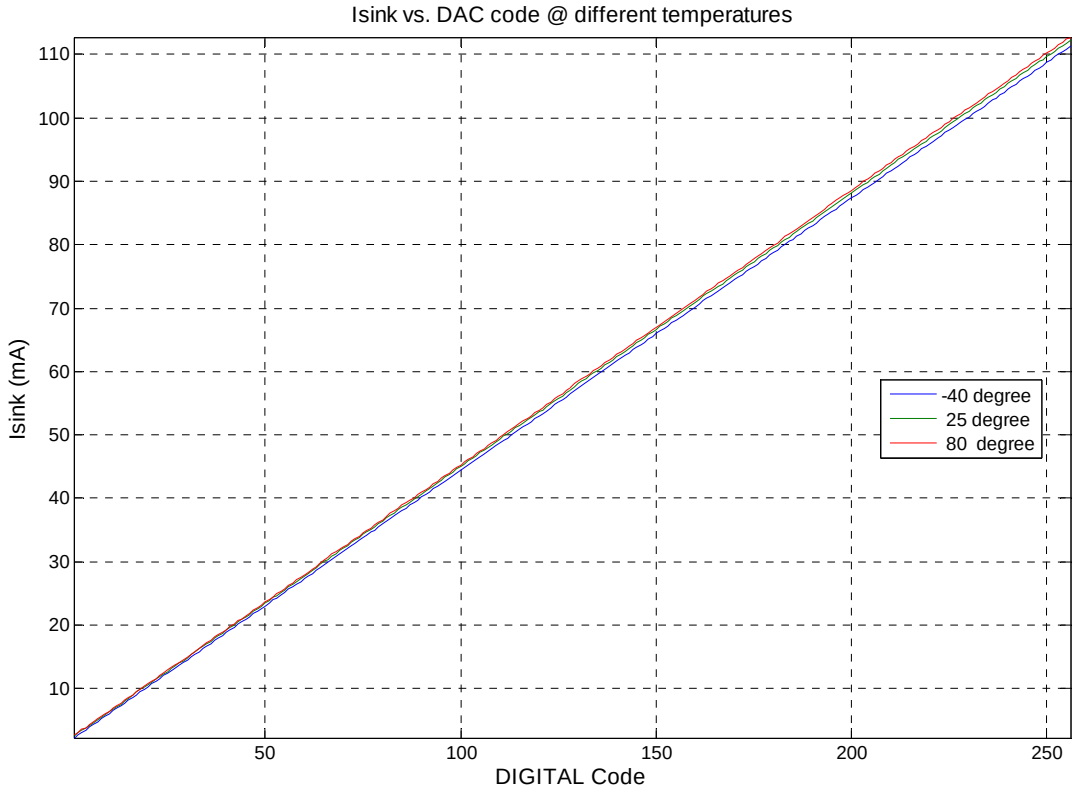
1. Typical DNL Plot



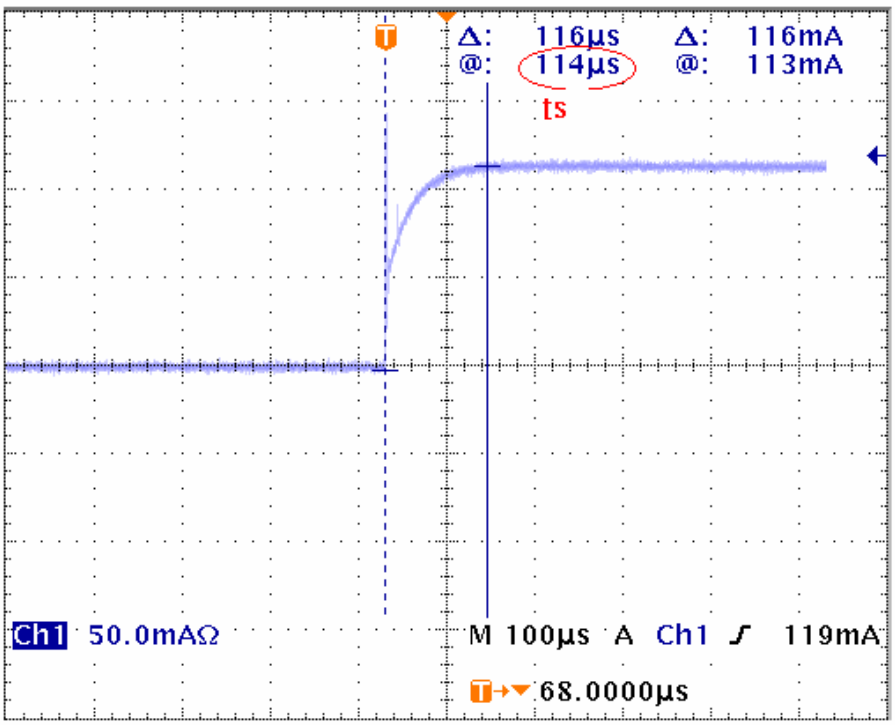
2. Typical INL Plot



3. Output Sink Current Plot

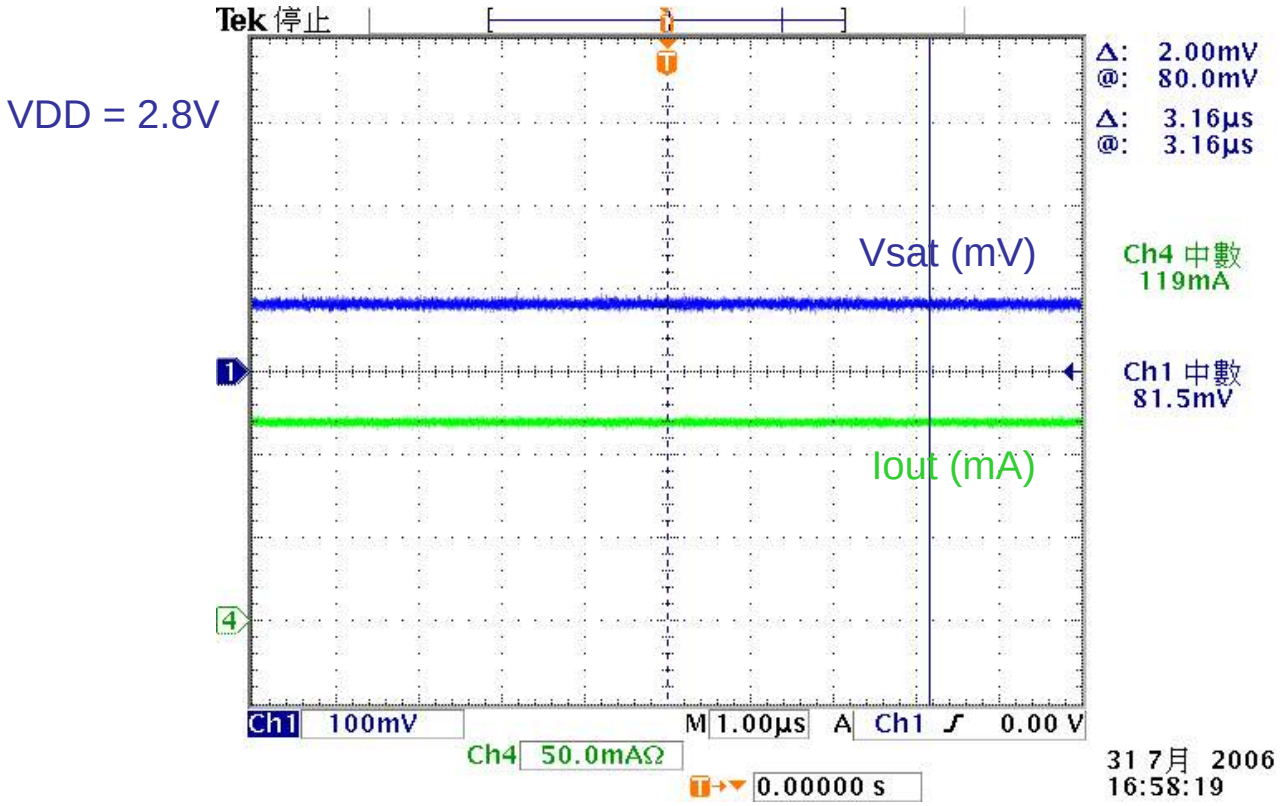


4. Maximum Settling Time (Which is current of SINK, I_{SINK}, from 0 to maximum constant current)

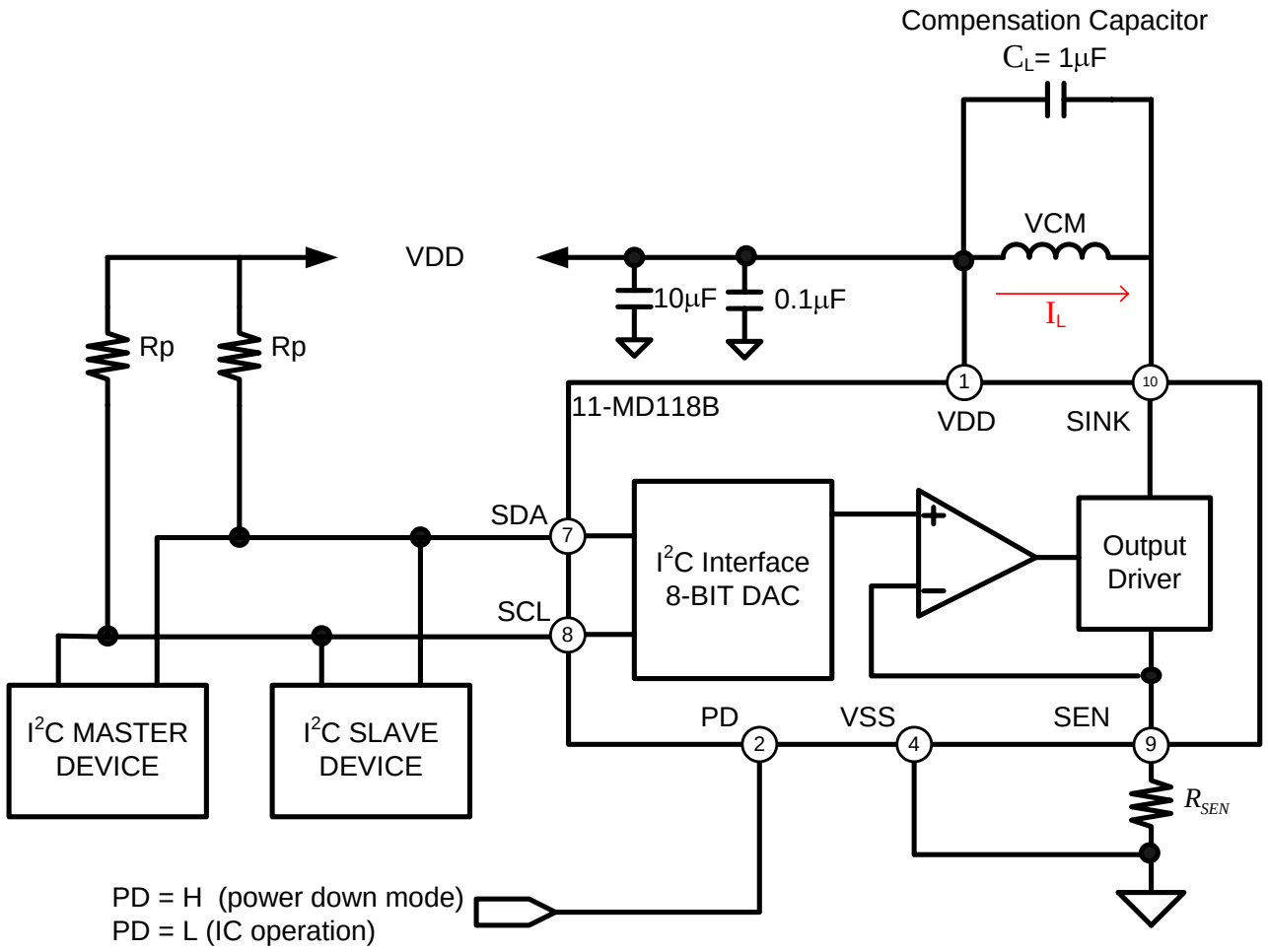


5. Saturation voltage (I_{SINK}@120mA)

11-MD118B



Application Circuit



The Least Significant Bit (**LSB**) driving current of Voice Coil Actuator is determined by **R_{SEN}**.

For example, R_{SEN}= 3.3Ω.

The Full Scale Voltage (**V_{FSR}**) of **SEN** is 365mV and the Zero Code Error (**I_{OS}**) is 5mA.

The LSB driving current of Voice Coil Actuator is

$$LSB = \frac{V_{FSR} - V_{OS}}{255 * R_{SEN}} = \frac{365mV - 5mA*3.3}{255 * 3.3} \cong 414\ \mu A$$

.

If input digital code is 0111-1111-00 (D9~D2 can be programmable, and D1~D0 are forced to logic 0).

The driving current of Voice Coil Actuator (I_L) is

$$I_L = I_{OS} + code * LSB = 5mA + 127 * 414uA \cong 57.6mA$$

Application Notes

- The 11-MD118B is a constant current control IC for application in Auto-Focus. The supply voltage range VDD of 11-MD118B is from 2.4V to 5.5V. The input range of digital control pin PD, and digital I/O pins SCL and SDA, are defined such that logic “H” is from 0.6*VDD to VDD+0.4V and logic “L” is from –0.4V to 0.2*VDD.

- The PD pin is the power down pin of 11-MD118B. Logic low level (PD = L) is for IC operation. On the other hand, its logic high level (PD = H) puts the chip into power down mode for power saving. It is recommended to keep PD at high level (PD = H) before operation to reach the maximum efficiency of power saving, especially for applications in portable devices.

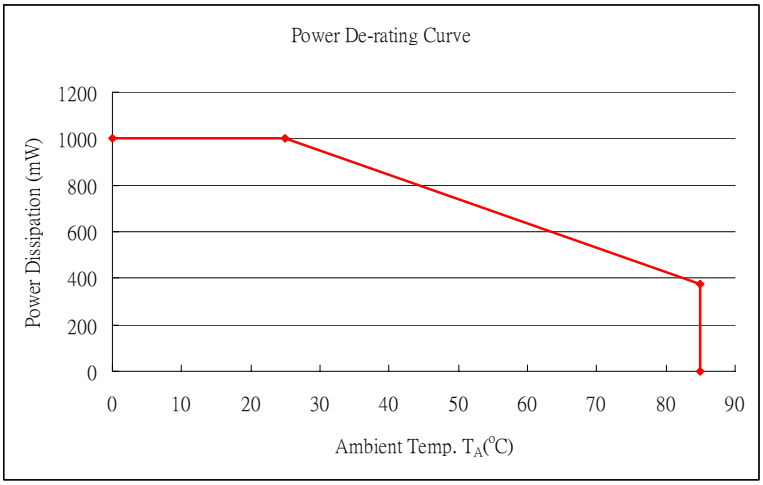
- In order to ensure the stability of output current, a compensation capacitance C_L is suggested to be placed across the two terminals of VCM. The suggested value of C_L is about 1uF and could be fine tuned for different VCM. The idea is to use frequency response compensation to ensure stability when VCM is operating.

- In order to guarantee 8-bit DAC resolution, DAC data, D1 and D0 are set to logic 0 only. There are 8-bit DAC data, D9~D2, are used for VCM constant current control via the two I^2C serial data lines, SCL and SDA. If all 10 bits are used for DAC programming in an attempt to reach 10-bit DAC resolution, the DNL might get larger than 1 LSB due to glitch effect. In order to guarantee output current monotonically increases as the DAC code increases, it is suggested to utilize only 8-bit data programming to reach a better performance.

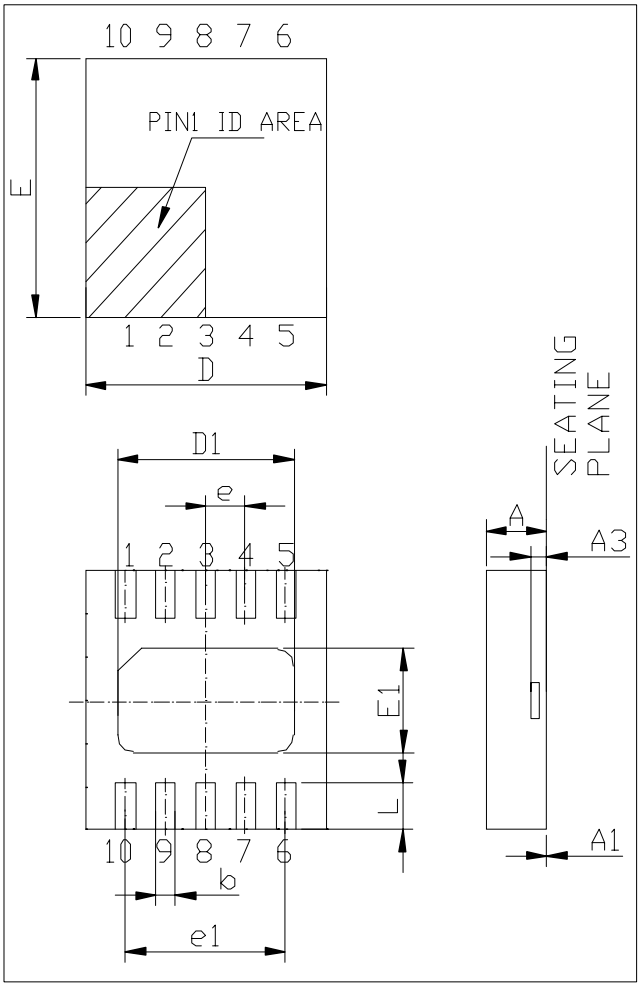
- The exposed paddle on the 11-MD118B should be soldered to ground to ensure the optimal thermal dissipation performance.

- IC packaging(WLCSP2) Power Dissipation

The power consumption of IC varies widely with supply voltage, output current, and actuator loading. It is important to ensure the application does not exceed the allowable power dissipation of the IC package. The recommended Power De-rating Curve, power dissipation versus ambient temperature is depicted as follows. The work is done under JEDEC51-9.



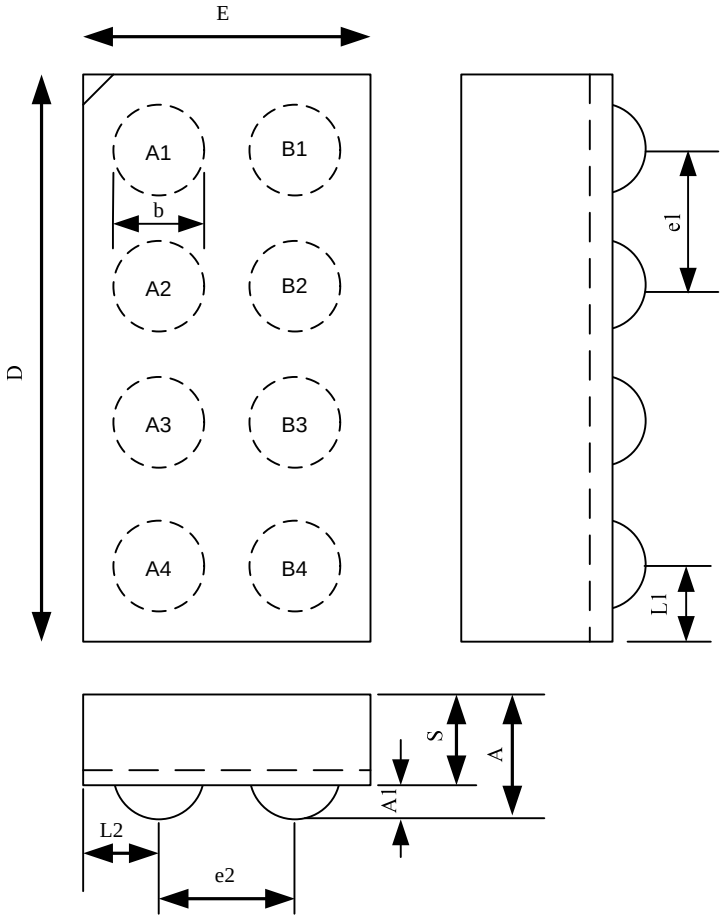
Package Specification
(DFN-10)



SYMBOL	DIMENSION (mm)			DIMENSION (mil)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	32
A1	0.00	0.02	0.05	0	0.8	2
A3		0.203 REF			8 REF	
b	0.18	0.25	0.30	7	10	12
D	2.90	3.00	3.10	114	118	122
D1	2.10	2.20	2.30	83	87	91
E	2.90	3.00	3.10	114	118	122
E1	1.10	1.20	1.30	86	87	91
L	0.45	0.55	0.65	18	22	26
e		0.50 BASIC			20 BASIC	
e1		2.00 BASIC			79 BASIC	

Package Specifications (WLCSP1) *(size: 0.84*1.84*0.5 mm)*

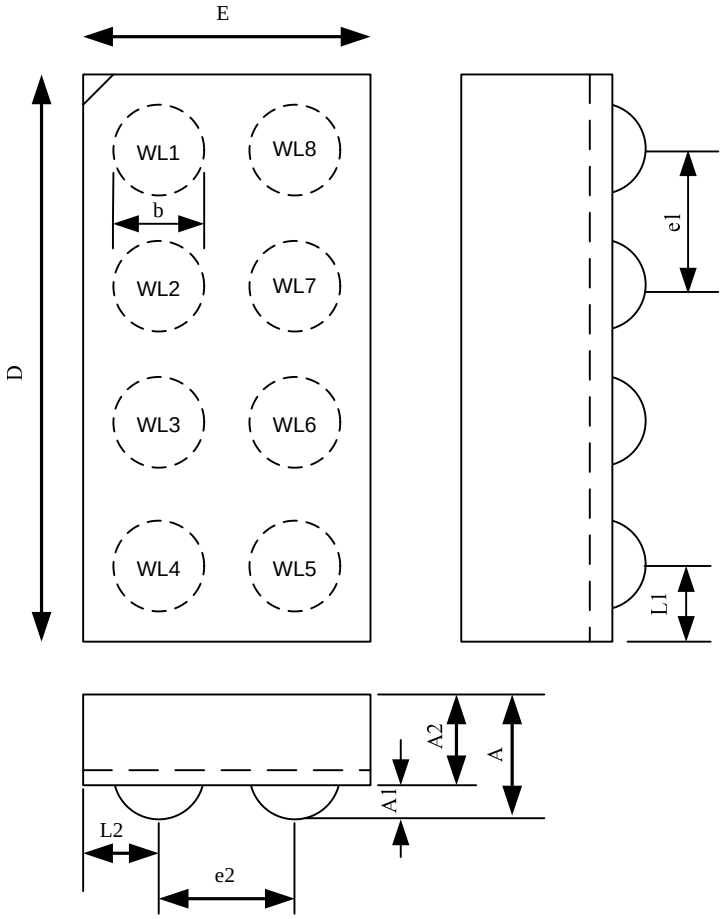
Top View



SYMBOL	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.445	0.50	0.555
A1	0.17	0.2	0.23
S	0.275	0.300	0.325
b	0.24	0.26	0.28
D	1.79	1.84	1.89
E	0.789	0.839	0.889
e1		0.4	
e2		0.4	
L1	0.295	0.320	0.345
L2	0.195	0.220	0.245

Package Specifications (WLCSP2) *(size: 1.0*2.0*0.45 mm)*

Top View



SYMBOL	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.08	0.10	0.12
A2	0.32	0.35	0.38
b	0.26	0.28	0.30
D	1.95	2.00	2.05
E	0.95	1.00	1.05
e1	0.48	0.50	0.52
e2	0.48	0.50	0.52
L1	0.22	0.25	0.28
L2	0.22	0.25	0.28

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.

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