

## 2-Mbit (128K x 16) Static RAM

### Features

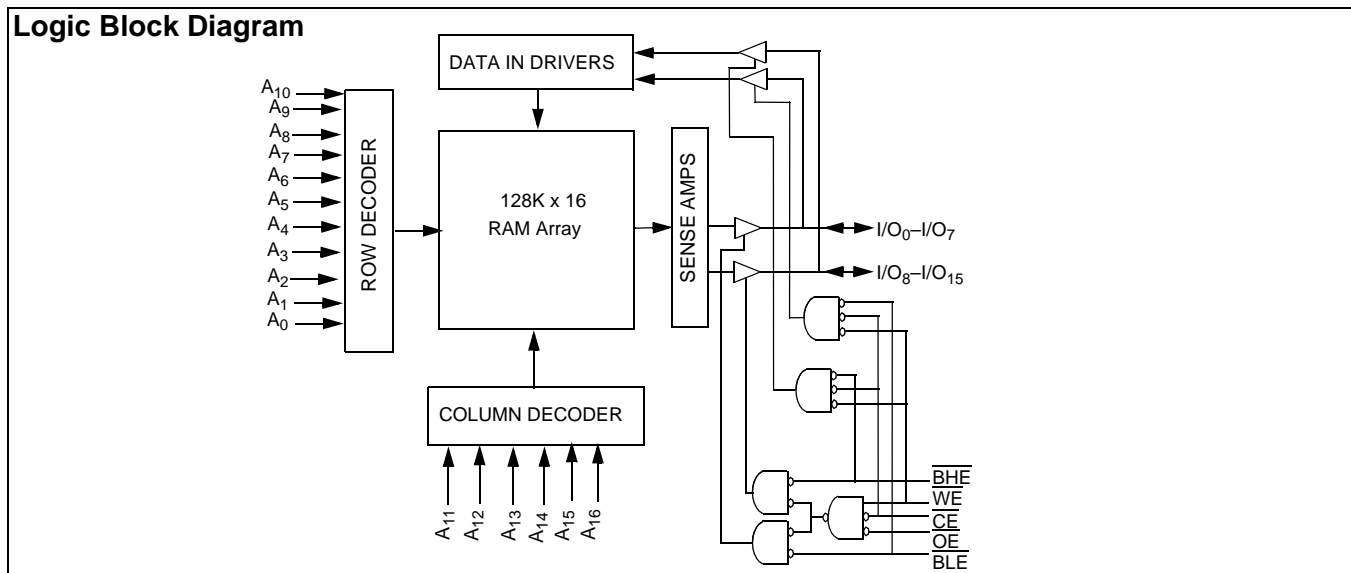
- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62136CV30**
- **Ultra low standby power**
  - **Typical standby current: 1 $\mu$ A**
  - **Maximum standby current: 7 $\mu$ A**
- **Ultra-low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
- **Easy memory expansion with  $\overline{CE}$ , and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in a Pb-free 48-ball VFBGA and 44-pin TSOP II packages**

### Functional Description<sup>[1]</sup>

The CY62136EV30 is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

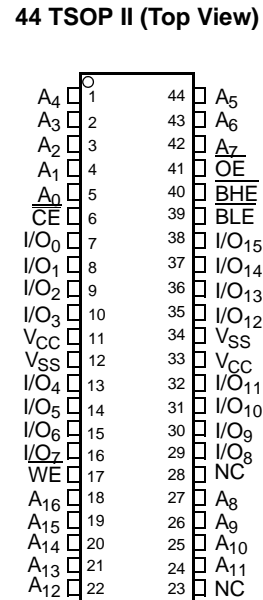
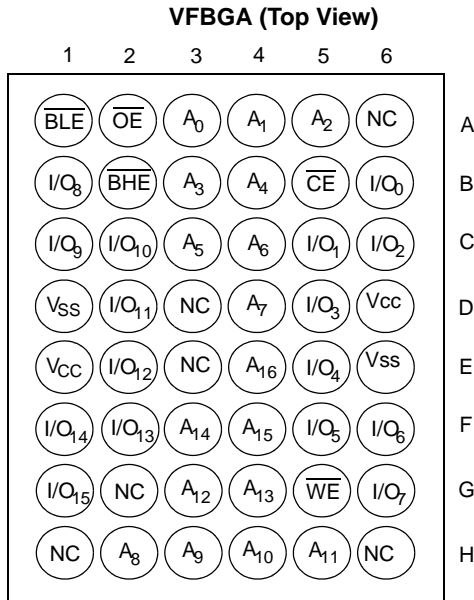
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.



**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2, 3]</sup>**



**Product Portfolio<sup>[4]</sup>**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1MHz		f = f <sub>max</sub>			
Min.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.		
CY62136EV30LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

**Notes:**

- NC pins are not connected on the die.
- Pins D3, H1, G2, and H6 in the BGA package are address expansion pins for 4 Mbit, 8 Mbit, 16 Mbit and 32 Mbit, respectively.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to + 150°C
- Ambient Temperature with Power Applied ..... -55°C to + 125°C
- Supply Voltage to Ground Potential ..... -0.3V to 3.9V ( $V_{CC\ MAX} + 0.3V$ )
- DC Voltage Applied to Outputs in High-Z State<sup>[5,6]</sup> ..... -0.3V to 3.9V ( $V_{CC\ MAX} + 0.3V$ )

- DC Input Voltage<sup>[5,6]</sup> ..... -0.3V to 3.9V ( $V_{CC\ MAX} + 0.3V$ )
  - Output Current into Outputs (LOW) ..... 20 mA
  - Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)
  - Latch-up Current ..... > 200 mA
- Operating Range<sup>[7]</sup>**

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[7]</sup>
CY62136EV30LL	Industrial	-40°C to +85°C	2.2V - 3.6V

**Electrical Characteristics** Over the Operating Range<sup>[5, 6, 7]</sup>

Parameter	Description	Test Conditions	45 ns			Unit
			Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA, V <sub>CC</sub> = 2.20V	2.0			V
		I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> = 2.70V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA, V <sub>CC</sub> = 2.20V			0.4	V
		I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.70V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> + 0.3	V
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.2V to 2.7V	-0.3		0.6	V
		V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , V <sub>CC</sub> = V <sub>CCmax</sub> , I <sub>OUT</sub> = 0 mA CMOS levels		15	20	mA
		f = 1 MHz		2	2.5	
I <sub>SB1</sub>	Automatic CE Power-down Current — CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, and WE), V <sub>CC</sub> = 3.60V		1	7	μA
I <sub>SB2</sub>	Automatic CE Power-down Current — CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V		1	7	μA

**Capacitance** (for all packages)<sup>[8]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

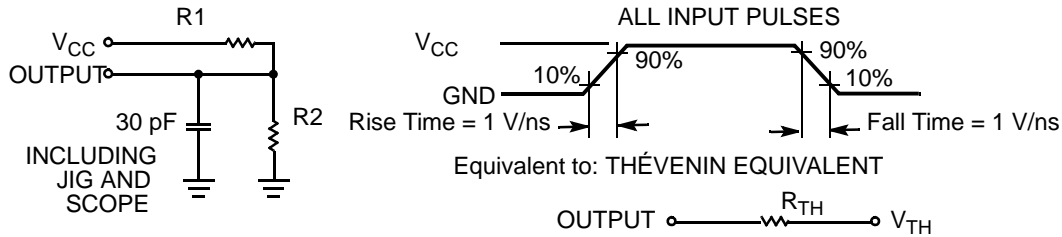
**Notes:**

5. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
6. V<sub>IH(max.)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20ns.
7. Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
8. Tested initially and after any design or process changes that may affect these parameters.

**Thermal Resistance<sup>[8]</sup>**

Parameter	Description	Test Conditions	VFBGA Package	TSOP II Package	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient) <sup>[8]</sup>	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	75	77	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case) <sup>[8]</sup>		10	13	°C/W

**AC Test Loads and Waveforms**

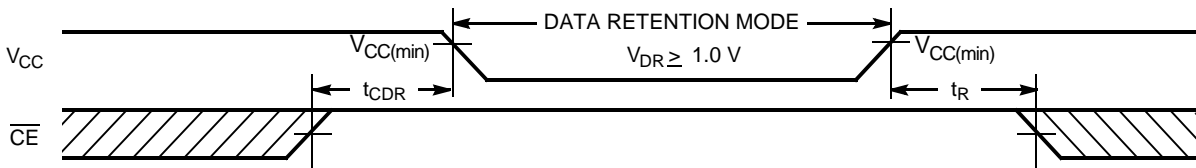


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

**Data Retention Characteristics (Over the Operating Range)<sup>[8, 9]</sup>**

Parameter	Description	Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.0			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		0.8	3	μA
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform**



**Notes:**

9. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 100 μs or stable at V<sub>CC(min.)</sub> ≥ 100 μs.

**Switching Characteristics** Over the Operating Range [10, 11, 12, 13]

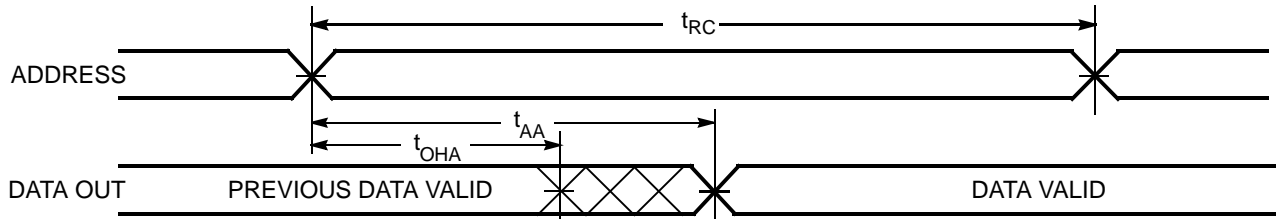
Parameter	Description	45 ns		Unit
		Min.	Max.	
<b>Read Cycle</b>				
t <sub>RC</sub>	Read Cycle Time	45		ns
t <sub>AA</sub>	Address to Data Valid		45	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to LOW Z <sup>[11]</sup>	5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[11, 12]</sup>		18	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[11]</sup>	10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[11, 12]</sup>		18	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		45	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		22	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[11]</sup>	5		ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z <sup>[11, 12]</sup>		18	ns
<b>Write Cycle<sup>[13]</sup></b>				
t <sub>WC</sub>	Write Cycle Time	45		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	35		ns
t <sub>AW</sub>	Address Set-Up to Write End	35		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[11, 12]</sup>		18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[11]</sup>	10		ns

**Notes:**

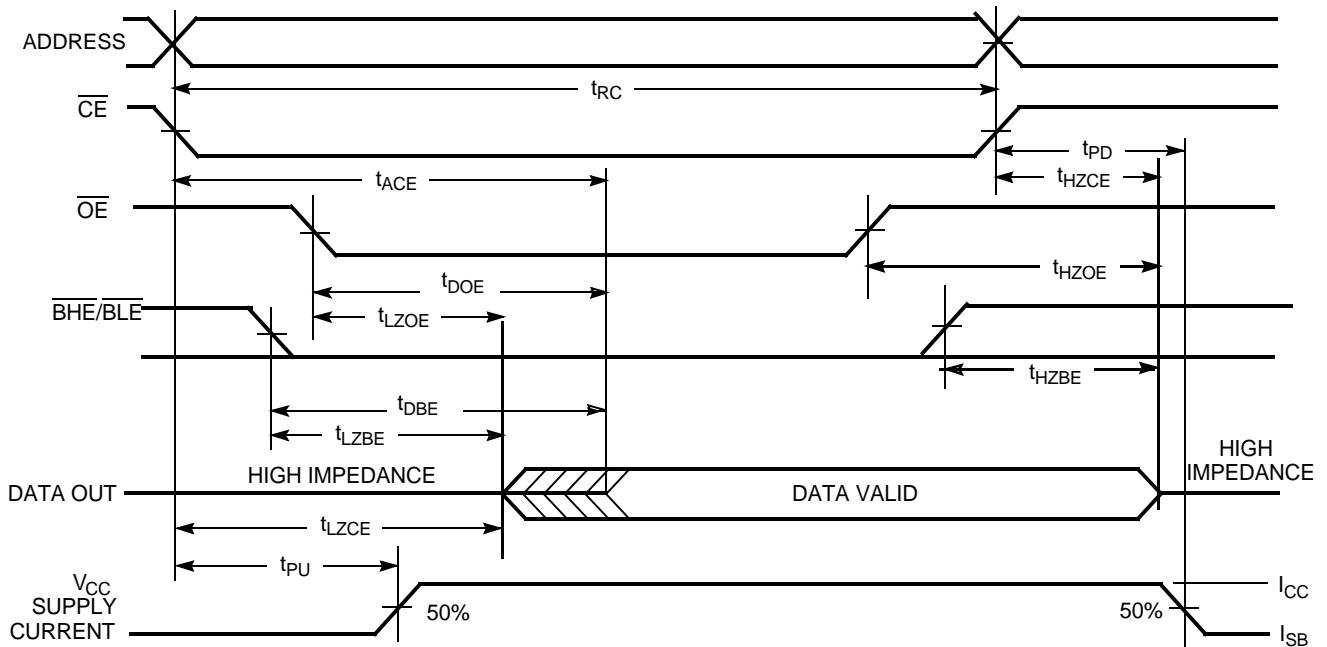
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0 to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
12. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
13. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

**Switching Waveforms** [14, 15]

**Read Cycle 1 (Address Transition Controlled)**[14, 15]



**Read Cycle No. 2 ( $\overline{OE}$  Controlled)**[15, 16]

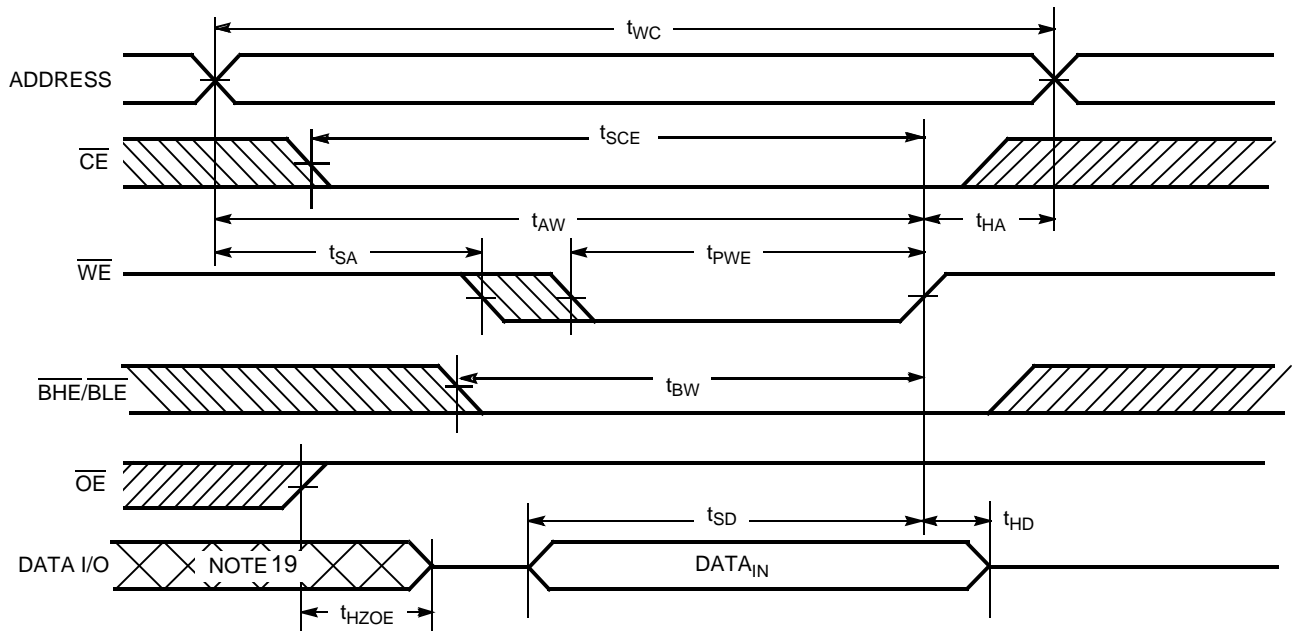


**Notes:**

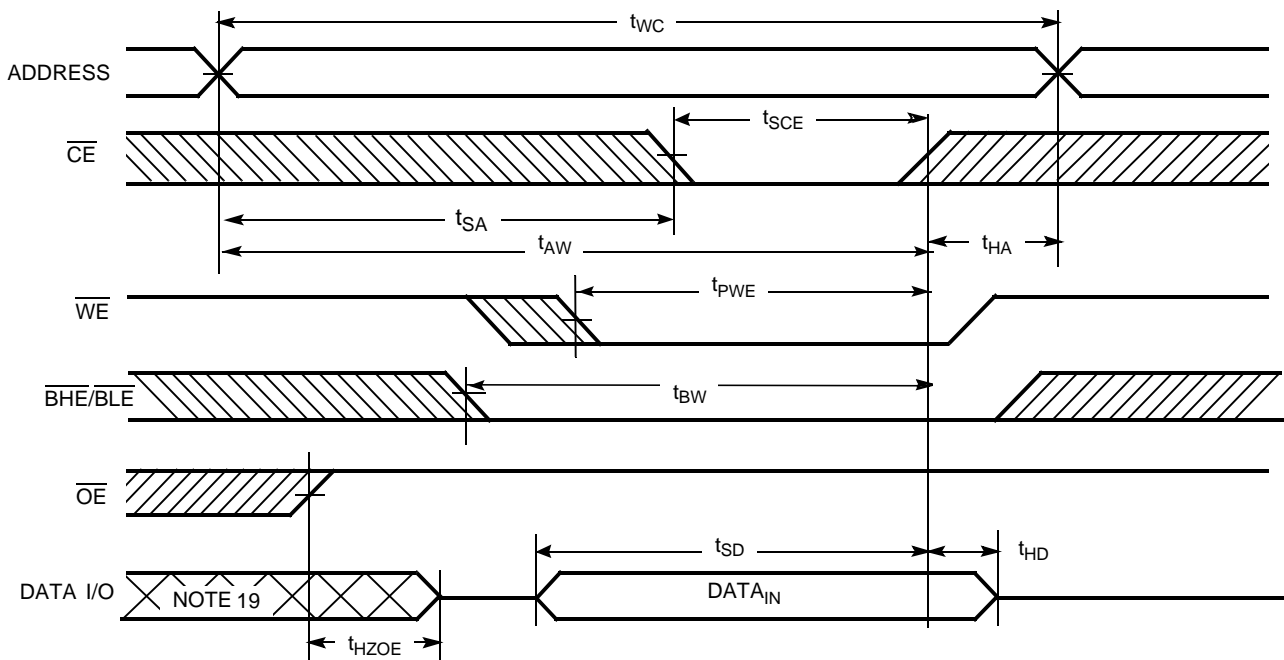
- 14. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
- 15.  $\overline{WE}$  is HIGH for read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

Switching Waveforms (continued)<sup>[14, 15]</sup>

Write Cycle No. 1 (WE Controlled)<sup>[13, 17, 18]</sup>



Write Cycle No. 2 (CE Controlled)<sup>[13, 17, 18]</sup>



Notes:

- 17. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 18. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.
- 19. During this period, the I/Os are in output state and input signals should not be applied.





**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	X	X	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Write	Active ( $I_{CC}$ )

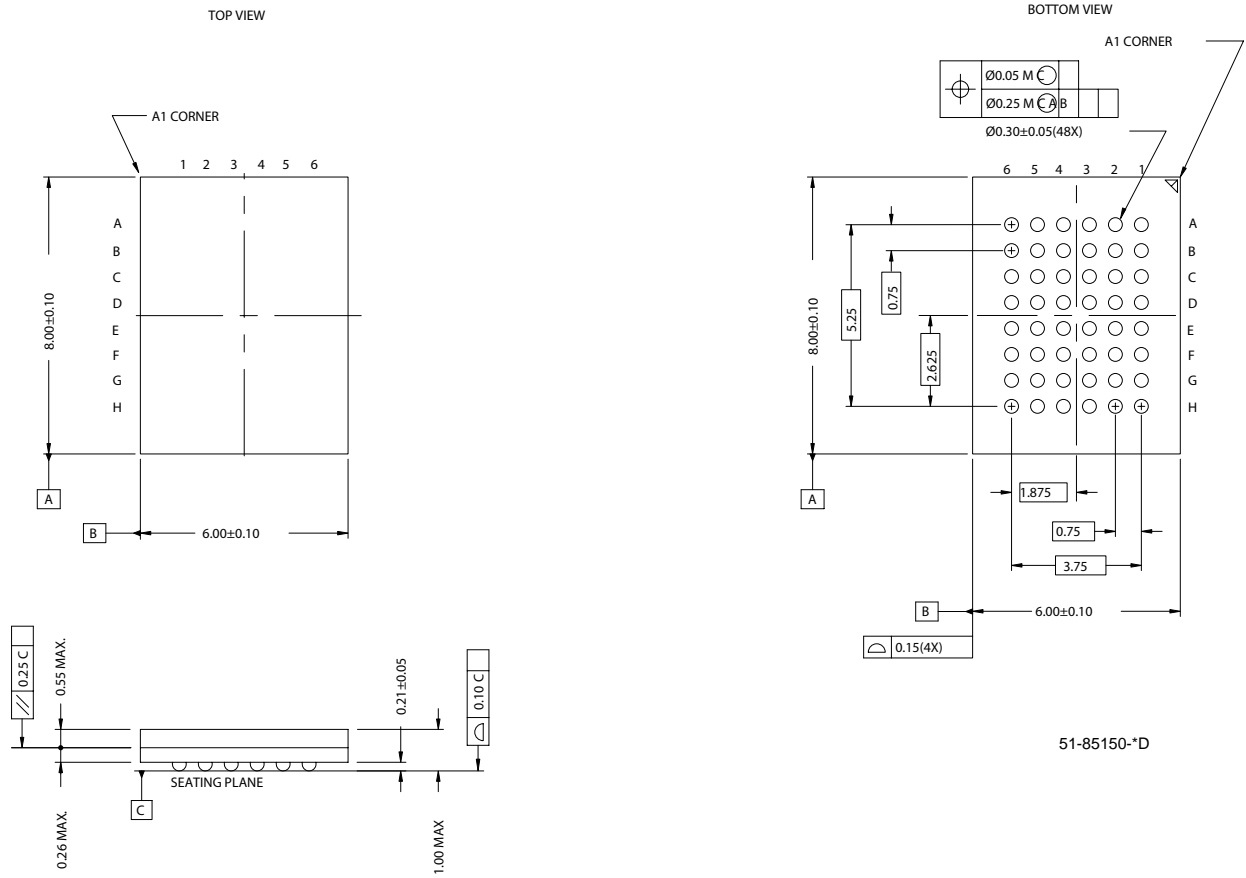
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136EV30LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62136EV30LL-45ZSXI	51-85087	44-pin Thin Small Outline Package II (Pb-free)	

Please contact your local Cypress sales representative for availability of other parts

Package Diagrams

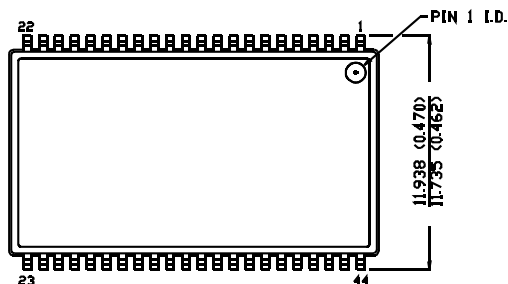
48-pin VFBGA (6 x 8 x 1 mm) (51-85150)



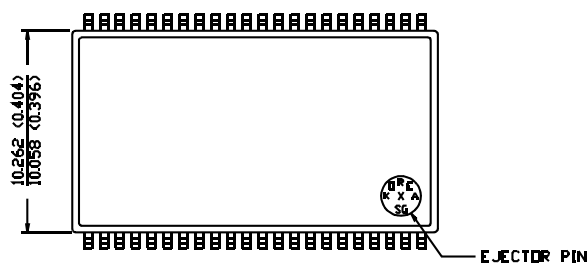
Package Diagrams (continued)

44-pin TSOP II (51-85087)

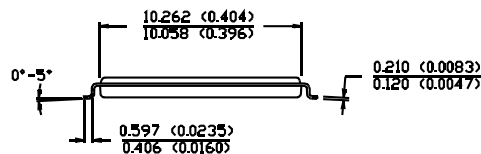
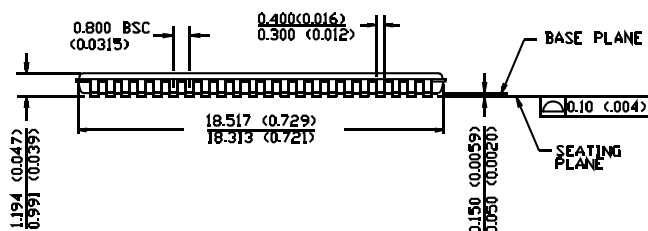
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

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**Document History Page**

Document Title: CY62136EV30 MoBL® 2-Mbit (128K x 16) Static RAM				
Document Number: 38-05569				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	237432	See ECN	AJU	New Data Sheet
*A	419988	See ECN	R XU	<p>Converted from Advanced Information to Final.</p> <p>Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed 35ns Speed Bin</p> <p>Removed "L" version of CY62136EV30</p> <p>Changed I<sub>CC</sub> (Max) value from 2 mA to 2.5 mA and I<sub>CC</sub> (Typ) value from 1.5 mA to 2 mA at f=1 MHz</p> <p>Changed I<sub>CC</sub> (Typ) value from 12 mA to 15 mA at f = f<sub>max</sub></p> <p>Changed I<sub>SB1</sub> and I<sub>SB2</sub> Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA.</p> <p>Changed the AC test load capacitance from 50pF to 30pF on Page# 4</p> <p>Changed V<sub>DR</sub> from 1.5V to 1V on Page# 4.</p> <p>Changed I<sub>CCDR</sub> from 2.5 μA to 3 μA.</p> <p>Added I<sub>CCDR</sub> typical value.</p> <p>Changed t<sub>OHA</sub>, t<sub>LZCE</sub> and t<sub>LZWE</sub> from 6 ns to 10 ns</p> <p>Changed t<sub>LZBE</sub> from 6 ns to 5 ns</p> <p>Changed t<sub>LZOE</sub> from 3 ns to 5 ns</p> <p>Changed t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub> and t<sub>HZWE</sub> from 15 ns to 18 ns</p> <p>Changed t<sub>SCE</sub>, t<sub>AW</sub> and t<sub>BW</sub> from 40 ns to 35 ns</p> <p>Changed t<sub>PWE</sub> from 30 ns to 35 ns</p> <p>Changed t<sub>SD</sub> from 20 ns to 25 ns</p> <p>Corrected typo in the Truth Table on Page# 9</p> <p>Updated the package diagram 48-pin VFBGA from *B to *D</p> <p>Updated the ordering Information table and replaced the Package Name column with Package Diagram.</p>
*B	427817	See ECN	NXR	Minor change: Moved datasheet to external web