

## SPS-7110V-1T1RG

**(RoHS Compliant)**

### 1310 nm / 1.5 Gb/s Medium Power Optical SM Transmitter/Receiver

#### FEATURES

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- | SMPTE 292M/297M/259M Compatible
- | Hot-Pluggable SFP Footprint LC Optical Transceiver
- | Speed from 50 Mbps to 1.5 Gbps with up to 30 km Single-mode Fiber
- | Distance up to 21 km for 1.5G-SDI
- | **Support Video Pathological Patterns for SD-SDI and HD-SDI**
- | Single Transmitter with Simplex LC
- | Single Receiver with Simplex LC
- | Based on Industry Standard SFP
- | TTL Laser Disable Input
- | Single +3.3 V Power Supply
- | RoHS-6 Compliant
- | 0 to 70°C Operation
- | Hot Pluggable
- | Class 1 Laser International Safety Standard IEC-60825 Compliant

#### DESCRIPTION

The SPS-7110V-1T1RG is a optical single mode transmitter/receiver module designed to transmit/receive optical serial digital signals as defined in SMPTE 292M/297M/259M. It supports from 50 Mbps to 1.5 Gbps and is specifically designed for transmitted the SMPTE 292M, SMPTE 297M and SMPTE 259M SDI pathological patterns. It is with the SFP 20-pin connector to allow hot plug capability. It is with 1310 nm laser transmitters. The transmitter can transmit signal from 50 Mbps to 1.5 Gbps with up to 30 km of single-mode fiber. A maximum distance of 21 km is achievable with 1.5 Gbps pathological signals.

#### LASER SAFETY

This single mode transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

#### APPLICATIONS

- | SMPTE 292M/297M/259M Compliant Electrical-to-Optical Interfaces
- | High-density Video Routers

#### ORDER INFORMATION

P/No.	Type	Bit Rate (Mb/s)	TX		RX		Package	Temp (°C)	RoHS Compliant
			λ (nm)	Power (dBm)	λ (nm)	Sen. (dBm)			
<b>SPS-7110V-1T1RG</b>	1-TX+1-RX	50 to 1500	1310	0 to -7	1260/1620	0 to -20	LC SFP	0 to 70	Yes

#### LINK DISTANCE

SDI	Bit Rate	Max. Link Distance (km)
HD-SDI	1.485Gbps	21
SD-SDI	270Mbos	30

## ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings					
Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T <sub>stg</sub>	-40	85	°C	
Operating Case Temperature	T <sub>c</sub>	0	70	°C	
Power Supply Voltage	V <sub>cc</sub>	0	4	V	
ESD Tolerance on all pins			1	KV HBM	
Relative Humidity	---	5	95	% RH	non-condensing

Recommended Operating Conditions					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Power Supply Voltage	V <sub>cc</sub>	3.13	3.3	3.47	V
Operating Case Temperature	T <sub>c</sub>	0		70	°C
Baud Rate		50	1485	1500	Mb/s
Power Supply Current	I <sub>cc</sub>		200	280	mA

Transmitter Specifications (0°C < T <sub>c</sub> < 70°C, 3.13V < V <sub>cc</sub> < 3.47V)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
<b>Optical</b>						
Optical Transmit Power	P <sub>o</sub>	-7		0	dBm	1
Output Center Wavelength	λ	1290	1310	1330	nm	At 25°C
Output Spectrum Width	Δλ	---		3	nm	RMS (σ)
Extinction Ratio	ER	5			dB	
Relative Intensity Noise	RIN			-120	dB/Hz	
Optical Rise Time / Fall Time	tr / tf			270	ps	2, SMPTE 292M
				800	ps	2, SMPTE 344M
				1.5	ns	2, SMPTE 259M
<b>Electrical</b>						
Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	200		1200	mVp-p	AC coupled input
Disable Input Voltage -- Low	V <sub>TDIS,L</sub>	0		0.8	V	TX Output Enabled
Disable Input Voltage -- High	V <sub>TDIS,H</sub>	2.0		V <sub>cc</sub> +0.3	V	TX Output Disabled
SCL, SDA	V <sub>OH</sub>	2.5		V <sub>cc</sub> +0.3	V	
	V <sub>OL</sub>	0		0.5	V	

- Output power is power coupled into a 9/125 μm single mode fiber.
- 20% to 80%, unfiltered.

Receiver Specifications (0°C < T <sub>c</sub> < 70°C, 3.13V < V <sub>cc</sub> < 3.47V)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
<b>Optical</b>						
Wavelength of Operation		1260	---	1620	nm	
Sensitivity for SMPTE 292M 1.485 Gb/s	Sen	0	---	-18	dBm	Pathological
		0	---	-20	dBm	PRBS 2 <sup>23</sup> -1, BER=1E-12
Signal Detect -- Asserted	Pa	---	---	-21	dBm	Transition: low to high
Signal Detect -- Deasserted	Pd	-31	---	---	dBm	Transition: high to low
Signal detect -- Hysteresis		1		6	dB	
Optical Return Loss			-27		dB	
<b>Electrical</b>						
CML Output (Differential)		550	660	850	mVp-p	AC coupled output
Optical Rise Time / Fall Time	tr / tf			270	ps	3, SMPTE 292M
				800	ps	3, SMPTE 344M
				1.5	ns	3, SMPTE 259M

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Output LOS Voltage -- Low	$V_{OL}$	0		0.5	V	$I_{OL}=-1.6mA$ , 1 TTL unit load
Output LOS Voltage -- High	$V_{OH}$	2.5		$V_{CC}+0.3$	V	$I_{OH}=40\mu A$ , 1 TTL unit load
SCL, SDA	$V_{OH}$	2.5		$V_{CC}+0.3$	V	
	$V_{OL}$	0		0.5	V	

3. 20% to 80%, unfiltered.

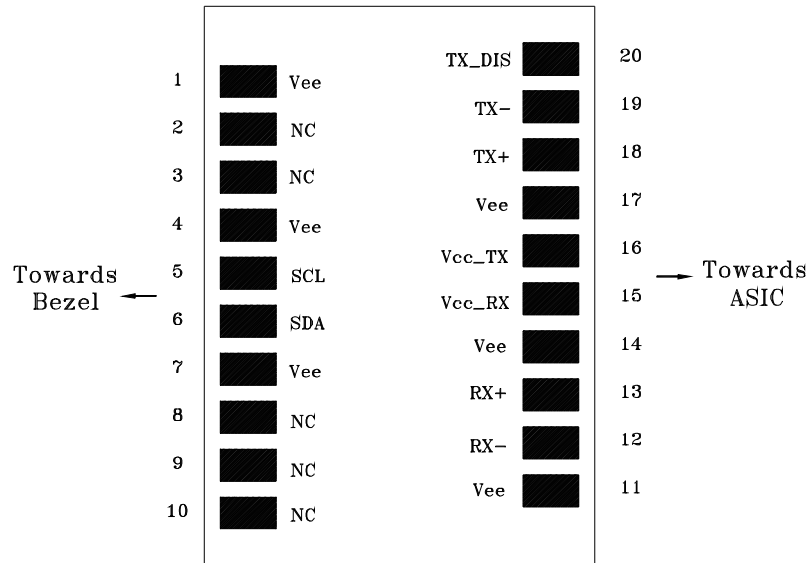
## MODULE DEFINITION

Module Definition	PIN 5	PIN 6	Interpretation by Host
4	SCL	SDA	Serial module definition protocol

Module Definition 4 specifies a serial definition protocol. For this definition, upon power up, SCL and SDA appear as no connector (NC). When the host system detects this condition, it activates the serial protocol. The protocol uses the 2-wire serial CMOS E<sup>2</sup>PROM protocol of the ATMEL AT24C01A/02/04 family of components.

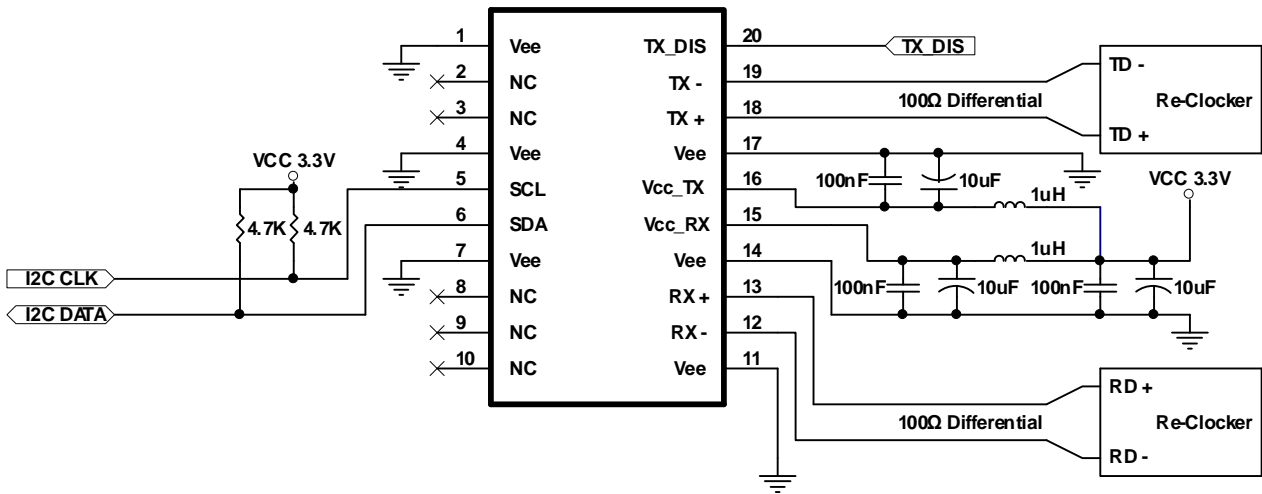
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CONNECTION DIAGRAM



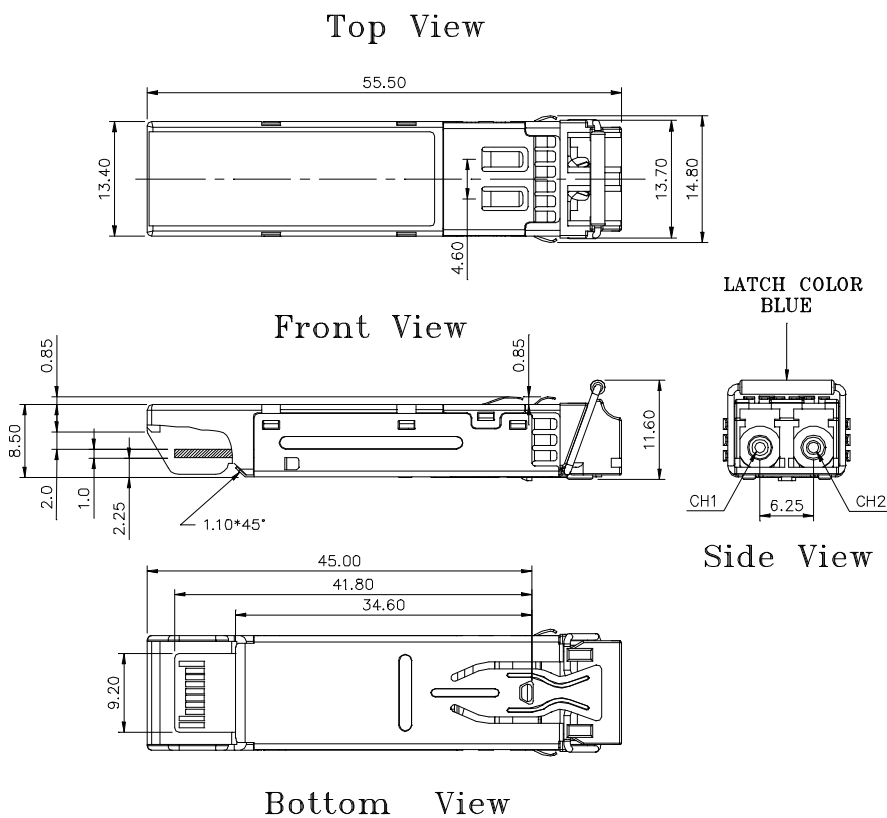
PIN	Name	Function	Notes
1	Vee	Signal Ground	
2	NC	No Connection	
3	NC	No Connection	
4	Vee	Signal Ground	
5	SCL	Serial I <sup>2</sup> C Clock	
6	SDA	Serial I <sup>2</sup> C Data	
7	Vee	Signal Ground	
8	NC	No Connection	
9	NC	No Connection	
10	NC	No Connection	
11	Vee	Signal Ground	
12	RX-	Negative Differential Output	
13	RX+	Positive Differential Output	
14	Vee	Signal Ground	
15	Vcc RX	Power Supply	+3.3V±5%, Internal connected
16	Vcc TX	Power Supply	
17	Vee	Signal Ground	
18	TX+	Positive Transmitter Data In	AC coupled differential lines with 100 ohm differential termination inside the module
19	TX-	Negative Transmitter Data In	
20	TX_DIS	Transmitter Disable	Internal 4.7 kΩ pull-up. The bias current and modulation current are turned off if TX1_DIS = HIGH.

RECOMMENDED CIRCUIT SCHEMATIC



1. Consult the Chipset manufacturer's applications information for biasing required for TX outputs. Some chipset outputs are internally biased and may not need external bias resistor.

PACKAGE DIAGRAM (Units in mm)



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REVISION HISTORY

Version	Subject	Release Date
1.0	Initial datasheet	2008/10/1