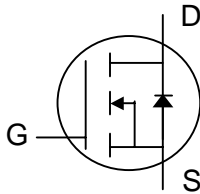


## N-channel Enhancement-mode Power MOSFET

- Low gate-charge
- Simple drive requirement
- Fast switching

 **Pb-free, RoHS compliant.**

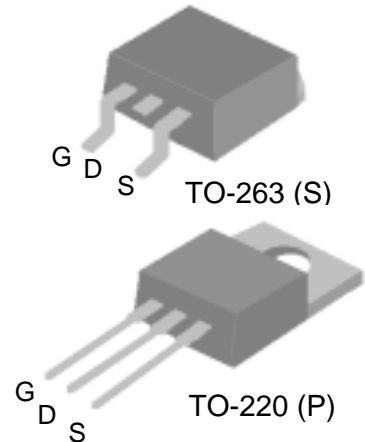


$BV_{DSS}$	30V
$R_{DS(ON)}$	4m $\Omega$
$I_D$	75A

### DESCRIPTION

The SSM90T03GS is in a TO-263 package, which is widely used for commercial and industrial surface mount applications. This device is suitable for low voltage applications such as DC/DC converters.

The through-hole version, the SSM90T03GP in TO-220, is available for vertical-mounting, where a small footprint is required on the board, and/or an external heatsink is to be attached.



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} = 4.5\text{V}$	75	A
$I_D @ T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} = 4.5\text{V}$	63	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	350	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	96	W
	Linear Derating Factor	0.7	W/ $^\circ\text{C}$
$E_{AS}$	Single Pulse Avalanche Energy <sup>3</sup>	29	mJ
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL DATA

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Maximum Thermal Resistance, Junction-case	1.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction-ambient	62	$^\circ\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS (at T<sub>j</sub>=25°C, unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =1mA	30	-	-	V
ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	-	0.02	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =45A	-	-	4	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =30A	-	-	6	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	0.8	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =30A	-	55	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	uA
	Drain-Source Leakage Current (T <sub>j</sub> =150°C)	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> = ±20V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =40A	-	60	96	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =24V	-	8.5	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	38	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =15V	-	14	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =30A	-	83	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =10V	-	66	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =0.5Ω	-	120	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	4090	6540	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V	-	1010	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	890	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =45A, V <sub>GS</sub> =0V	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time <sup>2</sup>	I <sub>S</sub> =30A, V <sub>GS</sub> =0V,	-	51	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	-	63	-	nC

**Notes:**

1. Pulse width limited by safe operating area.
2. Pulse width ≤300us, duty cycle ≤2%.
3. V<sub>DD</sub>=25V, L=100uH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=24A.

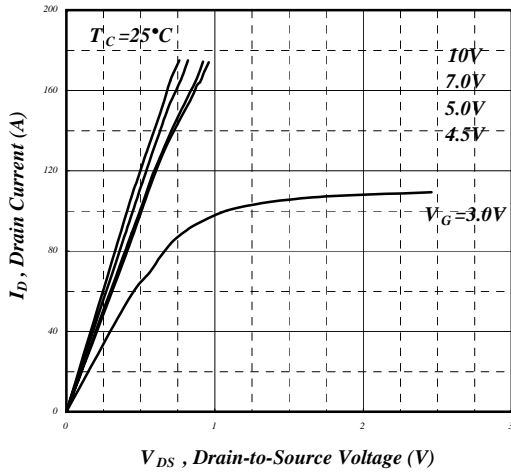


Fig 1. Typical Output Characteristics

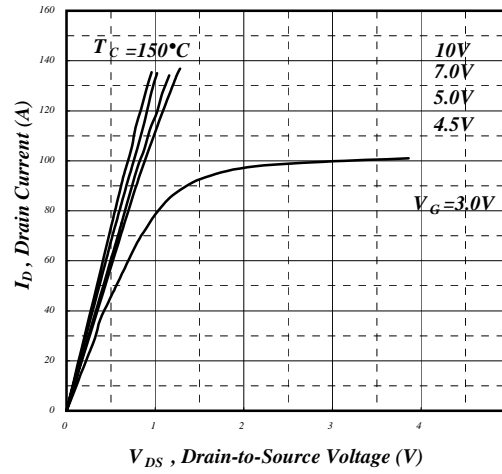


Fig 2. Typical Output Characteristics

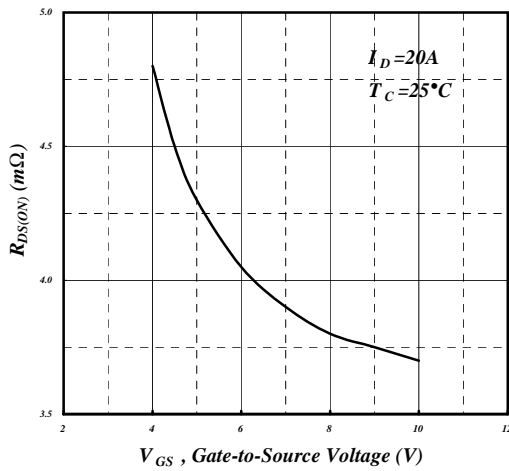


Fig 3. On-Resistance vs. Gate Voltage

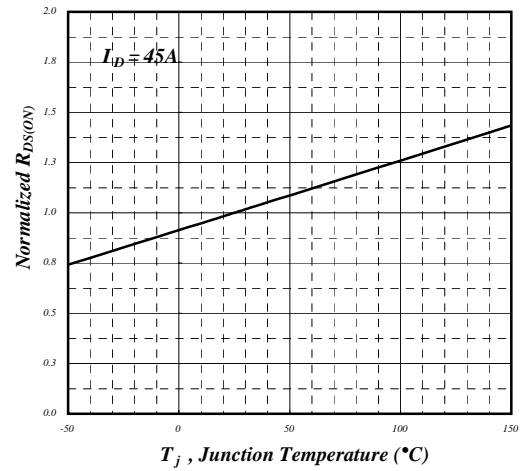


Fig 4. Normalized On-Resistance vs. Junction Temperature

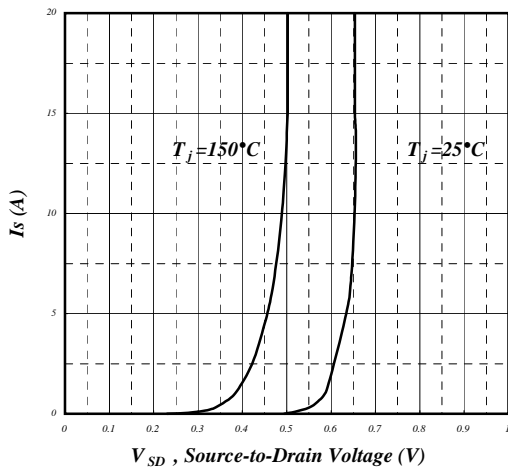


Fig 5. Forward Characteristic of Reverse Diode

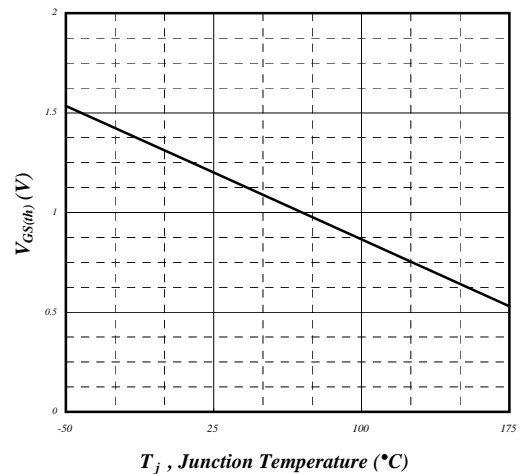


Fig 6. Gate Threshold Voltage vs. Junction Temperature

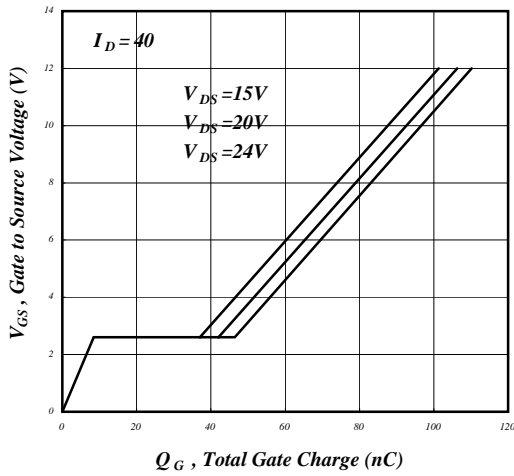


Fig 7. Gate Charge Characteristics

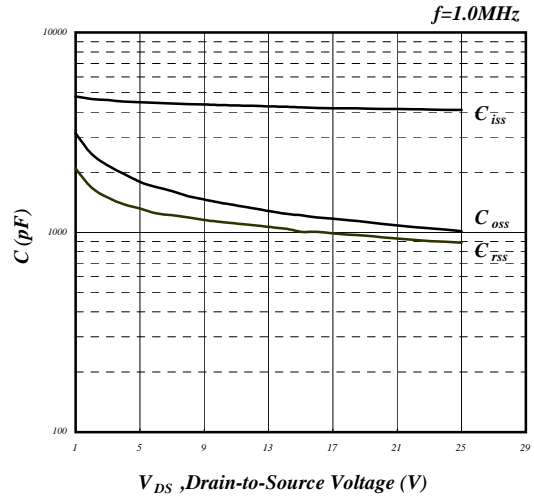


Fig 8. Typical Capacitance Characteristics

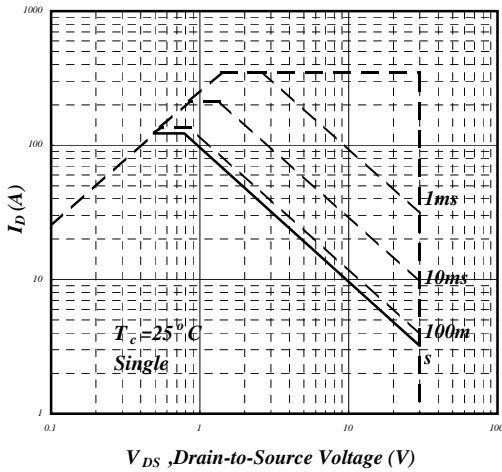


Fig 9. Maximum Safe Operating Area

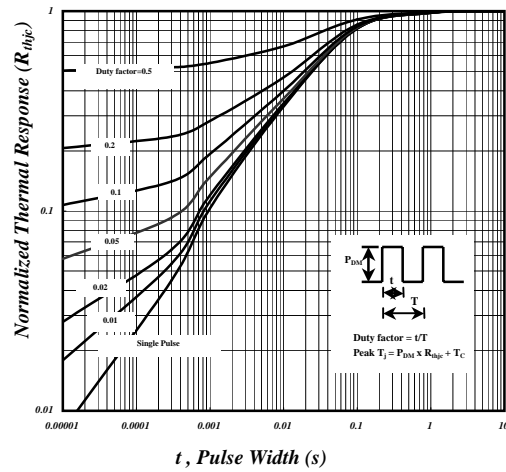


Fig 10. Effective Transient Thermal Impedance

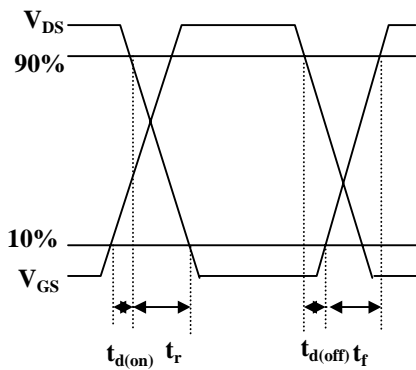


Fig 11. Switching Time Waveform

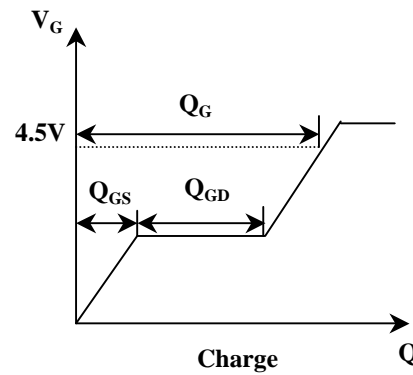


Fig 12. Gate Charge Waveform

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