UJA1061

Fault-tolerant CAN/LIN fail-safe system basis chip

Rev. 06 — 9 March 2010 Product data sheet

1. General description

The UJA1061 fail-safe System Basis Chip (SBC) replaces basic discrete components that are common in every Electronic Control Unit (ECU) with a Controller Area Network (CAN) and a Local Interconnect Network (LIN) interface. The fail-safe SBC supports all networking applications that control various power and sensor peripherals by using fault-tolerant CAN as the main network interface and LIN as a local sub-bus. The fail-safe SBC contains the following integrated devices:

- ISO11898-3 compliant fault-tolerant CAN transceiver, interoperable with TJA1054, TJA1054A and TJA1055
- LIN transceiver compliant with LIN 2.0 and SAE J2602, and compatible with LIN 1.3
- Advanced independent watchdog
- Dedicated voltage regulators for microcontroller and CAN transceiver
- Serial peripheral interface (full duplex)
- Local wake-up input port
- Inhibit/limp-home output port

In addition to the advantages of integrating these common ECU functions in a single package, the fail-safe SBC offers an intelligent combination of system-specific functions such as:

- Advanced low-power concept
- Safe and controlled system start-up behavior
- Advanced fail-safe system behavior that prevents any conceivable deadlock
- Detailed status reporting on system and subsystem levels

The UJA1061 is designed to be used in combination with a microcontroller that incorporates a CAN controller. The fail-safe SBC ensures that the microcontroller is always started up in a defined manner. In failure situations, the fail-safe SBC will maintain microcontroller functionality for as long as possible to provide full monitoring and a software-driven fall-back operation.

The UJA1061 is designed for 14 V single power supply architectures and for 14 V and 42 V dual power supply architectures.

2. Features and benefits

2.1 General

- Contains a full set of CAN and LIN ECU functions:
  - CAN transceiver and LIN transceiver
  - Voltage regulator for the microcontroller (3.3 V or 5.0 V)
  - Separate voltage regulator for the CAN transceiver (5 V)
  - Enhanced window watchdog with on-chip oscillator
  - Serial Peripheral Interface (SPI) for the microcontroller
  - ECU power management system
  - Fully integrated autonomous fail-safe system
- Designed for automotive applications:
  - Supports 14 V, 24 V and 42 V architectures
  - Excellent ElectroMagnetic Compatibility (EMC) performance
  - ±8 kV ElectroStatic Discharge (ESD) protection Human Body Model (HBM) for off-board pins
  - ±6 kV ElectroStatic Discharge (ESD) protection IEC 61000-4-2 for off-board pins
  - ±60 V short-circuit proof CAN/LIN-bus pins
  - Battery and CAN/LIN-bus pins are protected against transients in accordance with ISO 7637
  - Very low sleep current
- Supports remote flash programming via the CAN-bus
- Small 6.1 mm × 11 mm HTSSOP32 package with low thermal resistance

2.2 CAN transceiver

- ISO 11898-3 compliant fault-tolerant CAN transceiver
- Enhanced error signalling and reporting
- Dedicated low dropout voltage regulator for the CAN-bus:
  - Independent from microcontroller supply
  - Guarded by CAN-bus failure management
  - Significantly improves EMC performance
- Partial networking option with global wake-up feature, allows selective CAN-bus communication without waking up sleeping nodes
- Bus connections are truly floating when power is off
- Ground shift detection

2.3 LIN transceiver

- LIN 2.0 compliant LIN transceiver
- Enhanced error signalling and reporting
- Downward compatible with LIN 1.3 and the TJA1020

2.4 Power management

- Smart operating modes and power management modes
- Cyclic wake-up capability in Standby and Sleep modes
- Local wake-up input with cyclic supply feature
- Remote wake-up capability via the CAN-bus and LIN-bus
- External voltage regulators can easily be incorporated in the power supply system (flexible and fail-safe)
- 42 V battery-related high-side switch for driving external loads such as relays and wake-up switches
- Intelligent maskable interrupt output

2.5 Fail-safe features

- Safe and predictable behavior under all conditions
- Programmable fail-safe coded window and time-out watchdog with on-chip oscillator, guaranteeing autonomous fail-safe system supervision
- Fail-safe coded 16-bit SPI interface for the microcontroller
- Global enable pin for the control of safety-critical hardware
- Detection and detailed reporting of failures:
  - On-chip oscillator failure and watchdog alerts
  - Voltage regulator undervoltages
  - CAN and LIN-bus failures (short-circuits and open-circuit bus wires)
  - TXD and RXD clamping situations and short-circuits
  - Clamped or open reset line
  - SPI message errors
  - Overtemperature warning
  - ECU ground shift (two selectable thresholds)
- Rigorous error handling based on diagnostics
- 23 bits of access-protected RAM is available e.g. for logging of cyclic problems
- Reporting in a single SPI message; no assembly of multiple SPI frames needed
- limp-home output signal for activating application hardware in case system enters Fail-safe mode (e.g. for switching on warning lights)
- Fail-safe coded activation of Software development mode and Flash mode
- Unique SPI readable device type identification
- Software-initiated system reset

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UJA1061TW[1]	HTSSOP32	plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad	SOT549-1

[1] UJA1061TW/5V0 is for the 5 V version; UJA1061TW/3V3 is for the 3.3 V version.

4. Block diagram

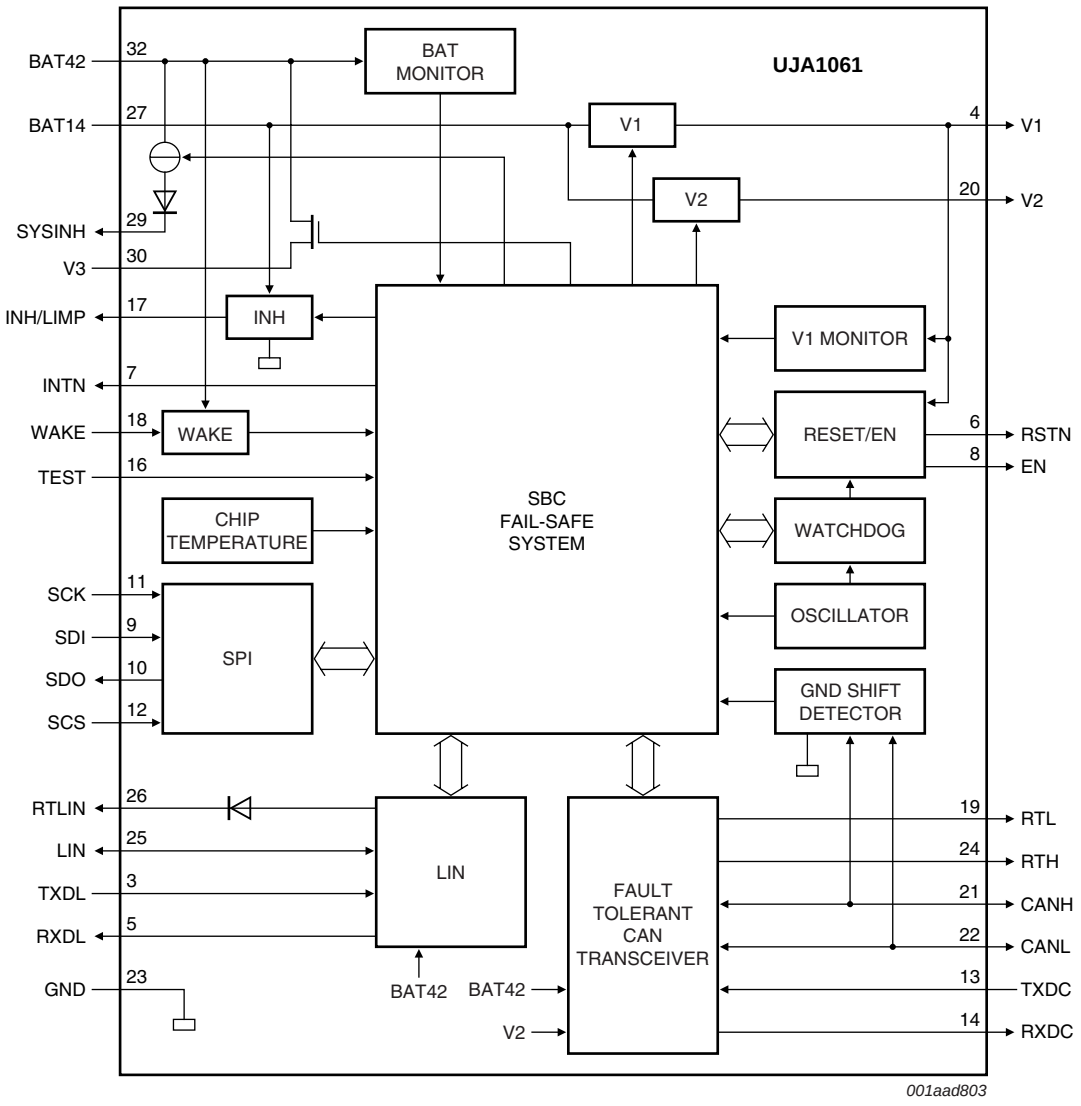


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

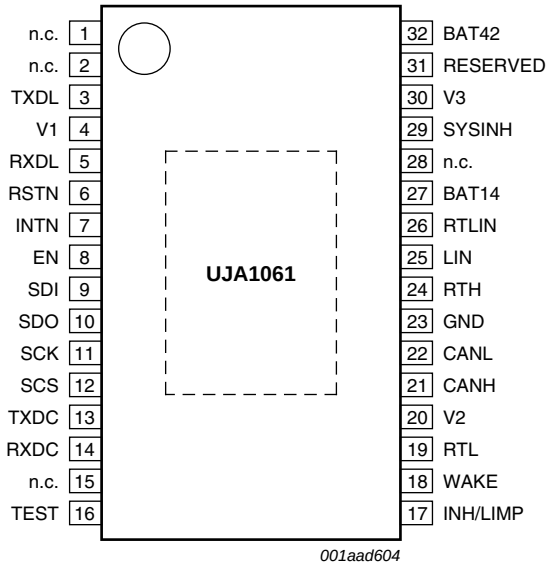


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
n.c.	2	not connected
TXDL	3	LIN transmit data input (LOW for dominant, HIGH for recessive)
V1	4	voltage regulator output for the microcontroller (3.3 V or 5 V depending on the SBC version)
RXDL	5	LIN receive data output (LOW when dominant, HIGH when recessive)
RSTN	6	reset output to microcontroller (active LOW; will detect clamping situations)
INTN	7	interrupt output to microcontroller (active LOW; open-drain, wire-AND this pin to other ECU interrupt outputs)
EN	8	enable output (active HIGH; push-pull, LOW with every reset / watchdog overflow)
SDI	9	SPI data input
SDO	10	SPI data output (floating when pin SCS is HIGH)
SCK	11	SPI clock input
SCS	12	SPI chip select input (active LOW)
TXDC	13	CAN transmit data input (LOW for dominant; HIGH for recessive)
RXDC	14	CAN receive data output (LOW when dominant; HIGH when recessive)
n.c.	15	not connected
TEST	16	test pin (should be connected to ground in application)

Table 2. Pin description *...continued*

Symbol	Pin	Description
INH/LIMP	17	inhibit/limp-home output (BAT14 related, push-pull, default floating)
WAKE	18	local wake-up input (BAT42 related, continuous or cyclic sampling)
RTL	19	CAN termination resistor connection; in case of a CANL bus wire error this line is terminated with a selectable impedance
V2	20	5 V voltage regulator output for CAN; connect a buffer capacitor to this pin
CANH	21	CANH bus line (HIGH in dominant state)
CANL	22	CANL bus line (LOW in dominant state)
GND	23	ground
RTH	24	CAN termination resistor connection; in case of a CANH bus wire error this line is terminated with a selectable impedance
LIN	25	LIN bus line (LOW in dominant state)
RTLIN	26	LIN-bus termination resistor connection
BAT14	27	14 V battery supply input
n.c.	28	not connected
SYSINH	29	system inhibit output (BAT42 related; e.g. for controlling external DC-to-DC converter)
V3	30	unregulated 42 V output (BAT42 related; continuous output, or Cyclic mode synchronized with local wake-up input)
reserved	31	must be connected to ground (GND)
BAT42	32	42 V battery supply input (connect this pin to BAT14 in 14 V applications)

The exposed die pad at the bottom of the package allows better dissipation of heat from the SBC via the printed-circuit board. The exposed die pad is not connected to any active part of the IC and can be left floating, or can be connected to GND for the best EMC performance.

6. Functional description

6.1 Introduction

The UJA1061 combines all peripheral functions around a microcontroller within typical automotive networking applications into one dedicated chip. The functions are as follows:

- Power supply for the microcontroller
- Power supply for the CAN transceiver
- Switched BAT42 output
- System reset
- Watchdog with Window mode and Time-out mode
- On-chip oscillator
- Fault-tolerant CAN and LIN transceivers for serial communication; suitable for 12 V and 42 V applications
- SPI control interface
- Local wake-up input
- Inhibit or limp-home output
- System inhibit output port
- Compatibility with 42 V power supply systems
- Fail-safe behavior

6.2 Fail-safe system controller

The fail-safe system controller is the core of the UJA1061 and is supervised by a watchdog timer that is clocked directly by the dedicated on-chip oscillator. The system controller manages the register configuration and controls all internal functions of the SBC. Detailed device status information is collected and presented to the microcontroller. The system controller also provides the reset and interrupt signals.

The fail-safe system controller is a state machine. The different operating modes and the transitions between these modes are illustrated in Figure 3. The following sections give further details about the SBC operating modes.

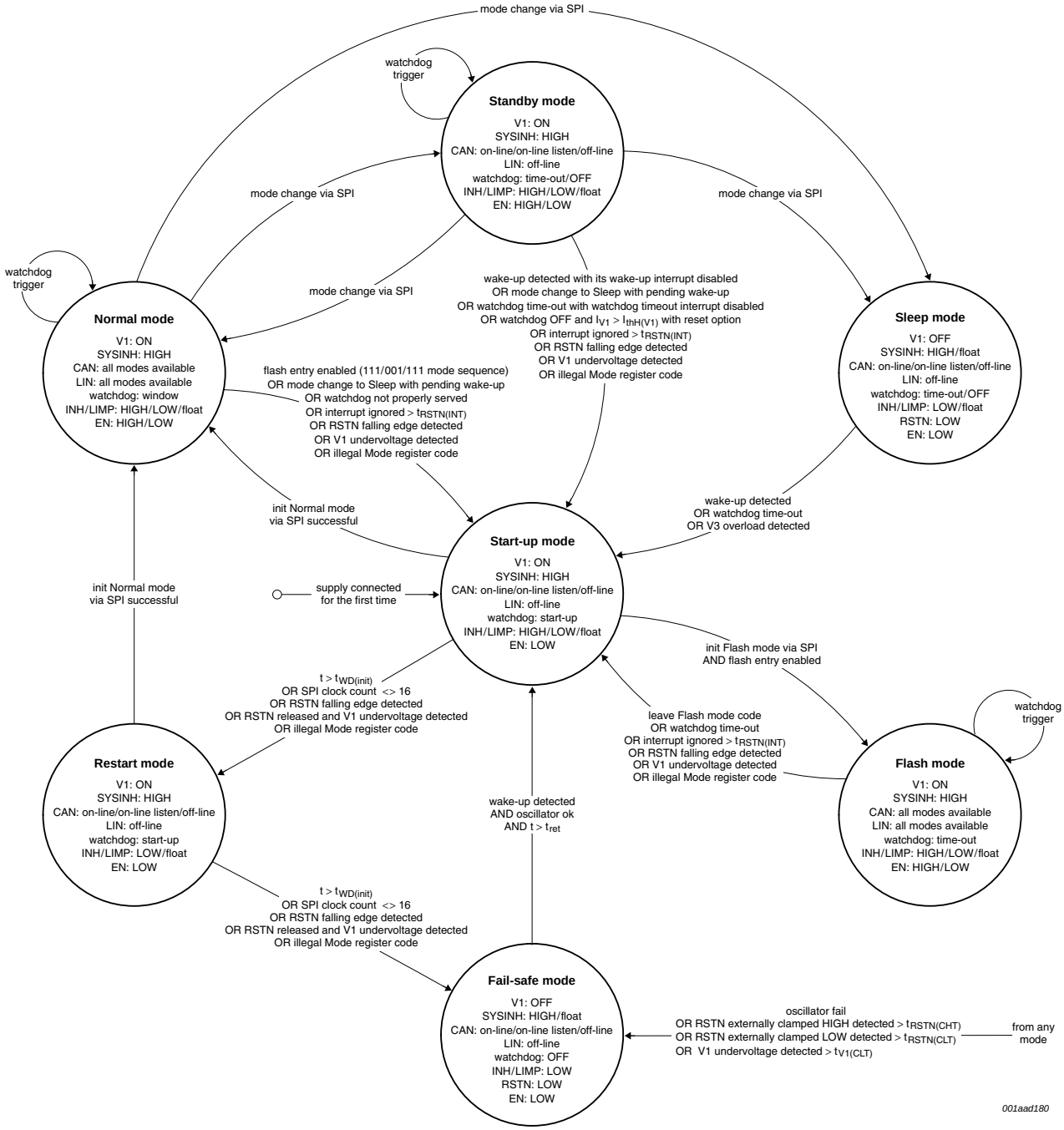


Fig 3. Main state diagram

6.2.1 Start-up mode

Start-up mode is the ‘home page’ of the SBC. This mode is entered when battery and ground are connected for the first time. Start-up mode is also entered after any event that results in a system reset. The reset source information is provided by the SBC to support different software initialization cycles that depend on the reset event.

It is also possible to enter Start-up mode via a wake-up from Standby mode, Sleep mode or Fail-safe mode. Such a wake-up can originate either from the CAN-bus, the LIN-bus or from the local WAKE pin.

On entering Start-up mode a lengthened reset time t_{RSTNL} is observed. This reset time is either user-defined (via the RLC bit in the System Configuration register) or defaults to the value as given in Section 6.13.12. During the reset lengthening time pin RSTN is held LOW by the SBC.

When the reset time is completed (pin RSTN is released and goes HIGH) the watchdog timer will wait for initialization. If the watchdog initialization is successful, the selected operating mode (Normal mode or Flash mode) will be entered. Otherwise the Restart mode will be entered.

6.2.2 Restart mode

The purpose of the Restart mode is to give the application a second chance to start up, should the first attempt from Start-up mode fail. Entering Restart mode will always set the reset lengthening time t_{RSTNL} to the higher value to guarantee the maximum reset length, regardless of previous events.

If start-up from Restart mode is successful (the previous problems do not reoccur and watchdog initialization is successful), then the selected operating mode will be entered. From Restart mode this must be Normal mode. If problems persist or if V1 fails to start up, then Fail-safe mode will be entered.

6.2.3 Fail-safe mode

Severe fault situations will cause the SBC to enter Fail-safe mode. Fail-safe mode is also entered if start-up from Restart mode fails. Fail-safe mode offers the lowest possible system power consumption from the SBC and from the external components controlled by the SBC.

A wake-up (via the CAN-bus, the LIN-bus or the WAKE pin) is needed to leave Fail-safe mode. This is only possible if the on-chip oscillator is running correctly. The SBC restarts from Fail-safe mode with a defined delay t_{ret}, to guarantee a discharged V1 before entering Start-up mode. Regulator V1 will restart and the reset lengthening time t_{RSTNL} is set to the higher value; see Section 6.5.1.

6.2.4 Normal mode

Normal mode gives access to all SBC system resources, including CAN, LIN, INH/LIMP and EN. Therefore in Normal mode the SBC watchdog runs in (programmable) Window mode, for strictest software supervision. Whenever the watchdog is not properly served a system reset is performed.

Interrupts from SBC to the host microcontroller are also monitored. A system reset is performed if the host microcontroller does not respond within $t_{RSTN(INT)}$.

Entering Normal mode does not activate the CAN or LIN transceiver automatically. The CAN Mode Control (CMC) bit must be used to activate the CAN medium if required, allowing local cyclic wake-up scenarios to be implemented without affecting the CAN-bus. The LIN Mode Control (LMC) bit must be used to activate the LIN medium if required, allowing local cyclic wake-up scenarios to be implemented without affecting the LIN-bus.

6.2.5 Standby mode

In Standby mode the system is set into a state with reduced current consumption. Entering Standby mode overrides the CMC bit, allowing the CAN transceiver to enter the low-power mode autonomously. The watchdog will, however, continue to monitor the microcontroller (Time-out mode) since it is powered via pin V1.

In the event that the host microcontroller can provide a low-power mode with reduced current consumption in its Standby mode or Stop mode, the watchdog can be switched off entirely in Standby mode of the SBC. The SBC monitors the microcontroller supply current to ensure that there is no unobserved phase with disabled watchdog and running microcontroller. The watchdog will remain active until the supply current drops below $I_{thL(V1)}$. Below this current limit the watchdog is disabled.

Should the current increase to $I_{thH(V1)}$, e.g. as result of a microcontroller wake-up from application specific hardware, the watchdog will start operating again with the previously used time-out period. If the watchdog is not triggered correctly, a system reset will occur and the SBC will enter Start-up mode.

If Standby mode is entered from Normal mode with the selected watchdog OFF option, the watchdog will use the maximum time-out as defined for Standby mode until the supply current drops below the current detection threshold; the watchdog is now OFF. If the current increases again, the watchdog is immediately activated, again using the maximum watchdog time-out period. If the watchdog OFF option is selected during Standby mode, the last used watchdog period will define the time for the supply current to fall below the current detection threshold. This allows the user to align the current supervisor function to the application needs.

Generally, the microcontroller can be activated from Standby mode via a system reset or via an interrupt without reset. This allows implementation of differentiated start-up behavior from Standby mode, depending on the application needs:

- If the watchdog is still running during Standby mode, the watchdog can be used for cyclic wake-up behavior of the system. A dedicated Watchdog Time-out Interrupt Enable (WTIE) bit enables the microcontroller to decide whether to receive an interrupt or a hardware reset upon overflow. The interrupt option will be cleared in hardware automatically with each watchdog overflow to ensure that a failing main routine is detected while the interrupt service still operates. So the application software must set the interrupt behavior each time before a standby cycle is entered.
- Any wake-up via the CAN-bus or the LIN-bus together with a local wake-up event will force a system reset event or an interrupt to the microcontroller. So it is possible to exit Standby mode without any system reset if required.

When an interrupt event occurs the application software has to read the Interrupt register within $t_{RSTN(INT)}$. Otherwise a fail-safe system reset is forced and Start-up mode will be entered. If the application has read out the Interrupt register within the specified time, it can decide whether to switch into Normal mode via an SPI access or to stay in Standby mode.

The following operations are possible from Standby mode:

- Cyclic wake-up by the watchdog via an interrupt signal to the microcontroller (the microcontroller is triggered periodically and checked for the correct response)
- Cyclic wake-up by the watchdog via a reset signal (a reset is performed periodically; the SBC provides information about the reset source to allow different start sequences after reset)
- Wake-up by activity on the CAN-bus or LIN-bus via an interrupt signal to the microcontroller
- Wake-up by bus activity on the CAN-bus or LIN-bus via a reset signal
- Wake-up by increasing the microcontroller supply current without a reset signal (where a stable supply is needed for the microcontroller RAM contents to remain valid and wake-up from an external application not connected to the SBC)
- Wake-up by increasing the microcontroller supply current with a reset signal
- Wake-up due to a falling edge at pin WAKE forcing an interrupt to the microcontroller
- Wake-up due to a falling edge at pin WAKE forcing a reset signal

6.2.6 Sleep mode

In Sleep mode the microcontroller power supply (V1) and the INH/LIMP controlled external supplies are switched off entirely, resulting in minimum system power consumption. In this mode, the watchdog runs in Time-out mode or is completely off.

Entering Sleep mode results in an immediate LOW level on pin RSTN, thus stopping any operation of the microcontroller. The INH/LIMP output is floating in parallel and pin V1 is disabled. Only pin SYSINH can remain active to support the V2 voltage supply; this depends on the V2C bit. It is also possible for V3 to be On, Off or in Cyclic mode to supply external wake-up switches.

If the watchdog is not disabled in software, it will continue to run and force a system reset upon overflow of the programmed period time. The SBC enters Start-up mode and pin V1 becomes active again. This behavior can be used for a cyclic wake-up from Sleep mode.

Depending on the application, the following operations can be selected from Sleep mode:

- Cyclic wake-up by the watchdog (only in Time-out mode); a reset is performed periodically, the SBC provides information about the reset source to allow different start sequences after reset
- Wake-up by activity on the CAN-bus, LIN-bus or falling edge at pin WAKE
- An overload on V3, only if V3 is in a cyclic or in continuously on mode

6.2.7 Flash mode

Flash mode can only be entered from Normal mode by entering a specific Flash mode entry sequence. This fail-safe control sequence comprises three consecutive write accesses to the Mode register, within the legal windows of the watchdog, using the operating mode codes 111, 001 and 111 respectively. As a result of this sequence, the SBC will enter Start-up mode and perform a system reset with the related reset source information (bits RSS = 0110).

From Start-up mode the application software now has to enter Flash mode within $t_{WD(init)}$ by writing Operating Mode code 011 to the Mode register. This feeds back a successfully received hardware reset (handshake between the SBC and the microcontroller). The transition from Start-up mode to Flash mode is possible only once after completing the Flash entry sequence.

The application can also decide not to enter Flash mode but to return to Normal mode by using the Operating Mode code 101 for handshaking. This erases the Flash mode entry sequence.

The watchdog behavior in Flash mode is similar to its time-out behavior in Standby mode, but Operating Mode code 111 must be used for serving the watchdog. If this code is not used or if the watchdog overflows, the SBC immediately forces a reset and enters Start-up mode. Flash mode is properly exited using the Operating Mode code 110 (leave Flash mode), which results in a system reset with the corresponding reset source information. Other Mode register codes will cause a forced reset with reset source code ‘illegal Mode register code’.

6.3 On-chip oscillator

The on-chip oscillator provides the clock signal for all digital functions and is the timing reference for the on-chip watchdog and the internal timers.

If the on-chip oscillator frequency is too low or the oscillator is not running at all, there is an immediate transition to Fail-safe mode. The SBC will stay in Fail-safe mode until the oscillator has recovered to its normal frequency and the system receives a wake-up event.

6.4 Watchdog

The watchdog provides the following timing functions:

- Start-up mode; needed to give the software the opportunity to initialize the system
- Window mode; detects too early and too late accesses in Normal mode
- Time-out mode; detects a too late access, can also be used to restart or interrupt the microcontroller from time to time (cyclic wake-up function)
- Off mode; fail-safe shut-down during operation thus preventing any blind spots in the system supervision

The watchdog is clocked directly by the on-chip oscillator.

To guarantee fail-safe control of the watchdog via the SPI, all watchdog accesses are coded with redundant bits. Therefore, only certain codes are allowed for a proper watchdog service.

The following corrupted watchdog accesses result in an immediate system reset:

- Illegal watchdog period coding; only ten different codes are valid
- Illegal operating mode coding; only six different codes are valid

Any microcontroller driven mode change is synchronized with a watchdog access by reading the mode information and the watchdog period information from the same register. This enables an easy software flow control with defined watchdog behavior when switching between different software modules.

6.4.1 Watchdog start-up behavior

Following any reset event the watchdog is used to monitor the ECU start-up procedure. It observes the behavior of the RSTN pin for any clamping condition or interrupted reset wire. In case the watchdog is not properly served within $t_{WD(init)}$, another reset is forced and the monitoring procedure is restarted. In case the watchdog is again not properly served, the system enters Fail-safe mode (see also Figure 3, Start-up and Restart modes).

6.4.2 Watchdog window behavior

Whenever the SBC enters Normal mode, the Window mode of the watchdog is activated. This ensures that the microcontroller operates within the required speed; a too fast as well as a too slow operation will be detected. Watchdog triggering using the Window mode is illustrated in Figure 4.

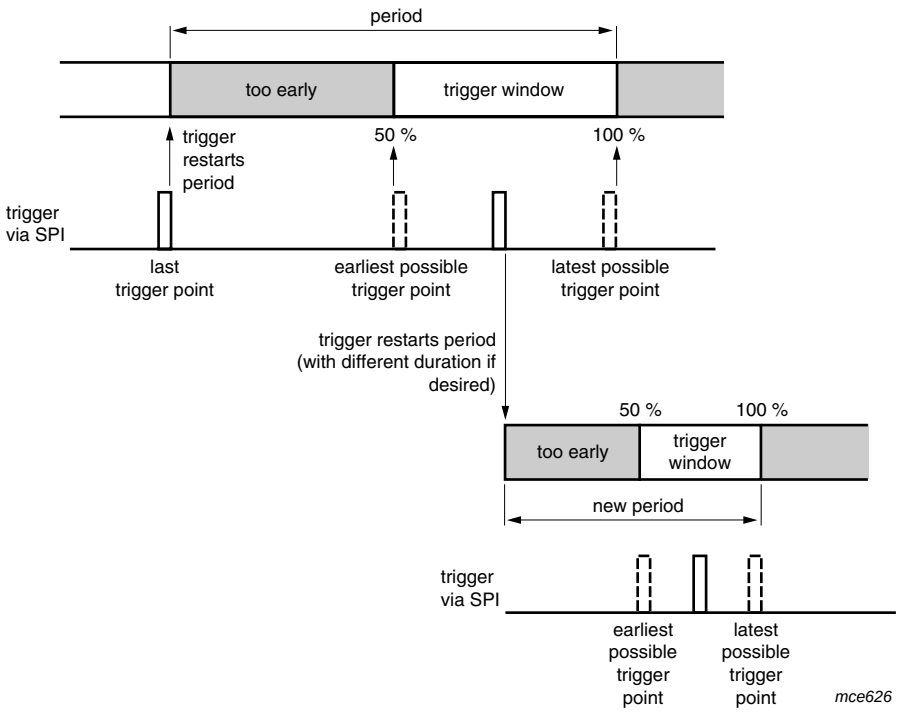


Fig 4. Watchdog triggering using Window mode

The SBC provides 10 different period timings, scalable with a 4-factor watchdog prescaler. The period can be changed within any valid trigger window. Whenever the watchdog is triggered within the window time, the timer will be reset to start a new period.

The watchdog window is defined to be between 50 % and 100 % of the nominal programmed watchdog period. Any too early or too late watchdog access or wrong Mode register code access will result in an immediate system reset, entering Start-up mode.

6.4.3 Watchdog time-out behavior

Whenever the SBC operates in Standby mode, in Sleep mode or in Flash mode, the active watchdog operates in Time-out mode. The watchdog has to be triggered within the actual programmed period time; see Figure 5. The Time-out mode can be used to provide cyclic wake-up events to the host microcontroller from Standby and Sleep modes.

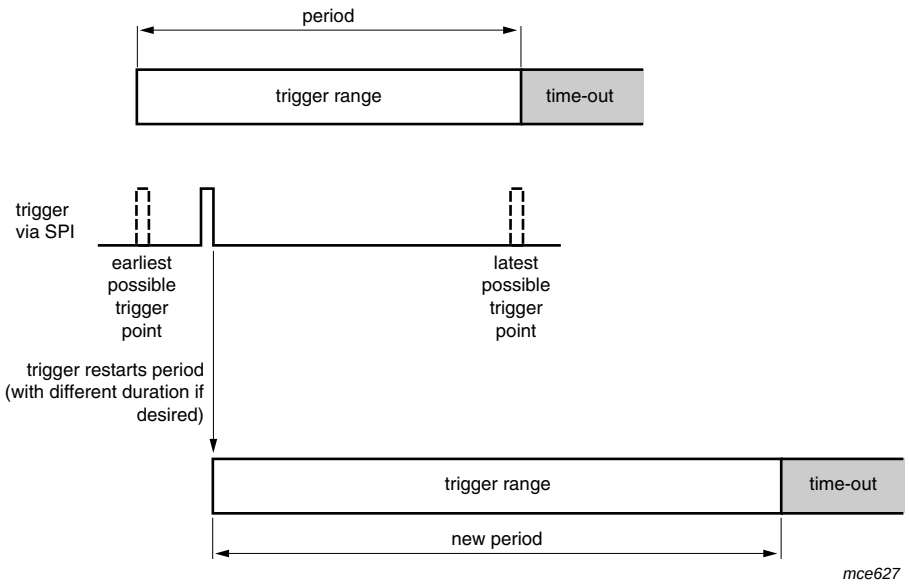


Fig 5. Watchdog triggering using Time-out mode

In Standby and in Flash mode the nominal periods can be changed with any SPI access to the Mode register.

Any illegal watchdog trigger code results in an immediate system reset, entering Start-up mode.

6.4.4 Watchdog OFF behavior

It is possible to switch the watchdog off completely In Standby and Sleep modes. For fail-safe reasons this is only possible if the microcontroller has stopped program execution. To ensure that there is no program execution, the V1 supply current is monitored by the SBC while the watchdog is switched off.

When selecting the watchdog OFF code, the watchdog remains active until the microcontroller supply current has dropped below the current monitoring threshold $I_{thL(V1)}$. After the supply current has dropped below the threshold, the watchdog stops at the end of the watchdog period. In case the supply current does not drop below the monitoring threshold, the watchdog stays active.

If the microcontroller supply current increases above $I_{thH(V1)}$ while the watchdog is OFF, the watchdog is restarted with the last used watchdog period time and a watchdog restart interrupt is forced, if enabled.

In case of a direct mode change towards Standby mode with watchdog OFF selected, the longest possible watchdog period is used. It should be noted that in Sleep mode V1 current monitoring is not active.

6.5 System reset

The reset function of the UJA1061 offers two signals to deal with reset events:

- RSTN; the global ECU system reset
- EN; a fail-safe global enable signal

6.5.1 RSTN pin

The system reset pin (RSTN) is a bidirectional input / output. Pin RSTN is active LOW with selectable pulse length upon the following events; see Figure 3:

- Power-on (first battery connection) or V_{BAT42} below power-on reset threshold voltage
- Low V1 supply
- V1 current above threshold during Standby mode while watchdog OFF behavior is selected
- V3 is down due to short-circuit condition during Sleep mode
- RSTN externally forced LOW, falling edge event
- Successful preparation for Flash mode completed
- Successful exit from Flash mode
- Wake-up from Standby mode via pins CAN, LIN or WAKE if programmed accordingly, or any wake-up event from Sleep mode
- Wake-up event from Fail-safe mode
- Watchdog trigger failures (too early, overflow, wrong code)
- Illegal mode code via SPI applied
- Interrupt not served within $t_{RSTN(INT)}$

All of these reset events have a dedicated reset source in the System Status register to allow distinction between the different events.

The SBC will lengthen any reset event to 1 ms or 20 ms to ensure that external hardware is properly reset. After the first battery connection, a short power-on reset of 1 ms is provided after voltage V1 is present. Once started, the microcontroller can set the Reset Length Control (RLC) bit within the System Configuration register; this allows the reset pulse to be adjusted for future reset events. With this bit set, all reset events are lengthened to 20 ms. Due to fail-safe behavior, this bit will be set automatically (to 20 ms) in Restart mode or Fail-safe mode. With this mechanism it is guaranteed that an erroneously shortened reset pulse will restart any microcontroller, at least within the second trial by using the long reset pulse.

The behavior of pin RSTN is illustrated in Figure 6. The duration of t_{RSTNL} depends on the setting of the RLC bit (defines the reset length). Once an external reset event is detected the system controller enters the Start-up mode. The watchdog now starts to monitor pin RSTN as illustrated in Figure 7. If the RSTN pin is not released in time then Fail-safe mode is entered as shown in Figure 3.

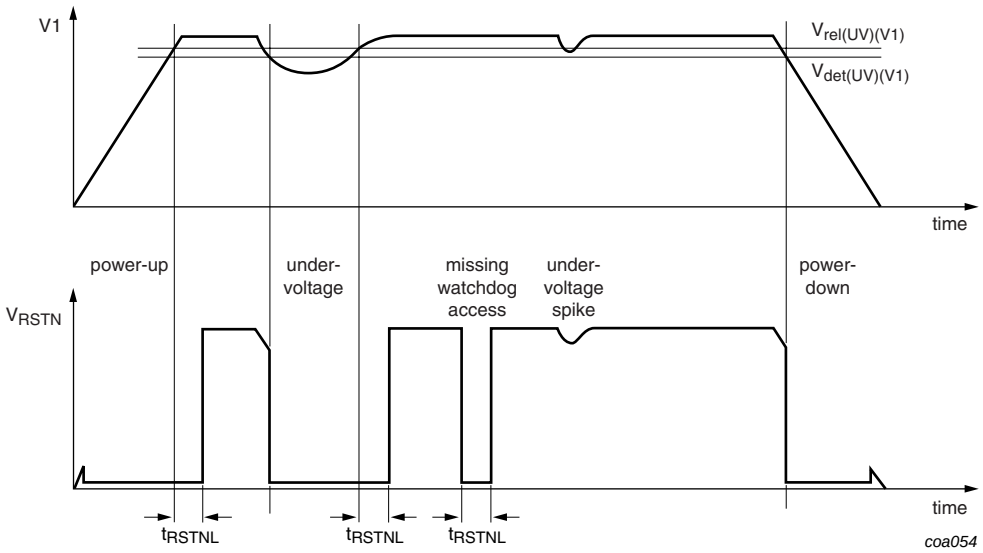


Fig 6. Reset pin behavior

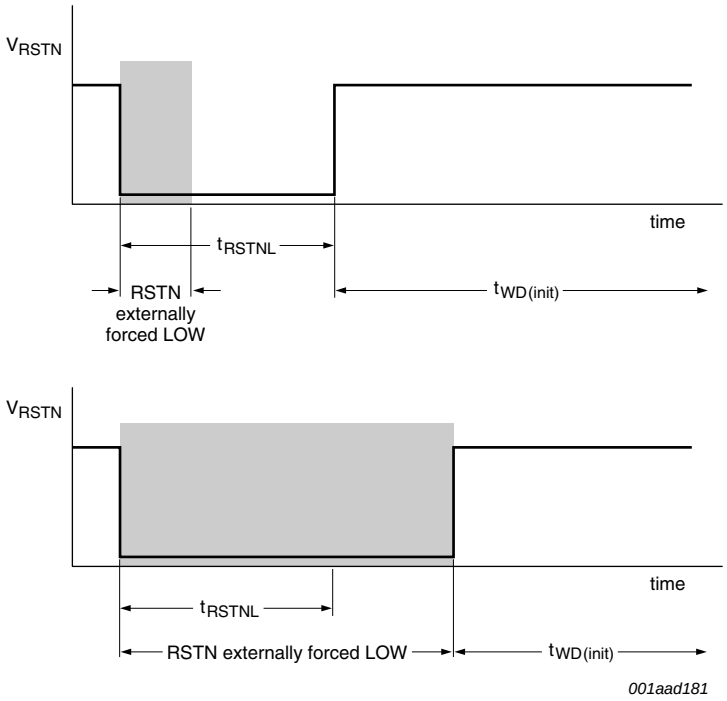


Fig 7. Reset timing diagram

Pin RSTN is monitored for a continuously clamped LOW situation. Once the SBC pulls pin RSTN HIGH but pin RSTN level remains LOW for longer than $t_{RSTN(CLT)}$, the SBC immediately enters Fail-safe mode since this indicates an application failure.

The SBC also detects if pin RSTN is clamped HIGH. If the HIGH-level remains on the pin for longer than $t_{RSTN(CHT)}$ while pin RSTN is driven internally to a LOW-level by the SBC, the SBC falls back immediately to Fail-safe mode since the microcontroller cannot be reset any more. By entering Fail-safe mode, the V1 voltage regulator shuts down and the microcontroller stops.

Additionally, chattering reset signals are handled by the SBC in such a way that the system safely falls back to Fail-safe mode with the lowest possible power consumption.

6.5.2 EN output

Pin EN can be used to control external hardware such as power components or as a general purpose output if the system is running properly. During all reset events, when pin RSTN is pulled LOW, the EN control bit will be cleared, pin EN will be pulled LOW and will stay LOW after pin RSTN is released. In Normal mode and Flash mode of the SBC, the microcontroller can set the EN control bit via the SPI. This results in releasing pin EN which then returns to a HIGH-level.

6.6 Power supplies

6.6.1 BAT14, BAT42 and SYSINH

The SBC has two supply pins, pin BAT42 and pin BAT14. Pin BAT42 supplies most of the SBC where pin BAT14 only supplies the linear voltage regulators and the INH/LIMP output pin. This supply architecture allows different supply strategies including the use of external DC-to-DC converters controlled by the pin SYSINH.

6.6.1.1 SYSINH output

The SYSINH output is a high-side switch from BAT42. It is activated whenever the SBC requires supply voltage to pin BAT14, e.g. when V1 or V2 is on (see Figure 3 and Figure 8). Otherwise pin SYSINH is floating. Pin SYSINH can be used to control e.g. an external step-down voltage regulator to pin BAT14, to reduce power consumption in low-power modes.

6.6.2 Voltage regulators V1 and V2

The UJA1061 has two independent voltage regulators supplied out of the BAT14 pin. Regulator V1 is intended to supply the microcontroller. Regulator V2 is reserved for the CAN transceiver.

6.6.2.1 Voltage regulator V1

The V1 voltage is continuously monitored to provide the system reset signal when undervoltage situations occur. Whenever the V1 voltage falls below one of the three programmable thresholds, a hardware reset is forced.

A dedicated V1 supply comparator (V1 Monitor) observes V1 for undervoltage events lower than $V_{UV(VFI)}$. This allows the application to receive a supply warning interrupt in case one of the lower V1 undervoltage reset thresholds is selected.

The V1 regulator is overload protected. The maximum output current available from pin V1 depends on the voltage applied at pin BAT14 (see Table 26). For thermal reasons, the total power dissipation should be taken into account.

6.6.2.2 Voltage regulator V2

Voltage regulator V2 provides a 5 V supply for the CAN transmitter. The pin V2 is intended for the connection of external buffering capacitors.

V2 is controlled autonomously by the CAN transceiver control system and is activated on any detected CAN-bus activity, or if the CAN transceiver is enabled by the application microcontroller. V2 is short-circuit protected and will be disabled in case of an overload situation. Dedicated bits in the System Diagnosis register and the Interrupt register provide V2 status feedback to the application.

Besides the autonomous control of V2 there is a software accessible bit which allows activation of V2 manually (V2C). This allows V2 to be used for other application purposes when CAN is not actively used (e.g. while CAN is off-line). Generally, V2 should not be used for other application hardware while CAN is in use.

If the regulator V2 is not able to start within the V2 clamped LOW time (> $t_{V2(CLT)}$), or if a short-circuit has been detected during an already activated V2, then V2 is disabled and the V2D bit in the System Diagnosis register is cleared. Additionally the CTC bit in the Physical Layer Control register is set and the V2C bit is cleared.

Reactivation of voltage regulator V2 can be done by:

- Clearing the CTC bit while CAN is in Active mode
- Wake-up via CAN while CAN is not in Active mode
- Setting the V2C bit
- When entering CAN Active mode

6.6.3 Switched battery output V3

V3 is a high-side switched BAT42-related output which is used to drive external loads such as wake-up switches or relays. The features of V3 are as follows:

- Three application-controlled operating modes; On, Off and Cyclic.
- Two different cyclic modes allow the supply of external wake-up switches; these switches are powered intermittently, thus reducing the system's power consumption in case a switch is continuously active; the wake-up input of the SBC is synchronized with the V3 cycle time.
- The switch is protected against current overloads. If V3 is overloaded, pin V3 is automatically disabled. The corresponding System Diagnosis register bit is reset and an interrupt is forced (if enabled). During Sleep mode, a wake-up is forced and the corresponding reset source code becomes available in the RSS bits of the System Status register. This signals that the wake-up source via V3 supplied wake-up switches has been lost.

6.7 CAN transceiver

The integrated fault-tolerant CAN transceiver of the UJA1061 is an advanced ISO11898-3 compliant transceiver and is interoperable with the TJA1054 and TJA1054A stand-alone transceivers. In addition to standard fault-tolerant CAN transceivers the UJA1061 transceiver provides the following features:

- Enhanced error handling and reporting of bus and RXD/TXD failures; these failures are separately identified in the System Diagnosis register
- Integrated autonomous control system for determining the mode of the CAN transceiver
- Ground shift detection with two selectable warning levels, to detect possible local ground problems before the CAN communication is affected
- On-line Listen mode with global wake-up message filter allows partial networking
- Bus connections are truly floating when power is off

6.7.1 Mode control

The controller of the CAN transceiver provides four modes of operation: Active mode, On-line mode, On-line Listen mode and Off-line mode; see Figure 8.

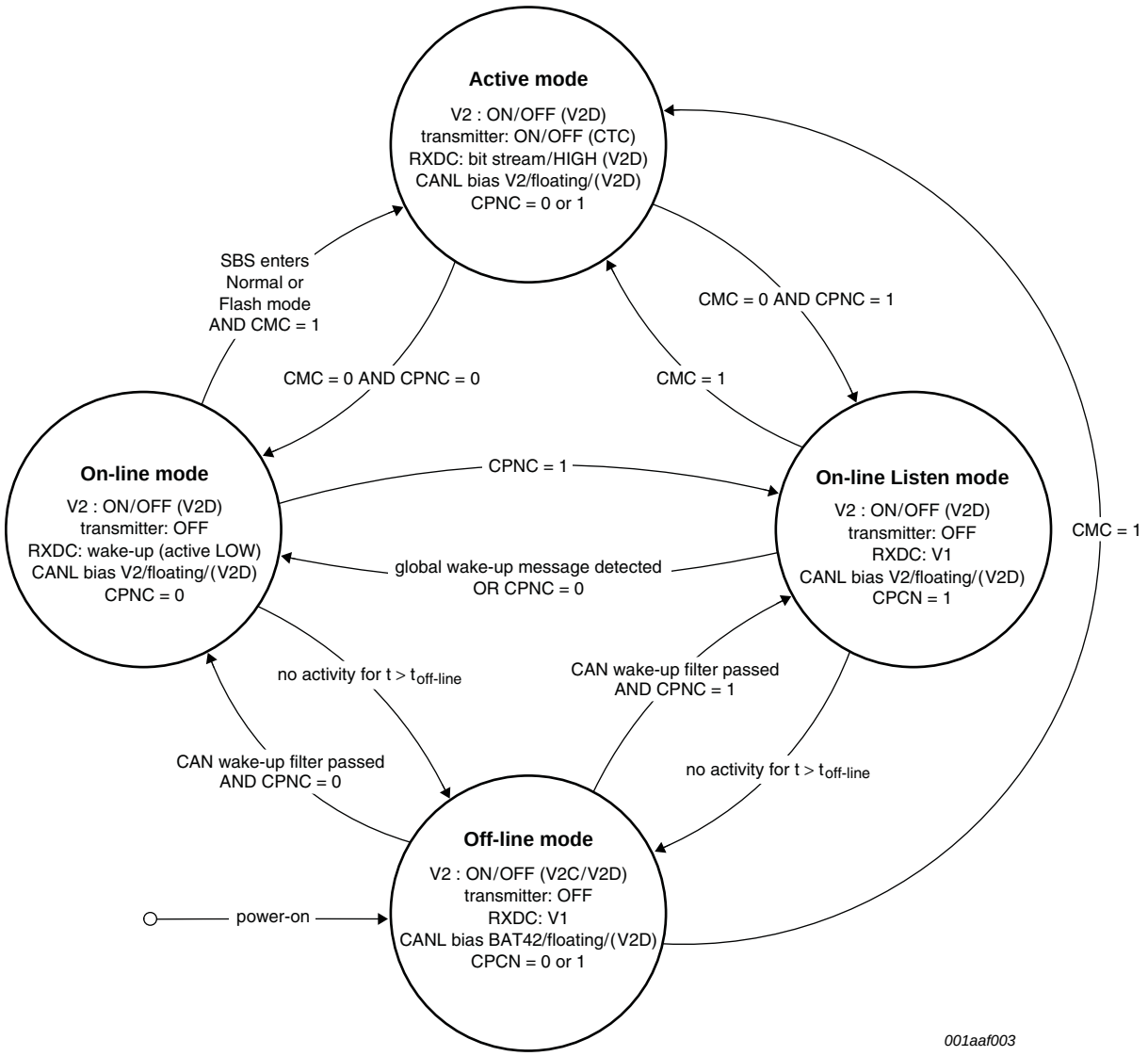


Fig 8. States of the CAN transceiver

In the System Diagnosis register two dedicated CAN status bits (CANMD) are available to signal the mode of the transceiver.

6.7.1.1 Active mode

In Active mode the CAN transceiver can transmit data to and receive data from the CAN bus. To enter Active mode the CMC bit must be set in the Physical Layer Control register and the SBC must be in Normal mode or Flash mode. In Active mode voltage regulator V2 is activated automatically.

The CTC bit can be used to set the CAN transceiver to a Listen-only mode. The transmitter output stage is disabled in this mode.

After an overload condition on voltage regulator V2, the CTC bit must be cleared for reactivating the CAN transmitter.

When leaving Active mode the CAN transmitter is disabled and the CAN receiver is monitoring the CAN-bus for a valid wake-up. The CAN termination is then working autonomously.

6.7.1.2 On-line mode

In On-line mode the CAN bus pins and RTL and RTH pins are biased to the normal levels. The CAN transmitter is deactivated and RXDC reflects the CAN wake-up status. A CAN wake-up event is signalled to the microcontroller by setting pin RXDC to LOW.

If the bus stays continuously dominant or recessive for the Off-line time ($t_{off\text{-}line}$), the Off-line state will be entered.

6.7.1.3 On-line Listen mode

On-line Listen mode behaves similar to On-line mode, but all activity on the CAN-bus, with exception of a special global wake-up request, is ignored. The global wake-up request is described in Section 6.7.2. Pin RXDC is kept HIGH.

6.7.1.4 Off-line mode

Off-line mode is the low-power mode of the CAN transceiver. The CAN transceiver is disabled to save supply current and is high-ohmic terminated to ground.

The CAN off-line time is programmable in two steps with the CAN Off-line Timer Control (COTC) bit. When entering On-line (Listen) mode from Off-line mode the CAN off-line time is temporarily extended to $t_{off\text{-}line(ext)}$.

6.7.2 CAN wake-up

To wake-up the UJA1061 via CAN it has to be distinguished between a conventional wake-up and a global wake-up in case partial networking is enabled (bit CPNC = 1).

To pass the wake-up filter for a conventional wake-up a dominant, recessive, dominant signal on the CAN-bus is needed.

For a global wake-up out of On-line Listen mode two distinct CAN data patterns are required (shown in hexadecimal code here):

- In the Initial message: C6EE EEEE EEEE EEEF
- In the Global wake-up message: C6EE EEEE EEEE EE37

The second pattern must be received within $t_{timeout}$ after receiving the first pattern. Any CAN-ID can be used with these data patterns.

If the CAN transceiver enters On-line Listen mode directly from Off-line mode the global wake-up message is sufficient to wake-up the SBC. This pattern must be received within $t_{timeout}$ after entering On-line Listen mode. Should $t_{timeout}$ elapse before receiving the global wake-up message, then both messages are required for a CAN wake-up.

6.7.3 Termination control

In Active mode, On-line mode and On-line Listen mode, CANH is terminated to GND and CANL is terminated to pin V2 via the external termination resistors applied to RTH and RTL. In case of detected bus failures, the termination changes according to the ISO 11898-3 standard. In Off-line mode pin CANH stays terminated to GND but with a diode in

between (reverse supply protection) while pin CANL becomes terminated to pin BAT42 (via pin RTH and pin RTL). If pin V2 is disabled due to an overload condition RTH and RTL become floating.

6.7.4 Bus, RXD and TXD failure detection

The UJA1061 can distinguish between bus, RXD and TXD failures as indicated in Table 3.

All failures are signalled separately in the CANFD bits in the System Diagnosis register. Any change (detection and recovery) forces an interrupt to the microcontroller, if this interrupt is enabled.

Table 3. CAN-bus, RXD and TXD failure detection

Failure	Description	Driver and biasing circuit disabling
HxVCC	CANH to V_{CC} (5 V) short-circuit	CANH off, weak RTH
HxBAT	CANH to BAT (14 V and 42 V) short-circuit	CANH off, weak RTH
HxGND	CANH to GND short-circuit	none
LxBAT	CANL to BAT (14 V and 42 V) short-circuit	CANL off, weak RTL[1]
LxGND	CANL to GND short-circuit	CANL off, weak RTL
LxVCC	CANL to V_{CC} (5 V) short-circuit	none
HxL	CANH to CANL short-circuit	CANL off, weak RTL
H//	CANH interrupted	none
L//	CANL interrupted	none
Bus Dom	bus is continuously clamped dominant (double failure); even within Single-wire mode the receiver remains dominant	CANL off, weak RTL
Bus Rec	bus is continuously clamped recessive (double failure); driving messages to the bus is not possible even while the driver is active	none
TxDC Dom	pin TXDC is continuously clamped dominant (handles also RXDC to TXDC short-circuits)	transmitter disabled but no change in biasing
RxDC Rec	pin RXDC is continuously clamped recessive	transmitter disabled but no change in biasing
RxDC Dom	pin RXDC is continuously clamped dominant	none

[1] CANL stays active with weak short-circuits to BAT due to wake-up requirements within large networks.

6.7.4.1 TXDC dominant clamping

If the TXDC pin is clamped dominant for longer than $t_{TXDC(dom)}$ the CAN transmitter is disabled. After the TXDC pin becomes recessive the transmitter is reactivated automatically when detecting bus activity or manually by setting and clearing the CTC bit.

6.7.4.2 RXDC recessive clamping

If the RXDC pin is clamped recessive while the CAN bus is dominant the CAN transmitter is disabled. The transmitter is reactivated automatically when RXDC becomes dominant or manually by setting and clearing the CTC bit.

6.7.4.3 GND shift detection

The SBC can detect ground shifts in reference to the CAN bus. Two different ground shift detection levels can be selected with the GSTHC bit in the System Configuration register. The failure can be read out in the System Diagnosis register. Any detected or recovered GND shift event is signalled with an interrupt, if enabled.

6.8 LIN transceiver

The integrated LIN transceiver of the UJA1061 is a LIN 2.0 compliant transceiver. The transceiver has the following features:

- SAE J2602 compliant and compatible with LIN revision 1.3
- Fail-safe LIN termination to BAT42 via dedicated RTLIN pin
- Enhanced error handling and reporting of bus and TXD failures; these failures are separately identified in the System Diagnosis register

6.8.1 Mode control

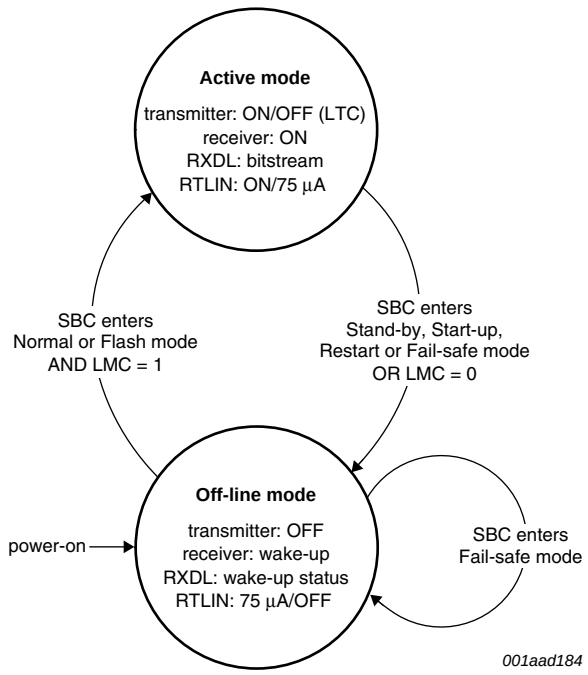


Fig 9. States LIN transceiver

The controller of the LIN transceiver provides two modes of operation: Active mode and Off-line mode; see Figure 9. In Off-line mode the transmitter and receiver do not consume current, but wake-up events will be recognized by the separate wake-up receiver.

6.8.1.1 Active mode

In Active mode the LIN transceiver can transmit data to and receive data from the LIN bus. To enter Active mode the LMC bit must be set in the Physical Layer Control register and the SBC must be in Normal mode or Flash mode.

The LTC bit can be used to set the LIN transceiver to a Listen-only mode. The transmitter output stage is disabled in this mode.

When leaving Active mode the LIN transmitter is disabled and the LIN receiver is monitoring the LIN-bus for a valid wake-up.

6.8.1.2 Off-line mode

Off-line mode is the low power mode of the LIN transceiver. The LIN transceiver is disabled to save supply current. Pin RXDL reflects any wake-up event at the LIN-bus.

6.8.2 LIN wake-up

For a remote wake-up via LIN a LIN-bus signal is required as shown in Figure 10.

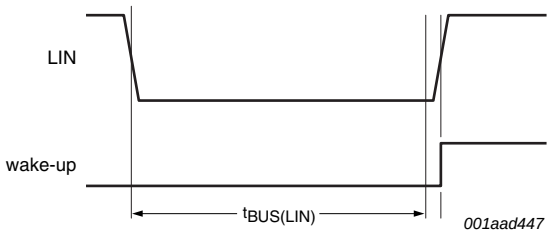


Fig 10. LIN wake-up timing diagram

6.8.3 Termination control

The RTLIN pin is in one of 3 different states: RTLIN = on, RTLIN = off or RTLIN = 75 μA; see Figure 11.

During Active mode, with no short-circuit between the LIN-bus and GND, pin RTLIN provides an internal switch to BAT42. For master and slave operation an external resistor, 1 kΩ or 30 kΩ respectively, can be applied between pins RTLIN and LIN. An external diode in series with the termination resistor is not required due to the incorporated internal diode.

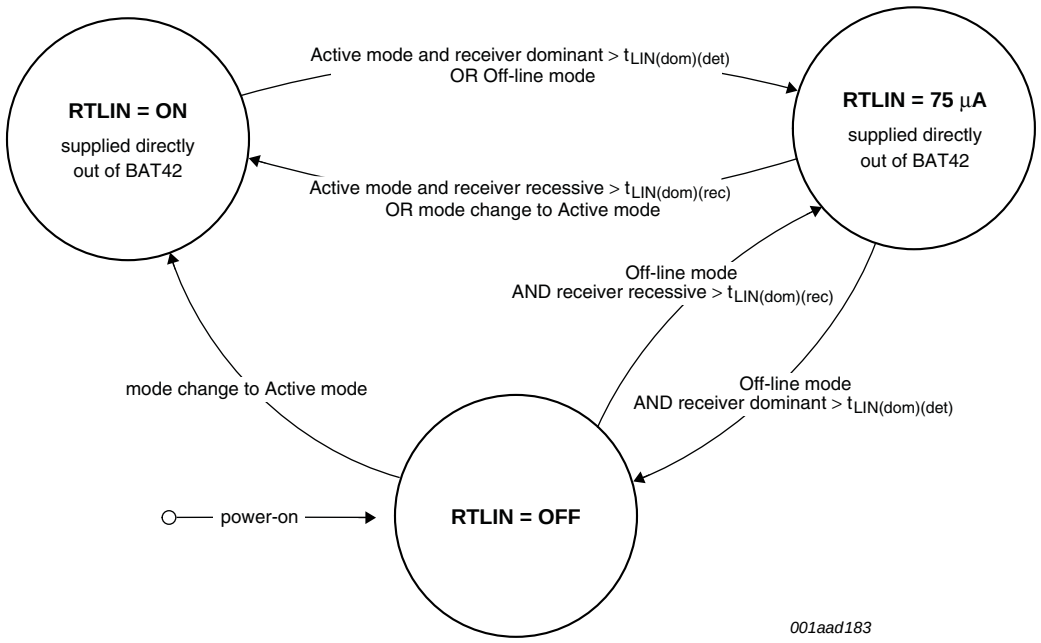


Fig 11. States of the RTLIN pin

6.8.4 LIN slope control

The LSC bit in the Physical Layer Control register offers a choice between two LIN slope times, allowing communication up to 20 kbit/s (normal) or up to 10.4 kbit/s (low slope).

6.8.5 LIN driver capability

Setting the LDC bit in the Physical Layer Control register will increase the driver capability of the LIN output stage. This feature is used in auto-addressing systems, where the standard LIN 2.0 drive capability is insufficient.

6.8.6 Bus and TXDL failure detection

The SBC handles and reports the following LIN-bus related failures:

- LIN-bus shorted to ground
- LIN-bus shorted to V_{BAT14} or V_{BAT42}; the transmitter is disabled
- TXDL clamped dominant; the transmitter is disabled

These failure events force an interrupt to the microcontroller whenever the status changes and the corresponding interrupt is enabled.

6.8.6.1 TXDL dominant clamping

If the TXDL pin is clamped dominant for longer than $t_{TXDL(dom)(dis)}$ the LIN transmitter is disabled. After the TXDL pin becomes recessive the transmitter is reactivated automatically when detecting bus activity or manually by setting and clearing the LTC bit.

6.8.6.2 LIN dominant clamping

When the LIN-bus is clamped dominant for longer than $t_{LIN(dom)(det)}$ (which is longer than $t_{TXDL(dom)(dis)}$), the state of the LIN termination is changed according to Figure 11.

6.8.6.3 LIN recessive clamping

If the LIN bus pin is clamped recessive while TXDL is driven dominant the LIN transmitter is disabled. The transmitter is reactivated automatically when the LIN bus becomes dominant or manually by setting and clearing the LTC bit.

6.9 Inhibit and limp-home output

The INH/LIMP output pin is a 3-state output pin which can be used either as an inhibit for an extra (external) voltage regulator, or as a 'limp-home' output. The pin is controlled via the ILEN bit and ILC bit in the System Configuration register; see Figure 12.

When pin INH/LIMP is used as inhibit output, a pull-down resistor to GND ensures a default LOW level. The pin can be set to HIGH according to the state diagram.

When pin INH/LIMP is used as limp-home output, a pull-up resistor to V_{BAT42} ensures a default HIGH level. The pin is automatically set to LOW when the SBC enters Fail-safe mode.

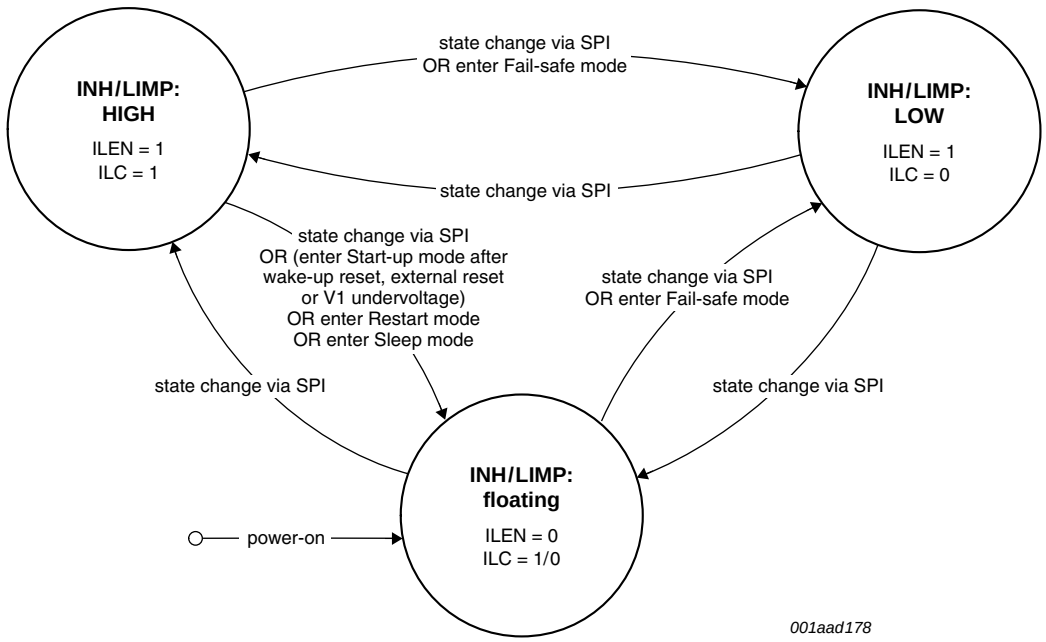


Fig 12. States of the INH/LIMP pin

6.10 Wake-up input

The WAKE input comparator is triggered by negative edges on pin WAKE. Pin WAKE has an internal pull-up resistor to BAT42. It can be operated in two sampling modes which are selected via the WAKE Sample Control bit (WSC):

- Continuous sampling (with an internal clock) if the bit is set
- Sampling synchronized to the cyclic behavior of V3 if the bit is cleared; see Figure 13. This is to save bias current within the external switches in low-power operation. Two repetition times are possible, 16 ms and 32 ms.

If V3 is continuously ON, the WAKE input will be sampled continuously, regardless of the level of bit WSC.

The dedicated bits Edge Wake-up Status (EWS) and WAKE Level Status (WLS) in the System Status register reflect the actual status of pin WAKE. The WAKE port can be disabled by clearing the WEN bit in the System Configuration register.

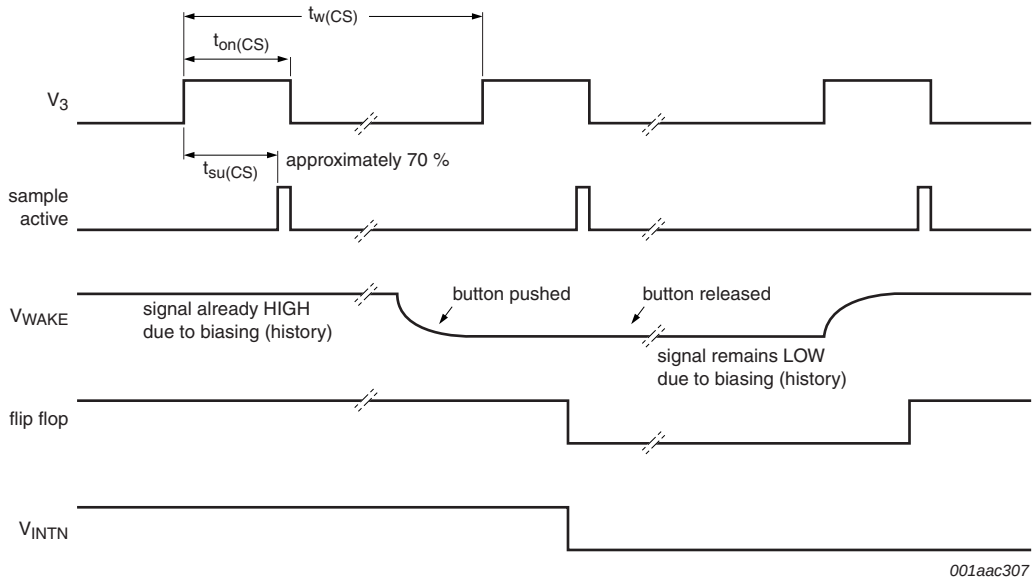


Fig 13. Pin WAKE, cyclic sampling via V3

6.11 Interrupt output

Pin INTN is an open-drain interrupt output. It is forced LOW whenever at least one bit in the Interrupt register is set. By reading the Interrupt register all bits are cleared. The Interrupt register will also be cleared during a system reset (RSTN LOW).

As the microcontroller operates typically with an edge-sensitive interrupt port, pin INTN will be HIGH for at least t_{INTN} after each read-out of the Interrupt register. Without further interrupts within t_{INTN} pin INTN stays HIGH, otherwise it will revert to LOW again.

To prevent the microcontroller from being slowed down by repetitive interrupts, in Normal mode some interrupts are only allowed to occur once per watchdog period; see Section 6.13.7.

If an interrupt is not read out within $t_{RSTN(INT)}$ a system reset is performed.

6.12 Temperature protection

The temperature of the SBC chip is monitored as long as the microcontroller voltage regulator V1 is active. To avoid an unexpected shutdown of the application by the SBC, the temperature protection will not switch-off any part of the SBC or activate a defined system stop of its own accord. If the temperature is too high it generates an interrupt to the microcontroller (μC), if enabled, and the corresponding status bit will be set. The microcontroller can then decide whether to switch-off parts of the SBC to decrease the chip temperature.

6.13 SPI interface

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave and multi-master operation. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCS - SPI chip select; active LOW
- SCK - SPI clock; default level is LOW due to low-power concept
- SDI - SPI data input
- SDO - SPI data output; floating when pin SCS is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge; see Figure 14.

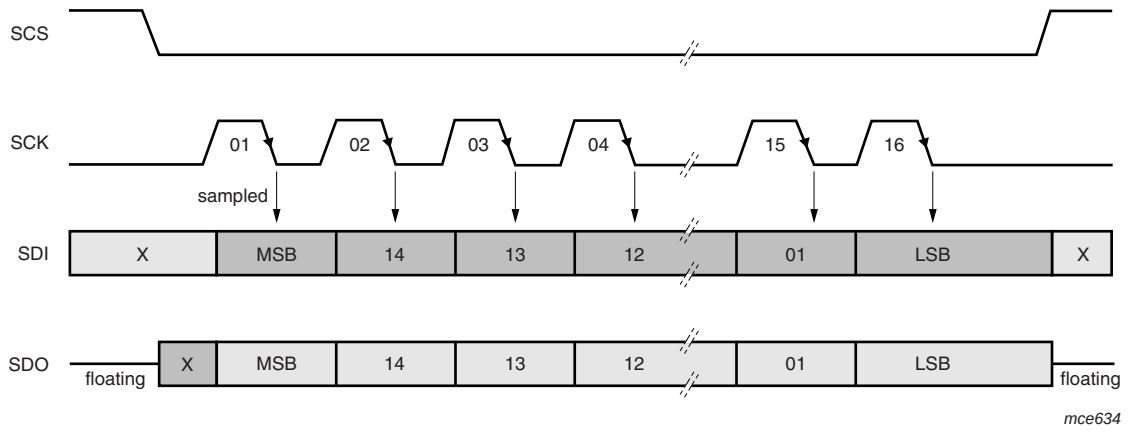


Fig 14. SPI timing protocol

To protect against wrong or illegal SPI instructions, the SBC detects the following SPI failures:

- SPI clock count failure (wrong number of clock cycles during one SPI access): only 16 clock periods are allowed within one SCS cycle. Any deviation from the 16 clock cycles results in an SPI failure interrupt, if enabled. The access is ignored by the SBC. In Start-up and Restart mode a reset is forced instead of an interrupt
- Forbidden mode changes according to Figure 3 result in an immediate system reset
- Illegal Mode register code. Undefined operating mode or watchdog period coding results in an immediate system reset; see Section 6.13.3

6.13.1 SPI register mapping

Any control bit which can be set by software is readable by the application. This allows software debugging as well as control algorithms to be implemented.

Watchdog serving and mode setting is performed within the same access cycle; this only allows an SBC mode change whilst serving the watchdog.

Each register carries 12 data bits; the other 4 bits are used for register selection and read/write definition.

6.13.2 Register overview

The SPI interface gives access to all SBC registers; see Table 4. The first two bits (A1 and A0) of the message header define the register address, the third bit is the read register select bit (RRS) to select one out of two possible feedback registers; the fourth bit (RO) allows 'read only' access to one of the feedback registers. Which of the SBC registers can be accessed also depends on the SBC operating mode.

Table 4. Register overview

Register address bits (A1, A0)	Operating mode	Write access (RO = 0)	Read access (RO = 0 or RO = 1)	
			Read Register Select (RRS) bit = 0	Read Register Select (RRS) bit = 1
00	all modes	Mode register	System Status register	System Diagnosis register
01	Normal mode; Standby mode; Flash mode	Interrupt Enable register	Interrupt Enable Feedback register	Interrupt register
	Start-up mode; Restart mode	Special Mode register	Interrupt Enable Feedback register	Special Mode Feedback register
10	Normal mode; Standby mode	System Configuration register	System Configuration Feedback register	General Purpose Feedback register 0
	Start-up mode; Restart mode; Flash mode	General Purpose register 0	System Configuration Feedback register	General Purpose Feedback register 0
11	Normal mode; Standby mode	Physical Layer Control register	Physical Layer Control Feedback register	General Purpose Feedback register 1
	Start-up mode; Restart mode; Flash mode	General Purpose register 1	Physical Layer Control Feedback register	General Purpose Feedback register 1

6.13.3 Mode register

In the Mode register the watchdog is defined and re-triggered, and the SBC operating mode is selected. The Mode register also contains the global enable output bit (EN) and the Software Development Mode (SDM) control bit. During system operation cyclic access to the Mode register is required to serve the watchdog. This register can be written to in all modes.

At system start-up the Mode register must be written to within $t_{WD(init)}$ from releasing RSTN (HIGH-level on pin RSTN). Any write access is checked for proper watchdog and system mode coding. If an illegal code is detected, access is ignored by the SBC and a system reset is forced in accordance with the state diagram of the system controller; see Figure 3.

Table 5. Mode register bit description (bits 15 to 12 and 5 to 0)

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	00	select Mode register
13	RRS	Read Register Select	1	read System Diagnosis register
			0	read System Status register
12	RO	Read Only	1	read selected register without writing to Mode register
			0	read selected register and write to Mode register
11 to 6	NWP[5:0]	see Table 6		
5 to 3	OM[2:0]	Operating Mode	001	Normal mode
			010	Standby mode
			011	initialize Flash mode[1]
			100	Sleep mode
			101	initialize Normal mode
			110	leave Flash mode
			111	Flash mode[1]
2	SDM	Software Development Mode	1	Software Development mode enabled[2]
			0	normal watchdog, interrupt, reset monitoring and fail-safe behavior
1	EN	Enable	1	EN output pin HIGH
			0	EN output pin LOW
0	-	reserved	0	reserved for future use; should remain cleared to ensure compatibility with future functions which might use this bit

[1] Flash mode can be entered only with the watchdog service sequence ‘Normal mode to Flash mode to Normal mode to Flash mode’, while observing the watchdog trigger rules. With the last command of this sequence the SBC forces a system reset, and enters Start-up mode to prepare the microcontroller for flash memory download. The four RSS bits in the System Status register reflect the reset source information, confirming the Flash entry sequence. By using the Initializing Flash mode (within $t_{WD(init)}$ after system reset) the SBC will now successfully enter Flash mode.

[2] See Section 6.14.1.

Table 6. Mode register bit description (bits 11 to 6)[1]

Bit	Symbol	Description	Value	Time			
				Normal mode (ms)	Standby mode (ms)	Flash mode (ms)	Sleep mode (ms)
11 to 6	NWP[5:0]	Nominal Watchdog Period WDPRE = 00 (as set in the Special Mode register)	00 1001	4	20	20	160
			00 1100	8	40	40	320
			01 0010	16	80	80	640
			01 0100	32	160	160	1024
			01 1011	40	320	320	2048
			10 0100	48	640	640	3072
			10 1101	56	1024	1024	4096
			11 0011	64	2048	2048	6144
			11 0101	72	4096	4096	8192
			11 0110	80	OFF[2]	8192	OFF[3]

Table 6. Mode register bit description (bits 11 to 6)[1] *...continued*

Bit	Symbol	Description	Value	Time			
				Normal mode (ms)	Standby mode (ms)	Flash mode (ms)	Sleep mode (ms)
11 to 6	NWP[5:0]	Nominal Watchdog Period WDPRE = 01 (as set in the Special Mode register)	00 1001	6	30	30	240
			00 1100	12	60	60	480
			01 0010	24	120	120	960
			01 0100	48	240	240	1536
			01 1011	60	480	480	3072
			10 0100	72	960	960	4608
			10 1101	84	1536	1536	6144
			11 0011	96	3072	3072	9216
			11 0101	108	6144	6144	12288
			11 0110	120	OFF[2]	12288	OFF[3]
		Nominal Watchdog Period WDPRE = 10 (as set in the Special Mode register)	00 1001	10	50	50	400
			00 1100	20	100	100	800
			01 0010	40	200	200	1600
			01 0100	80	400	400	2560
			01 1011	100	800	800	5120
			10 0100	120	1600	1600	7680
			10 1101	140	1560	1560	10240
			11 0011	160	5120	5120	15360
			11 0101	180	10240	10240	20480
			11 0110	200	OFF[2]	20480	OFF[3]
		Nominal Watchdog Period WDPRE = 11 (as set in the Special Mode register)	001001	14	70	70	560
			001100	28	140	140	1120
			010010	56	280	280	2240
			010100	112	560	560	3584
			011011	140	1120	1120	7168
			100100	168	2240	2240	10752
			101101	196	3584	3584	14336
			110011	224	7168	7168	21504
			110101	252	14336	14336	28672
			110110	280	OFF[2]	28672	OFF[3]

[1] The nominal watchdog periods are directly related to the SBC internal oscillator. The given values are valid for f_{osc} = 512 kHz.

[2] See Section 6.4.4.

[3] The watchdog is immediately disabled on entering Sleep mode, with watchdog OFF behavior selected, because pin RSTN is immediately pulled LOW by the mode change. V1 is switched off after pulling pin RSTN LOW to guarantee a safe Sleep mode entry without dips on V1; see Section 6.4.4.

6.13.4 System Status register

This register allows status information to be read back from the SBC. This register can be read in all modes.

Table 7. System Status register bit description

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	00	read System Status register
13	RRS	Read Register Select	0	
12	RO	Read Only	1	read System Status register without writing to Mode register
			0	read System Status register and write to Mode register
11 to 8	RSS[3:0]	Reset Source[1]	0000	power-on reset; first connection of BAT42 or BAT42 below power-on voltage threshold **or** RSTN was forced LOW externally
			0001	cyclic wake-up out of Sleep mode
			0010	low V1 supply; V1 has dropped below the selected reset threshold
			0011	V1 current above threshold within Standby mode while watchdog OFF behavior and reset option (V1CMC bit) are selected
			0100	V3 voltage is down due to overload occurring during Sleep mode
			0101	SBC successfully left Flash mode
			0110	SBC ready to enter Flash mode
			0111	CAN wake-up event
			1000	LIN wake-up event
			1001	local wake-up event (via pin WAKE)
			1010	wake-up out of Fail-safe mode
			1011	watchdog overflow
			1100	watchdog not initialized in time; $t_{WD(init)}$ exceeded
			1101	watchdog triggered too early; window missed
			1110	illegal SPI access
			1111	interrupt not served within $t_{RSTN(INT)}$
7	CWS	CAN Wake-up Status	1	CAN wake-up detected; cleared upon read
			0	no CAN wake-up
6	LWS	LIN Wake-up Status	1	LIN wake-up detected; cleared upon read
			0	no LIN wake-up
5	EWS	Edge Wake-up Status	1	pin WAKE negative edge detected; cleared upon read
			0	pin WAKE no edge detected
4	WLS	WAKE Level Status	1	pin WAKE above threshold
			0	pin WAKE below threshold
3	TWS	Temperature Warning Status	1	chip temperature exceeds the warning limit
			0	chip temperature is below the warning limit
2	SDMS	Software Development Mode Status	1	Software Development mode on
			0	Software Development mode off

Table 7. System Status register bit description *...continued*

Bit	Symbol	Description	Value	Function
1	ENS	Enable status	1	pin EN output activated (V1-related HIGH level)
			0	pin EN output released (LOW level)
0	PWONS	Power-on reset Status	1	power-on reset; cleared after a successfully entered Normal mode
			0	no power-on reset

[1] The RSS bits are updated with each reset event and not cleared. The last reset event is captured.

6.13.5 System Diagnosis register

This register allows diagnosis information to be read back from the SBC. This register can be read in all modes.

Table 8. System Diagnosis register bit description

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	00	read System Diagnosis register
13	RRS	Read Register Select	1	
12	RO	Read Only	1	read System Diagnosis register without writing to Mode register
			0	read System Diagnosis register and write to Mode register
11	GSD	Ground Shift Diagnosis	1	system GND shift is outside selected threshold
			0	system GND shift is within selected threshold
10 to 7	CANFD [3:0]	CAN failure diagnosis	1111	TXDC is clamped dominant
			1110	RXDC is clamped dominant
			1100	BUS is clamped dominant (dual failure situation)
			1101	RXDC is clamped recessive
			1011	BUS is clamped recessive (dual failure situation)
			1010	reserved
			1001	CANH is shorted to CANL (failure case 7)
			1000	CANL is shorted to V_{CC} (failure case 6a)
			0111	CANL is shorted to VBAT (failure case 6)
			0110	CANH is shorted to GND (failure case 5)
			0101	CANL is shorted to GND (failure case 4)
			0100	CANH is shorted to V_{CC} (failure case 3a)
			0011	CANH is shorted to VBAT (failure case 3)
			0010	CANL wire is interrupted (failure case 2)
			0001	CANH wire is interrupted (failure case 1)
			0000	no failure
6 and 5	LINFD[1:0]	LIN failure diagnosis	11	TXDL is clamped dominant
			10	LIN is shorted to GND (dominant clamped)
			01	LIN is shorted to VBAT (recessive clamped)
			00	no failure
4	V3D	V3 diagnosis	1	OK
			0	fail; V3 is disabled due to an overload situation

Table 8. System Diagnosis register bit description *…continued*

Bit	Symbol	Description	Value	Function
3	V2D	V2 diagnosis	1	OK[1]
			0	fail; V2 is disabled due to an overload situation
2	V1D	V1 diagnosis	1	OK; V1 always above $V_{UV(VFI)}$ since last read access
			0	fail; V1 was below $V_{UV(VFI)}$ since last read access; bit is set again with read access
1 and 0	CANMD [1:0]	CAN Mode Diagnosis	11	CAN is in Active mode
			10	CAN is in On-line mode
			01	CAN is in On-line Listen mode
			00	CAN is in Off-line mode, or V2 is not active

[1] V2D will be set when V2 is reactivated after a failure. See Section 6.6.2.2.

6.13.6 Interrupt Enable register and Interrupt Enable Feedback register

These registers allow setting, clearing and reading back the interrupt enable bits of the SBC.

Table 9. Interrupt Enable register and Interrupt Enable Feedback register bit description

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	01	select the Interrupt Enable register
13	RRS	Read Register Select	1	read the Interrupt register
			0	read the Interrupt Enable Feedback register
12	RO	Read Only	1	read the register selected by RRS without writing to Interrupt Enable register
			0	read the register selected by RRS and write to Interrupt Enable register
11	WTIE	Watchdog Time-out Interrupt Enable[1]	1	a watchdog overflow during Standby causes an interrupt instead of a reset event (interrupt based cyclic wake-up feature)
			0	no interrupt forced on watchdog overflow; a reset is forced instead
10	OTIE	Over-Temperature Interrupt Enable	1	exceeding or dropping below the temperature warning limit causes an interrupt
			0	no interrupt forced
9	GSIE	Ground Shift Interrupt Enable	1	exceeding or dropping below the GND shift limit causes an interrupt
			0	no interrupt forced
8	SPIFIE	SPI clock count Failure Interrupt Enable	1	wrong number of CLK cycles (more than, or less than 16) forces an interrupt; from Start-up mode and Restart mode a reset is performed instead of an interrupt
			0	no interrupt forced; SPI access is ignored if the number of cycles does not equal 16
7	-	reserved	0	should always be set to logic 0
6	VFIE	Voltage Failure Interrupt Enable	1	clearing of V1D, V2D or V3D forces an interrupt
			0	no interrupt forced

Table 9. Interrupt Enable register and Interrupt Enable Feedback register bit description *...continued*

Bit	Symbol	Description	Value	Function
5	CANFIE	CAN Failure Interrupt Enable	1	any change of the CAN Failure status bits forces an interrupt
			0	no interrupt forced
4	LINFIE	LIN Failure Interrupt Enable	1	any change of the LIN Failure status bits forces an interrupt
			0	no interrupt forced
3	WIE	WAKE Interrupt Enable[2]	1	a negative edge at pin WAKE generates an interrupt in Normal mode, Flash mode or Standby mode
			0	a negative edge at pin WAKE generates a reset in Standby mode; No interrupt in any other mode
2	WDRIE	Watchdog Restart Interrupt Enable	1	a watchdog restart during watchdog OFF generates an interrupt
			0	no interrupt forced
1	CANIE	CAN Interrupt Enable	1	CAN-bus event results in a wake-up interrupt in Standby mode and in Normal or Flash mode (unless CAN is in Active mode already)
			0	CAN-bus event results in a reset in Standby mode; No interrupt in any other mode
0	LINIE	LIN Interrupt Enable	1	LIN-bus event results in a wake-up interrupt in Standby mode and in Normal or Flash mode (unless LIN is in Active mode already)
			0	LIN-bus event results in a reset in Standby mode; no interrupt in any other mode

[1] This bit is cleared automatically upon each overflow event. It has to be set in software each time the interrupt behavior is required (fail-safe behavior).

[2] WEN (in the System Configuration register) has to be set to activate the WAKE port function globally.

6.13.7 Interrupt register

The Interrupt register allows the cause of an interrupt event to be read. The register is cleared upon a read access and upon any reset event. Hardware ensures that no interrupt event is lost in case there is a new interrupt forced while reading the register. After reading the Interrupt register pin INTN is released for t_{INTN} to guarantee an edge event at pin INTN.

The interrupts can be classified into two groups:

- Timing critical interrupts which require immediate reaction (SPI clock count failure which needs a new SPI command to be resent immediately, and a BAT failure which needs critical data to be saved immediately into the nonvolatile memory)
- Interrupts which do not require an immediate reaction (overtemperature, Ground Shift, CAN and LIN failures, V1, V2 and V3 failures and the wake-ups via CAN, LIN and WAKE. These interrupts will be signalled in Normal mode to the microcontroller once per watchdog period (maximum); this prevents overloading the microcontroller with unexpected interrupt events (e.g. a chattering CAN failure). However, these interrupts are reflected in the Interrupt register

Table 10. Interrupt register bit description

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	01	read Interrupt register
13	RRS	Read Register Select	1	
12	RO	Read Only	1	read the Interrupt register without writing to the Interrupt Enable register
			0	read the Interrupt register and write to the Interrupt Enable register
11	WTI	Watchdog Time-out Interrupt	1	a watchdog overflow during Standby mode has caused an interrupt (interrupt-based cyclic wake-up feature)
			0	no interrupt
10	OTI	OverTemperature Interrupt	1	the temperature warning status (TWS) has changed
			0	no interrupt
9	GSI	Ground Shift Interrupt	1	the ground shift diagnosis bit (GSD) has changed
			0	no interrupt
8	SPIFI	SPI clock count Failure Interrupt	1	wrong number of CLK cycles (more than, or less than 16) during SPI access
			0	no interrupt; SPI access is ignored if the number of CLK cycles does not equal 16
7	-	reserved	0	should always be set to logic 0
6	VFI	Voltage Failure Interrupt	1	V1D, V2D or V3D has been cleared
			0	no interrupt
5	CANFI	CAN Failure Interrupt	1	CAN failure status has changed
			0	no interrupt
4	LINFI	LIN Failure Interrupt	1	LIN failure status has changed
			0	no interrupt
3	WI	Wake-up Interrupt	1	a negative edge at WAKE has been detected
			0	no interrupt
2	WDRI	Watchdog Restart Interrupt	1	A watchdog restart during watchdog OFF has caused an interrupt
			0	no interrupt
1	CANI	CAN Wake-up Interrupt	1	CAN wake-up event has caused an interrupt
			0	no interrupt
0	LINI	LIN Wake-up Interrupt	1	LIN wake-up event has caused an interrupt
			0	no interrupt

6.13.8 System Configuration register and System Configuration Feedback register

These registers allow configuration of the behavior of the SBC, and allow the settings to be read back.

Table 11. System Configuration register and System Configuration Feedback register bit description

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	10	select System Configuration register
13	RRS	Read Register Select	1	read the General Purpose Feedback register 0
			0	read the System Configuration Feedback register
12	RO	Read Only	1	read register selected by RRS without writing to System Configuration register
			0	read register selected by RRS and write to System Configuration register
11 and 10	-	reserved	0	reserved for future use; should remain cleared to ensure compatibility with future functions which might use this bit
9	GSTHC	GND Shift Threshold Control	1	$V_{det(GSD)(CANH)}$ widened threshold
			0	$V_{det(GSD)(CANH)}$ normal threshold
8	RLC	Reset Length Control	1[1]	t_{RSTNL} long reset lengthening time selected
			0	t_{RSTNL} short reset lengthening time selected
7 and 6	V3C[1:0]	V3 Control	11	Cyclic mode 2; $t_{w(CS)}$ long period; see Figure 13
			10	Cyclic mode 1; $t_{w(CS)}$ short period; see Figure 13
			01	continuously ON
			00	OFF
5	-	reserved	0	reserved for future use; should remain cleared to ensure compatibility with future functions which might use this bit
4	V1CMC	V1 Current Monitor Control	1	an increasing V1 current causes a reset if the watchdog was disabled during Standby mode
			0	an increasing V1 current just reactivates the watchdog during Standby mode
3	WEN	WAKE Enable[2]	1	WAKE pin enabled
			0	WAKE pin disabled
2	WSC	WAKE Sample Control	1	WAKE mode cyclic sample
			0	WAKE mode continuous sample
1	ILEN	INH/LIMP Enable	1	INH/LIMP pin active (see ILC bit)
			0	INH/LIMP pin floating
0	ILC	INH/LIMP Control	1	INH/LIMP pin HIGH if ILEN bit is set
			0	INH/LIMP pin LOW if ILEN bit is set

[1] RLC is set automatically with entering Restart mode or Fail-safe mode. This guarantees a safe reset period in case of serious failure situations. External reset spikes are lengthened by the SBC until the programmed reset length is reached.

[2] If WEN is not set, the WAKE port is completely disabled. There is no change of the bits EWS and WLS within the System Status register.

6.13.9 Physical Layer Control register and Physical Layer Control Feedback register

These registers allow configuration of the CAN transceiver and LIN transceiver of the SBC and allow the settings to be read back.

Table 12. Physical Layer Control register and Physical Layer Control Feedback register bit description

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	11	select Physical Layer Control register
13	RRS	Read Register Select	1	read the General Purpose Feedback register 1
			0	read the Physical Layer Control Feedback register
12	RO	Read Only	1	read the register selected by RRS without writing to the Physical Layer Control register
			0	read the register selected by RRS and write to Physical Layer Control register
11	V2C	V2 Control	0	V2 is OFF in CAN Off-line mode
			1	V2 remains active in CAN Off-line mode
10	CPNC	CAN Partial Networking Control	1	CAN transceiver enters On-line Listen mode instead of On-line mode; cleared whenever the SBC enters On-line mode or Active mode
			0	On-line Listen mode disabled
9	COTC	CAN Off-line Time Control[1]	1	$t_{off\text{-}line}$ long period (extended to $t_{off\text{-}line(ext)}$ after wake-up)
			0	$t_{off\text{-}line}$ short period (extended to $t_{off\text{-}line(ext)}$ after wake-up)
8	CTC	CAN Transmitter Control[2]	1	CAN transmitter is disabled
			0	CAN transmitter is enabled
7	CRC	CAN Receiver Control	1	TXD signal is forwarded directly to RXD for self-test purposes (loopback behavior); only if CTC = 1
			0	TXD signal is not forwarded to RXD (normal behavior)
6	CMC	CAN Mode Control	1	CAN Active mode (in Normal mode and Flash mode only)
			0	CAN Active mode disabled
5	-	reserved	0	reserved for future use; should remain cleared to ensure compatibility with future functions which might use this bit
4	LMC	LIN Mode Control	1	LIN Active mode (in Normal mode and Flash mode only)
			0	LIN Active mode disabled
3	LSC	LIN Slope Control	1	up to 10.4 kbit/s (low slope)
			0	up to 20 kbit/s (normal)
2	LDC	LIN Driver Control	1	increased LIN driver current capability
			0	LIN driver in conformance with the LIN 2.0 standard
1	LWEN	LIN Wake-up Enable	1	Wake-up via the LIN-bus enabled
			0	Wake-up via the LIN-bus disabled
0	LTC	LIN Transmitter Control[3]	1	LIN transmitter is disabled
			0	LIN transmitter is enabled

[1] For the CAN transceiver to enter Off-Line mode from On-line or On-line Listen mode a minimum time without bus activity is needed. This minimum time $t_{off\text{-}line}$ is defined by COTC; see Section 6.7.1.4.

[2] In case of an RXDC / TXDC interfacing failure the CAN transmitter is disabled without setting CTC. Recovery from such a failure is automatic when CAN communication (with correct interfacing levels) is received. Manual recovery is also possible by setting and clearing the CTC bit under software control.

[3] In case of an RXDC / TXDC interfacing failure the LIN transmitter is disabled without setting LTC. Recovery from such a failure is automatic when LIN communication (with correct interfacing levels) is received. Manual recovery is also possible by setting and clearing the LTC bit under software control.

6.13.10 Special Mode register and Special Mode Feedback register

These registers allow configuration of global SBC parameters during start-up of a system, and allow the settings to be read back.

Table 13. Special Mode register and Special Mode Feedback register bit description

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	01	select Special Mode register
13	RRS	Read Register Select	0	read the Interrupt Enable Feedback register
			1	read the Special Mode Feedback register
12	RO	Read Only	1	read the register selected by RRS without writing to the Special Mode register
			0	read the register selected by RRS and write to the Special Mode register
11 and 10	-	reserved	0	reserved for future use; should remain cleared to ensure compatibility with future functions which might use this bit
9	ISDM	Initialize Software Development Mode[1]	1	initialization of Software Development mode
			0	normal watchdog interrupt, reset monitoring and fail-safe behavior
8	ERREM	Error-pin Emulation Mode	1	pin EN reflects the status of the CANFD bits:
				EN is set if CANFD = 0000 (no error)
				EN is cleared if CANFD is not 0000 (error)
			0	pin EN behaves as an enable pin; see Section 6.5.2
7	-	reserved	0	reserved for future use; should remain cleared to ensure compatibility with future functions which might use this bit
6 and 5	WDPRE [1:0]	Watchdog Prescaler	00	watchdog prescale factor 1
			01	watchdog prescale factor 1.5
			10	watchdog prescale factor 2.5
			11	watchdog prescale factor 3.5
4 and 3	V1RTHC [1:0]	V1 Reset Threshold Control	11	V1 reset threshold = $0.9 \times V_{V1(nom)}$
			10	V1 reset threshold = $0.7 \times V_{V1(nom)}$[2]
			01	V1 reset threshold = $0.8 \times V_{V1(nom)}$
			00	V1 reset threshold = $0.9 \times V_{V1(nom)}$
2 to 0	-	reserved	0	reserved for future use; should remain cleared to ensure compatibility with future functions which might use this bit

[1] See Section 6.14.1.

[2] Not supported in the UJA1061TW/3V3 version.

6.13.11 General Purpose registers and General Purpose Feedback registers

The UJA1061 offers two 12-bit General Purpose registers (and accompanying General Purpose Feedback registers) with no predefined bit definition. These registers can be used by the microcontroller for advanced system diagnosis, or for storing critical system status information outside the microcontroller. After Power-up General Purpose register 0 will contain a 'Device Identification Code' consisting of the SBC type and SBC version. This code is available until it is overwritten by the microcontroller (as indicated by the DIC bit).

Table 14. General Purpose register 0 and General Purpose Feedback register 0 bit description

Bit	Symbol	Description	Value	Function
15, 14	A1, A0	register address	10	select General Purpose Feedback register 0
13	RRS	Read Register Select	1	read the General Purpose Feedback register 0
			0	read the System Configuration Feedback register
12	RO	Read Only	1	read the register selected by RRS without writing to the General Purpose register 0
			0	read the register selected by RRS and write to the General Purpose register 0
11	DIC	Device Identification Control[1]	1	General Purpose register 0 contains user-defined bits
			0	General Purpose register 0 contains the Device Identification Code
10 to 0	GP0[10:0]	General Purpose bits[2]	1	user-defined
			0	user-defined

[1] The Device Identification Control bit is cleared during power-up of the SBC, indicating that General Purpose register 0 is loaded with the Device Identification Code. Any write access to General Purpose register 0 will set the DIC bit, regardless of the value written to DIC.

[2] During power-up the General Purpose register 0 is loaded with a 'Device Identification Code' consisting of the SBC type and SBC version, and the DIC bit is cleared.

Table 15. General Purpose register 1 and General Purpose Feedback register 1 bit description

Bit	Symbol	Description	Value	Function
15 and 14	A1, A0	register address	11	select General Purpose register 1
13	RRS	Read Register Select	1	read the General Purpose Feedback register 1
			0	read the Physical Layer Control Feedback register
12	RO	Read Only	1	read the register selected by RRS without writing to the General Purpose register 1
			0	read the register selected by RRS and write to the General Purpose register 1
11 to 0	GP1[11:0]	General Purpose bits	1	user-defined
			0	user-defined

6.13.12 Register configurations at reset

At power-on, Start-up and Restart the setting of the SBC registers is predefined.

Table 16. System Status register: status at reset

Symbol	Name	Power-on	Start-up[1]	Restart[1]
RSS	Reset Source Status	0000 (power-on reset)	any value except 1100	0000 or 0010 or 1100 or 1110
CWS	CAN Wake-up Status	0 (no CAN wake-up)	1 if reset is caused by a CAN wake-up, otherwise no change	no change
LWS	LIN Wake-up Status	0 (no LIN wake-up)	1 if reset is caused by a LIN wake-up, otherwise no change	no change
EWS	Edge Wake-up Status	0 (no edge detected)	1 if reset is caused by a wake-up via pin WAKE, otherwise no change	no change
WLS	WAKE Level Status	actual status	actual status	actual status
TWS	Temperature Warning Status	0 (no warning)	actual status	actual status
SDMS	Software Development Mode Status	actual status	actual status	actual status
ENS	Enable Status	0 (EN = LOW)[2]	0 (EN = LOW)[2]	0 (EN = LOW)[2]
PWONS	Power-on Status	1 (power-on reset)	no change	no change

[1] Depends on history.

[2] In case the ERREM bit in the Special Mode register is 0. Otherwise ENS shows the actual CAN failure status.

Table 17. System Diagnosis register: status at reset

Symbol	Name	Power-on	Start-up	Restart
GSD	Ground Shift Diagnosis	0 (OK)	actual status	actual status
CANFD	CAN Failure Diagnosis	0000 (no failure)	actual status	actual status
LINFD	LIN Failure Diagnosis	00 (no failure)	actual status	actual status
V3D	V3 Diagnosis	1 (OK)	actual status	actual status
V2D	V2 Diagnosis	1 (OK)	actual status	actual status
V1D	V1 Diagnosis	0 (fail)	actual status	actual status
CANMD	CAN Mode Diagnosis	00 (Off-line)	actual status	actual status

Table 18. Interrupt Enable register and Interrupt Enable Feedback register: status at reset

Symbol	Name	Power-on	Start-up	Restart
All	all bits	0 (interrupt disabled)	no change	no change

Table 19. Interrupt register: status at reset

Symbol	Name	Power-on	Start-up	Restart
All	all bits	0 (no interrupt)	0 (no interrupt)	0 (no interrupt)

Table 20. System Configuration register and System Configuration Feedback register: status at reset

Symbol	Name	Power-on	Start-up	Restart	Fail-safe
GSTHC	GND Shift level Threshold Control	0 (normal)	no change	no change	no change
RLC	Reset Length Control	0 (short)	no change	1 (long)	1 (long)
V3C	V3 Control	00 (off)	no change	no change	no change
V1CMC	V1 Current Monitor Control	0 (watchdog restart)	no change	no change	no change
WEN	Wake Enable	1 (enabled)	no change	no change	no change
WSC	Wake Sample Control	0 (control)	no change	no change	no change
ILEN	INH/LIMP Enable	0 (floating)	see Figure 12 if ILC = 1, otherwise no change	0 (floating) if ILC = 1, otherwise no change	1 (active)
ILC	INH/LIMP Control	0 (LOW)	no change	no change	0 (LOW)

Table 21. Physical Layer Control register and Physical Layer Control Feedback register: status at reset

Symbol	Name	Power-on	Start-up	Restart	Fail-safe
V2C	V2 Control	0 (auto)	no change	no change	0 (auto)
CPNC	CAN Partial Networking Control	0 (On-line Listen mode disabled)	0 if reset is caused by a CAN wake-up, otherwise no change	no change	0 (On-line Listen mode disabled)
COTC	CAN Off-line Time Control	1 (long)	no change	no change	no change
CTC	CAN Transmitter Control	0 (on)	no change	no change	no change
CRC	CAN Receiver Control	0 (normal)	no change	no change	no change
CMC	CAN Mode Control	0 (Active mode disabled)	no change	no change	no change
LMC	LIN Mode Control	0 (Active mode disabled)	no change	no change	no change
LSC	LIN Slope Control	0 (normal)	no change	no change	no change
LDC	LIN Driver Control	0 (LIN 2.0)	no change	no change	no change
LWEN	LIN Wake-up Enable	1 (enabled)	no change	no change	no change
LTC	LIN Transmitter Control	0 (on)	no change	no change	no change

Table 22. Special Mode register: status at reset

Symbol	Name	Power-on	Start-up	Restart
ISDM	Initialize Software Development Mode	0 (no)	no change	no change
ERREM	Error pin emulation mode	0 (EN function)	no change	no change
WDPRE	Watchdog Prescale Factor	00 (factor 1)	no change	no change
V1RTHC	V1 Reset Threshold Control	00 (90 %)	no change	00 (90 %)

Table 23. General Purpose register 0 and General Purpose Feedback register 0: status at reset

Symbol	Name	Power-on	Start-up	Restart
DIC	Device Identification Control	0 (Device ID)	no change	no change
GP0[10:7]	general purpose bits 10 to 7 (version)	Mask version	no change	no change
GP0[6:0]	general purpose bits 6 to 0 (SBC type)	000 0001 (UJA1061)	no change	no change

Table 24. General Purpose register 1 and General Purpose Feedback register 1: status at reset

Symbol	Name	Power-on	Start-up	Restart
GP1[11:0]	general purpose bits 11 to 0	0000 0000 0000	no change	no change

6.14 Test modes

6.14.1 Software Development mode

The Software Development mode is intended to support software developers in writing and pretesting application software without having to work around watchdog triggering and without unwanted jumps to Fail-safe mode.

In Software Development mode the following events do not force of a system reset:

- Watchdog overflow in Normal mode
- Watchdog window miss
- Interrupt time-out
- Elapsed start-up time

However, in case of a watchdog trigger failure the reset source information is still provided in the System Status register as if there was a real reset event.

The exclusion of watchdog related resets allows simplified software testing, because possible problems in the watchdog triggering can be indicated by interrupts instead of resets. The SDM bit does not affect the watchdog behavior in Standby and Sleep mode. This allows the cyclic wake-up behavior to be evaluated during Standby and Sleep mode of the SBC.

All transitions to Fail-safe mode are disabled. This allows working with an external emulator that clamps the reset line LOW in debugging mode. A V1 undervoltage of more than $t_{V1(CLT)}$ is the only exception that results in entering Fail-safe mode (to protect the SBC). Transitions from Start-up mode to Restart mode are still possible.

There are two possibilities to enter Software Development mode. One is by setting the ISDM bit via the Special Mode register; possible only once after a first battery connection while the SBC is in Start-up mode. The second possibility to enter Software Development mode is by applying the correct $V_{th(TEST)}$ input voltage at pin TEST before the battery is applied to pin BAT42.

To stay in Software Development mode the SDM bit in the Mode register has to be set with each Mode register access (i.e. watchdog triggering) regardless of how Software Development mode was entered.

The Software Development mode can be exited at any time by clearing the SDM bit in the Mode register. Reentering the Software Development mode is only possible by reconnecting the battery supply (pin BAT42), thereby forcing a new power-on reset.

6.14.2 Forced Normal mode

For system evaluation purposes the UJA1061 offers the Forced Normal mode. This mode is strictly for evaluation purposes only. In this mode the characteristics as defined in Section 9 and Section 10 cannot be guaranteed.

In Forced normal mode the SBC behaves as follows:

- SPI access (writing and reading) is blocked
- Watchdog disabled
- Interrupt monitoring disabled
- Reset monitoring disabled
- Reset lengthening disabled
- All transitions to Fail-safe mode are disabled, except a V1 undervoltage for more than $t_{V1(CLT)}$
- V1 is started with the long reset time t_{RSTNL}. In case of a V1 undervoltage, a reset is performed until V1 is restored (normal behavior), and the SBC stays in Forced Normal mode; in case of a continuous overload at V1 > $t_{V1(CLT)}$ Fail-safe mode is entered
- V2 is on; overload protection active
- V3 is on; overload protection active
- CAN and LIN are in Active mode and cannot switch to Off-line mode
- INH/LIMP pin is HIGH
- SYSINH is HIGH
- EN pin at same level as RSTN pin

Forced Normal mode is activated by applying the correct $V_{th(TEST)}$ input voltage at the TEST pin during first battery connection.

7. Limiting values

Table 25. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT42}	BAT42 supply voltage			–0.3	+60	V
		load dump; $t \leq 500$ ms		-	60	V
V_{BAT14}	BAT14 supply voltage	$V_{BAT42} \geq V_{BAT14} - 1$ V				
		continuous		–0.3	+33	V
		load dump; $t \leq 500$ ms		-	45	V
$V_{DC(n)}$	DC voltages	on pins				
		V1 and V2		–0.3	+5.5	V
		V3 and SYSINH		–1.5	V_{BAT42} + 0.3	V
		WAKE		–1.5	+60	V
		INH/LIMP		–0.3	V_{BAT42} + 0.3	V
		CANH, CANL, RTH, RTL LIN and RTLIN; with respect to any other pin		–60	+60	V
		TXDC, RXDC, TXDL, RXDL, SDO, SDI, SCK, SCS, RSTN, INTN and EN		–0.3	V_{V1} + 0.3	V
		TEST		–0.3	+15	V
V_{trt}	transient voltage	at pins CANH, CANL and LIN; in accordance with ISO 7637-3		–150	+100	V
I_{WAKE}	DC current at pin WAKE		[1]	–15	-	mA
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+125	°C
T_{vj}	virtual junction temperature		[2]	–40	+150	°C
V_{esd}	electrostatic discharge voltage	HBM	[3]			
		at pins CANH, CANL, RTH, RTL, LIN, RTLIN, WAKE, BAT42, V3; with respect to GND	[4]	–8.0	+8.0	kV
		at any other pin		–2.0	+2.0	kV
		MM; at any pin	[5]	–200	+200	V

[1] Only relevant if $V_{WAKE} < V_{GND} - 0.3$ V; current will flow into pin GND.

[2] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P_d \times R_{th(vj\text{-}amb)}$, where $R_{th(vj\text{-}amb)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P_d) and ambient temperature (T_{amb}).

[3] Human Body Model (HBM): C = 100 pF; R = 1.5 kΩ.

[4] ESD performance according to IEC 61000-4-2 (C = 150 pF, R = 330 Ω) of pins CANH, CANL, RTH, RTL, LIN, RTLIN, WAKE, BAT42 and V3 with respect to GND was verified by an external test house. Following results were obtained:

a) equal or better than ±6 kV (unaided).

b) equal or better than ±20 kV (using external ESD protection: NXP Semiconductors PESD1CAN and PESD1LIN diode).

[5] Machine Model (MM): C = 200 pF; L = 0.75 μH; R = 10 Ω.

8. Thermal characteristics

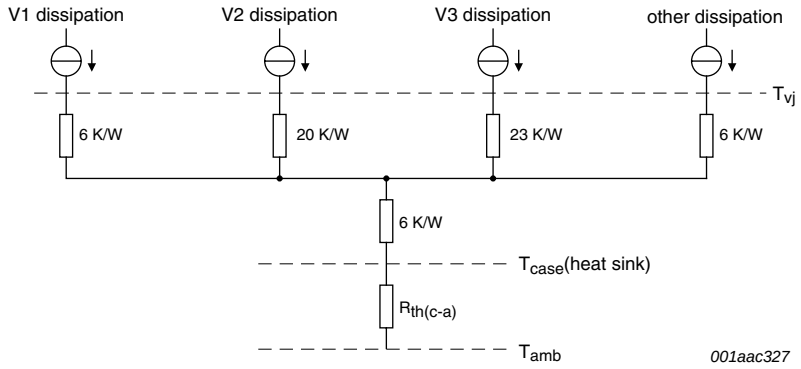


Fig 15. Thermal model of the HTSSOP32 package

9. Static characteristics

Table 26. Static characteristics[1]

T_{vj} = −40 °C to +150 °C; V_{BAT42} = 5.5 V to 52 V;V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT42						
I_{BAT42}	BAT42 supply current	V1, V2 and V3 off; CAN and LIN in Off-line mode; OTIE = BATFIE = 0; I_{SYSINH} = I_{WAKE} = I_{RTLIN} = I_{LIN} = 0 mA				
		V_{BAT42} = 8.1 V to 52 V	-	50	70	µA
		V_{BAT42} = 5.5 V to 8.1 V	-	70	93	µA
$I_{BAT42(add)}$	additional BAT42 supply current	V1 and / or V2 on; I_{SYSINH} = 0 mA	-	53	76	µA
		V3 in cyclic mode; I_{V3} = 0 mA	-	0	1	µA
		V3 continuously on; I_{V3} = 0 mA	-	30	50	µA
		T_{vj} warning enabled; OTIE = 1	-	20	40	µA
		CAN in Active mode; CMC = 1	-	100	400	µA
		LIN in Active mode; LMC = 1; V_{TXDL} = V_{V1}; I_{RTLIN} = I_{LIN} = 0 mA	-	650	1300	µA
		LIN in Active mode; LMC = 1; V_{TXDL} = 0 V ($t < t_{LIN(dom)(det)}$); I_{RTLIN} = I_{LIN} = 0 mA; V_{BAT42} = 12 V	-	1.5	5	mA
		LIN in Active mode; LMC = 1; V_{TXDL} = 0 V ($t < t_{LIN(dom)(det)}$); I_{RTLIN} = I_{LIN} = 0 mA; V_{BAT42} = 27 V	-	3	10	mA
$V_{POR(BAT42)}$	BAT42 voltage level for Power-on reset status bit change	for setting PWONS				
		PWONS = 0; V_{BAT42} falling	4.45	-	5	V
		for clearing PWONS				
		PWONS = 1; V_{BAT42} rising	4.75	-	5.5	V
Supply; pin BAT14						
V_{BAT14}	BAT14 supply voltage	normal output current capability at V1	9	-	27	V
		high output current capability at V1	6	-	8	V
I_{BAT14}	BAT14 supply current	V1 and V2 off; CAN and LIN in Off-line mode; ILEN = CSC = 0; $I_{INH/LIMP}$ = 0 mA	-	2	5	µA

Table 26. Static characteristics[1] *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT42} = 5.5 V to 52 V;V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{BAT14(add)}$	additional BAT14 supply current	V1 on; I_{V1} = 0 mA		-	200	300	µA
		V1 on; I_{V1} = 0 mA; V_{BAT14} = 12 V		-	150	200	µA
		V2 on; I_{V2} = 0 mA		-	200	320	µA
		V2 on; I_{V2} = 0 mA; V_{BAT14} = 12 V		-	200	250	µA
		INH/LIMP enabled; ILEN = 1; $I_{INH/LIMP}$ = 0 mA		-	1	2	µA
		CAN in Active mode; CMC = 1; I_{CANH} = I_{CANl} = 0 mA; V_{TXD} = 0 V					
		Differential mode		-	10	20	mA
		Single-ended mode		-	13	25	mA
		CAN in Active mode; CMC = 1; V_{TXD} = V_{V1}					
		Differential mode		-	5	10	mA
		Single-ended mode		-	8	15	mA
Voltage source; pin V1[2]; see also Figure 16 to 22							
$V_{o(V1)}$	output voltage	V_{BAT14} = 5.5 V to 18 V; I_{V1} = −120 mA to −5 mA; T_j = 25 °C		$V_{V1(nom)}$ − 0.1	$V_{V1(nom)}$	$V_{V1(nom)}$ + 0.1	V
		V_{BAT14} = 14 V; I_{V1} = −5 mA; T_j = 25 °C		$V_{V1(nom)}$ − 0.025	$V_{V1(nom)}$	$V_{V1(nom)}$ + 0.025	V
ΔV_{V1}	supply voltage regulation	V_{BAT14} = 9 V to 16 V; I_{V1} = −5 mA; T_j = 25 °C		-	1	25	mV
	load regulation	V_{BAT14} = 14 V; I_{V1} = −50 mA to −5 mA; T_j = 25 °C		-	5	25	mV
	voltage drift with temperature	V_{BAT14} = 14 V; I_{V1} = −5 mA; T_j = −40 °C to +150 °C	[3]	-	-	200	ppm/K
$V_{det(UV)(V1)}$	undervoltage detection and reset activation level	V_{BAT14} = 14 V; V1RTHC = 00 or 11		0.90 × $V_{V1(nom)}$	0.92 × $V_{V1(nom)}$	0.95 × $V_{V1(nom)}$	V
		V_{BAT14} = 14 V; V1RTHC = 01		0.80 × $V_{V1(nom)}$	0.82 × $V_{V1(nom)}$	0.85 × $V_{V1(nom)}$	V
		V_{BAT14} = 14 V; V1RTHC = 10		0.70 × $V_{V1(nom)}$	0.72 × $V_{V1(nom)}$	0.75 × $V_{V1(nom)}$	V
$V_{rel(UV)(V1)}$	undervoltage detection release level	V_{BAT14} = 14 V; V1RTHC = 00 or 11		-	0.94 × $V_{V1(nom)}$	-	V
		V_{BAT14} = 14 V; V1RTHC = 01		-	0.84 × $V_{V1(nom)}$	-	V
		V_{BAT14} = 14 V; V1RTHC = 10		-	0.74 × $V_{V1(nom)}$	-	V
$V_{UV(VFI)}$	undervoltage level for generating a VFI interrupt	V_{BAT14} = 14 V; VFIE = 1		0.90 × $V_{V1(nom)}$	0.93 × $V_{V1(nom)}$	0.97 × $V_{V1(nom)}$	V

Table 26. Static characteristics[1] *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT42} = 5.5 V to 52 V;V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{thH(V1)}$	undercurrent threshold for watchdog enable		−10	−5	−2	mA
$I_{thL(V1)}$	undercurrent threshold for watchdog disable		−6	−3	−1.5	mA
I_{V1}	output current capability	V_{BAT14} = 9 V to 27 V; $\delta V_{V1} = 0.05 \times V_{V1(nom)}$	−200	−135	−120	mA
		V_{BAT14} = 9 V to 27 V; V1 shorted to GND	−200	−110	-	mA
		V_{BAT14} = 8 V to 9 V; $\delta V_{V1} = 0.05 \times V_{V1(nom)}$	-	-	−120	mA
		V_{BAT14} = 5.5 V to 8 V; $\delta V_{V1} = 0.05 \times V_{V1(nom)}$	-	-	−150	mA
$Z_{ds(on)}$	regulator impedance between pins BAT14 and V1	V_{BAT14} = 4 V to 5 V	-	3	5	Ω
Voltage source; pin V2[4]						
$V_{o(V2)}$	output voltage	V_{BAT14} = 9 V to 16 V; I_{V2} = −50 mA to −5 mA	4.8	5.0	5.2	V
		V_{BAT14} = 14 V; I_{V2} = −10 mA; T_j = 25 °C	4.95	5.0	5.05	V
ΔV_{V2}	supply voltage regulation	V_{BAT14} = 9 V to 16 V; I_{V2} = −10 mA; T_j = 25 °C	-	1	25	mV
	load regulation	V_{BAT14} = 14 V; I_{V2} = −50 mA to −5 mA; T_j = 25 °C	-	-	50	mV
	voltage drift with temperature	V_{BAT14} = 14 V; I_{V2} = −10 mA; −40 °C < T_j < 150 °C [3]	-	-	200	ppm/K
I_{V2}	output current capability	V_{BAT14} = 9 V to 27 V; δV_{V2} = 300 mV	−200	-	−120	mA
		V_{BAT14} = 9 V to 27 V; V2 shorted to GND	−300	-	-	mA
		V_{BAT14} = 6 V to 8 V; δV_{V2} = 300 mV	-	-	−80	mA
		V_{BAT14} = 5.5 V; δV_{V2} = 300 mV	-	-	−50	mA
$V_{det(UV)(V2)}$	undervoltage detection threshold	V_{BAT14} = 14 V	4.5	4.6	4.8	V
Voltage source; pin V3						
$V_{BAT42-V3(drop)}$	V_{BAT42} to V_{V3} voltage drop	V_{BAT42} = 9 V to 52 V; I_{V3} = −20 mA	-	-	1.0	V
$I_{det(OL)(V3)}$	overload current detection threshold	V_{BAT42} = 9 V to 52 V	−165	-	−60	mA

Table 26. Static characteristics[1] *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT42} = 5.5 V to 52 V;V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System inhibit output; pin SYSINH						
$V_{BAT42-SYSINH(drop)}$	V_{BAT42} to V_{SYSINH} voltage drop	I_{SYSINH} = −0.2 mA	-	1.0	2.0	V
$\|I_L\|$	leakage current	V_{SYSINH} = 0 V	-	-	5	µA
Inhibit / limp-home output; pin INH/LIMP						
$V_{BAT14-INH(drop)}$	V_{BAT14} to V_{INH} voltage drop	$I_{INH/LIMP}$ = −10 µA; ILEN = ILC = 1	-	0.7	1.0	V
		$I_{INH/LIMP}$ = −200 µA; ILEN = ILC = 1	-	1.2	2.0	V
$I_{o(INH/LIMP)}$	output current capability	$V_{INH/LIMP}$ = 0.4 V; ILEN = 1; ILC = 0	0.8	-	4	mA
$\|I_L\|$	leakage current	$V_{INH/LIMP}$ = 0 V to V_{BAT14}; ILEN = 0	-	-	5	µA
Wake input; pin WAKE						
$V_{th(WAKE)}$	WAKE voltage threshold		2.0	3.3	5.2	V
$I_{WAKE(pu)}$	pull-up input current	V_{WAKE} = 0 V	−25	-	−1.3	µA
Serial peripheral interface inputs; pins SDI, SCK and SCS						
$V_{IH(th)}$	HIGH-level input threshold voltage		0.7 × V_{V1}	-	V_{V1} + 0.3	V
$V_{IL(th)}$	LOW-level input threshold voltage		−0.3	-	0.3 × V_{V1}	V
$R_{pd(SCK)}$	pull-down resistor at pin SCK	V_{SCK} = 2 V; $V_{V1} \geq$ 2 V	50	130	400	kΩ
$R_{pu(SCS)}$	pull-up resistor at pin SCS	V_{SCS} = 1 V; $V_{V1} \geq$ 2 V	50	130	400	kΩ
$I_{LI(SDI)}$	input leakage current at pin SDI	V_{SDI} = 0 V to V_{V1}	−5	-	+5	µA
Serial peripheral interface data output; pin SDO						
I_{OH}	HIGH-level output current	$V_O = V_{V1}$ − 0.4 V; V_{SCS} = 0 V	−50	-	−1.6	mA
I_{OL}	LOW-level output current	V_O = 0.4 V; V_{SCS} = 0 V	1.6	-	20	mA
$I_{LO(off)}$	OFF-state output leakage current	V_O = 0 V to V_{V1}; $V_{SCS} = V_{V1}$	−5	-	+5	µA
Reset output with clamping detection; pin RSTN						
I_{OH}	HIGH-level output current	V_{RSTN} = 0.7 × $V_{V1(nom)}$	−1000	-	−50	µA
I_{OL}	LOW-level output current	V_{RSTN} = 0.9 V	1	-	5	mA
V_{OL}	LOW-level output voltage	V_{V1} = 1.5 V to 5.5 V; pull-up resistor to V1 = ≥ 4 kΩ	0	-	0.2 × V_{V1}	V
$V_{IH(th)}$	HIGH-level input threshold voltage		0.7 × V_{V1}	-	V_{V1} + 0.3	V

Table 26. Static characteristics[1] *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT42} = 5.5 V to 52 V;V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(th)}$	LOW-level input threshold voltage		−0.3	-	+0.3 × V_{V1}	V
Enable output; pin EN						
I_{OH}	HIGH-level output current	$V_{OH} = V_{V1} - 0.4$ V	−20	-	−1.6	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.6	-	20	mA
V_{OL}	LOW-level output voltage	I_{OL} = 20 μA; V_{V1} = 1.2 V	0	-	0.4	V
Interrupt output; pin INTN						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.6	-	15	mA
CAN transmit data input; pin TXDC						
V_{IH}	HIGH-level input voltage		0.7 × V_{V1}	-	V_{V1} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.3 × V_{V1}	V
$R_{TXDC(pu)}$	TXDC pull-up resistor	V_{TXDC} = 0 V	5	12	25	kΩ
CAN receive data output; pin RXDC						
I_{OH}	HIGH-level output current	$V_{OH} = V_{V1} - 0.4$ V	−25	-	−1.6	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.6	-	25	mA
Fault-tolerant CAN-bus lines; pins CANH and CANL						
$V_{dif(CANH-CANL)}$	differential receiver threshold voltage	Active mode, On-line, Partial Networking or On-Line Listen mode; V_{V2} = 5 V; no failures and bus failures H//, L//, HxGND and LxVCC	−3.5	−3.2	−2.9	V
$V_{se(CANH)}$	pin CANH single ended receiver threshold voltage	Active mode, On-line, Partial Networking or On-Line Listen mode; V_{V2} = 5 V; bus failures LxGND, LxBAT and HxL	1.5	1.7	1.85	V
$V_{se(CANL)}$	pin CANL single ended receiver threshold voltage	Active mode, On-line, Partial Networking or On-Line Listen mode; V_{V2} = 5 V; bus failures HxBAT and HxVCC	3.15	3.3	3.45	V
$V_{det(HxBAT)}$, $V_{det(LxBAT)}$	detection threshold voltage for bus failures HxBAT and LxBAT	Active mode, On-line, Partial Networking or On-Line Listen mode; V_{V2} = 5 V	6.5	7.1	8.0	V
$V_{det(GSD)(CANH)}$	pin CANH ground shift detection threshold voltage	Active mode; V_{V2} = 5 V				
		SPI bit GSTHC = logic 0	−1.25	−0.75	−0.25	V
		SPI bit GSTHC = logic 1	−2.0	−1.5	−1.0	V

Table 26. Static characteristics[1] *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT42} = 5.5 V to 52 V;V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{wu(CANH)}$	pin CANH wake-up threshold voltage	off-line	2.5	3.2	3.9	V
$V_{wu(CANL)}$	pin CANL wake-up threshold voltage	off-line	1.1	1.8	2.5	V
$\Delta V_{wu(CANH-CANL)}$	wake-up threshold difference voltage	CANH to CANL; off-line	0.8	1.4	-	V
$V_{O(reces)}$	CANH recessive output voltage	Active mode, On-line, Partial Networking or On-Line Listen mode; V_{V2} = 4.75 V to 5.25 V; $V_{TXDC} = V_{V2}$; R_{RTH} < 4 kΩ	-	-	0.2	V
	CANL recessive output voltage	Active mode, On-line, Partial Networking or On-Line Listen mode; V_{V2} = 4.75 V to 5.25 V; $V_{TXDC} = V_{V2}$; R_{RTL} < 4 kΩ	V_{V2} − 0.2	-	-	V
$V_{O(dom)}$	CANH dominant output voltage	Active mode, On-line, Partial Networking or On-Line Listen mode; V_{TXDC} = 0 V; V_{V2} = 5 V; I_{CANH} = −40 mA	V_{V2} − 1.4	-	-	V
	CANL dominant output voltage	Active mode, On-line, Partial Networking or On-Line Listen mode; V_{TXDC} = 0 V; V_{V2} = 5 V; I_{CANL} = 40 mA	-	-	1.4	V
$I_{O(CANH)}$	pin CANH output current	Active mode; V_{CANH} = 0 V; V_{TXDC} = 0 V; V_{V2} = 5 V	−110	−75	−45	mA
		Auto mode; V_{CANH} = 0 V; V_{BAT14} = 14 V	-	−0.25	-	µA
$I_{O(CANL)}$	pin CANL output current	Active mode; V_{CANL} = 5 V; V_{TXDC} = 0 V; V_{V2} = 5 V	45	75	110	mA
		Auto mode; V_{CANL} = 14 V; V_{BAT14} = 14 V	-	0	-	µA
CAN termination resistor (pin RTH)						
$R_{sw(RTH)}$	switch-on resistance	measured between RTH and GND; Active mode, On-line or Selective Sleep; $\lvert I_o \rvert$ = 10 mA; V_{TXDC} = 5 V	-	40	100	Ω
$V_{O(RTH)}$	output voltage	off-line; I_O = 100 µA	-	0.7	1.0	V
$I_{O(RTH)}$	pin CANH output current during bus failure	Active mode; $V_{RTH} = V_{CANH} = V_{V2}$ = 5 V	-	95	-	µA
CAN termination resistor (pin RTL)						
$R_{sw(RTL)}$	switch-on resistance	Active mode, On-line or Selective Sleep; $\lvert I_o \rvert$ = 10 mA; V_{TXDC} = 5 V; V_{V2} = 5 V	-	40	100	µΩ
$I_{O(RTL)}$	output current	off-line; V_{RTL} = 0 V	−1.50	−0.65	−0.1	mA
		during bus failure at CANL; Active mode; $V_{RTL} = V_{CANL}$ = 0 V; V_{V2} = 5 V	-	−95	-	µA

Table 26. Static characteristics[1] *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT42} = 5.5 V to 52 V;V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN transmit data input; pin TXDL						
V_{IL}	LOW-level input voltage		−0.3	-	$0.3 \times V_{V1}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{V1}$	-	$V_{V1} + 0.3$	V
$R_{TXDL(pu)}$	TXDL pull-up resistor	V_{TXDL} = 0 V	5	12	25	kΩ
LIN receive data output; pin RXDL						
I_{OH}	HIGH-level output current	$V_{RXDL} = V_{V1} - 0.4$ V	−50	-	−1.6	mA
I_{OL}	LOW-level output current	V_{RXDL} = 0.4 V	1.6	-	20	mA
LIN-bus line; pin LIN						
$V_{o(dom)}$	LIN dominant output voltage	Active mode; V_{BAT42} = 7 V to 18 V; LDC = 0; $t < t_{TXDL(dom)(dis)}$; V_{TXDL} = 0 V; $R_{BAT42-LIN}$ = 500 Ω	0	-	$0.20 \times V_{BAT42}$	V
		Active mode; V_{BAT42} = 7.6 V to 18 V; LDC = 1; $t < t_{TXDL(dom)(dis)}$; V_{TXDL} = 0 V; I_{LIN} = 40 mA	0.7	1.4	2.1	V
I_{LIH}	HIGH-level input leakage current	$V_{LIN} = V_{BAT42}$; $V_{TXDL} = V_{V1}$	−10	0	+10	µA
		V_{BAT42} = 8 V; V_{LIN} = 8 V to 18 V; $V_{TXDL} = V_{V1}$	−10	-	+10	µA
I_{LIL}	LOW-level input leakage current	V_{BAT42} = 12 V; V_{LIN} = 0 V; $V_{TXDL} = V_{V1}$	−100	-	-	µA
$I_{o(sc)}$	short-circuit output current	Active mode; $V_{LIN} = V_{BAT42}$ = 12 V; V_{TXDL} = 0 V; $t < t_{TXDL(dom)(dis)}$; LDC = 0	27	40	60	mA
		Active mode; $V_{LIN} = V_{BAT42}$ = 18 V; V_{TXDL} = 0 V; $t < t_{TXDL(dom)(dis)}$; LDC = 0	40	60	90	mA
$V_{th(dom)}$	receiver dominant state	V_{BAT42} = 7 V to 27 V	-	-	$0.4 \times V_{BAT42}$	V
$V_{th(reces)}$	receiver recessive state	V_{BAT42} = 7 V to 27 V	$0.6 \times V_{BAT42}$	-	-	V
$V_{th(hyst)}$	receiver threshold voltage hysteresis	V_{BAT42} = 7 V to 27 V	$0.05 \times V_{BAT42}$	-	$0.175 \times V_{BAT42}$	V
$V_{th(cen)}$	receiver threshold voltage centre	V_{BAT42} = 7 V to 27 V	$0.475 \times V_{BAT42}$	$0.500 \times V_{BAT42}$	$0.525 \times V_{BAT42}$	V
C_{in}	input capacitance	[3]	-	-	10	pF
I_L	leakage current	V_{LIN} = 0 V to 18 V; V_{BAT42} = 0 V	−5	0	+5	µA
		V_{LIN} = 0 V to 18 V; $V_{BAT42} = V_{GND}$ = 12 V (loss of ground)	−10	-	+10	µA

Table 26. Static characteristics[1] *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT42} = 5.5 V to 52 V; V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

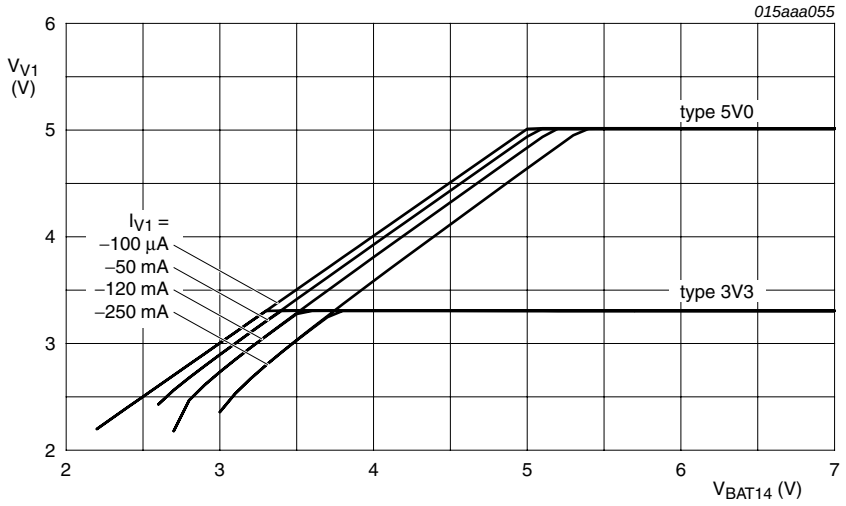
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN-bus termination resistor connection; pin RTLIN						
V_{RTLIN}	RTLIN output voltage	Active mode; I_{RTLIN} = −10 μA; V_{BAT42} = 7 V to 27 V	V_{BAT42} − 1.0	V_{BAT42} − 0.7	V_{BAT42} − 0.2	V
		Off-line mode; I_{RTLIN} = −10 μA; V_{BAT42} = 7 V to 27 V	V_{BAT42} − 1.2	V_{BAT42} − 1.0	-	V
ΔV_{RTLIN}	RTLIN load regulation	Active mode; I_{RTLIN} = −10 μA to −10 mA; V_{BAT42} = 7 V to 27 V	-	0.65	2	V
$I_{RTLIN(pu)}$	RTLIN pull-up current	Active mode; $V_{RTLIN} = V_{LIN}$ = 0 V ($t > t_{LIN(dom)(det)}$)	−150	−60	−35	μA
		Off-line mode; $V_{RTLIN} = V_{LIN}$ = 0 V ($t < t_{LIN(dom)(det)}$)	−150	−60	−35	μA
I_{LIL}	LOW-level input leakage current	Off-line mode; $V_{RTLIN} = V_{LIN}$ = 0 V ($t > t_{LIN(dom)(det)}$)	−10	0	+10	μA
TEST input; pin TEST						
$V_{th(TEST)}$	input threshold voltage	for entering Software Development mode; T_j = 25 °C	1	5	8	V
		for entering Forced Normal mode; T_j = 25 °C	2	10	13.5	V
$R_{(pd)TEST}$	pull-down resistor	between pin TEST and GND	2	4	8	kΩ
Temperature detection						
$T_{j(warn)}$	high junction temperature warning level		160	175	190	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Products are 100 % tested at T_{amb} = 125 °C on wafer level (pretesting). Cased products are 100 % tested at T_{amb} = 25 °C (final testing). Both pretesting and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

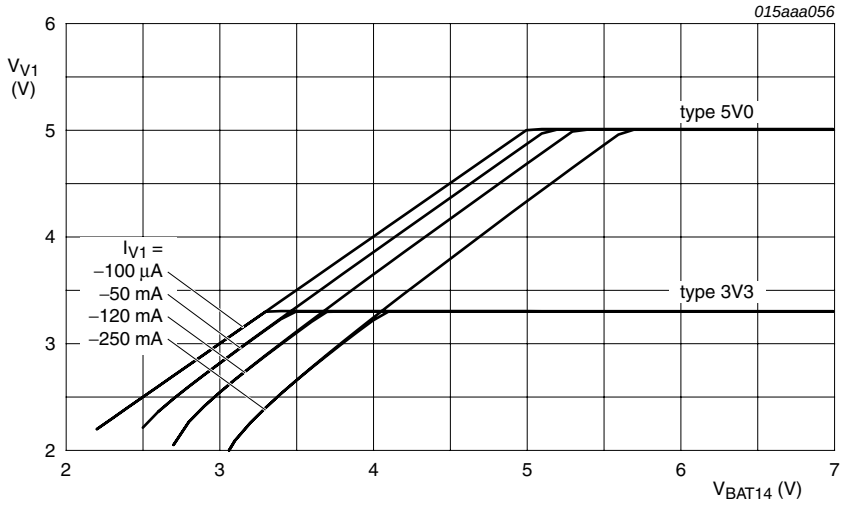
[2] $V_{V1(nom)}$ is 3.3 V or 5 V, depending on the SBC version.

[3] Not tested in production.

[4] V2 internally supplies the SBC CAN transceiver. The supply current needed for the CAN transceiver reduces the pin V2 output capability. The performance of the CAN transceiver can be impaired if V2 is also used to supply other circuitry while the CAN transceiver is in use.

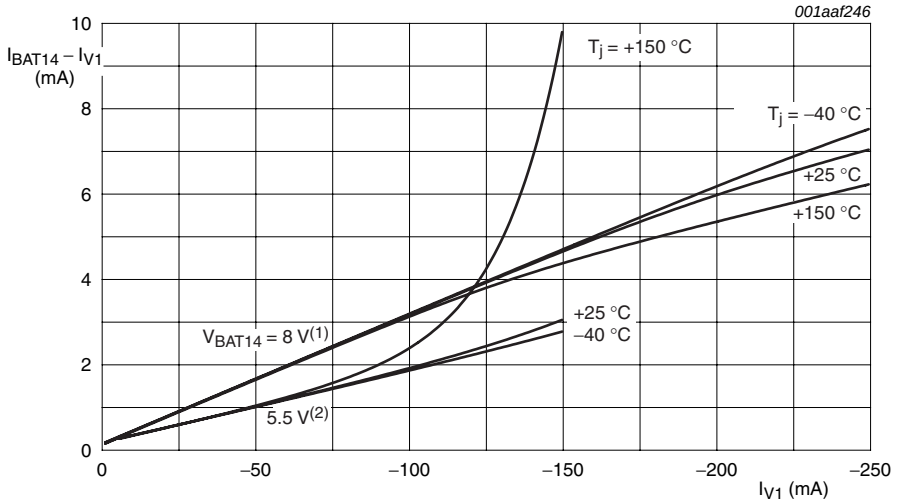


a. T_j = 25 °C.



b. T_j = 150 °C.

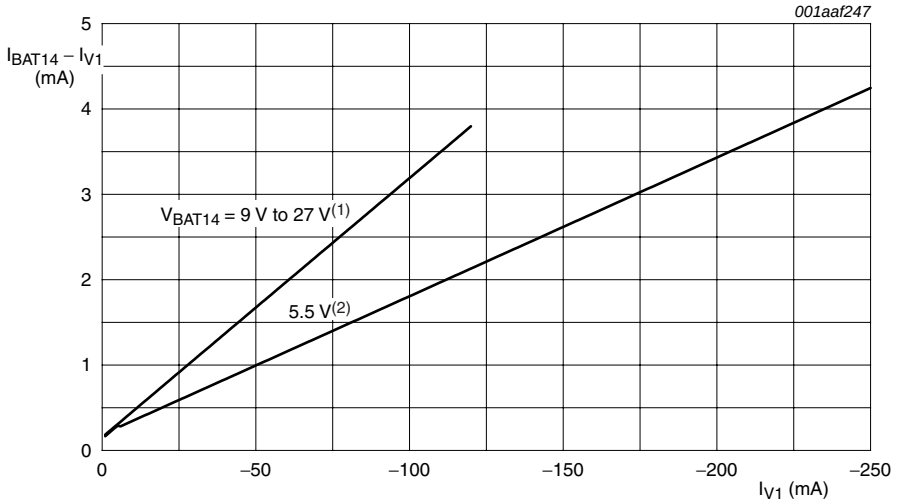
Fig 16. V1 output voltage (dropout) as a function of battery voltage



(1) Types 5V0 and 3V3.

(2) Type 5V0 only.

a. At T_j = −40 °C, +25 °C and +150 °C.

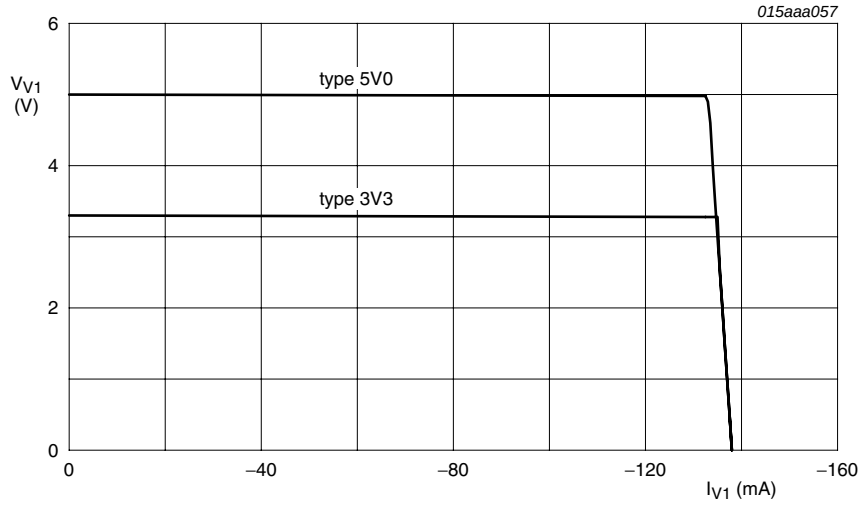


(1) Types 5V0 and 3V3.

(2) Type 3V3 only.

b. At T_j = −40 °C to +150 °C.

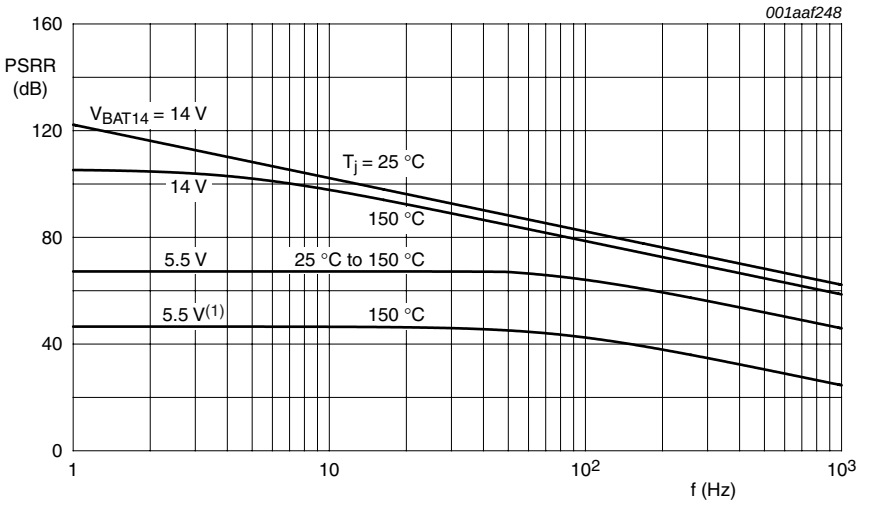
Fig 17. V1 quiescent current as a function of output current



V_{BAT14} = 9 V to 27 V.

T_j = 25 °C to 125 °C.

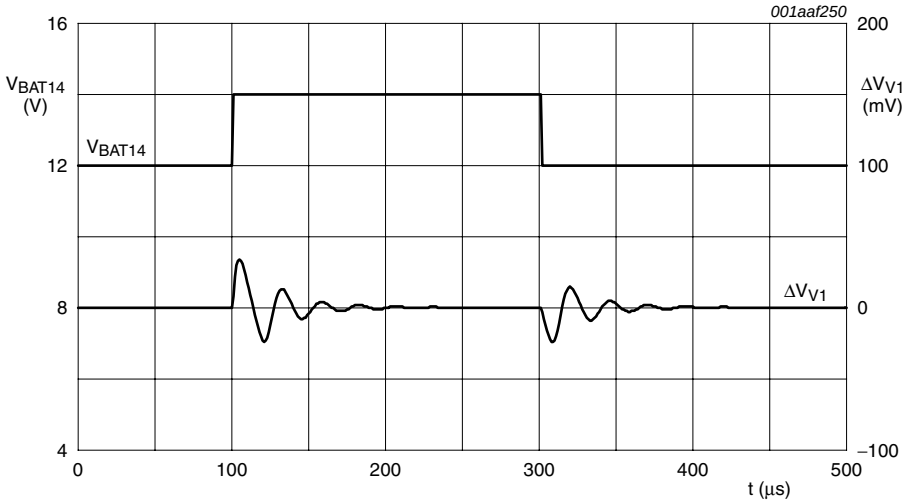
Fig 18. V1 output voltage as a function of output current



I_{V1} = −120 mA.

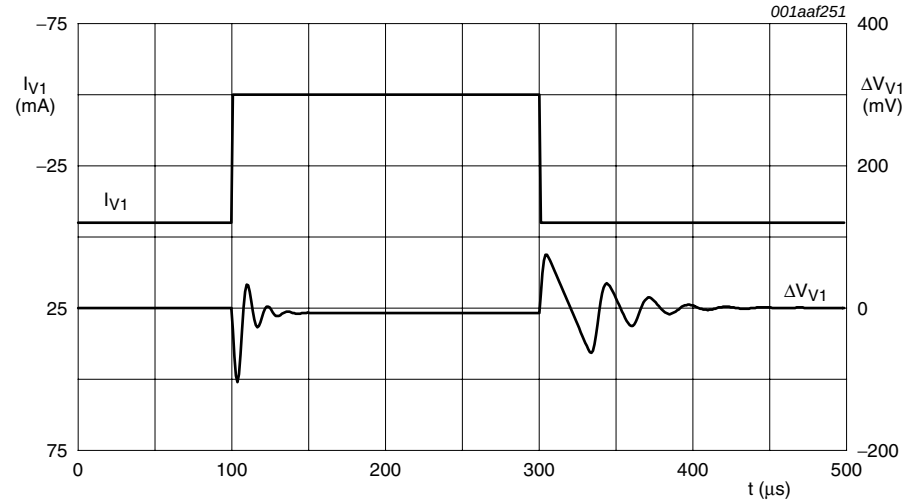
(1) Type 5V0 only.

Fig 19. V1 power supply ripple rejection as a function of frequency



I_{V1} = −5 mA; C = 1 µF; ESR = 0.01 Ω; T_j = 25 °C.

a. Line transient response



V_{BAT14} = 14 V; C = 1 µF; ESR = 0.01 Ω; T_j = 25 °C.

b. Load transient response

Fig 20. V1 transient response as a function of time

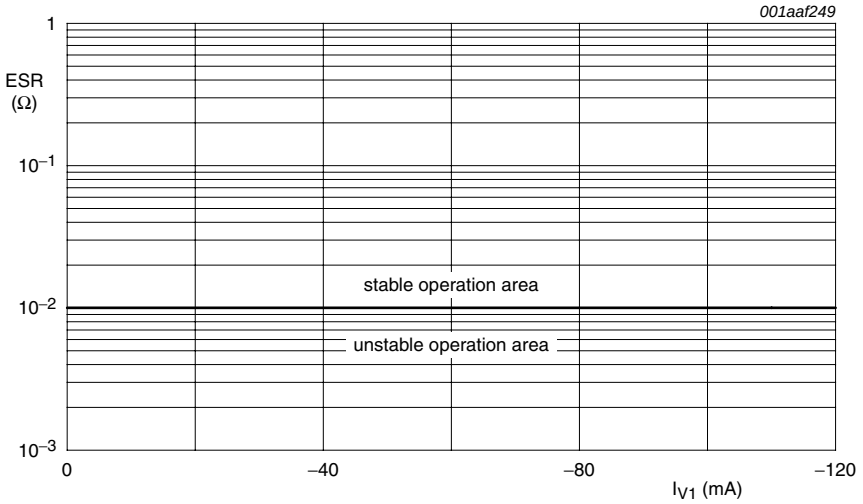
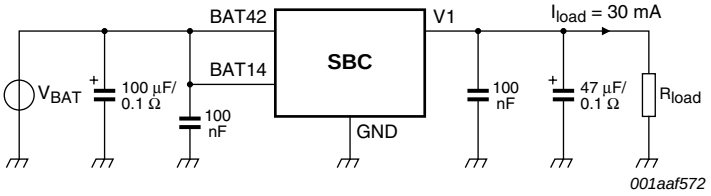
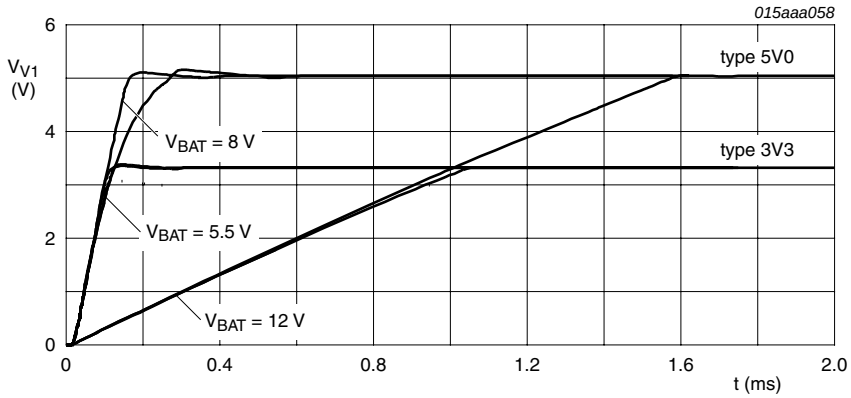


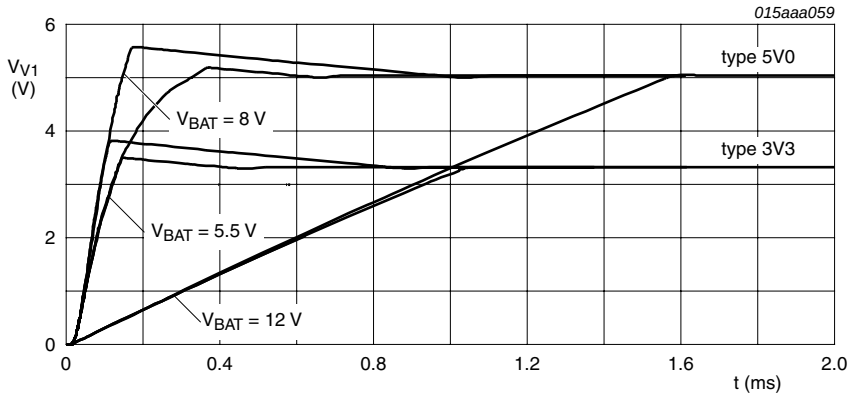
Fig 21. V1 output stability related to ESR value of output capacitor



a. Switch-on test circuit.



b. Behavior at T_j = 25 °C.



c. Behavior at T_j = 85 °C.

Fig 22. Switch-on behavior of V_{V1}

10. Dynamic characteristics

Table 27. Dynamic characteristics[1]

T_{vj} = −40 °C to + 150 °C; V_{BAT42} = 5.5 V to 52 V; V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial peripheral interface timing; pins SCS, SCK, SDI and SDO (see Figure 27)[2]						
T_{cyc}	clock cycle time		960	-	-	ns
t_{lead}	enable lead time	clock is low when SPI select falls	240	-	-	ns
t_{lag}	enable lag time	clock is low when SPI select rises	240	-	-	ns
t_{SCKH}	clock HIGH time		480	-	-	ns
t_{SCKL}	clock LOW time		480	-	-	ns
t_{su}	input data setup time		80	-	-	ns
t_h	input data hold time		400	-	-	ns
t_{DOV}	output data valid time	pin SDO; C_L = 10 pF	-	-	400	ns
t_{SSH}	SPI select HIGH time		480	-	-	ns
CAN transceiver (pins CANL, CANH, TXDC and RXDC)						
$t_{t(rec-dom)}$	output transition time recessive to dominant	between 10 % to 90 %; $R_{CAN\_L} = R_{CAN\_H}$ = 125 Ω; $C_{CAN\_L} = C_{CAN\_H}$ = 1 nF; see Figure 23 and Figure 24	0.3	0.4	-	µs
$t_{t(dom-rec)}$	output transition time dominant to recessive	between 10 % to 90 %; $R_{CAN\_L} = R_{CAN\_H}$ = 125 Ω; $C_{CAN\_L} = C_{CAN\_H}$ = 1 nF; see Figure 23 and Figure 24	0.3	0.6	-	µs
t_{PHL}	propagation delay TXDC to RXDC (HIGH to LOW transition)	between 10 % to 90 %; $R_{CAN\_L} = R_{CAN\_H}$ = 125 Ω; $C_{CAN\_L} = C_{CAN\_H}$ = 1 nF; see Figure 23 and Figure 24	-	-	1.5	µs
t_{PLH}	propagation delay TXDC to RXDC (LOW to HIGH transition)	between 10 % to 90 %; $R_{CAN\_L} = R_{CAN\_H}$ = 125 Ω; $C_{CAN\_L} = C_{CAN\_H}$ = 1 nF; see Figure 23 and Figure 24	-	1.2	1.9	µs
$t_{BUS(fail)(det)}$	bus failure detection time	bus failure HxBAT; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	7	-	38	µs
		bus failure HxVCC	1.6	-	8.0	ms
		bus failures LxGND and HxL	0.3	-	1.6	ms
		bus failure LxBAT; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	0.3	-	1.6	ms
		continuously dominant clamped CAN-bus detection time (start after detecting HxVCC); Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	0.3	-	1.6	ms

Table 27. Dynamic characteristics[1] *…continued*

T_{vj} = −40 °C to + 150 °C; V_{BAT42} = 5.5 V to 52 V; V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{BUS(fail)(recover)}$	bus failure recovery time	bus failure HxBAT	125	-	750	µs
		bus failure HxVCC	0.3	-	1.6	ms
		bus failures LxGND and HxL; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	7	-	38	µs
		bus failures LxGND and HxL	0.3	-	1.6	ms
		bus failure LxBAT; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	125	-	750	µs
		continuously dominant clamped CAN-bus Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	1	-	5	µs
$t_{TXDC(dom)}$	TXDC permanent dominant disable time	Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V; TXDC = logic 0 V	1.5	-	6	ms
$t_{CANH(d1)}$, $t_{CANL(d1)}$	minimum dominant time first pulse for wake-up on pins CANH, CANL	off-line	7	-	38	µs
$t_{CANH(rec)}$, $t_{CANL(rec)}$	minimum recessive time pulse (after first dominant) for wake-up on pins CANH, CANL	off-line	3	-	10	µs
$t_{CANH(d2)}$, $t_{CANL(d2)}$	minimum dominant time second pulse for wake-up on pins CANH, CANL	off-line	0	-	4	µs
$t_{CANL(dom)}$	CANL dominant time entering Normal mode and TXDC goes dominant	V_{CANL} > 8 V, first dominant bit after entering Active mode	3	-	10	µs
$t_{timeout}$	time-out period between wake-up message and confirm message	On-line Listen mode	115	-	285	ms
$t_{offline}$	required recessive or dominant time for entering off-line	On-line or Selective Sleep mode; COTC = logic 0; CMC = logic 0	50	-	66	ms
		On-line or Selective Sleep mode; COTC = logic 1; CMC = logic 0	200	-	265	ms
$t_{off-line(ext)}$	extended minimum time before entering Off-line mode	On-line or On-line Listen mode after CAN wake-up event; TXDC = V_{V1}; V2D = 1; no bus activity	400	-	530	ms

Table 27. Dynamic characteristics[1] …continued

T_{vj} = −40 °C to + 150 °C; V_{BAT42} = 5.5 V to 52 V; V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{CANH}, t_{CANL}	ground shift sampling time required for CANH, CANL voltage level	Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V; TXDC recessive		20	-	80	µs
Δt_{PC}	pulse count difference between CANH and CANL for failure detection	bus failures H//, L//, HxGND and LxVCC; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V		-	4	-	pulses
	dominant pulse count on CANH and CANL for failure recovery	bus failures H//, L//, HxGND and LxVCC; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V		-	4	-	pulses
LIN transceiver; pins LIN, TXDL and RXDL[3]							
δ1	duty cycle 1	$V_{th(reces)(max)} = 0.744 \times V_{BAT42}$; $V_{th(dom)(max)} = 0.581 \times V_{BAT42}$; LSC = 0; t_{bit} = 50 µs; V_{BAT42} = 7 V to 18 V	[4]	0.396	-	-	
δ2	duty cycle 2	$V_{th(reces)(min)} = 0.422 \times V_{BAT42}$; $V_{th(dom)(min)} = 0.284 \times V_{BAT42}$; LSC = 0; t_{bit} = 50 µs; V_{BAT42} = 7.6 V to 18 V	[5]	-	-	0.581	
δ3	duty cycle 3	$V_{th(reces)(max)} = 0.778 \times V_{BAT42}$; $V_{th(dom)(max)} = 0.616 \times V_{BAT42}$; LSC = 1; t_{bit} = 96 µs; V_{BAT42} = 7 V to 27 V	[4]	0.417	-	-	
δ4	duty cycle 4	$V_{th(reces)(min)} = 0.389 \times V_{BAT42}$; $V_{th(dom)(min)} = 0.251 \times V_{BAT42}$; LSC = 1; t_{bit} = 96 µs; V_{BAT42} = 7.6 V to 27 V	[5]	-	-	0.590	
$t_{p(rx)}$	propagation delay of receiver	C_{RXDL} = 20 pF		-	-	6	µs
$t_{p(rx)(sym)}$	symmetry of receiver propagation delay	rising edge with respect to falling edge; C_{RXDL} = 20 pF		−2	-	+2	µs
$t_{BUS(LIN)}$	minimum dominant time for wake-up of the LIN-transceiver	Off-line mode		30	-	150	µs
$t_{LIN(dom)(det)}$	continuously dominant clamped LIN-bus detection time	Active mode; LIN = 0 V		40	-	160	ms
$t_{LIN(dom)(rec)}$	continuously dominant clamped LIN-bus recovery time	Active mode		0.8	-	2.2	ms
$t_{TXDL(dom)(dis)}$	TXDL permanent dominant disable time	Active mode; TXDL = 0 V		20	-	80	ms

Table 27. Dynamic characteristics[1] *…continued*

T_{vj} = −40 °C to + 150 °C; V_{BAT42} = 5.5 V to 52 V; V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Battery monitoring						
$t_{BAT42(L)}$	BAT42 LOW time for setting PWONS		5	-	20	µs
Power supply V1; pin V1						
$t_{V1(CLT)}$	V1 clamped LOW time during ramp-up of V1	Start-up mode; V1 active	229	-	283	ms
Power supply V2; pin V2						
$t_{V2(CLT)}$	V2 clamped LOW time during ramp-up of V2	V2 active	28	-	36	ms
Power supply V3; pin V3						
$t_{W(CS)}$	cyclic sense period	V3C = 10; see Figure 13	14	-	18	ms
		V3C = 11; see Figure 13	28	-	36	ms
$t_{on(CS)}$	cyclic sense on-time	V3C = 10; see Figure 13	345	-	423	µs
		V3C = 11; see Figure 13	345	-	423	µs
Wake-up input; pin WAKE						
$t_{WU(ipf)}$	input port filter time	V_{BAT42} = 5 V to 27 V	5	-	120	µs
		V_{BAT42} = 27 V to 52 V	30	-	250	µs
$t_{su(CS)}$	cyclic sense sample setup time	V3C = 11 or 10; see Figure 13	310	-	390	µs
Watchdog						
$t_{WD(ETP)}$	earliest watchdog trigger point	programmed Nominal Watchdog Period (NWP); Normal mode	0.45 × NWP	-	0.55 × NWP	
$t_{WD(LTP)}$	latest watchdog trigger point	programmed nominal watchdog period; Normal mode, Standby mode and Sleep mode	0.9 × NWP	-	1.1 × NWP	
$t_{WD(init)}$	watchdog initializing period	watchdog time-out in Start-up mode	229	-	283	ms
Fail-safe mode						
t_{ret}	retention time	Fail-safe mode; wake-up detected	1.3	1.5	1.7	s
Reset output; pin RSTN						
$t_{RSTN(CHT)}$	clamped HIGH time, pin RSTN	RSTN driven LOW internally but RSTN pin remains HIGH	115	-	141	ms
$t_{RSTN(CLT)}$	clamped LOW time, pin RSTN	RSTN driven HIGH internally but RSTN pin remains LOW	229	-	283	ms
$t_{RSTN(INT)}$	interrupt monitoring time	INTN = 0	229	-	283	ms

Table 27. Dynamic characteristics[1] *...continued*

T_{vj} = −40 °C to + 150 °C; V_{BAT42} = 5.5 V to 52 V; V_{BAT14} = 5.5 V to 27 V; $V_{BAT42} \geq V_{BAT14} - 1$ V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RSTNL}	reset lengthening time	after internal or external reset has been released; RLC = 0	0.9	-	1.1	ms
		after internal or external reset has been released; RLC =1	18	-	22	ms
Interrupt output; pin INTN						
t_{INTN}	interrupt release	after SPI has read out the Interrupt register	2	-	-	µs
Oscillator						
f_{osc}	oscillator input frequency		460.8	512	563.2	kHz

[1] All parameters are guaranteed over the virtual junction temperature range by design. Products are 100 % tested at T_{amb} = 125 °C on wafer level (pretesting). Cased products are 100 % tested at T_{amb} = 25 °C (final testing). Both pretesting and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] SPI timing is guaranteed for V_{BAT42} voltages down to 5 V. For V_{BAT42} voltages down to 4.5 V the guaranteed SPI timing values double, so at these lower voltages a lower maximum SPI communication speed must be observed.

[3] t_{bit} = selected bit time, depends on LSC-bit; 50 µs or 96 µs (20 kbit/s or 10.4 kbit/s respectively); bus load conditions (R_1/R_2/C_1): 1 kΩ/1 kΩ/10 nF; 1 kΩ/1 kΩ/6.8 nF; 1 kΩ/open/1 nF; see Figure 25 and Figure 26.

[4] $$\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$$

[5] $$\delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$$

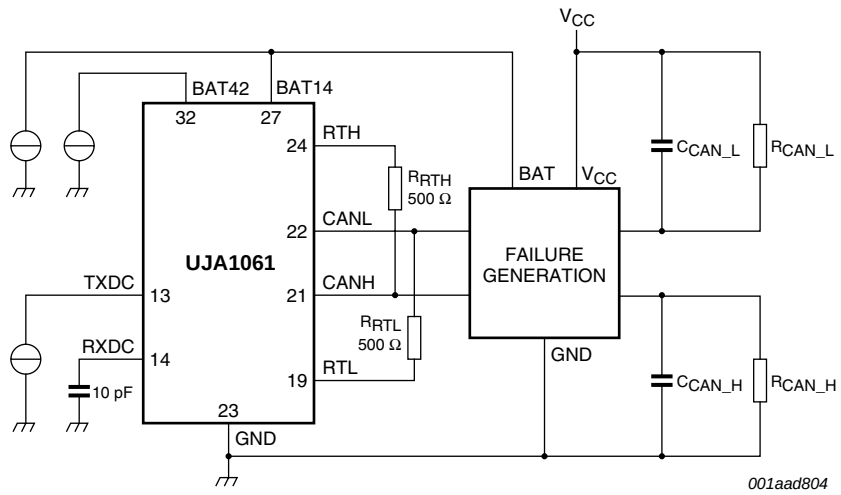


Fig 23. Timing test circuit for CAN transceiver

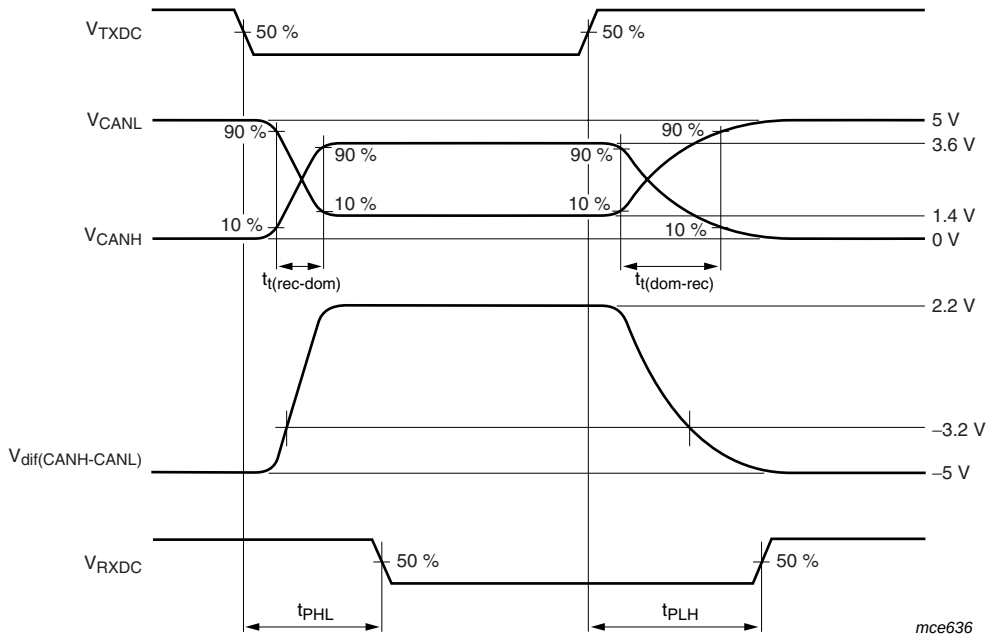


Fig 24. Timing diagram CAN transceiver

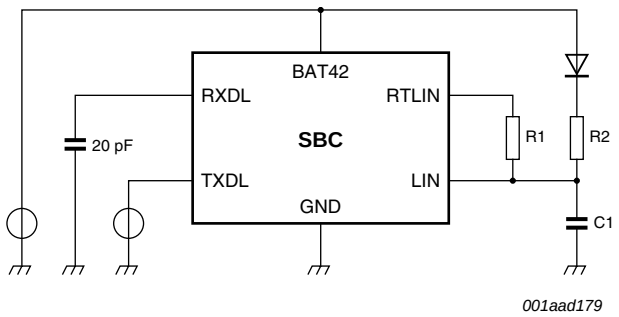


Fig 25. Timing test circuit for LIN transceiver

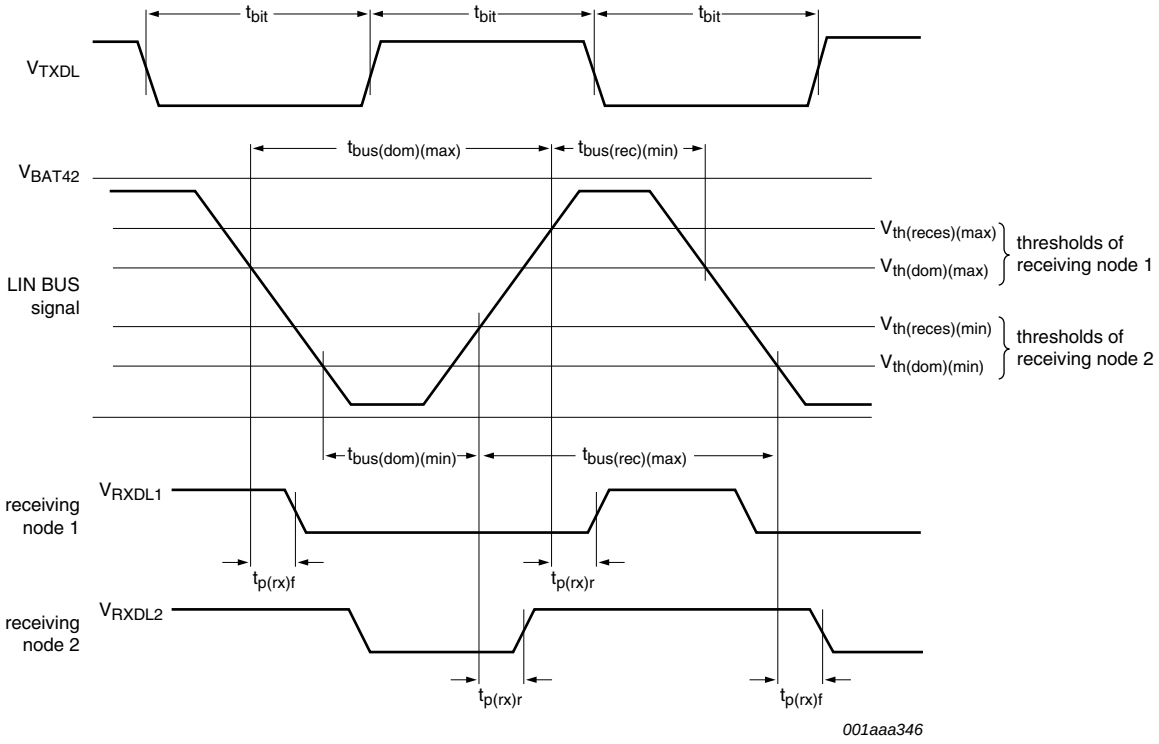


Fig 26. Timing diagram LIN transceiver

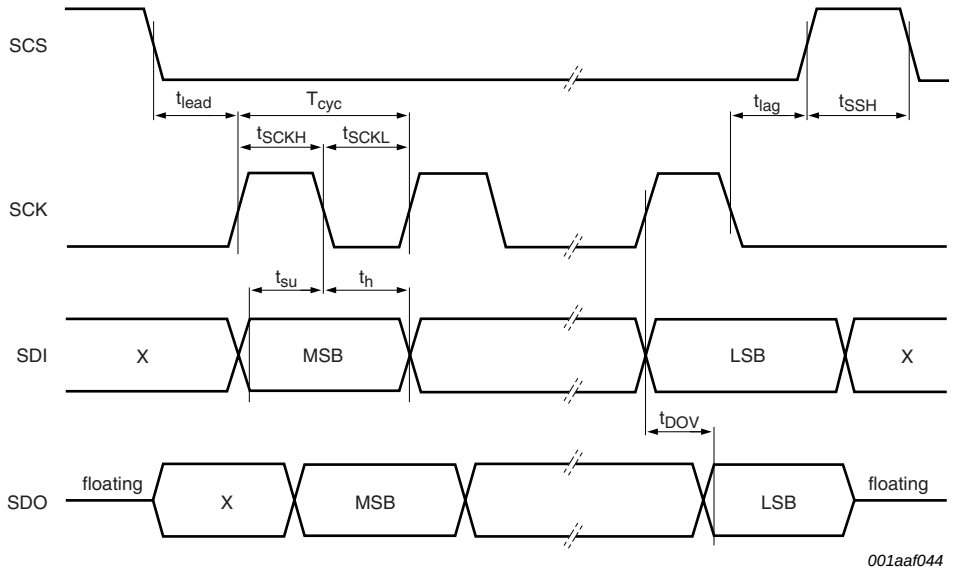


Fig 27. SPI timing

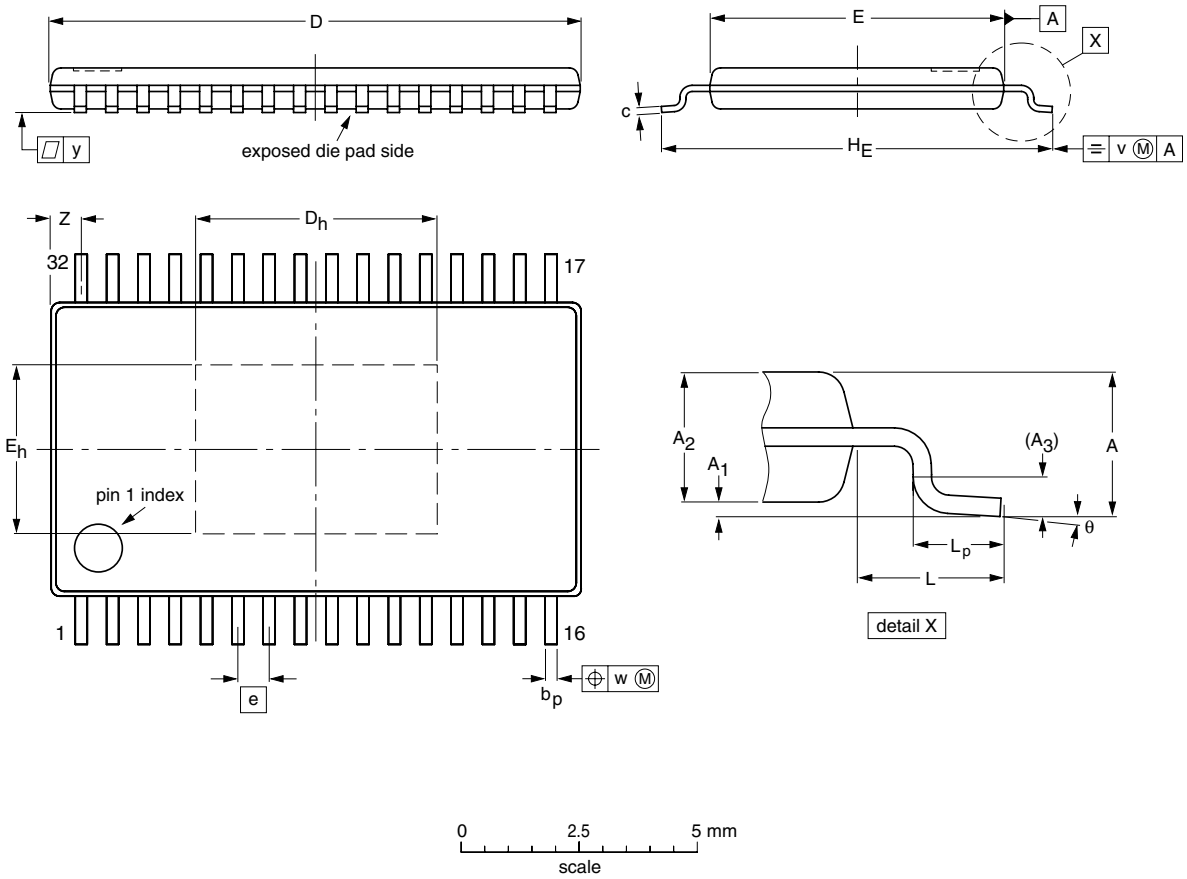
11. Test information

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

12. Package outline

HTSSOP32: plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad **SOT549-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(2)}$	E_h	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.09	11.1 10.9	5.1 4.9	6.2 6.0	3.6 3.4	0.65	8.3 7.9	1	0.75 0.50	0.2	0.1	0.1	0.78 0.48	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT549-1		MO-153				~~03-04-07~~ 05-11-02

Fig 28. Package outline SOT549-1 (HTSSOP32)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 29) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 28 and 29

Table 28. SnPb eutectic process (from J-STD-020C)

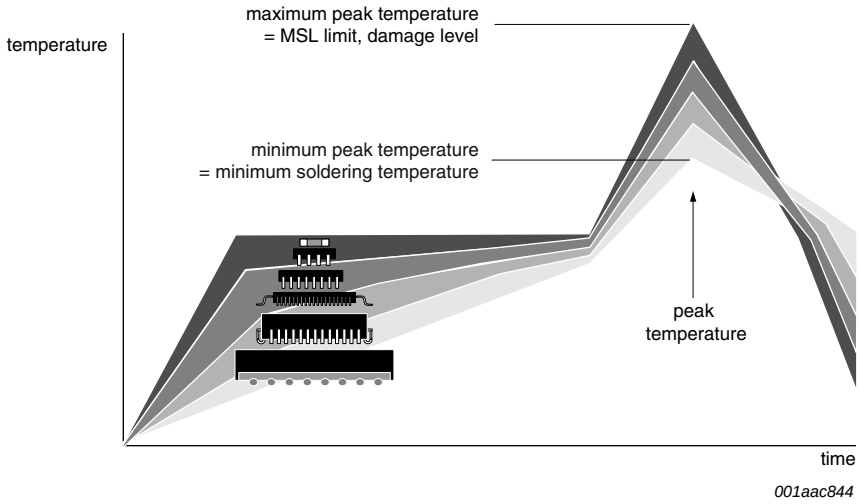
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 29. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 29.



MSL: Moisture Sensitivity Level

Fig 29. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UJA1061_6	20100309	Product data sheet	-	UJA1061_5
Modifications:	• 3.0 V version (UJA1061TW/3V0) discontinued • Table 26: updated conditions for $V_{O(reces)}$ - CANL recessive output voltage • Section 6.2.5: text of third paragraph revised • Table 11: text of bit 4, V1CMC, revised • Section 11.1: text revised • Section 2.1: text revised			
UJA1061_5	20071122	Product data sheet	-	UJA1061_4
UJA1061_4	20070427	Product data sheet	-	UJA1061_3
UJA1061_3	20060627	Preliminary data sheet	-	UJA1061_2
UJA1061_2 (9397 750 14201)	20051122	Objective data sheet	-	UJA1061_1
UJA1061_1 (9397 750 11708)	20040322	Objective specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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