STRUCTURE Silicon Monolithic Integrated Circuit
PRODUCT SERIES 7-Channel Switching Regulator Controleer for Digital Camera
TYPE **BD9749MWV**
PIN ASSIGNMENT Fig.1
BLOCK DIAGRAM Fig.1
PACKAGE Fig.2

Functions
- 1.5V minimum input operating
- Supplies power for the internal circuit by using charge-pump circuit which outputs a voltage twice bigger than VBAT voltage. or a equal voltage as VBAT + VIN.
- Contains step-up converter(1ch), step-down converter(1ch), cross converter(1ch), configurable for step-up/step-down converter(2ch).
- Contains 4FETs for the cross converter channel
- 3channels contain transistor for synchronous rectifying action mode.
- Contains a FET for step-up converter for CCD.
- ALL channels contain internal compensation between inputs outputs of error amps.
- Contains sequence control circuit for ch2,3 and 4. Sequence for ch5 and 6 are configurable for two types.
- Two channels have high side switches with soft start function.
- Two channels have PMOS back gate control circuit.
- thermally enhanced QFN48 package.(7mm x 7mm, 0.4mm pitch)

○Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Units
Power Supply Boltage	VBAT	−0.3～7	V
Power Input Voltage	VHx1～4	−0.3～7	V
	HS6H,HS7H	−0.3～7	V
	VLx6	−0.3～18	V
	VIN	-0.3～7	V
Output Current	IomaxLx1	±1.2	A
	IomaxHx2	±1.5	A
	IomaxHx3～4	±1.2	A
	IomaxHS6～7	±1.2	A
	IomaxLx6	±0.8	A
Power Dissipation	Pd	0.60 *1	W
Operating Temperature	Topr	−25～+85	°C
Storage Temperature	Tstg	−55～+150	°C
Junction Tempareture	Tjmax	+150	°C

(*1) Without external heat sink, the power dissipation reduces by 4.8mW/°C over 25°C。

○Recommended operating conditions

Parameter	Symbol	Spec			Unit
		MIN	TYP	MAX	
Power Supply Voltage	VBAT	1.5		5.5	V
VREF Pin Connecting Capacitor	CVREF	0.47	1.0	4.7	μF
VREGA Pin Connecting Capacitor	CVREGA	0.47	1.0	4.7	μF
SCP Pin Connecting Capacitor	CSCP	—	—	0.47	μF
C+H to C+L connecting Capacitor	CF	1.0	-	-	μF
【Oscillator】					
Oscillator Frequency	fosc	0.6	1.2	1.5	MHz
OSC Timing Resistor	RT	47	62	120	kΩ

Status of this document
The Japanese version of this document is the official specification. Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

○Electrical characteristics (Ta=25°C, VBAT=3V, RT=62k, STB1～7=3V)

Parameter	Symbol	Standard value			Units	Conditions
		MIN	TYP	MAX		
【Charge Pump Circuit】						
Output Voltage (Regulated)	Vcpout1	5.2	5.4	—	V	Io=1mA, INV1～7=1.2V NON5=-0.2V
Output Voltage (X2 Step up)	Vcpout2	4.5	4.8	—	V	Only for internal Current VBAT=2.5V, INV1～7=1.2V NON5=-0.2V
Output Resistance	Vcpro	—	35	50	Ω	CF=1μF, VBAT=2.5V
Operating Frequency	fcp	60	75	90	kHz	RT=62kΩ
Minimum VBAT Voltage	Vst1	1.5	—	—	V	
【Internal Regulator VREGA】						
Output Voltage	VREGA	2.4	2.5	2.6	V	Io=5mA
【Prevention Circuit of Miss Operation by Low voltage Input】						
Threshold Voltage	Vstd1	—	2.15	2.30	V	VREGA Monitor
Hysteresis Width	⊿Vstd1	50	100	200	mA	
【Short Circuit Protection】						
SCP Stand by Voltage	Vssc	—	22	170	mV	
SCP Out Source Current	Iscp	2	4	6	μA	Vscp=0.1V
SCP Threshold Voltage	Vscp	0.9	1.0	1.1	V	
【Oscillator】						
Frequency CH1～4	fosc1	1.0	1.2	1.4	MHz	RT=62kΩ
Frequency CH5～7	fosc2	0.5	0.6	0.7	MHz	RT=62kΩ
Max Duty 1,3,4 (Step Down)	Dmax1d	—	—	100	%	Vscp=0V ※
Max Duty 1,4 (Step Up)	Dmax1u	86	92	96	%	
Max Duty 5,6,7	Dmax2	86	92	96	%	
Max Duty CH2 LX21	Dmax3	—	—	100	%	
Max Duty CH2 LX22	Dmax4	78	84	90	%	
【Error AMP】						
Input Bias Current	IINV	—	0	50	nA	INV1～7, NON5=3.0V
INV Threshold Voltage1	VINV1	0.79	0.80	0.81	V	CH1～4
INV Threshold Voltage2	VINV2	0.99	1.00	1.01	V	CH6, 7V
INV Threshold Voltage3	VINV3	380	400	420	mV	CH7I
【Base Bias Voltage Vref for inverted Channel】						
CH5 OutputVoltage	VOUT5	-6.09	-6.00	-5.91	V	NON5 resistor12kΩ, 72kΩ
Line Regulation	DVLi	—	4.0	12.5	mV	CPOUT=1.5～5.5V
Load Regulation	DVLo	—	1.0	7.5	mV	Iref=10uA～100uA
Output Current When shorted	Ios	0.2	1.0	—	mA	Vref=0V
【Soft Start】						
CH1,2,4 Soft Start Time	Tss1	3.4	4.4	5.4	msec	RT=62kΩ
CH3 Soft Start Time	Tss2	1.2	2.2	3.2	msec	RT=62kΩ
CH5 Soft Start Time	Tss3	3.4	4.4	5.4	msec	RT=62kΩ
CH6,7 Soft Start Time	Tss4	4.4	5.5	6.6	msec	RT=62kΩ

Parameter	Symbol	Standard value			Units	Conditions
		Min	TYP	MAX		
【Output Driver】						
CH1 Highside SW ON Resistance	RON1P	—	280	380	mΩ	HX1=5V
CH1 Lowside SW ON Resistance	RON1N	—	120	180	mΩ	CPOUT=5.4V
CH2 LX21 端子 Highside SW ON Resistance	RON21P	—	160	240	mΩ	HX2=3.0V, CPOUT=5.4V
CH2 LX21Pin Lowside SW ON Resistance	RON21N	—	130	200	mΩ	CPOUT=5.4V
CH2 LX22Pin Highside SW ON Resistance	RON22P	—	180	280	mΩ	VOUT2=5.0V
CH2 LX22Pin Lowside SW ON Resistance	RON22N	—	130	200	mΩ	CPOUT=5.4V
CH3 Highside SW ON Resistance	RON3P	—	160	260	mΩ	HX3=3.0V, CPOUT=5.4V
CH3 Lowside SW ON Resistance	RON3N	—	130	200	mΩ	CPOUT=5.4V
CH4 Highside SW ON Resistance	RON4P	—	280	380	mΩ	HX4=5.0V
CH4 Lowside SW ON Resistance	RON4N	—	130	200	mΩ	CPOUT=5.4V
CH6 NMOS SW ON 抵抗	RON6N	—	400	700	mΩ	CPOUT=5.4V
CH6,7 Load SW ON Resistance	RON67P	—	200	300	mΩ	HS6H,HS7H=3.0V CPOUT=5.4V
CH5 Driver Output Voltage H	Vout5H	—	PVCC5 -1.5	—	V	
CH5 Driver Output Voltage L	Vout5L	—	0.5	1.0	V	
OUT7 Driver Output Voltage H	Vout7H	—	CPOUT -1.5	—	V	
OUT7 Driver Output Voltage L	Vout7L	—	0.5	1.0	V	
【Switch to configure step up/down, Switch to configure CCD sequence】						
UDSEL1,4 Control Voltage — Step down	VUDDO	CPOUT ×0.7	—	CPOUT	V	
UDSEL1,4 Control Voltage — Step up	VUDUP	0	—	CPOUT ×0.3	V	
CCD SEQ Control Voltage — with sequence	VSEQG	0	—	CPOUT ×0.3	V	
CCD SEQ Control Voltage — without sequence	VSEQV	CPOUT ×0.7	—	CPOUT	V	
【STB1～7】						
STB control Voltage — Active	VSTBH1	1.5	—	5.5	V	
STB control Voltage — Non Active	VSTBL1	-0.3	—	0.3	V	
STB1 Pin Pull down Resistance	RSTB1	150	240	350	kΩ	
STB234, 56, 7 Pin Pull down Resistance	RSTB2	250	400	700	kΩ	
【Circuit Current】						
Stand-by Current — VBAT terminal	ISTB1	—	—	5	μA	
Stand-by Current — HX terminal	ISTB2	—	—	5	μA	Step-down UDSEL1,4=CPOUT
Stand-by Current — LX terminal	ISTB3	—	—	5	μA	Step-up UDSEL1,4=0V
Stand-by Current — HS67H terminal	ISTB4	—	—	5	μA	
Circuit Current1 (VBAT current when voltage supplied for the terminal)	Icc1	—	7.0	11.0	mA	INV1～7=1.2V, NON5=-0.2V, VBAT=3.0V
Circuit Current2 (CPOUT current when voltage supplied for the terminal)	Icc2	—	3.0	5.0	mA	INV1～7=1.2V, NON5=-0.2V, CPOUT=5.4V C-H, C-L=OPEN

◎This product is not designed for normal operation with in a radioactive environment

※The protective circuit start working when circuit is operated by 100% duty.

So it is possible to use only for transition time shorter than charge time for SCP.

○Pin Assignment ・Block Diagram

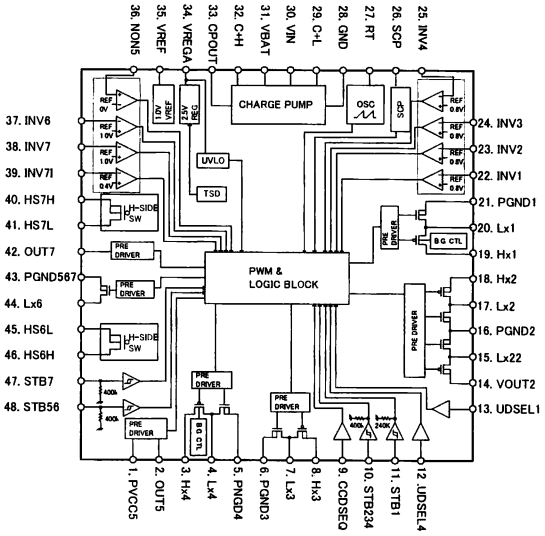

Fig. 1

○Pin Description

Pin Name	Description
VBAT	Input for battery boltage
VIN	Peturning voltage from output terminal
CPOUT	Output terminal for Charge Pump
GND	Ground terminal
C+H	Terminal for connecting flying capasitor for Charege Pump (H side)
C+L	Terminal for connecting flying capasitor for Charege Pump (L side)
PGND1,2,3,4,567	Ground terminal for internal FET
VREGA	VREGA output
VREF	CH5 base bias voltage
PVCC5	CH5 PMOS VCC input for driver
OUT5	Terminal for connecting gate of CH5 PMOS
OUT7	Terminal for connecting gate of CH7 NMOS
Hx1,3,4	Input terminal for synchronous High side switch, Power supply for Pch Driver
Lx1,3,4,6	Terminal for connecting inductors
Hx2	Power supply for channel 2

PinName	Description
Lx21	Terminal for connecting inductor for CH2 input
Lx22	Terminal for connecting inductor for CH2 output
VOUT2	CH2 output voltage
HS6H,HS7H	Power supply for internal load switch
HS6L,HS7L	Output terminal for internal load switch
INV1,2,3,4,6,7	Error AMP inverted input
NON5	Error AMP non-inverted input
INV7I	Error AMP inverted input
RT	For connecting a resistor to set the OSC frequency
SCP	for connecting a capacitor to set up the delay time of the SCP
UDSEL1,4	Step-up/down switching mode selection (H: step-down / L: step-up)
STB1,234,7,56	ON/OFF switch H: Operating over 1.5V
CCDSEQ	Terminal for setting CCD sequence (H: Independent, L: Inverted channel starts after step-up starts)

○Package

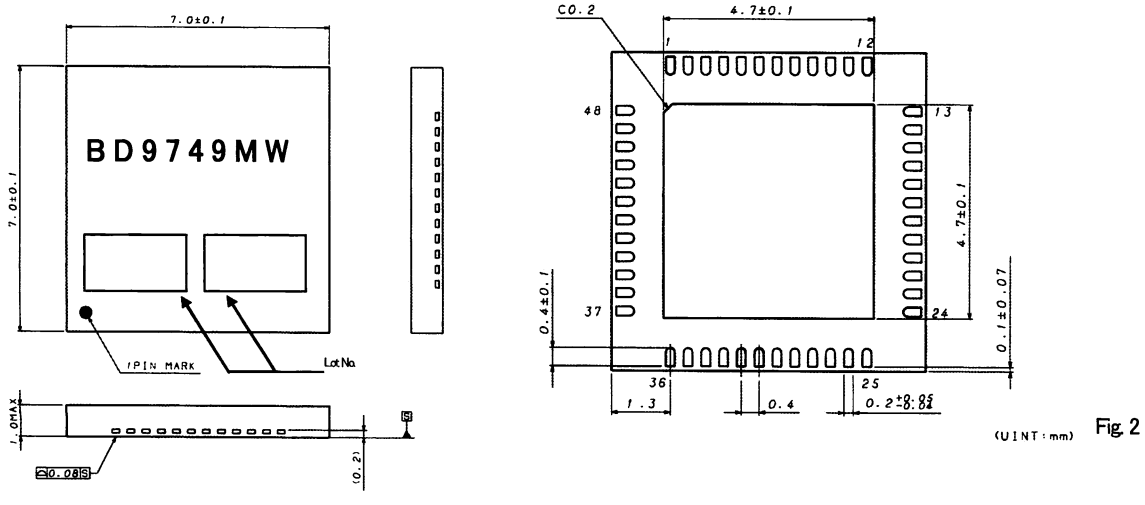

Fig. 2

○Operation Notes

1.) Absolute maximum ratings
This product is produced with strict quality control. However, the IC may be destroyed if operated beyond its absolute maximum ratings. If the device is destroyed by exceeding the recommended maximum ratings, the failure mode will be difficult to determine. (E.g. short mode, open mode) Therefore, physical protection counter-measures (like fuse) should be implemented when operating conditions beyond the absolute maximum ratings anticipated.

2.) GND potential
Make sure GND is connected at lowest potential. All pins except NON5, must not have voltage below GND. Also, NON5 pin must not have voltage below - 0.3V on start up.

3.) Setting of heat
Make sure that power dissipation does not exceed maximum ratings.

4.) Pin short and mistake fitting
Avoid placing the IC near hot part of the PCB. This may cause damage to IC. Also make sure that the output-to-output and output to GND condition will not happen because this may damage the IC.

5.) Actions in strong magnetic field
Exposing the IC within a strong magnetic field area may cause malfunction.

6.) Mutual impedance
Use short and wide wiring tracks for the main supply and ground to keep the mutual impedance as small as possible. Use inductor and capacitor network to keep the ripple voltage minimum.

7.) Voltage of STB pin
The threshold voltages of STB pin are 0.3V and 1.5V. STB state is set below 0.3V while action state is set beyond 1.5V.
The region between 0.3V and 1.5V is not recommended and may cause improper operation.
The rise and fall time must be under 10msec. In case to put capacitor to STB pin, it is recommended to use under 0.01 μF.

8.) Thermal shutdown circuit (TSD circuit)
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

9.)Rush current at the time of power supply injection.
An IC which has plural power supplies, or CMOS IC could have momentary rush current at the time of power supply injection. Please take care about power supply coupling capacity and width of power Supply and GND pattern wiring.

10.)IC Terminal Input
This IC is a monolithic IC that has a P- board and P+ isolation for the purpose of keeping distance between elements. A P-N junction is formed between the P-layer and the N-layer of each element, and various types of parasitic elements are then formed.
For example, an application where a resistor and a transistor are connected to a terminal (shown in Fig.15):
○When GND > (terminal A) at the resistor and GND > (terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.
○When GND > (terminal B) at the transistor (NPN), a parasitic NPN transistor operates as a result of the NHayers of other elements in the proximity of the aforementioned parasitic diode.
Parasitic elements are structurally inevitable in the IC due to electric potential relationships. The operation of parasitic elements Induces the interference of circuit operations, causing malfunctions and possibly the destruction of the IC. Please be careful not to use the IC in a way that would cause parasitic elements to operate. For example, by applying a voltage that is lower than the GND (P-board) to the input terminal.

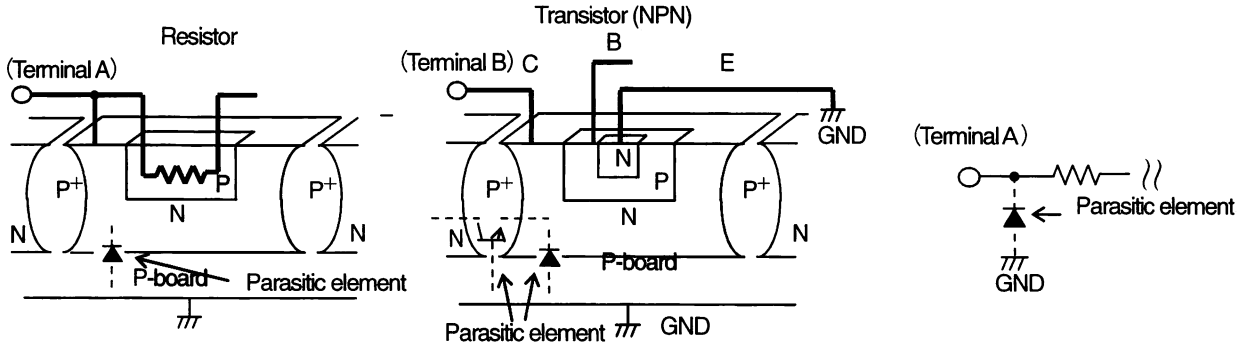

Fig - 3 Simplified structure of a Bipolar IC

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