MAAD-008789-000100

Digital Attenuator
32.0 dB, 2-Bit, TTL Driver, DC-4.0 GHz

Rev. V1

Features

- Attenuation: Two 16 dB bits
- Low DC Power Consumption
- Small Footprint, PQFN Package
- Integral TTL Driver
- 50 ohm Impedance
- Test Boards are Available
- RoHS* Compliant

Description

M/A-COM's MAAD-008789-000100 is a GaAs FET 2-bit digital attenuator with two 16 dB steps and 32 dB total attenuation with integral TTL driver. This device is in a RoHS compliant PQFN plastic surface mount package. MAAD-008789-000100 is ideally suited for use where accuracy, very low power consumption and low costs are required. Typical applications include dynamic range setting in precision receiver circuits and other gain/leveling control circuits. Environmental screening is available. Contact the factory for information.

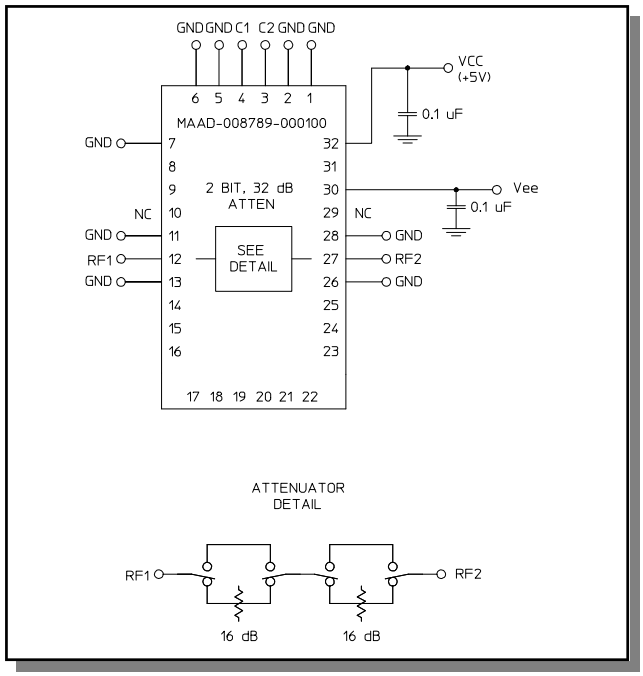
Ordering Information

Part Number	Package
MAAD-008789-000100	Bulk Packaging
MAAD-008789-0001TR	1000 piece reel
MAAD-008789-0001TB	Sample Test Board

Note: Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Functional Schematic



Pin Configuration[1]

Pin No.	Function	Pin No.	Function
1	GND	17	NC
2	GND	18	NC
3	C2	19	NC
4	C1	20	NC
5	GND	21	NC
6	GND	22	NC
7	GND	23	NC
8	NC	24	NC
9	NC	25	NC
10	NC[2]	26	GND
11	GND	27	RF2
12	RF1	28	GND
13	GND	29	NC[2]
14	NC	30	Vee
15	NC	31	NC
16	NC	32	+Vcc

1. The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages)
2. Pins 10 & 29 must be isolated

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Electrical Specifications: T_A = 25°C, Z_0 = 50Ω, V_{CC} = +5.0V, V_{EE} = -5.0V

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Operating Power	—	—	dBm	—	—	+20
Insertion Loss	—	DC - 4.0 GHz	dB	—	—	0.9
Attenuation Accuracy Relative to Reference Loss State	16 dB Bit (C1 Control) 32 dB Attenuation	DC - 4.0 GHz DC - 4.0 GHz	±(0.2 +3% of atten setting in dB) ±(0.2 +3% of atten setting in dB)			
VSWR	Reference Loss	DC - 4.0 GHz	Ratio	—	—	1.5:1
	16 dB Bit (C1 Control) or 32 dB Attenuation	DC - 4.0 GHz	Ratio	—	—	1.8:1
Switching Speed Ton Toff Trise Tfall	 1.3 V Cntl to 90% RF 1.3 V Cntl to 10% RF 10% RF to 90% RF 90% RF to 10% RF	 — — — —	 ns ns ns ns	 — — — —	 190 15 190 6	 — — — —
1 dB Compression[3]	Reference State Reference State	50 MHz 0.5 - 4.0 GHz	dBm dBm	— —	+25 >+27	— —
Input IP3	Two-tone inputs up to +5 dBm at reference state	50 MHz 0.5-4.0 GHz	dBm dBm	— —	+40 +40	— —
Vcc Vee	— —	— —	V V	4.75 -8.0	5.0 -5.0	5.25 -4.75
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	— —	V V	0.0 1.8	0 2.0	0.8 5.0
Iin (Input Leakage Current)	Vin = V_{CC} or GND	—	uA	-1	—	1
Icc (Quiescent Supply Current)	Vcntrl = V_{CC} or GND	—	uA	—	250	400
ΔIcc (Additional Supply Current Per TTL Input Pin)	V_{CC} = Max Vcntrl = V_{CC} - 2.1 V	—	mA	—	—	1.5
I_{EE}	V_{EE} min to max Vin = V_{IL} or V_{IH}	—	mA	-1.0	-0.2	—
Thermal Resistance θjc	—	—	°C/W	—	15	—

3. 1 dB Compression was measured up to +27 dBm, which is the absolute maximum rating for this device.

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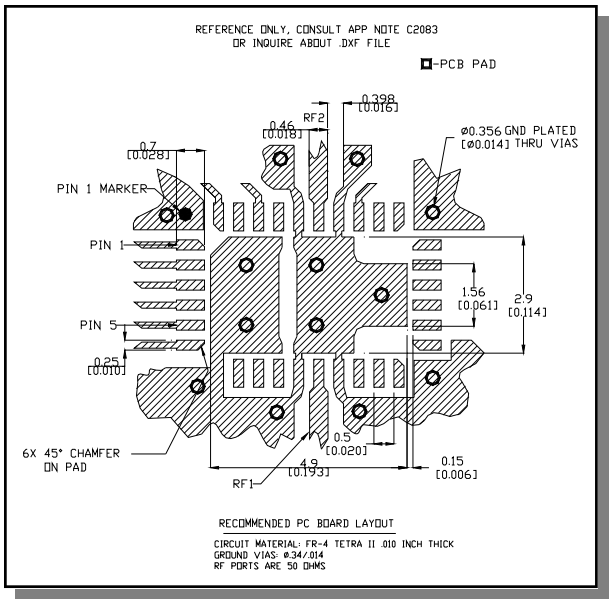
Absolute Maximum Ratings [4,5]

Parameter	Absolute Maximum
Max. Input Power	+27 dBm
V_{CC}	-0.5V ≤ V_{CC} ≤ +7.0V
V_{EE}	-8.5V ≤ V_{EE} ≤ +0.5V
V_{CC} - V_{EE}	-0.5V ≤ V_{CC} - V_{EE} ≤ 14.5V
Vin[6]	-0.5V ≤ Vin ≤ V_{CC} + 0.5V
Operating Temperature	-40ºC to +85ºC
Storage Temperature	-65ºC to +125ºC

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. M/A-COM does not recommend sustained operation near these survivability limits.
6. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Recommended PCB Configuration[7]



7. Application Note S2083 is available on line at www.macom.com

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Moisture Sensitivity

The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

Truth Table (Digital Attenuator)[8]

C2	C1	Attenuation
0	0	Loss, Reference
0	1	16.0 dB
1	1	32.0 dB

0 = TTL Low; 1 = TTL High

8. C1 is specified as the control for the 16 dB bit. We show data for the performance with the C2 control - note that the electrical performance of the 16 dB bit controlled by C2 is not specified.

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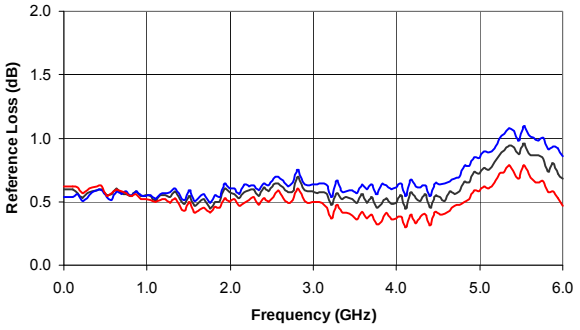
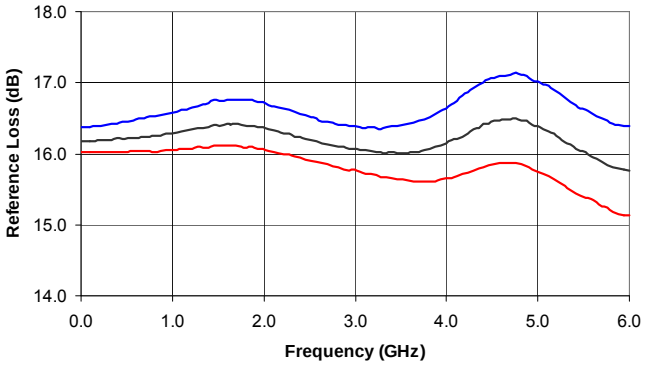
Typical Performance

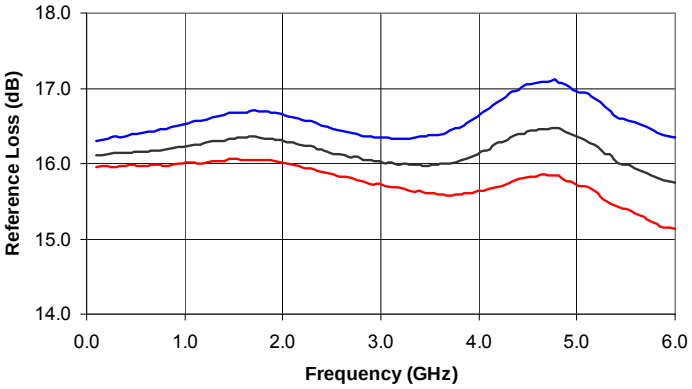
Reference Loss vs. Frequency



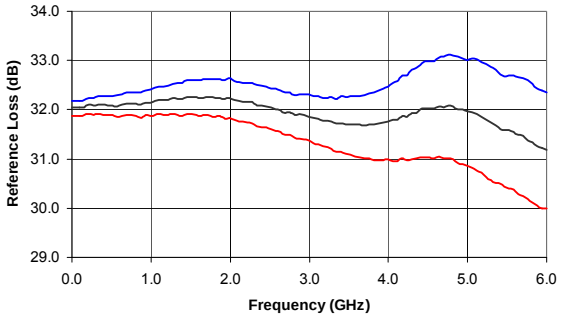
Attenuation - 16 dB bit (C1) Bit vs. Frequency



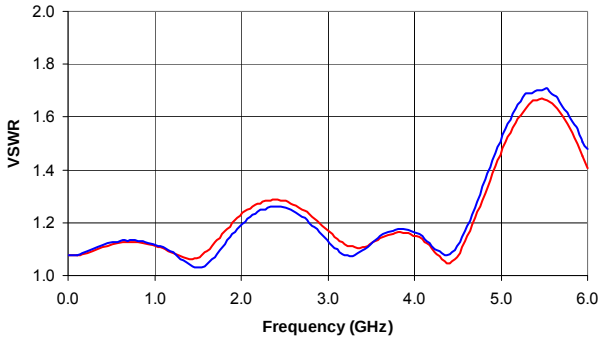
Attenuation - 16 dB Bit (C2) vs. Frequency



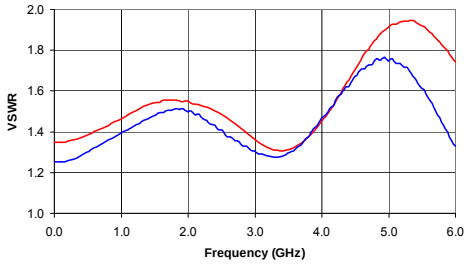
Attenuation - 32 dB Attenuation vs. Frequency



VSWR - Reference Loss State vs. Frequency



VSWR - 16 dB Bit (C1) vs. Frequency



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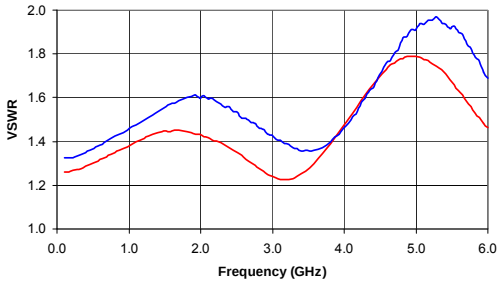
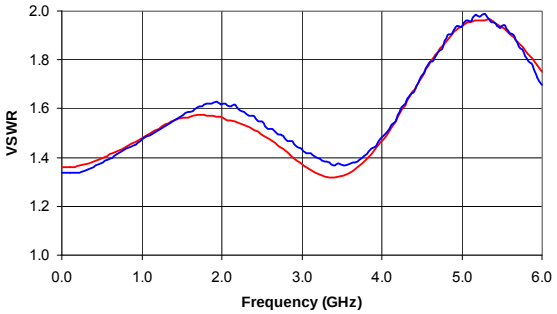
Typical Performance

VSWR - 16 dB Bit (C2) vs. Frequency



VSWR - 32 dB Attenuation vs. Frequency



Typical IP2 and IP3 at Room Temperature[9]

Attenuation	IP2			IP3			Units
	50 MHz	500 MHz	2 GHz	50 MHz	500 MHz	2 GHz	
Reference State	59	80	80	40	45	42	dBm
16 dB	48	60	60	33	35	33	dBm
32 dB	47	54	54	33	30	30	dBm

9. IP2 and IP3 are measured with two-tone inputs F1 and F2 up to +5 dBm with 1 MHz spacing.

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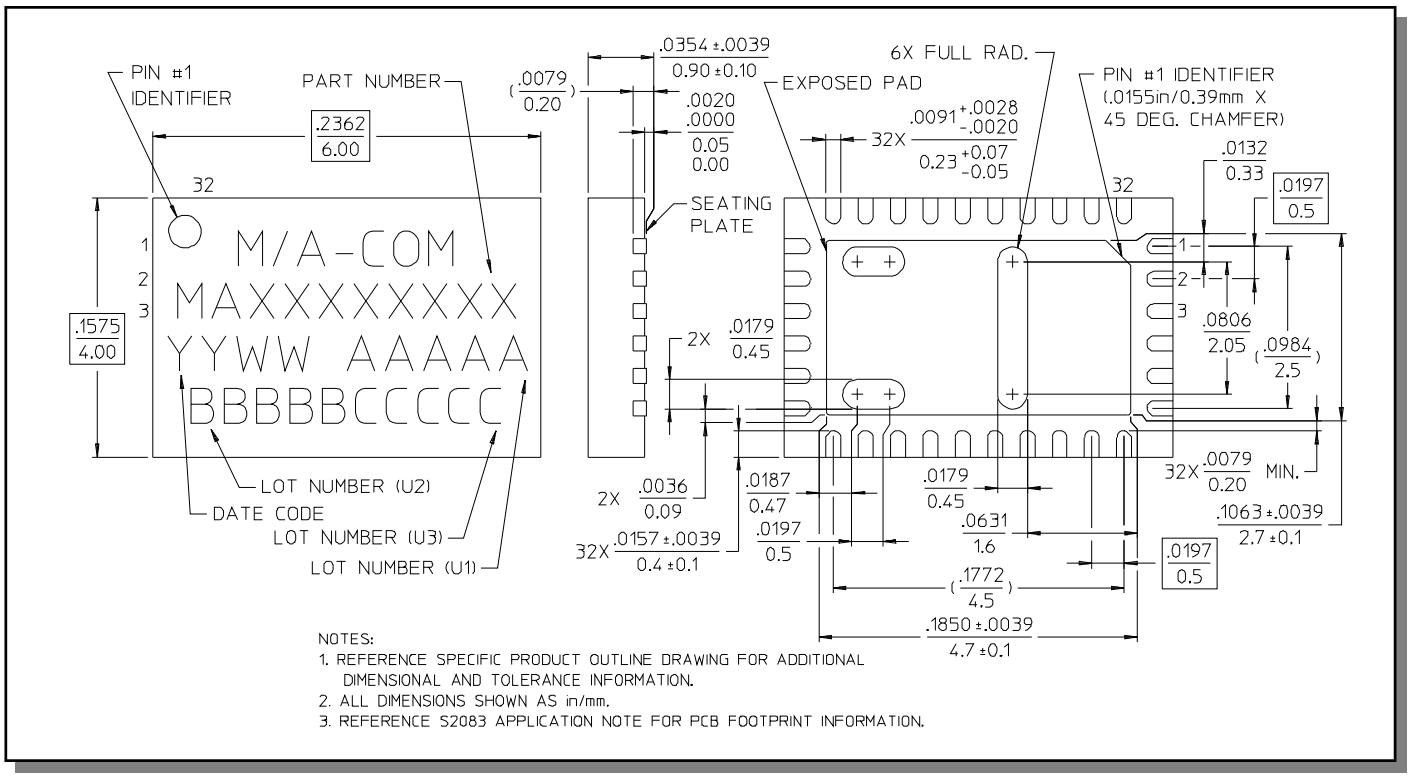
CSP-1, 4 x 6 mm, 32-lead PQFN†



† Reference Application Note M538 for lead-free solder reflow recommendations.

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