



128MB Direct Rambus DRAM SO-RIMM™ Module

EBR12EC8ABSA (64M words × 18 bits)

Description

The Direct Rambus SO-RIMM module is a generalpurpose high-performance memory module subsystem suitable for use in a broad range of applications including computer memory, mobile personal computers, networking systems and other applications where high bandwidth and low latency are required.

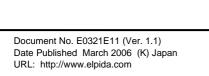
The EBR12EC8ABSA consists of 4 pieces of 288M Direct Rambus DRAM (Direct RDRAM) devices. These are extremely high-speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits 1066MHz or 800MHz transfer rates while using conventional system and board design technologies.

The architecture of the Direct RDRAM enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions.

The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAM's 32 banks support up to four simultaneous transactions per device.

Features

- 128MB Direct RDRAM storage and 128 banks total on module
- High speed 1066MHz/800MHz Direct RDRAM devices
- 160 edge connector pads with 0.65mm pad spacing
- Module PCB size: 67.60mm × 31.25mm × 1.00mm
- Gold plated edge connector pads contacts
- Serial Presence Detect (SPD) support
- Operates from a 2.5V supply
- Low power and power down self refresh modes
- Separate Row and Column buses for higher efficiency
- RDRAM®s uses Chip Scale Package (CSP)
 - FBGA package



Ordering Information

| Part number | Organization | I/O Freq. (MHz) | RAS access time (ns) | Package | Mounted devices |
|-----------------|--------------|--------------------|----------------------|--|-----------------|
| EBR12EC8ABSA-AD | 64M x 18 | 1066 | 35 | 160 edge connector pads SO-RIMM with heat spreader | EDR2518ABSE |
| EBR12EC8ABSA-8C | | 800 | 40 | Edge connector: Gold plated | |

Module Pad Names

| Pad | Signal Name | Pad | Signal Name |
|-----|-------------|-----|-------------|
| A1 | GND | B1 | GND |
| A2 | LDQA8 | B2 | LDQA7 |
| A3 | GND | B3 | GND |
| A4 | LDQA6 | B4 | LDQA5 |
| A5 | GND | B5 | GND |
| A6 | LDQA4 | B6 | LDQA3 |
| A7 | GND | B7 | GND |
| A8 | LDQA2 | B8 | LDQA1 |
| A9 | GND | B9 | GND |
| A10 | LDQA0 | B10 | LCFM |
| A11 | GND | B11 | GND |
| A12 | LCTM | B12 | LCFMN |
| A13 | GND | B13 | GND |
| A14 | LCTMN | B14 | LROW2 |
| A15 | GND | B15 | GND |
| A16 | LROW1 | B16 | LROW0 |
| A17 | GND | B17 | GND |
| A18 | LCOL4 | B18 | LCOL3 |
| A19 | GND | B19 | GND |
| A20 | LCOL2 | B20 | LCOL1 |
| A21 | GND | B21 | GND |
| A22 | LCOL0 | B22 | LDQB1 |
| A23 | GND | B23 | GND |
| A24 | LDQB0 | B24 | LDQB3 |
| A25 | GND | B25 | GND |
| A26 | LDQB2 | B26 | LDQB5 |
| A27 | GND | B27 | GND |
| A28 | LDQB4 | B28 | LDQB7 |
| A29 | GND | B29 | GND |
| A30 | LDQB6 | B30 | LDQB8 |
| A31 | GND | B31 | GND |
| A32 | LSCK | B32 | LCMD |
| A33 | GND | B33 | GND |
| A34 | SOUT | B34 | SIN |
| A35 | VDD | B35 | VDD |
| A36 | NC | B36 | NC |
| | | | |

| A41 NC B41 NC A42 VREF B42 VREF A43 SCL B43 SA0 A44 VDD B44 VDD A45 SDA B45 SA1 A46 VDD B46 VDD A47 SVDD B47 SWP A48 GND B48 GND A49 RSCK B49 RCMD A50 GND B50 GND A50 GND B50 GND A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A67 RDQB3 B57 RDQB0 A58 GND B58 GND A69 RDQB1 B59 | Pad | Signal Name | Pad | Signal Name |
|--|-----|-------------|-----|-------------|
| A43 SCL B43 SA0 A44 VDD B44 VDD A45 SDA B45 SA1 A46 VDD B46 VDD A47 SVDD B47 SWP A48 GND B48 GND A49 RSCK B49 RCMD A50 GND B50 GND A50 GND B50 GND A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B68 GND A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B | A41 | NC | B41 | NC |
| A44 VDD B44 VDD A45 SDA B45 SA1 A46 VDD B46 VDD A47 SVDD B47 SWP A48 GND B48 GND A49 RSCK B49 RCMD A50 GND B50 GND A50 GND B50 GND A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A69 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND < | A42 | VREF | B42 | VREF |
| A45 SDA B45 SA1 A46 VDD B46 VDD A47 SVDD B47 SWP A48 GND B48 GND A49 RSCK B49 RCMD A50 GND B50 GND A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW1 | A43 | SCL | B43 | SA0 |
| A46 VDD B46 VDD A47 SVDD B47 SWP A48 GND B48 GND A49 RSCK B49 RCMD A50 GND B50 GND A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 | A44 | VDD | B44 | VDD |
| A47 SVDD B47 SWP A48 GND B48 GND A49 RSCK B49 RCMD A50 GND B50 GND A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND | A45 | SDA | B45 | SA1 |
| A48 GND B48 GND A49 RSCK B49 RCMD A50 GND B50 GND A51 RDQB8 B51 RDQB6 A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND <td>A46</td> <td>VDD</td> <td>B46</td> <td>VDD</td> | A46 | VDD | B46 | VDD |
| A49 RSCK B49 RCMD A50 GND B50 GND A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A69 RCFMN </td <td>A47</td> <td>SVDD</td> <td>B47</td> <td>SWP</td> | A47 | SVDD | B47 | SWP |
| A50 GND B50 GND A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A69 RCFMN B69 RCTM A70 GND <td>A48</td> <td>GND</td> <td>B48</td> <td>GND</td> | A48 | GND | B48 | GND |
| A51 RDQB8 B51 RDQB6 A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM </td <td>A49</td> <td>RSCK</td> <td>B49</td> <td>RCMD</td> | A49 | RSCK | B49 | RCMD |
| A52 GND B52 GND A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM | A50 | GND | B50 | GND |
| A53 RDQB7 B53 RDQB4 A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 </td <td>A51</td> <td>RDQB8</td> <td>B51</td> <td>RDQB6</td> | A51 | RDQB8 | B51 | RDQB6 |
| A54 GND B54 GND A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 | A52 | GND | B52 | GND |
| A55 RDQB5 B55 RDQB2 A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND <td>A53</td> <td>RDQB7</td> <td>B53</td> <td>RDQB4</td> | A53 | RDQB7 | B53 | RDQB4 |
| A56 GND B56 GND A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 | A54 | GND | B54 | GND |
| A57 RDQB3 B57 RDQB0 A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A55 | RDQB5 | B55 | RDQB2 |
| A58 GND B58 GND A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A56 | GND | B56 | GND |
| A59 RDQB1 B59 RCOL0 A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A57 | RDQB3 | B57 | RDQB0 |
| A60 GND B60 GND A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A58 | GND | B58 | GND |
| A61 RCOL1 B61 RCOL2 A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A59 | RDQB1 | B59 | RCOL0 |
| A62 GND B62 GND A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A60 | GND | B60 | GND |
| A63 RCOL3 B63 RCOL4 A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A61 | RCOL1 | B61 | RCOL2 |
| A64 GND B64 GND A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A62 | GND | B62 | GND |
| A65 RROW0 B65 RROW1 A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A63 | RCOL3 | B63 | RCOL4 |
| A66 GND B66 GND A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A64 | GND | B64 | GND |
| A67 RROW2 B67 RCTMN A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A65 | RROW0 | B65 | RROW1 |
| A68 GND B68 GND A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A66 | GND | B66 | GND |
| A69 RCFMN B69 RCTM A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A67 | RROW2 | B67 | RCTMN |
| A70 GND B70 GND A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A68 | GND | B68 | GND |
| A71 RCFM B71 RDQA0 A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A69 | RCFMN | B69 | RCTM |
| A72 GND B72 GND A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A70 | GND | B70 | GND |
| A73 RDQA1 B73 RDQA2 A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A71 | RCFM | B71 | RDQA0 |
| A74 GND B74 GND A75 RDQA3 B75 RDQA4 | A72 | GND | B72 | GND |
| A75 RDQA3 B75 RDQA4 | A73 | RDQA1 | B73 | RDQA2 |
| - | A74 | GND | B74 | GND |
| A76 GND B76 GND | A75 | RDQA3 | B75 | RDQA4 |
| | A76 | GND | B76 | GND |



| Pad | Signal Name |
|-----|-------------|-----|-------------|-----|-------------|-----|-------------|
| A37 | GND | B37 | GND | A77 | RDQA5 | B77 | RDQA6 |
| A38 | NC | B38 | NC | A78 | GND | B78 | GND |
| A39 | VCMOS | B39 | VCMOS | A79 | RDQA7 | B79 | RDQA8 |
| A40 | NC | B40 | NC | A80 | GND | B80 | GND |

Module Connector Pad Description

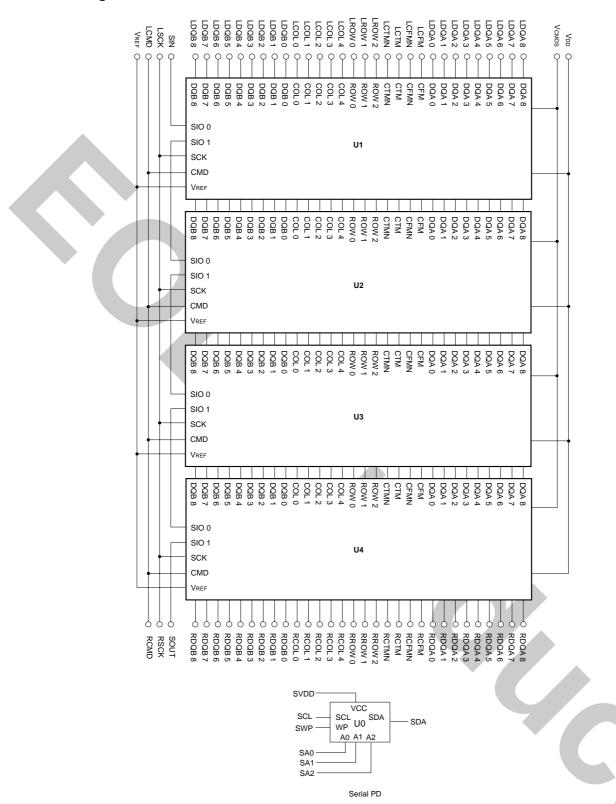
| | Module | | | |
|------------|--|--------|-------|--|
| Signal | Connector Pads | I/O | Type | Description |
| GND | A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29,A31, A33, A37, A48, A50, A52, A54,A56, A58, A60, A62, A64, A66, A68,A70, A72, A74, A76, A78, A80, B1,B3, B5, B7, B9, B11, B13, B15, B17,B19, B21, B23, B25, B27, B29, B31,B33, B37, B48, B50, B52, B54, B56, B58, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80 | - - | - | Ground reference for RDRAM core and interface. |
| LCFM | B10 | I | RSL | Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity. |
| LCFMN | B12 | 1 | RSL | Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity. |
| LCMD | B32 | 1 | VCMOS | Serial Command used to read from and write to the control registers. Also used for power management. |
| LCOL4LCOL0 | A18, B18, A20, B20, A22 | 21 | RSL | Column bus. 5-bit bus containing control and address information for column accesses. |
| LCTM | A12 | I | RSL | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity. |
| LCTMN | A14 | 1 | RSL | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity. |
| LDQA8LDQA0 | A2, B2, A4, B4, A6, B6, A8, B8, A10 | I/O | RSL | Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM |
| LDQB8LDQB0 | B30, B28, A30, B26, A28, B24, A26, B22, A24 | I/O | RSL | Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. |
| LROW2LROW0 | B14, A16, B16 | I | RSL | Row bus. 3-bit bus containing control and address information for row accesses. |
| LSCK | A32 | I | VCMOS | Serial clock input. Clock source used to read from and write to the RDRAM control registers. |
| NC | A36, B36, A38, B38, A40, B40, A41, B41 | - | - | These pads are not connected. These 8 connector pads are reserved for future use. |
| RCFM | A71 | I | RSL | Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity. |
| RCFMN | A69 | I | RSL | Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity. |
| RCMD | B49 | I | VCMOS | Serial Command Input used to read from and write to the control registers. Also used for power management. |
| RCOL4RCOL0 | B63, A63, B61, A61, B59 |) [| RSL | Column bus. 5-bit bus containing control and address information for column accesses. |
| RCTM | B69 | I | RSL | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity. |
| RCTMN | B67 | I | RSL | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity. |



| Signal | Module Connector Pads | I/O | Type | Description |
|------------|--|-----|-------|--|
| Signal | | 1/0 | туре | · |
| RDQA8RDQA0 | B79, A79, B77, A77, B75, A75, B73, A73, B71 | I/O | RSL | Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. |
| RDQB8RDQB0 | A51, A53, B51, A55, B53, A57, B55, A59, B57 | I/O | RSL | Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. |
| RROW2RROW0 | A67, B65, A65 | I | RSL | Row bus. 3-bit bus containing control and address information for row accesses. |
| RSCK | A49 | I | VCMOS | Serial clock input. Clock source used to read from and write to the RDRAM control registers. |
| SA0 | B43 | 1 | SVDD | Serial Presence Detect Address 0. |
| SA1 | A43 | 1 | SVDD | Serial Presence Detect Address 1. |
| SCL | B45 | 1 | SVDD | Serial Presence Detect Clock. |
| SDA | A45 | I/O | SVDD | Serial Presence Detect Data (Open Collector I/O). |
| SIN | B34 | I/O | VCMOS | Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module. |
| SOUT | A34 | I/O | VCMOS | Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module. |
| SVDD | A47 | _ | _ | SPD Voltage. Used for signals SCL, SDA, SWP, SA0, SA1 and SA2. |
| SWP | B47 | I | SVDD | Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read. |
| VCMOS | A39, B39 | | _ | CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT. |
| VDD | A35, B35, A44, B44, A46, B46 | | _ | Supply voltage for the RDRAM core and interface logic. |
| VREF | A42, B42 | - / | - | Logic threshold reference voltage for RSL signals. |



Block Diagram



Note: 1. Rambus Channel signals form a loop through the SO-RIMM module, with the exception of the SIO chain.

2. See Serial Presence Detection Specification for information on the SPD device and its contents.

Electrical Specifications

Absolute Maximum Ratings

| Symbol | Parameter | min. | max. | Unit |
|---------|---|------|-----------|------|
| VI,ABS | Voltage applied to any RSL or CMOS signal pad with respect to GND | -0.3 | VDD + 0.3 | V |
| VDD,ABS | Voltage on VDD with respect to GND | -0.5 | VDD + 1.0 | V |
| TSTORE | Storage temperature | -50 | +100 | °C |

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Recommended Electrical Conditions

| Symbol | Parameter and conditions | min. | max. | Unit |
|--------|---|-------------|-------------|------|
| VDD | Supply voltage*1 | 2.50 - 0.13 | 2.50 + 0.13 | V |
| VCMOS | CMOS I/O power supply at pad 2.5V controllers | 2.50 – 0.13 | 2.50 + 0.25 | V |
| | 1.8V controllers | 1.8 – 0.1 | 1.8 + 0.2 | V |
| VREF | Reference voltage*1 | 1.4 – 0.2 | 1.4 + 0.2 | V |
| VSPD | Serial Presence Detector- positive supply | e power 2.2 | 3.6 | V |

Note: 1. See Direct RDRAM datasheet for more details.



AC Electrical Specifications

| Symbol | Parameter and Conditions | Grade | min. | typ. | max. | Unit |
|---------------|---|------------|------|------|------|------|
| Z | Module Impedance of RSL signals | | 25.2 | 28.0 | 30.8 | Ω |
| | Module Impedance of SCK and CMD signals | | 23.8 | 28.0 | 32.2 | Ω |
| TPD | Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN,CFM, and CFMN) | | _ | _ | TBD | ns |
| ΔΤΡΟ | Propagation delay variation of RSL signals with respect to TPD $^{\star 1,2}$ | | TBD | _ | TBD | ps |
| ΔTPD-CMOS | Propagation delay variation of SCK signal with respect to an average clock delay *1 | | TBD | _ | TBD | ps |
| ΔTPD- SCK,CMD | Propagation delay variation of CMD signal with respect to SCK signal | | TBD | _ | TBD | ps |
| Vα/VIN | Attenuation Limit | -AD -8C | _ | _ | TBD | % |
| VXF/VIN | Forward crosstalk coefficient (300ps input rise time 20% - 80%) | -AD -8C | _ | _ | TBD | % |
| VXB/VIN | Backward crosstalk coefficient (300ps input rise time 20% - 80%) | -AD -8C | _ | _ | TBD | % |
| RDC | DC Resistance Limit | -AD -8C | _ | _ | TBD | Ω |

- Notes 1. TPD or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).
 - 2. If the SO-RIMM module meets the following specification, then it is compliant to the specification. If the SO-RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted Δ TPD Specification" table.

Adjusted ATPD Specification

| | | | Absolute | ! | |
|--------|--|------------------------------------|----------|------|------|
| Symbol | Parameter and conditions | Adjusted min./max. | min. | max. | Unit |
| ΔTPD | Propagation delay variation of RSL signals with respect to TPD | +/- [17+(18*N*ΔZ0)] * ¹ | TBD | TBD | ps |

Note: 1 N = Number of RDRAM devices installed on the SO-RIMM module.

 Δ Z0 = delta Z0% = (max. Z0 - min. Z0) / (min. Z0)

(max. Z0 and min. Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the module.)



SO-RIMM Module Current Profile

| IDD | SO-RIMM module power conditions *1 | Grade | max. | Unit |
|------|--|------------|------|------|
| IDD1 | One RDRAM device in Read *2, balance in NAP mode | -AD -8C | TBD | mA |
| IDD2 | One RDRAM device in Read *2, balance in Standby mode | -AD -8C | TBD | mA |
| IDD3 | One RDRAM device in Read *2, balance in Active mode | -AD -8C | TBD | mA |
| IDD4 | One RDRAM device in Write, balance in NAP mode | -AD -8C | TBD | mA |
| IDD5 | One RDRAM device in Write, balance in Standby mode | -AD -8C | TBD | mA |
| IDD6 | One RDRAM device in Write, balance in Active mode | -AD -8C | TBD | mA |

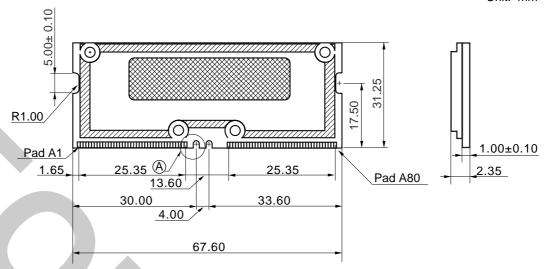
Notes: 1. Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Power does not include Refresh Current.

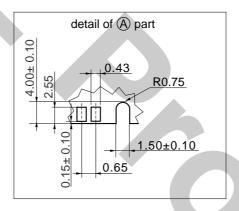
2. I/O current is a function of the % of 1's, to add I/O power for 50 % 1's for a x18 need to add 276mA for the following: VDD = 2.5V, VTERM = 1.8V, VREF = 1.4V and VDIL = VREF – 0.5V.



Physical Outline

Unit: mm





Note: The dimensions without tolerance specification use the default tolerance of \pm 0.13.

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CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.

Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES -

1 PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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