PHASE LOCKED LOOP

564

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The NE564 is a versatile, high frequency phase locked loop which requires a single 5V supply for operation and has TTL compatible inputs and outputs. As shown in the block diagram, it consists of a VCO, a limiter to improve AM rejection and a phase comparator. There is also facility for external control of the loop gain. To obtain a demodulated signal which is TTL compatible, a post detection processor is also provided. This consists of a d-c retriever and a schmitt trigger with variable hysterisis which reduce the effects of d-c variations and carrier feedthrough on the output digital signal.

FEATURES

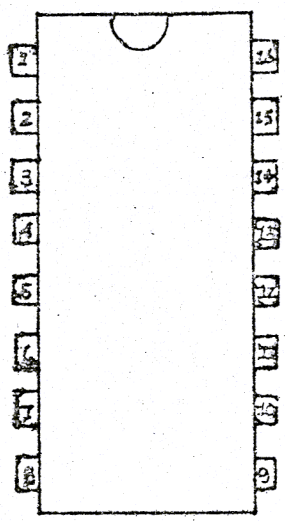
- Operation with single 5V supply
- TTL compatible inputs and outputs
- Operation to 50 MHz
- Operates as a modulator
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications

ABSOLUTE MAXIMUM RATINGS

Voltage at pin 1	14V
Voltage at pin 10	6V
Power dissipation	400mW
Operating temperature	0°C to 70°C
Storage temperature	-65°C to 150°C

PIN CONFIGURATION (Top View)

N* Package



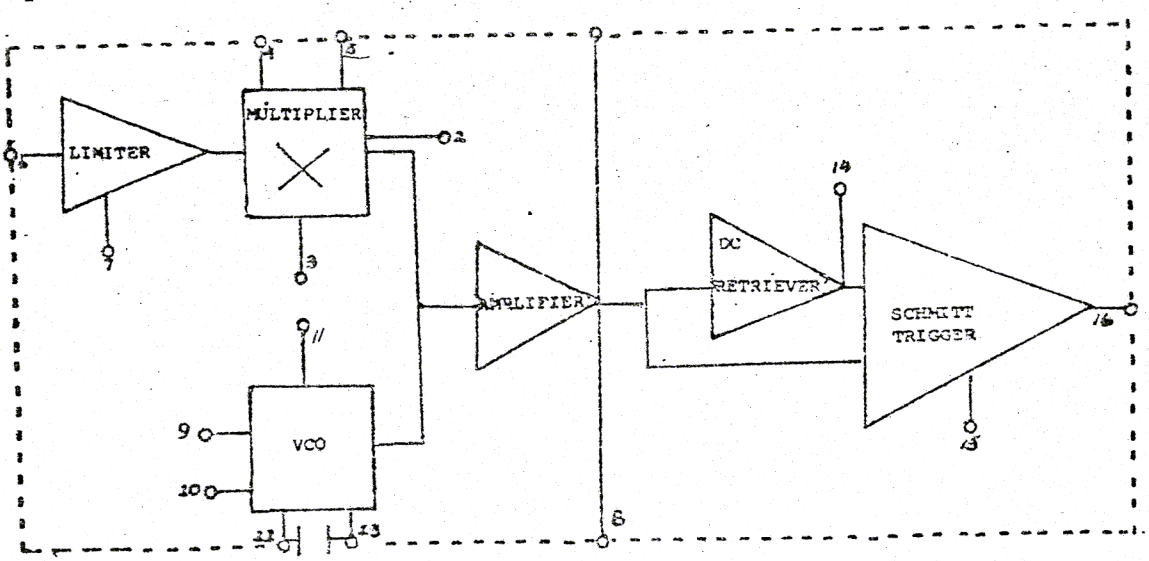
1) V+
2) Loop Gain Control
3) Input to Phase Comparator from VCO
4) Loop Filter
5) Loop Filter
6) FM/RF Input
7) Bias Filter
8) Ground
9) VCO output TTL
10) V+
11) VCO output #2
12) Freq. Set Cap.
13) Freq. Set Cap.
14) Analog output
15) Hysterisis Set
16) TTL Output

APPLICATIONS

High speed modems
FSK receivers and transmitters
Frequency Synthesizers
Signal generators

*Present ordering information should be for a BA pkg.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS $V^+ = 5V$, $T_A = 25°C$ (unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Lock Range	T_A=25°C I_2 = 400uA	25	40		%
Frequency of Operation of VCO	Fig. 1	45	50		MHZ
Frequency drift with temperature	T_A=0°C to 70°C fo= 5 MHZ		400	850	ppm/°C
Frequency change with supply voltage	V^+= 4.5V to V^+=5.5V		3	6	%/V
Demodulated output voltage (ms)	% input deviation 10% input deviation fo=5 MHZ	14 140	17 170		mV mV
Output Voltage linearity			3		%
Signal to noise ratio			40		dB
AM rejection			35		dB
Supply current	5V		30	40	mA
Leakage Current	Pin 9 Pin 16		1 1	10 10	uA uA
Output Current	Pin 9 Pin 16	6 6	10 10		mA mA
Supply Voltage	Pin 1 Pin 10	4.5 4.5		12 5.5	V V

SYSTEM DESCRIPTION

This is a brief system description of a monolithic phase locked loop with a post detection processor. A single 5V supply is sufficient for operation and the circuit has TTL compatible inputs and outputs. The use of Schottky clamped transistors and optimized geometries for devices extends the frequency of operation up to 50 MHz. The circuit can also be used as a modulator with a controllable frequency deviation.

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a d-c retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysterisis so that phase jitter in the output signal can be eliminated.

A block diagram of the system appears in Fig. 1. The PLL consists of a VCO and a multiplier which is used as a phase comparator. A limiter a lifier is used ahead of the phase comparator to limit the signal and thus improve AM rejection. The output voltage of the PLL can be written as

$$v_o = \frac{(f_{in} - f_o)}{K_{vco}} \qquad (1)$$

where

K_{vco} = Conversion gain of the VCO

f_{in} = Frequency of the input signal

f_o = Free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into digital, logic compatible signals. For high data rates, a c siderable amount of carrier will be present at the output due to the wideband nature of the loop filter. To recover the signal buried in this noise without the use of complicated filters, a comparator with hysterisis or Schmitt Trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Eq. (1) varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysterisis of the Schmitt Trigger should be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysterisis of the Schmitt Trigger.

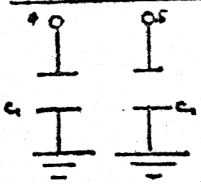
For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Eq. (1) it will lead to a change in the d-c levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be

Design Formula

Free Running freq. of VCO $f_o = \frac{1}{16RC}$ in Hz

where R = 100 Ω and C - External cap in farads.

Loop Filter



$$F(s) = \frac{1}{1 + sRC_1}$$ where $R = R_{12} = R_{13} = 1.3k\,\Omega$

Applications

FM Demodulator

The 564 can be used as a FM demodulator, the connections for operation at 5V and 12V being shown in Figs. A and B. The input signal is a-c coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal, the frequency deviation in the input signal should be fairly high (1% or higher).

FM Demodulator with TTL Compatible Output Signal

An FM demodulator with the output signal being a TTL signal can be obtained from the 564 by correcting it as shown in Fig. C. This operation requires the use of the d-c retriever, the capacitance for which is connected at pin 14. The hysterisis of the Schmitt Trigger can be adjusted by connecting a potentiometer at pin 15. The output signal appears at pin 16, which requires an external resistor. If necessary, the duty cycle of the output signal can be adjusted by applying a voltage at pin 14 (around 2.5V) and varying it. The connection for a similar application appears in Fig. D.

Gated PLL Demodulator

The lock range adjust pin of the 564 can be used to gate the PLL when it is operating in the demodulator mode. The circuit is connected as shown in Fig. E. The gating voltage which can be a TTL signal is applied to pin 2. When this voltage is high, the loop is in lock and the demodulated output signal appears at Pin 16. When the input to pin 2 is low, the loop is out of lock and the VCO will be at its center frequency. It is also possible to use pin 2 to adjust the loop gain so that a large capture range and small lock range can be obtained.

eliminated if the D-c or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the d-c levels of the PLL output do not affect the FSK output.

The VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, whose equivalent circuit appears in Fig. 3, transistors Q_{21} and Q_{23} with current sources Q_{25} - Q_{26} form the basic oscillator. The free running frequency of the oscillator is

$$f_o = \frac{1}{16R_cC} \qquad (2)$$

$R_c = R_{19} = R_{20}$

C_1 = Frequency setting External Capacitor

Variation of V_d changes the frequency of the oscillator. As indicated by Eq. (2), the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNP's are used to obtain TTL level inputs. The loop gain can be varied changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

The Post Detection Processor Section

As shown in Fig. 2, the d-c retriever is formed by the transconductance amplifier Q_{42} - Q_{43} with a capacitor at the output (Pin 14). This forms an integrator whose output voltage is

$$V_0 = \frac{g_m}{C_2} \int V_{in}\, dt \qquad (3)$$

g_m = transconductance of the amplifier

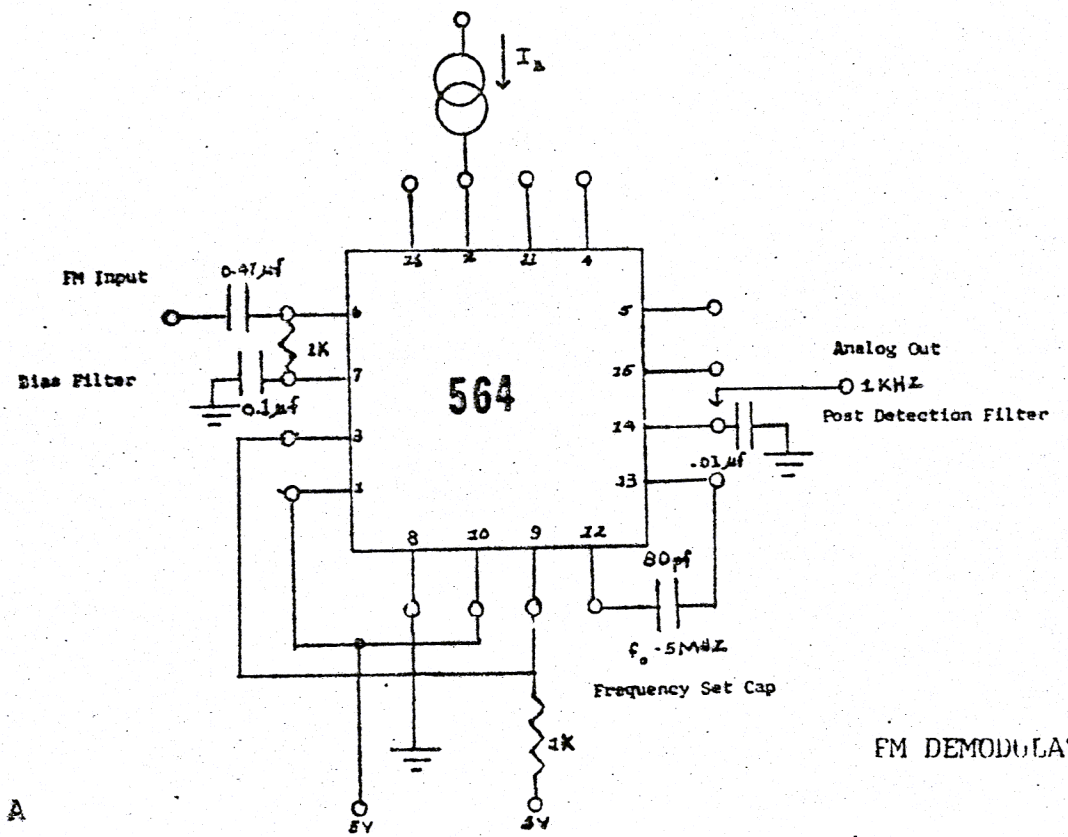
C_2 = capacitor at the output (pin 14)

V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied, so that the output voltage is the d-c or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysterisis is made up of Q_{49} - Q_{50} with positive feedback being provided by Q_{47} - Q_{48}. The hysterisis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysterisis control, which is a d-c control, provides a symmetric variation around the nominal value.

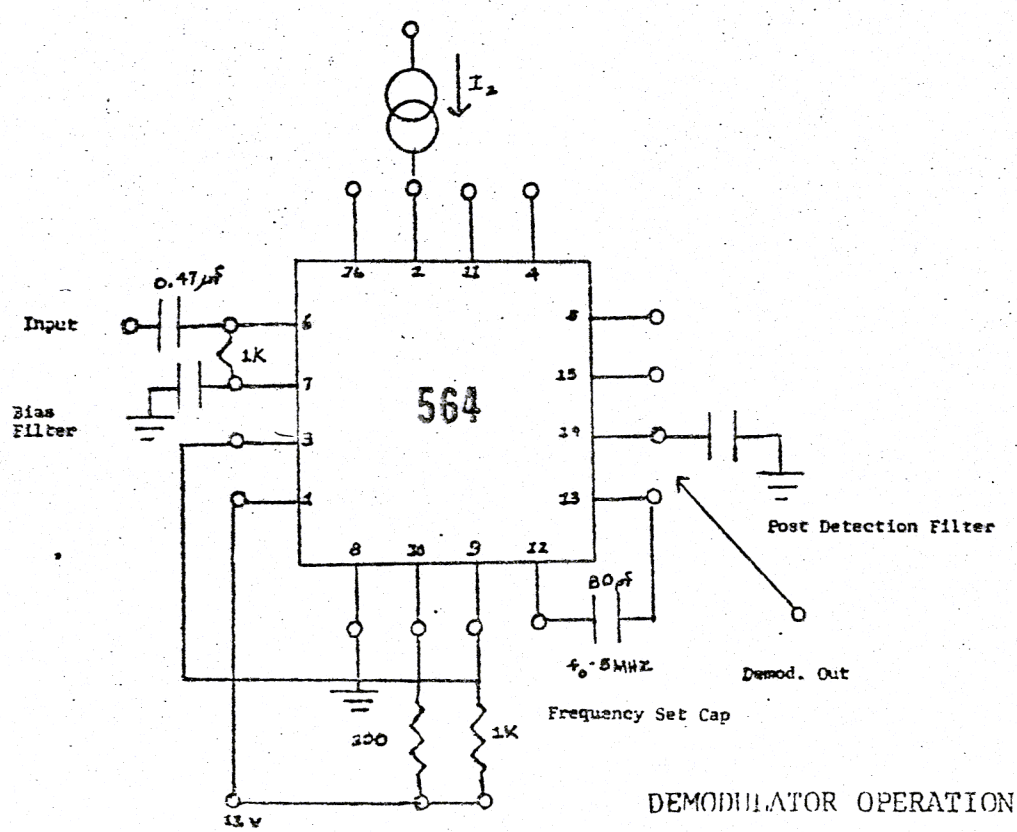
Lock Range Adjustment



FM DEMODULATOR

Fig. A

Lock Range Adjustment



DEMODULATOR OPERATION AT 12V

Fig. B

LOCK RANGE ADJUSTMENT

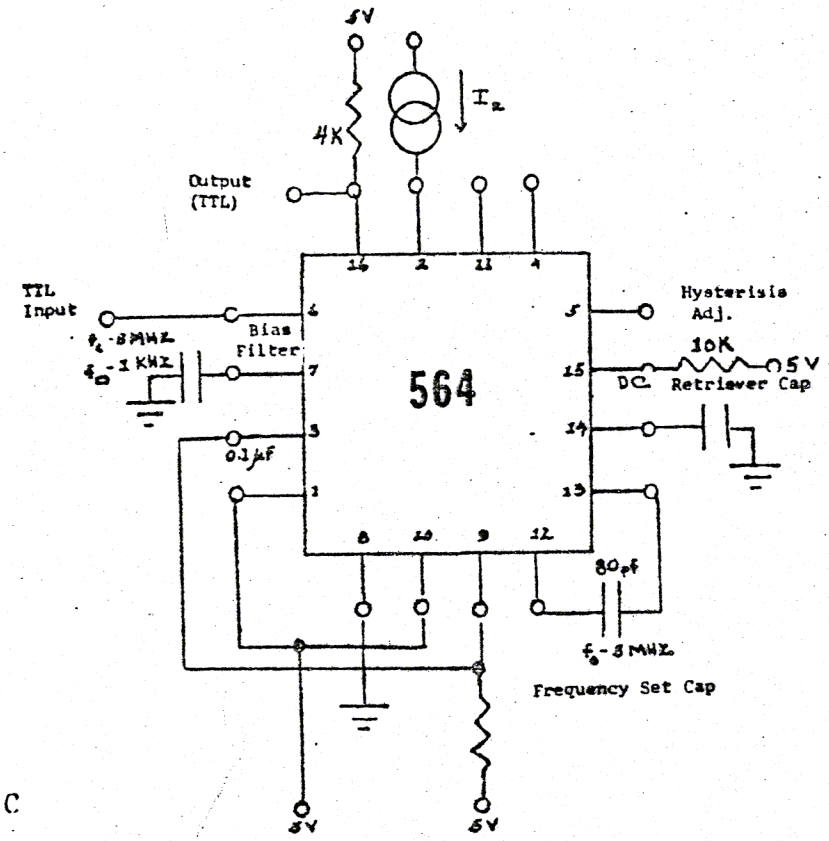


Fig. C

FM DEMODULATOR WITH TTL COMPATIBLE DEMODULATED OUTPUT SIGNAL

LOCK RANGE ADJUSTMENT

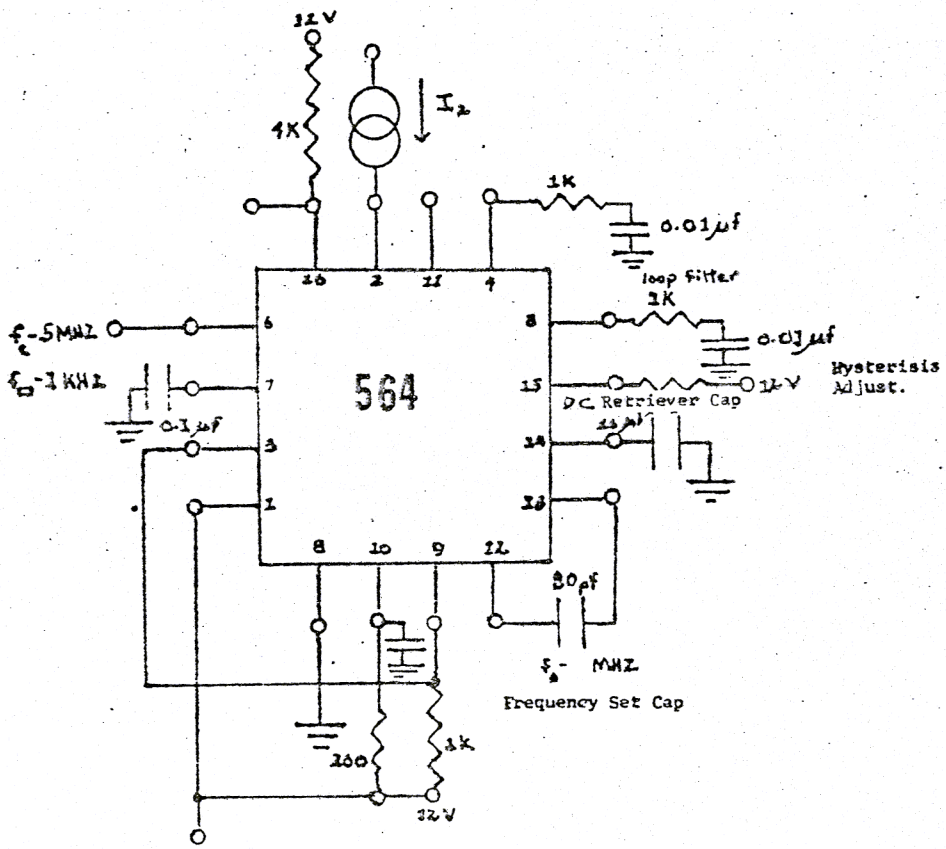
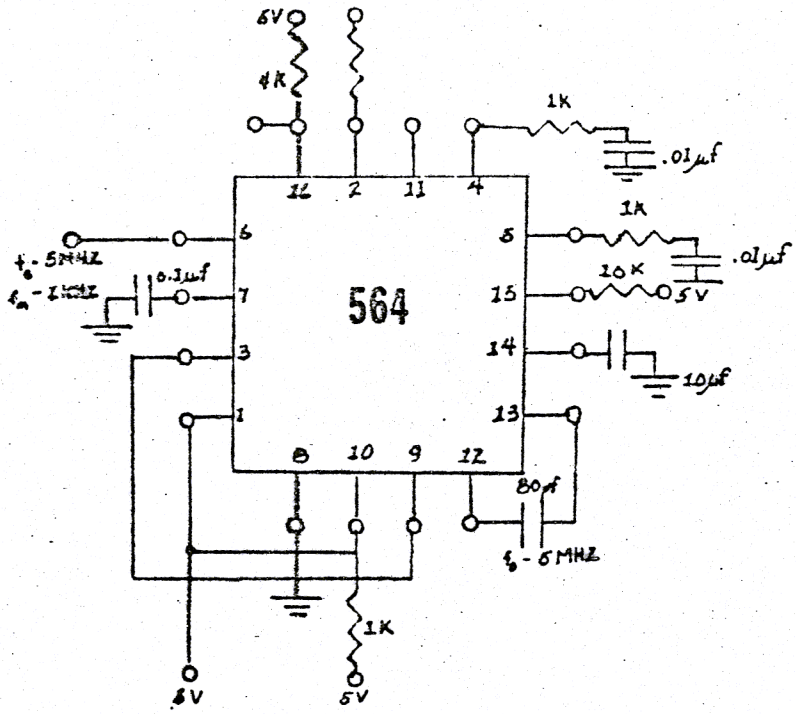


Fig. D

12V Demodulator With Digital Output

Loop Gating Voltage (see note below)



Note: When the input to pin 2 is high (TTL level), the loop is in lock and the demodulated output at pin 16 is present. When the input to pin 2 is low (TTL level) the loop is out of lock with the VCO at its center frequency.

Fig. E GATED PLL DEMODULATOR

LOCK RANGE ADJUSTMENT

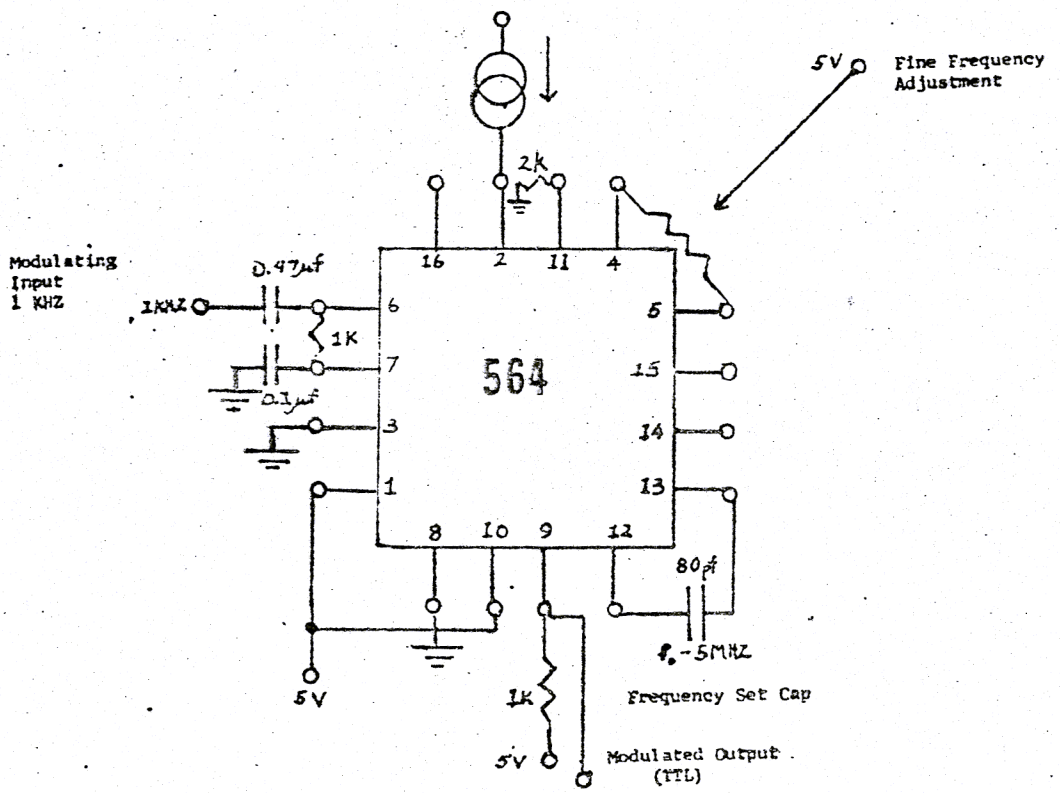
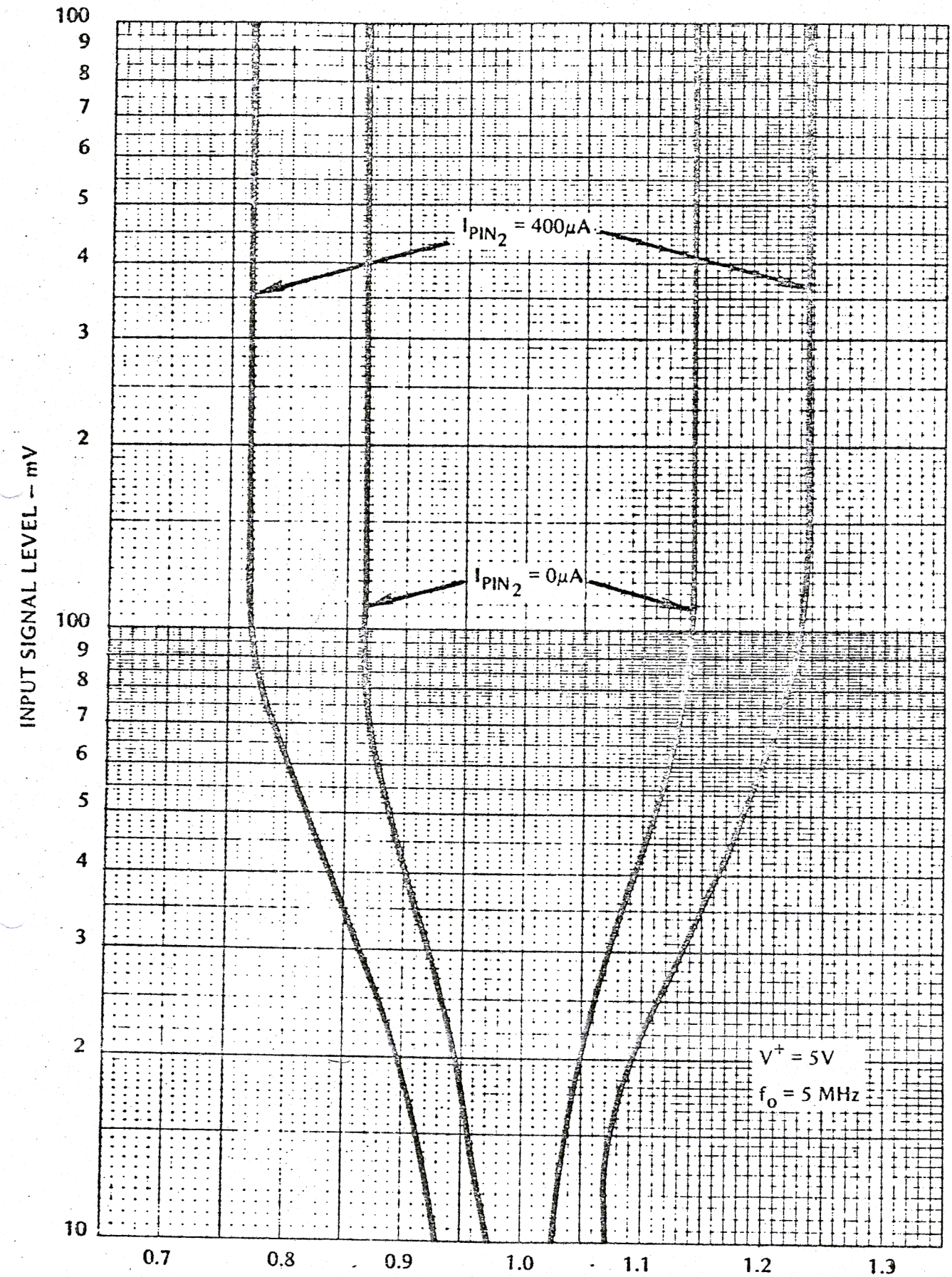
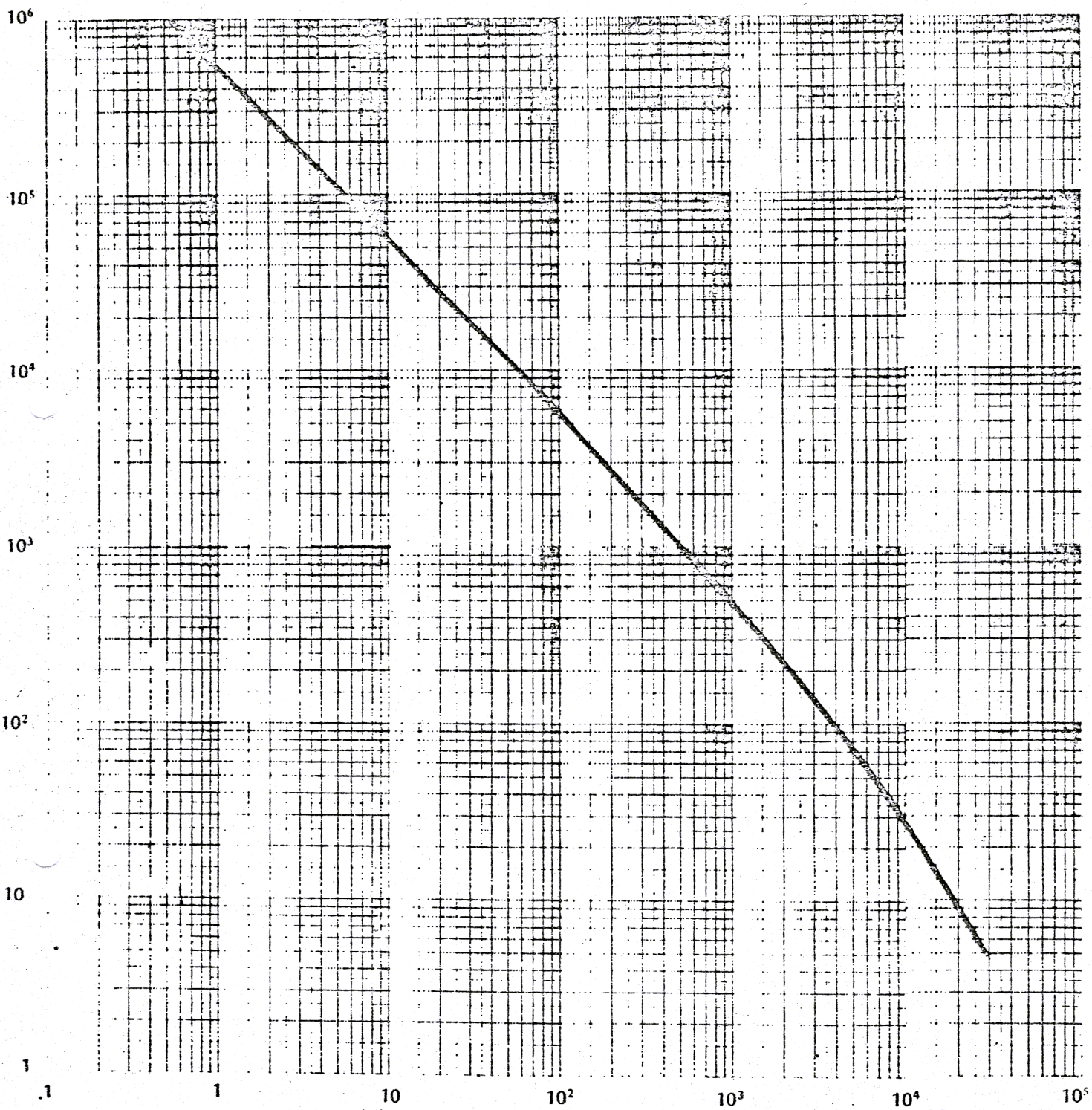


Fig. F Modulator

LOCK RANGE VS. SIGNAL INPUT



VCO CAPACITOR VS. FREQUENCY

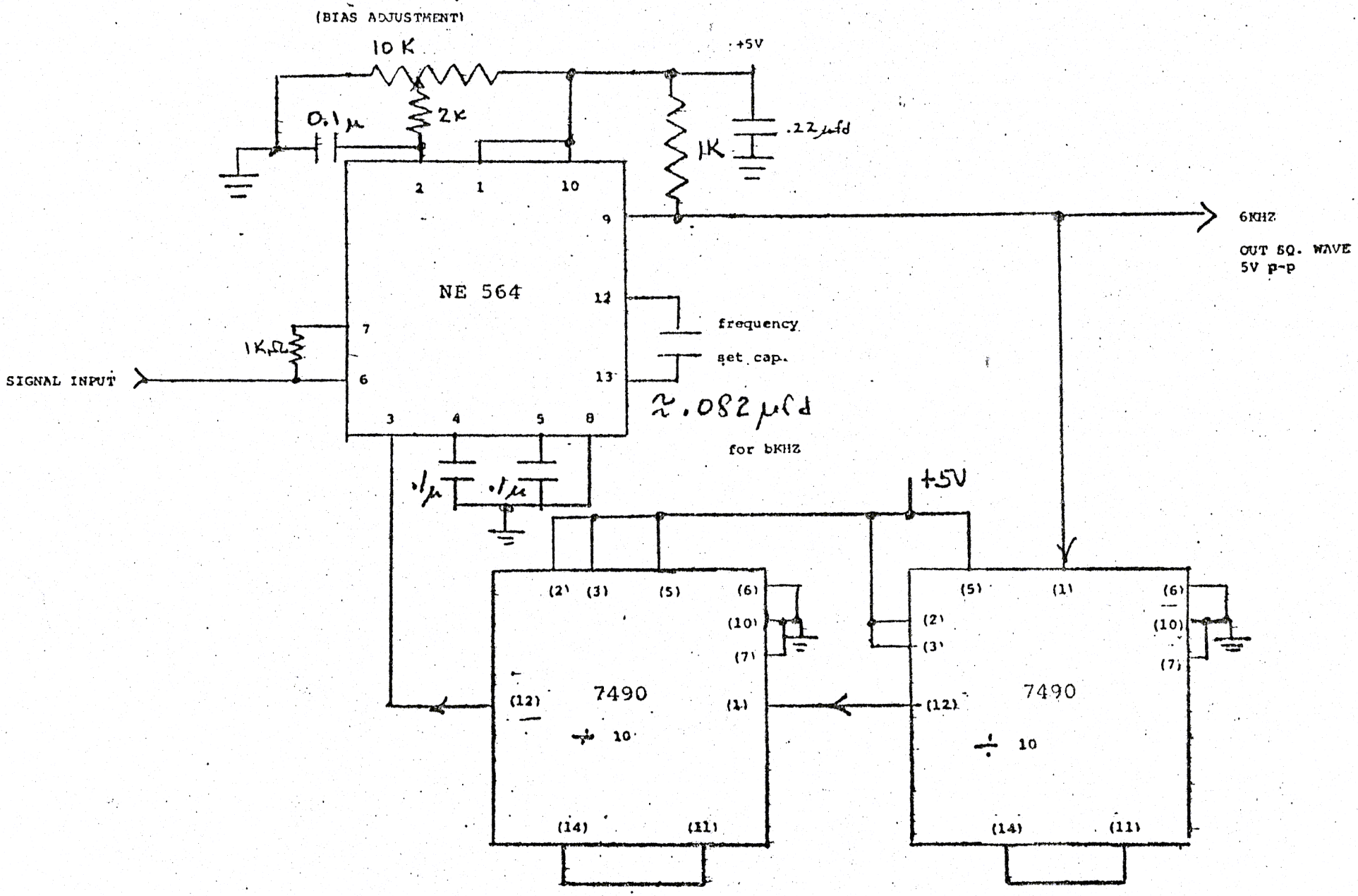


FREQUENCY SYNTHESIS

Frequency Multiplication can be achieved with the NE564 with the insertion of a counter (digital frequency divider) in the loop.

A block diagram is shown in Figure 8-9. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input frequency so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property, is the use of the 564 in wide range frequency synthesizers.

In frequency multiplication applications, it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency component is dc and is the error voltage which drives the VCO to keep the 564 in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more underdamped loop transient response.


(BIAS ADJUSTMENT)
10 K
+5V
0.1 μ
2K
1K
.22 μfd
2
1
10
9
NE 564
12
7
1KΩ
frequency
set cap.
SIGNAL INPUT
6
13
≈.082 μfd
for 6KHZ
3
4
5
8
.1μ
.1μ
6KHZ
OUT SQ. WAVE
5V p-p
+5V
(2)
(3)
(5)
(6)
(10)
(7)
(12)
7490
(1)
÷ 10
(14)
(11)
(5)
(1)
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7490
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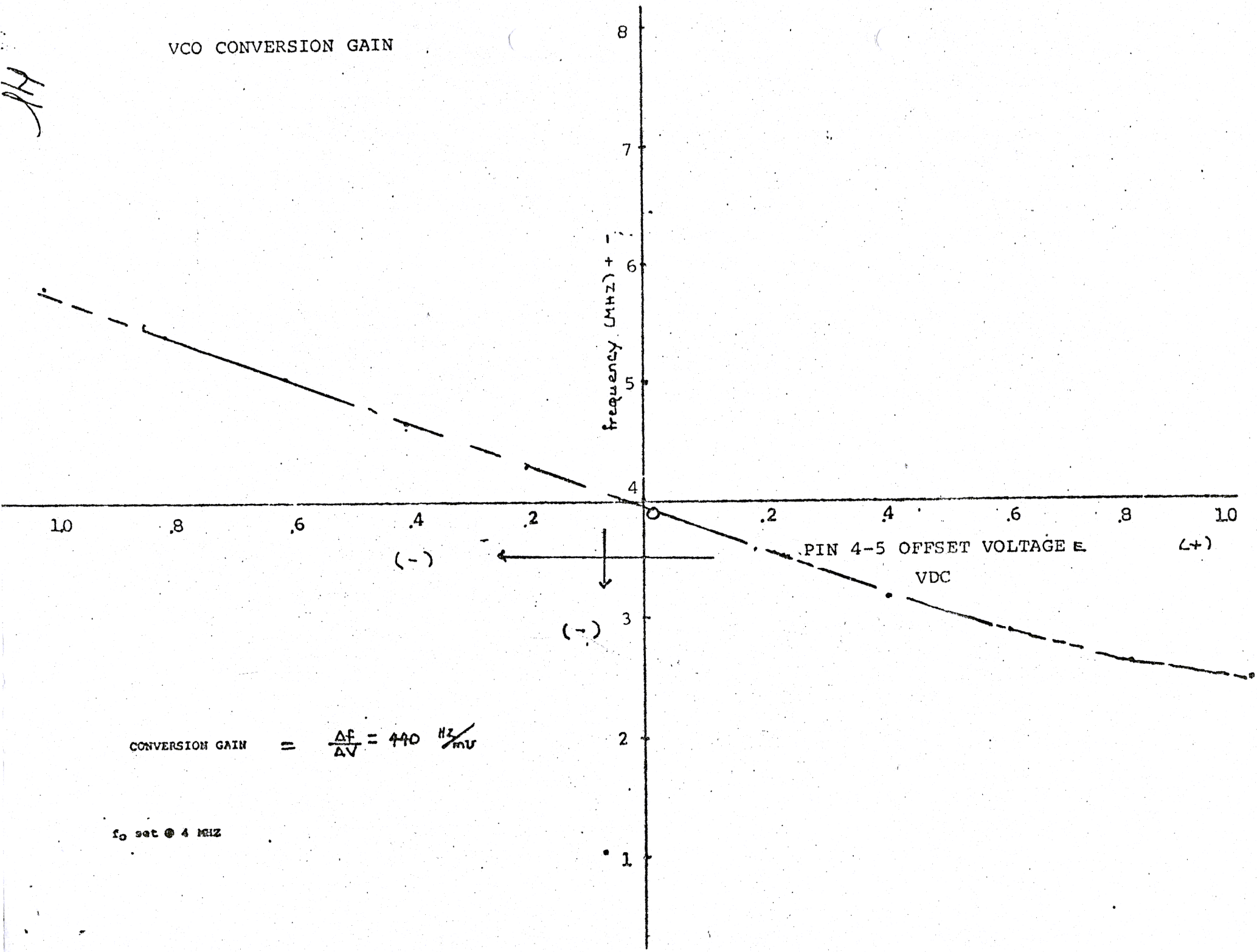
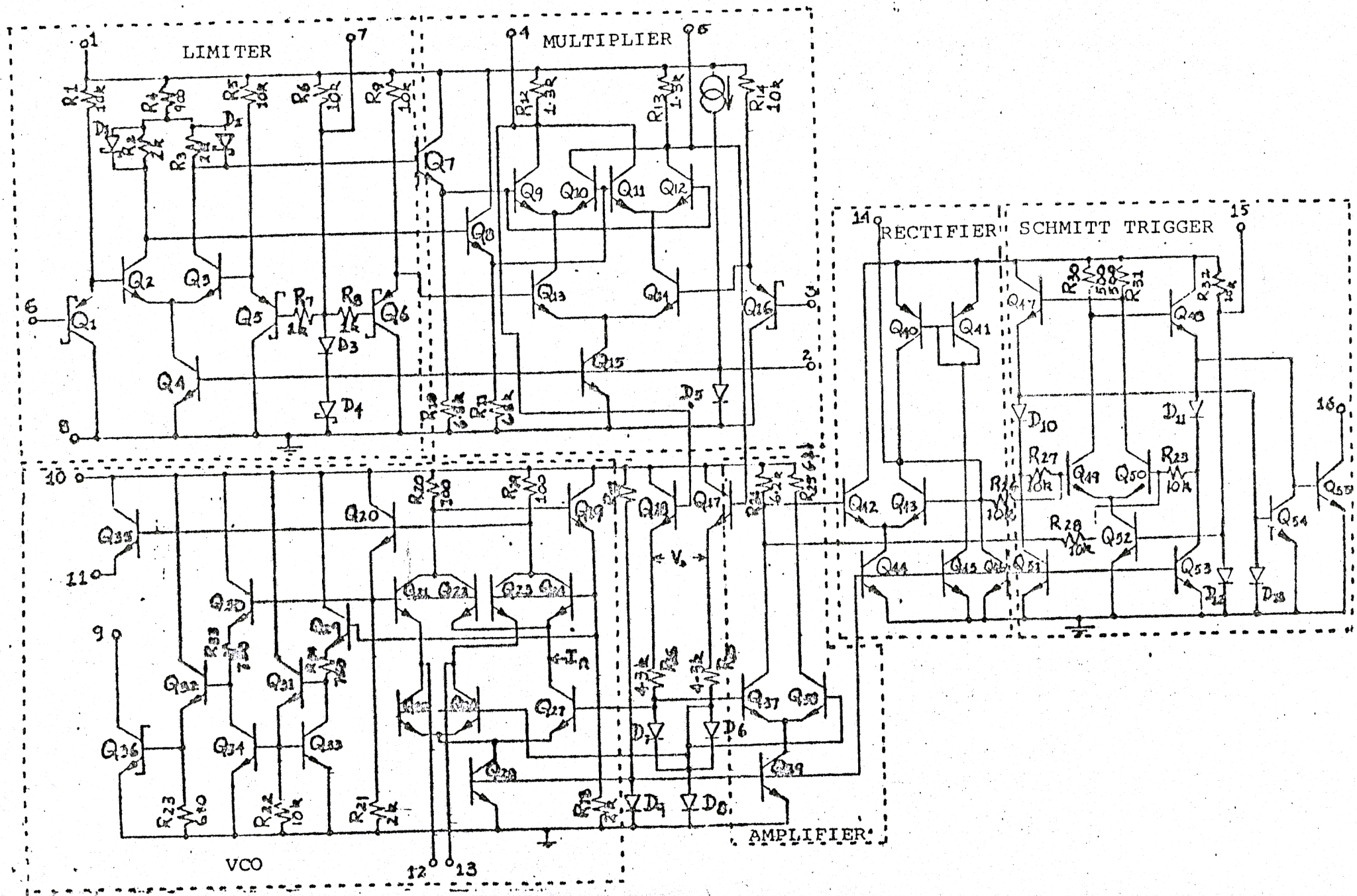
VCO CONVERSION GAIN



CONVERSION GAIN = $\frac{\Delta f}{\Delta V}$ = 440 Hz/mV

f_o set @ 4 MHz


LIMITER
MULTIPLIER
RECTIFIER
SCHMITT TRIGGER
VCO
AMPLIFIER