



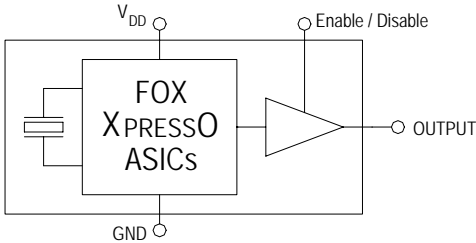
for **ETHERNET**

Model: FXO-PC735RGB-156

**LVPECL 7 x 5mm 3.3V 50ppm XO Freq: 156.25MHz**

**Features**

- ✔ Low Jitter
- ✔ Low Cost
- ✔ Tri-State Enable / Disable Feature
- ✔ Industry Standard Package
- ✔ Gold over Nickel Termination Finish



**Electrical Characteristics**

Parameters	Symbol	Condition	Maximum Value (unless otherwise noted)
Frequency	F <sub>O</sub>		156.25 MHz
Frequency Stability 1			50 ppm
Temperature Range	T <sub>O</sub> T <sub>STG</sub>	Standard operating Storage	-40°C to +85°C -55°C to +125°C
Supply Voltage	V <sub>DD</sub>	Standard	3.3V ± 5%
Input Current	I <sub>DD</sub>	Standard Load	120 mA
Output Load	Differential	Standard	50 ohms into V <sub>DD</sub> -2.0V <sub>DC</sub>
Start-Up Time	T <sub>S</sub>		10 mS
Output Enable / Disable Time			100 nS
Moisture Sensitivity Level	MSL		1
Termination Finish			Au

Note 1 – Stability is inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.

**Output Wave Characteristics**

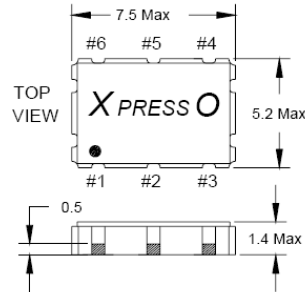
Parameters	Symbol	Condition	Maximum Value
Output LOW Voltage	V <sub>OL</sub>	Standard Load	1.35V ~ 1.65V
Output HIGH Voltage	V <sub>OH</sub>	Standard Load	2.055V ~ 2.405V
Output Symmetry		@ 50% V <sub>p-p</sub> Level	45% ~ 55%
Output Enable (PIN # 1) Voltage	V <sub>IH</sub>		≥70% V <sub>DD</sub>
Output Disable (PIN # 1) Voltage	V <sub>IL</sub>		≤ 30% V <sub>DD</sub>
Cycle Rise Time	T <sub>R</sub>	20% ~ 80% V <sub>p-p</sub>	400 pS
Cycle Fall Time	T <sub>F</sub>	80% ~ 20% V <sub>p-p</sub>	400 pS

DWG-100723 | Rev. 6/2/2010



**LVPECL 7 x 5mm 3.3V 50ppm XO Freq: 156.25MHz**

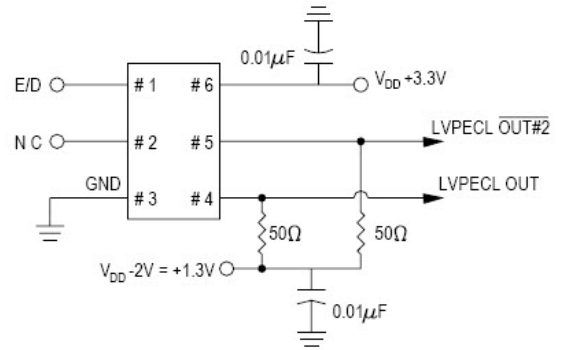
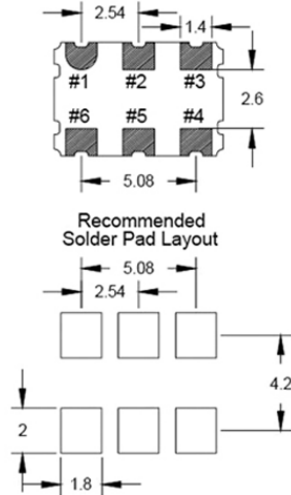
**Dimensional Drawing & Pad Layout**



Note: Xpresso LVPECL XOs are designed to fit on industry standard, 6 pad, layouts.

- Pin Connections**
- #1) E/D
  - #2) NC
  - #3) GND
  - #4) Output
  - #5) Output 2
  - #6) V<sub>DD</sub>

Actual marking is depicted.



Drawing is for reference to critical specifications defined by size measurements. Certain non-critical visual attributes, such as side castellations, reference pin shape, etc. may vary

**Phase Jitter & Time Interval Error (TIE) (Typical Measurements)**

Frequency	Phase Jitter (12kHz to 20MHz)	TIE (Sigma of Jitter Distribution)	Units
156.25 MHz	0.86	3.5	pS RMS

**Phase Jitter** is integrated from HP3048 Phase Noise Measurement System; measured directly into 50 ohm input; V<sub>DD</sub> = 3.3V.  
**TIE** was measured on LeCroy LC684 Digital Storage Scope, directly into 50 ohm input, with Amherst M1 software; V<sub>DD</sub> = 3.3V.  
 Per *MJSQ spec (Methodologies for Jitter and Signal Quality specifications)*

**Random & Deterministic Jitter Composition (Typical Measurements)**

Frequency	Random (Rj) (pS RMS)	Deterministic (Dj) (pS P-P)	Total Jitter (Tj) (14 x Rj) + Dj
156.25 MHz	1.29	9.3	27.7 pS

**Rj and Dj**, measured on LeCroy LC684 Digital Storage Scope, directly into 50 ohm input, with Amherst M1 software.  
 Per *MJSQ spec (Methodologies for Jitter and Signal Quality specifications)*

**Pin Functional Description**

Pin #	Name	Type	Function
1	E / D <sup>1</sup>	Logic	Enable / Disable Control of Output (0 = Disabled)
2	NC <sup>2</sup>		No Connection – Leave Open
3	GND	Ground	Electrical Ground for V <sub>DD</sub>
4	Output	Output	LVPECL Oscillator Output
5	Output 2	Output	Complementary LVPECL Output
6	V <sub>DD</sub> <sup>3</sup>	Power	Power Supply Source Voltage

- NOTES:**
- <sup>1</sup> Includes pull-up resistor to V<sub>DD</sub> to provide output when the pin (1) is No Connect. (Also see note 2)
  - <sup>2</sup> An optional pin # 2 Enable / disable is available.
  - <sup>3</sup> Installation should include a 0.01μF bypass capacitor placed between V<sub>DD</sub> (Pin 6) and GND (Pin 3) to minimize power supply line noise.