PCA9545A/45B/45C

4-channel I²C-bus switch with interrupt logic and reset

Rev. 07 — 19 June 2009 Product data sheet

1. General description

The PCA9545A/45B/45C is a quad bidirectional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs, $\overline{INT0}$ to $\overline{INT3}$, one for each of the downstream pairs, are provided. One interrupt output, $\overline{INT}$, acts as an AND of the four interrupt inputs.

An active LOW reset input allows the PCA9545A/45B/45C to recover from a situation where one of the downstream I²C-buses is stuck in a LOW state. Pulling the $\overline{RESET}$ pin LOW resets the I²C-bus state machine and causes all the channels to be deselected as does the internal power-on reset function.

The pass gates of the switches are constructed such that the V_{DD} pin can be used to limit the maximum high voltage which will be passed by the PCA9545A/45B/45C. This allows the use of different bus voltages on each pair, so that 1.8 V or 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

The PCA9545A, PCA9545B and PCA9545C are identical except for the fixed portion of the slave address.

2. Features

- 1-of-4 bidirectional translating switches
- I²C-bus interface logic; compatible with SMBus standards
- 4 active LOW interrupt inputs
- Active LOW interrupt output
- Active LOW reset input
- 2 address pins allowing up to 4 devices on the I²C-bus
- Alternate address versions A, B and C allow up to a total of 12 devices on the bus for larger systems or to resolve address conflicts
- Channel selection via I²C-bus, in any combination
- Power-up with all switch channels deselected
- Low R_{on} switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V

- 5 V tolerant Inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up protection exceeds 100 mA per JESD78
- Three packages offered: SO20, TSSOP20, and HVQFN20

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA9545ABS	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 × 5 × 0.85 mm	SOT662-1
PCA9545AD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCA9545APW	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
PCA9545BPW			
PCA9545CPW			

3.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
PCA9545ABS	9545A	–40 °C to +85 °C
PCA9545AD	PCA9545AD	–40 °C to +85 °C
PCA9545APW	PA9545A	–40 °C to +85 °C
PCA9545BPW	PA9545B	–40 °C to +85 °C
PCA9545CPW	PA9545C	–40 °C to +85 °C

4. Block diagram

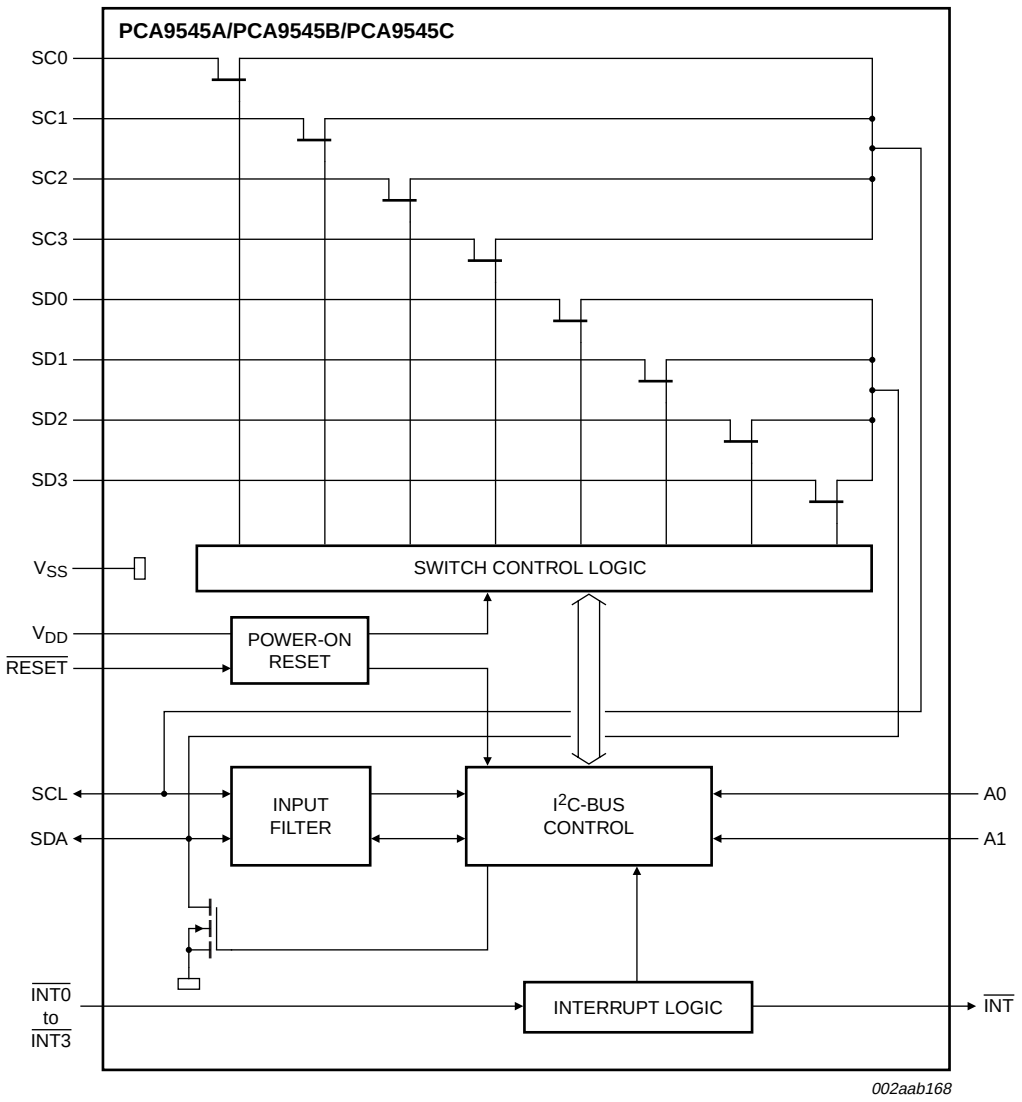


Fig 1. Block diagram of PCA9545A/45B/45C

5. Pinning information

5.1 Pinning

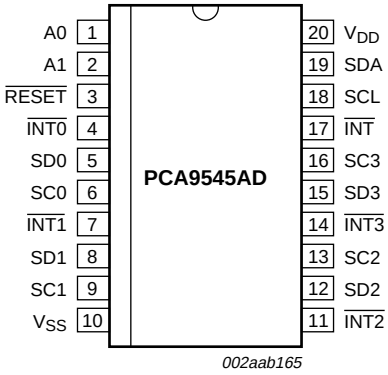


Fig 2. Pin configuration for SO20

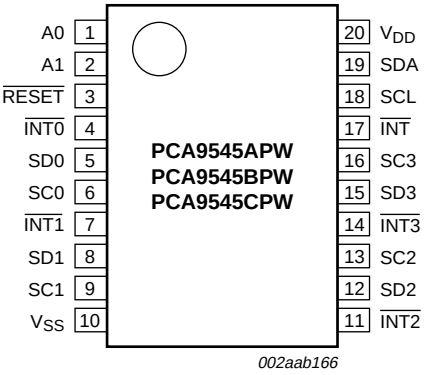


Fig 3. Pin configuration for TSSOP20

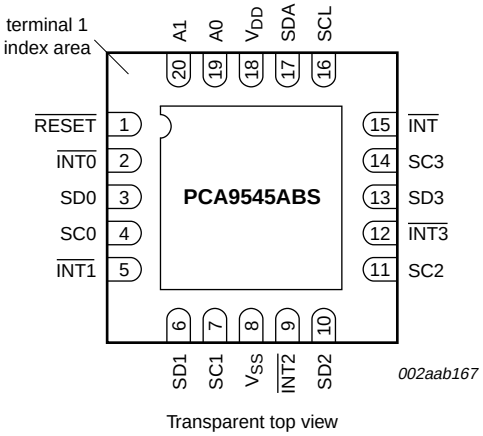


Fig 4. Pin configuration for HVQFN20 (transparent top view)

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO20, TSSOP20	HVQFN20	
A0	1	19	address input 0
A1	2	20	address input 1
$\overline{RESET}$	3	1	active LOW reset input
$\overline{INT0}$	4	2	active LOW interrupt input 0
SD0	5	3	serial data 0
SC0	6	4	serial clock 0
$\overline{INT1}$	7	5	active LOW interrupt input 1
SD1	8	6	serial data 1
SC1	9	7	serial clock 1
V_{SS}	10	8[1]	supply ground
$\overline{INT2}$	11	9	active LOW interrupt input 2
SD2	12	10	serial data 2
SC2	13	11	serial clock 2
$\overline{INT3}$	14	12	active LOW interrupt input 3
SD3	15	13	serial data 3
SC3	16	14	serial clock 3
$\overline{INT}$	17	15	active LOW interrupt output
SCL	18	16	serial clock line
SDA	19	17	serial data line
V_{DD}	20	18	supply voltage

[1] HVQFN20 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

Refer to Figure 1 “Block diagram of PCA9545A/45B/45C”.

6.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9545A is shown in Figure 5. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

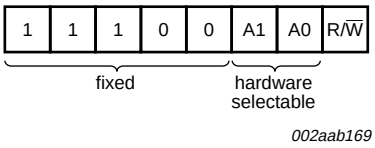


Fig 5. Slave address PCA9545A

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

The PCA9545BPW and PCA9545CPW are alternate address versions if needed for larger systems or to resolve conflicts. The data sheet will reference the PCA9545A, but the PCA9545B and PCA9545C function identically except for the slave address.

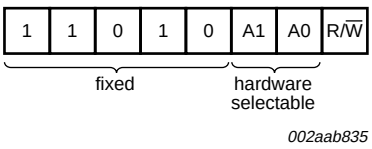


Fig 6. Slave address PCA9545B

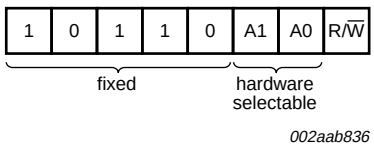


Fig 7. Slave address PCA9545C

6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9545A/45B/45C, which will be stored in the control register. If multiple bytes are received by the PCA9545A/45B/45C, it will save the last byte received. This register can be written and read via the I²C-bus.

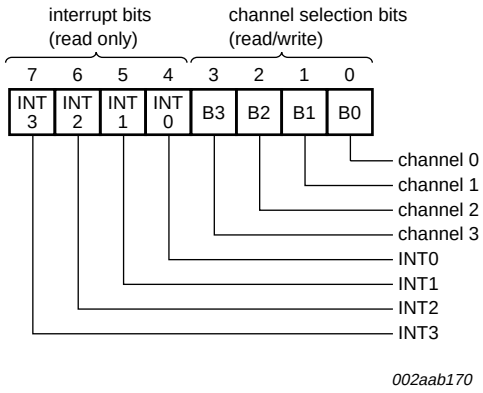


Fig 8. Control register

6.2.1 Control register definition

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9545A/45B/45C has been addressed. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 4. Control register: write (channel selection); read (channel status)

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
						1		channel 1 enabled
X	X	X	X	X	0	X	X	channel 2 disabled
					1			channel 2 enabled
X	X	X	X	0	X	X	X	channel 3 disabled
				1				channel 3 enabled
0	0	0	0	0	0	0	0	no channel selected; power-up/reset default state

Remark: Several channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and channel 3 are disabled and channel 1 and channel 2 are enabled. Care should be taken not to exceed the maximum bus capacity.

6.2.2 Interrupt handling

The PCA9545A/45B/45C provides 4 interrupt inputs, one for each channel, and one open-drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9545A/45B/45C and the interrupt output will be driven LOW. The channel does not need to be active for detection of the interrupt. A bit is also set in the control register.

Bit 4 through bit 7 of the control register corresponds to channel 0 through channel 3 of the PCA9545A/45B/45C, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9545A/45B/45C and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9545A/45B/45C to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{DD} through a pull-up resistor.

Table 5. Control register: Read—interrupt

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	0	X	X	X	X	no interrupt on channel 0
			1					interrupt on channel 0
X	X	0	X	X	X	X	X	no interrupt on channel 1
		1						interrupt on channel 1
X	0	X	X	X	X	X	X	no interrupt on channel 2
	1							interrupt on channel 2
0	X	X	X	X	X	X	X	no interrupt on channel 3
1								interrupt on channel 3

Remark: Several interrupts can be active at the same time. Example: INT3 = 0, INT2 = 1, INT1 = 1, INT0 = 0, means that there is no interrupt on channel 0 and channel 3, and there is interrupt on channel 1 and channel 2.

6.3 $\overline{\text{RESET}}$ input

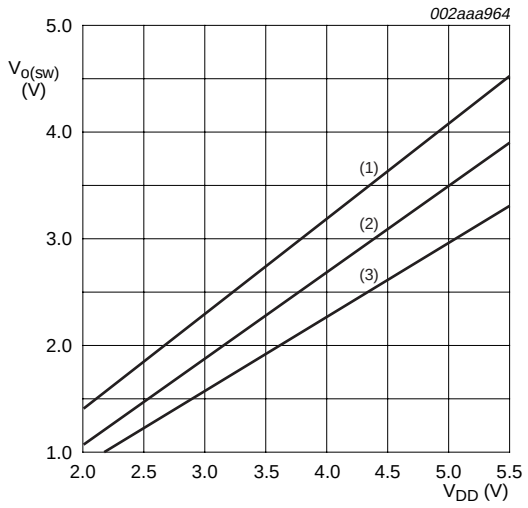
The $\overline{\text{RESET}}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of $t_{w(rst)L}$, the PCA9545A/45B/45C will reset its registers and I²C-bus state machine and will deselect all channels. The $\overline{\text{RESET}}$ input must be connected to V_{DD} through a pull-up resistor.

6.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9545A/45B/45C in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9545A/45B/45C registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

6.5 Voltage translation

The pass gate transistors of the PCA9545A/45B/45C are constructed such that the V_{DD} voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.



(1) maximum
(2) typical
(3) minimum

Fig 9. Pass gate voltage versus supply voltage

Figure 9 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section 10 “Static characteristics” of this data sheet). In order for the PCA9545A/45B/45C to act as a voltage translator, the $V_{O(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{O(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 9, we see that $V_{O(sw)(max)}$ will be at 2.7 V when the PCA9545A/45B/45C supply voltage is 3.5 V or lower, so the PCA9545A/45B/45C supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 16).

More Information can be found in Application Note *AN262: PCA954X family of I²C/SMBus multiplexers and switches*.

7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 10).

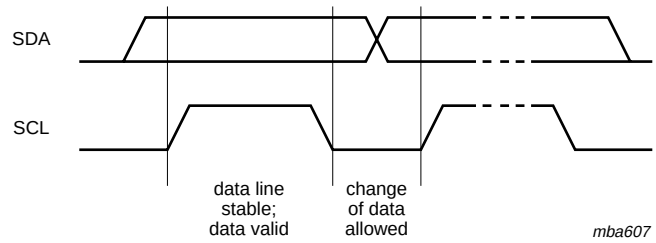


Fig 10. Bit transfer

7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 11).

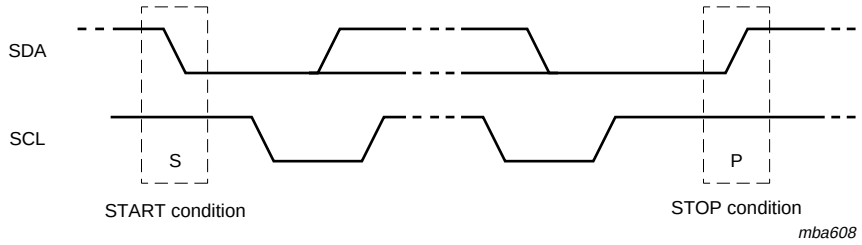


Fig 11. Definition of START and STOP conditions

7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 12).

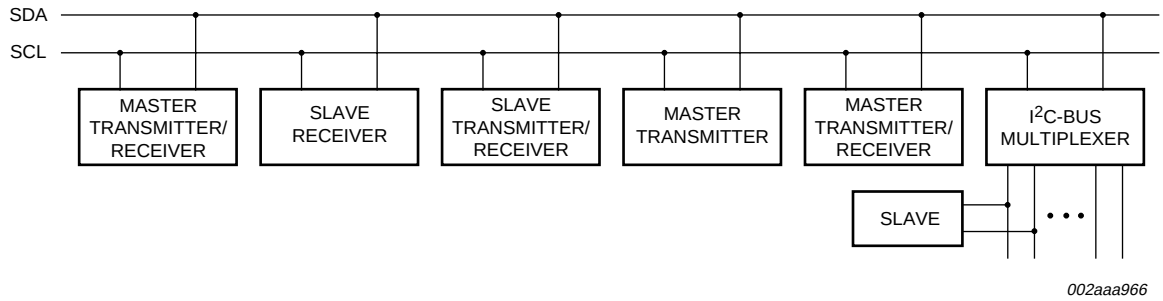


Fig 12. System configuration

7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

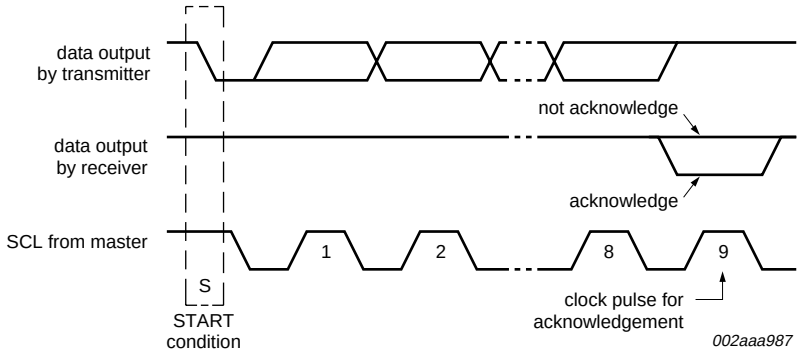


Fig 13. Acknowledgement on the I²C-bus

7.5 Bus transactions

Data is transmitted to the PCA9545A/45B/45C control register using the Write mode as shown in Figure 14.

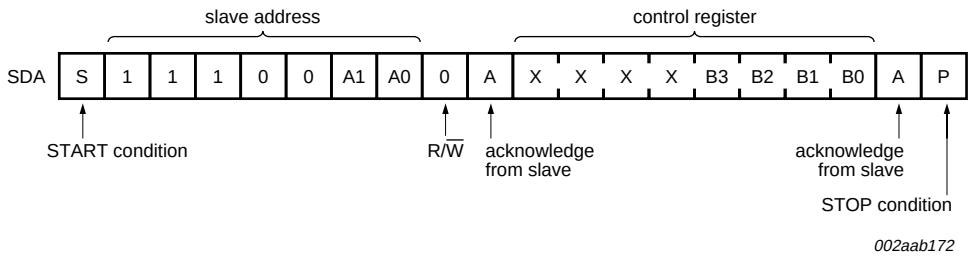


Fig 14. Write control register

Data is read from PCA9545A/45B/45C using the Read mode as shown in Figure 15.

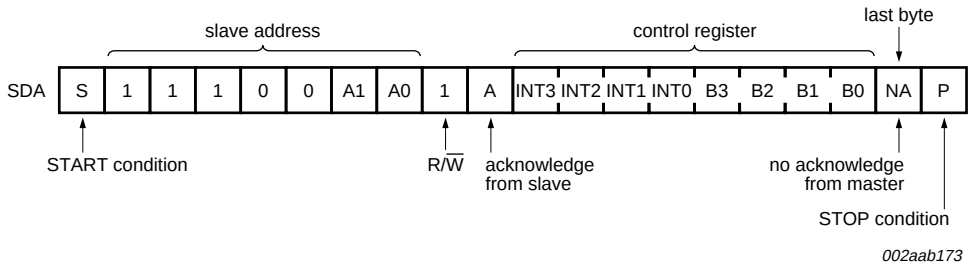
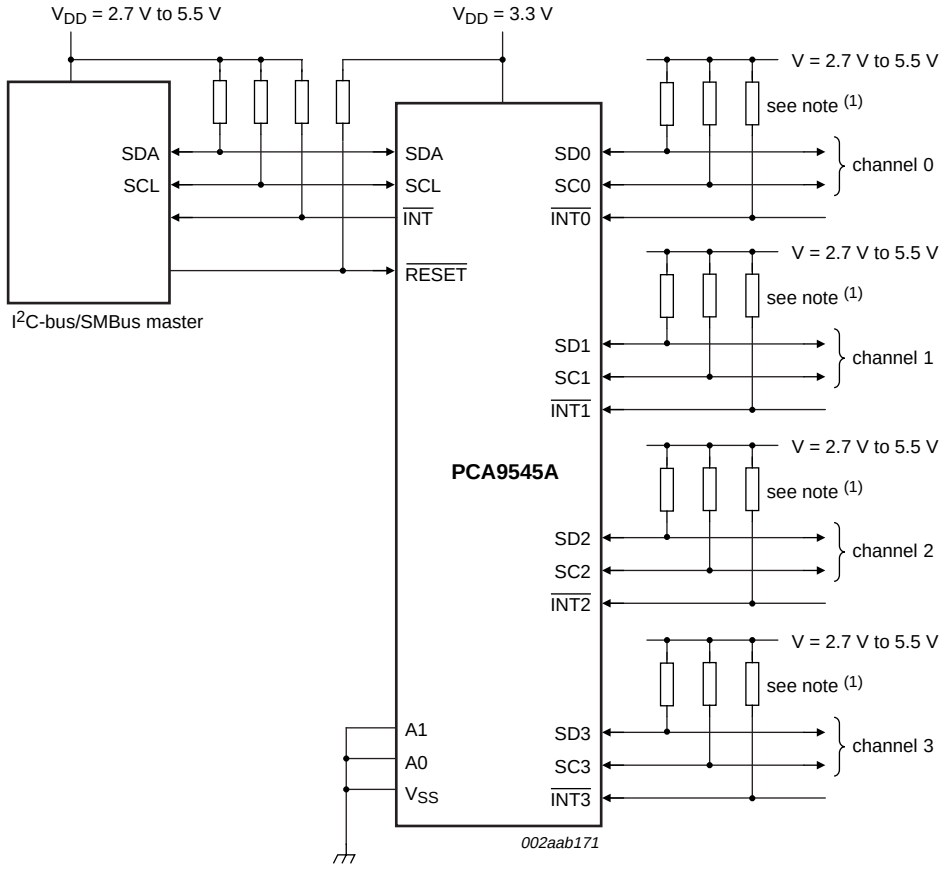


Fig 15. Read control register

8. Application design-in information



(1) If the device generating the interrupt has an open-drain output structure or can be 3-stated, a pull-up resistor is required.

If the device generating the interrupt has a totem-pole output structure and cannot be 3-stated, a pull-up resistor is not required.

The interrupt inputs should not be left floating.

Fig 16. Typical application

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} (ground = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_I	input current		-	±20	mA
I_O	output current		-	±25	mA
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±100	mA
P_{tot}	total power dissipation		-	400	mW
T_{stg}	storage temperature		–60	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

10. Static characteristics

Table 7. Static characteristics at V_{DD} = 2.3 V to 3.6 V

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. See Table 8 on page 16 for V_{DD} = 4.5 V to 5.5 V[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.3	-	3.6	V
I_{DD}	supply current	Operating mode; V_{DD} = 3.6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	-	10	30	µA
I_{stb}	standby current	Standby mode; V_{DD} = 3.6 V; no load; $V_I = V_{DD}$ or V_{SS}	-	0.1	1	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS} [2]	-	1.6	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	7	-	mA
		V_{OL} = 0.6 V	6	10	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	10	13	pF
Select inputs A0, A1, $\overline{INT0}$ to $\overline{INT3}$, $\overline{RESET}$						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	1.6	3	pF
Pass gate						
R_{on}	ON-state resistance	V_{DD} = 3.6 V; V_O = 0.4 V; I_O = 15 mA	5	11	30	Ω
		V_{DD} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 10 mA	7	16	55	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)} = V_{DD}$ = 3.3 V; $I_{o(sw)}$ = −100 µA	-	1.9	-	V
		$V_{i(sw)} = V_{DD}$ = 3.0 V to 3.6 V; $I_{o(sw)}$ = −100 µA	1.6	-	2.8	V
		$V_{i(sw)} = V_{DD}$ = 2.5 V; $I_{o(sw)}$ = −100 µA	-	1.5	-	V
		$V_{i(sw)} = V_{DD}$ = 2.3 V to 2.7 V; $I_{o(sw)}$ = −100 µA	1.1	-	2.0	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
C_{io}	input/output capacitance	$V_I = V_{SS}$	-	3	5	pF
$\overline{INT}$ output						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
I_{OH}	HIGH-level output current		-	-	+10	µA

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] V_{DD} must be lowered to 0.2 V in order to reset part.

Table 8. Static characteristics at V_{DD} = 4.5 V to 5.5 V

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. See Table 7 on page 15 for V_{DD} = 2.3 V to 3.6 V[1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			4.5	-	5.5	V
I_{DD}	supply current	Operating mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz		-	25	100	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}		-	0.3	1	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	[2]	-	1.7	2.1	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
		V_{OL} = 0.6 V		6	-	-	mA
I_L	leakage current	V_I = V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	10	13	pF
Select inputs A0, A1, $\overline{INT0}$ to $\overline{INT3}$, $\overline{RESET}$							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	2	5	pF
Pass gate							
R_{on}	ON-state resistance	V_{DD} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA		4	9	24	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)}$ = V_{DD} = 5.0 V; $I_{o(sw)}$ = −100 µA		-	3.6	-	V
		$V_{i(sw)}$ = V_{DD} = 4.5 V to 5.5 V; $I_{o(sw)}$ = −100 µA		2.6	-	4.5	V
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_{io}	input/output capacitance	V_I = V_{SS}		-	3	5	pF
$\overline{INT}$ output							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
I_{OH}	HIGH-level output current			-	-	+10	µA

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] V_{DD} must be lowered to 0.2 V in order to reset part.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
t_{PD}	propagation delay	from SDA to SDx, or SCL to SCx		-	0.3[1]	-	0.3[1]	ns
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		[2]	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0[3]	3.45	0[3]	0.9	µs
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$[4]	300	ns
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$[4]	300	ns
C_b	capacitive load for each bus line			-	400	-	400	pF
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
$t_{VD;DAT}$	data valid time	HIGH-to-LOW	[5]	-	1	-	1	µs
		LOW-to-HIGH	[5]	-	0.6	-	0.6	µs
$t_{VD;ACK}$	data valid acknowledge time			-	1	-	1	µs
$\overline{INT}$								
$t_{v(INTnN-INTN)}$	valid time from $\overline{INTn}$ to $\overline{INT}$ signal			-	4	-	4	µs
$t_{d(INTnN-INTN)}$	delay time from $\overline{INTn}$ to $\overline{INT}$ inactive			-	2	-	2	µs
$t_{w(rej)L}$	LOW-level rejection time	$\overline{INTn}$ inputs		1	-	1	-	µs
$t_{w(rej)H}$	HIGH-level rejection time	$\overline{INTn}$ inputs		0.5	-	0.5	-	µs
$\overline{RESET}$								
$t_{w(rst)L}$	LOW-level reset time			4	-	4	-	ns
t_{rst}	reset time	SDA clear		500	-	500	-	ns
$t_{REC;STA}$	recovery time to START condition			0	-	0	-	ns

[1] Pass gate propagation delay is calculated from the 20 Ω typical R_{on} and the 15 pF load capacitance.

[2] After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

[5] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

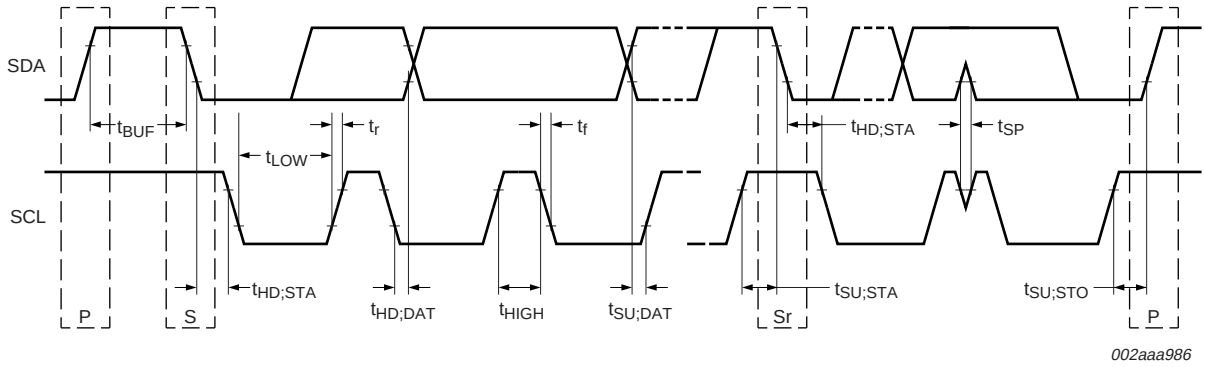


Fig 17. Definition of timing on the I²C-bus

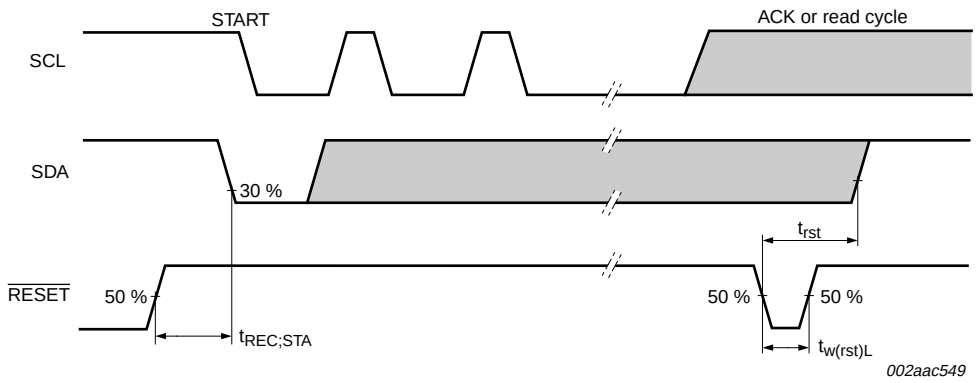
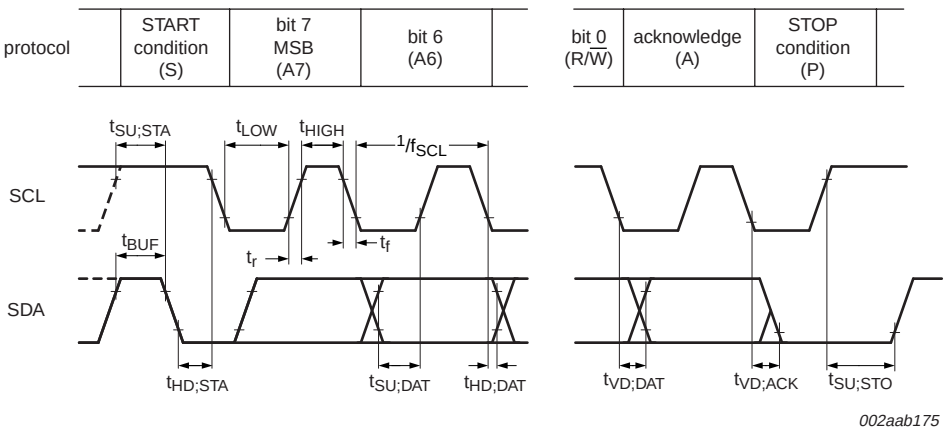


Fig 18. Definition of $\overline{\text{RESET}}$ timing



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 19. I²C-bus timing diagram

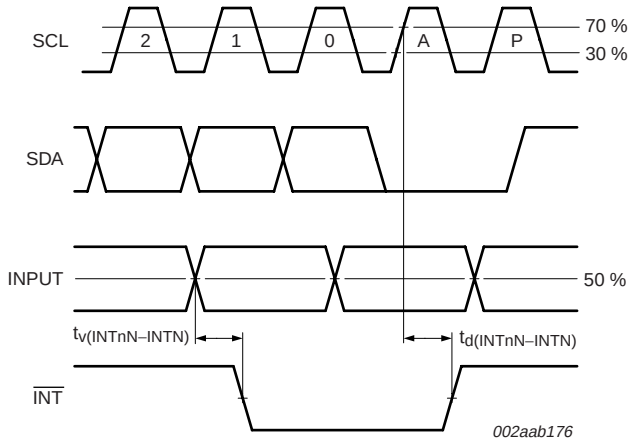
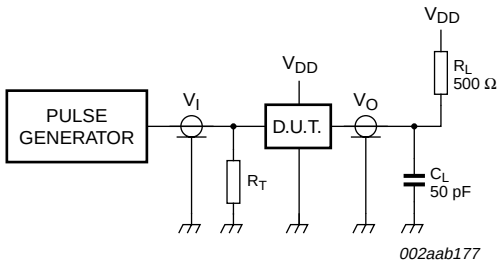


Fig 20. Expanded view of read input port register

12. Test information



Definitions test circuit:

R_L = Load resistance.

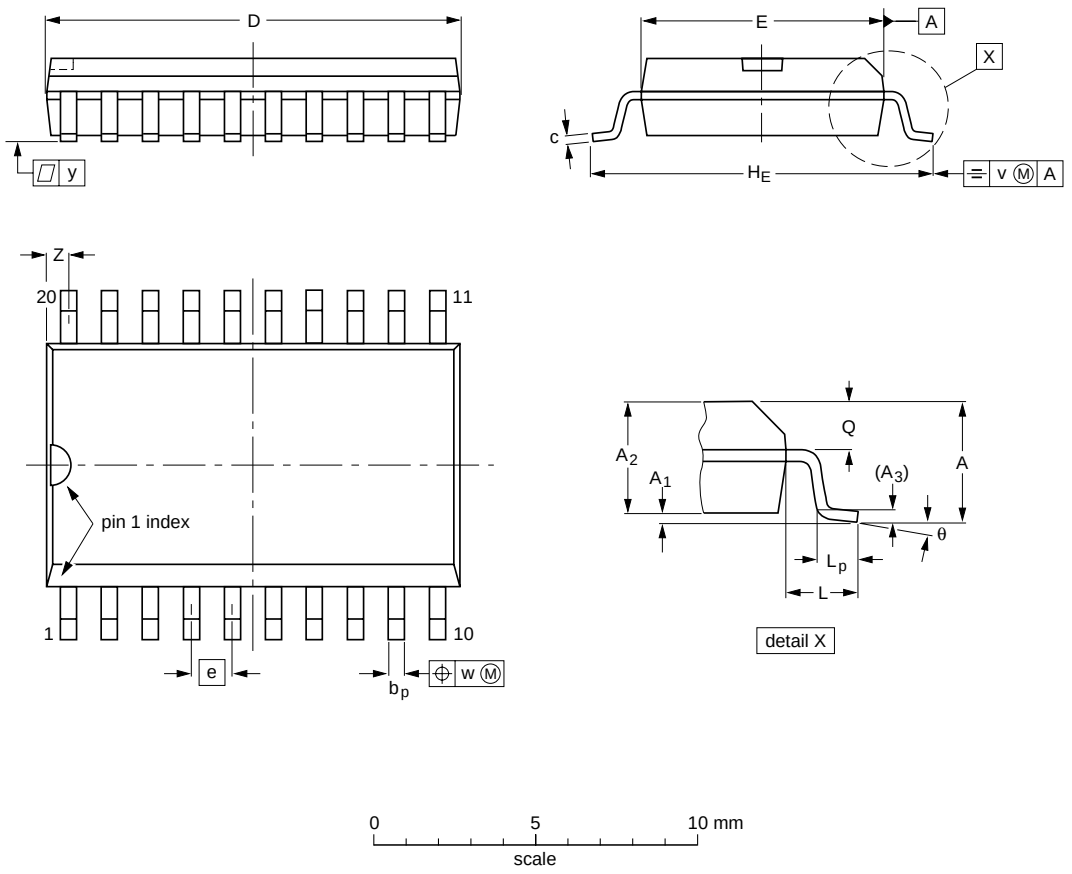
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 21. Test circuitry for switching times

13. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

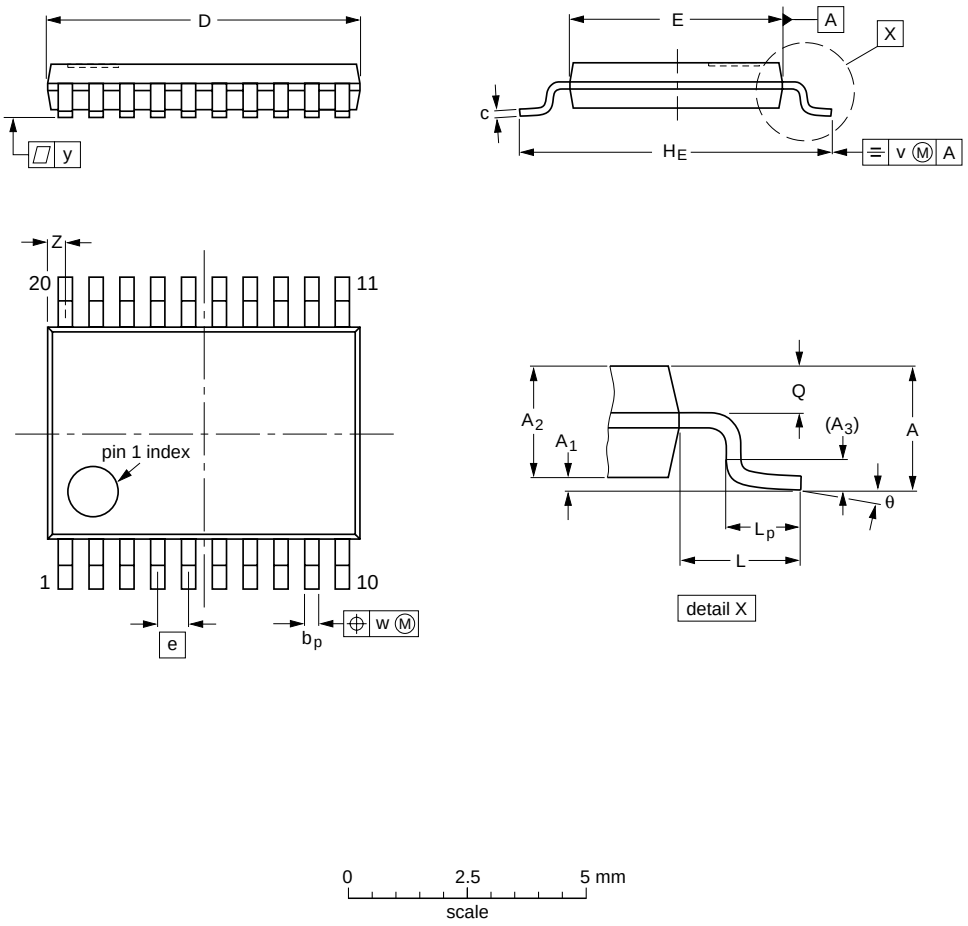
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 22. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

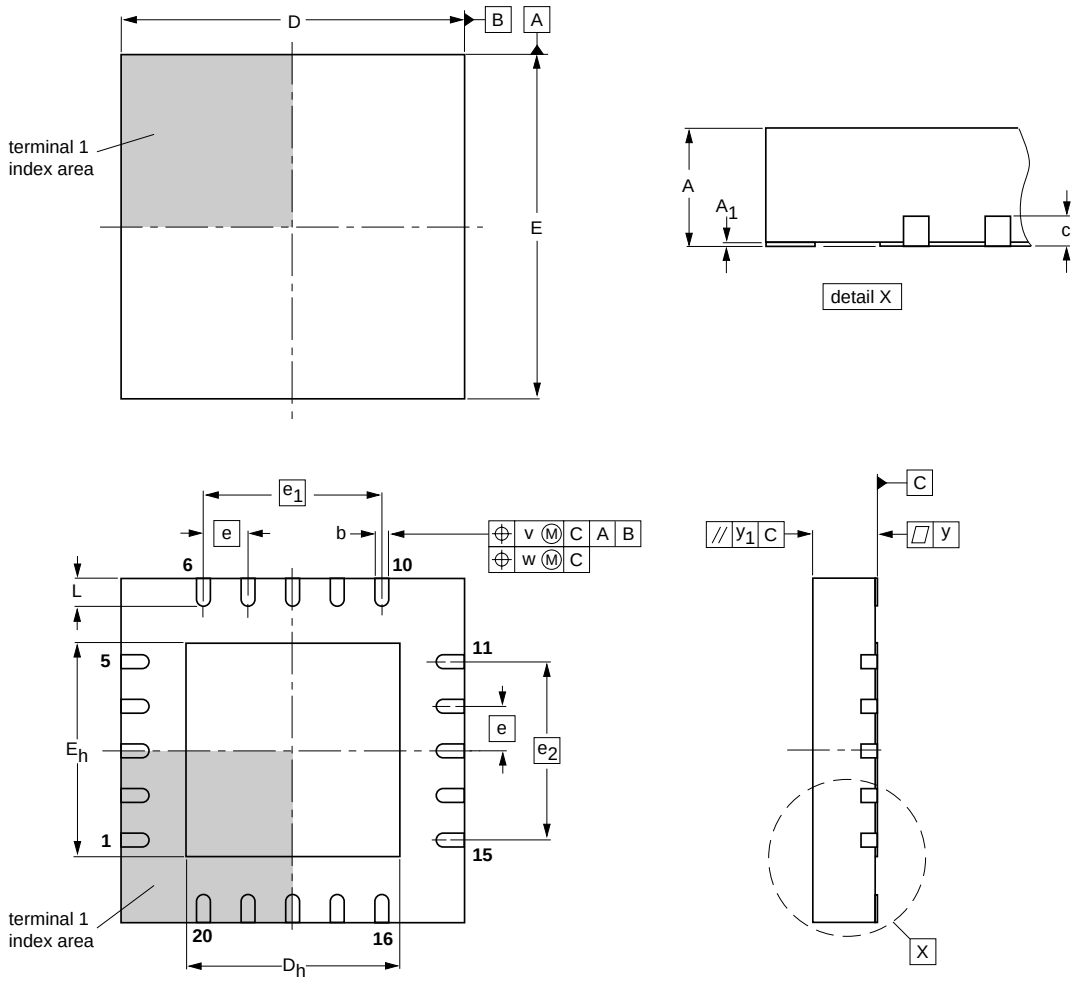
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 23. Package outline SOT360-1 (TSSOP20)

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 x 5 x 0.85 mm **SOT662-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.65	2.6	2.6	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT662-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 24. Package outline SOT662-1 (HVQFN20)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

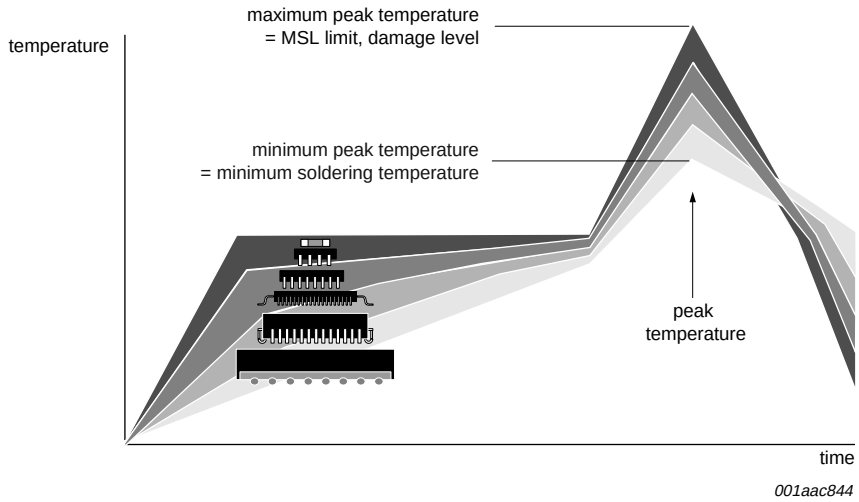
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
IC	Integrated Circuit
I²C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
SMBus	System Management Bus

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9545A_45B_45C_7	20090619	Product data sheet	-	PCA9545A_45B_45C_6
Modifications:	• Table 9 “Dynamic characteristics”: – Symbol t_f: changed Unit from “µs” to “ns” – Symbol C_b: changed Unit from “µs” to “pF” • Updated soldering information.			
PCA9545A_45B_45C_6	20070319	Product data sheet	-	PCA9545A_45B_45C_5
PCA9545A_45B_45C_5	20061017	Product data sheet	-	PCA9545A_4
PCA9545A_4	20060925	Product data sheet	-	PCA9545A_3
PCA9545A_3 (9397 750 14311)	20050303	Product data sheet	-	PCA9545A_2
PCA9545A_2 (9397 750 13989)	20040929	Objective data sheet	-	PCA9545A_1
PCA9545A_1 (9397 750 13309)	20040728	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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19. Contents

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